Dhruv **Wagh**

Graduate Research Associate · Teaching Assistant
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As I approach the completion of my master's degree, I am seeking opportunities to apply my skills in VLSI, storage architecture, and digital logic design, driving innovation at the intersection of research and industry.

Education

Tel Aviv University — *Tel Aviv, Israel*
Master of Science (MSc) in Electrical Engineering — *Oct 2022 – Dec 2024*
GPA: 91.4%

Tel Aviv University — *Tel Aviv, Israel*
Bachelor of Science (BSc) in Electrical and Electronics Engineering — *Oct 2018 – July 2022*
GPA: 81.93%

Experience

Graduate Research Associate — *Tel Aviv, Israel*
Tel Aviv University — *Oct 2022 – Present*
- Research on novel storage accelerator architecture.
- Implementation on PCIe FPGA.

Organizer, Mentor, and Judge — *Tel Aviv, Israel*
Apple - Tel Aviv University Electrical Engineering Hackathon — *Aug 2024*
- Designed the FPGA based environment for competitive stone paper scissors games and provided mentorship.
- Made various scripts to test participant projects.

Teaching Assistant and Instructor — *Tel Aviv, Israel*
Tel Aviv University — *Oct 2022 – Present*
- Introduction to VLSI.
- Advanced Computer Structures Lab.

Hardware Intern — *Tel Aviv, Israel*
CADY Solutions — *Aug 2021 – Oct 2021*
- Verification of the CADY AI schematic checker model.
- Tested and analyzed 90+ bona fide industrial schematics.

Undergraduate Research Assistant — *Tel Aviv, Israel*
Tel Aviv University — *Mar 2020 – Nov 2020*
- Conducted experiments on Balls and Bin Problem with Matlab/Python.
- Extensive Data Analysis of the results and latex documentation.

Projects

Attention and BiLSTM Model on Maestro V2 Dataset
Course: Deep Learning — *2023*
- Developed model to generate MIDI signals, trained on Maestro V2 dataset.
- Evaluation and ablation study of the model.

Pipelined Implementation of DLX Processor on RESA Bus
Final Year Project — *2022*
- Designed and Implemented DLX Processor to fit in the lab's proprietary communication protocol on Spartan-6 FPGA.
- Performance analysis compared to the non pipelined DLX.

ALU Design
Course: Introduction to VLSI — *2022*
- Developed opcodes, schematic, and layout in Virtuoso.
- Rigorous testing of the design.

Skills

Programming Languages Verilog, VHDL, Python, C, C++, Matlab, Java
Technical Skills Vivado, Cadence Virtuoso, OrCAD, Xylinx ISE, Logic Design, PSPICE, Raspberry Pi, Arduino

Languages

English Professional Fluency
Hindi Professional Fluency
Marathi Native
Hebrew Beginner