CS232 Project Report

IITB-RISC-22 (multi-cycle processor)

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DESCRIPTION:

We have designed a multi-cycle processor, IITB-RISC-22, with the given instruction set architecture. There are 8 (16 bit each) registers. There is a memory block of 2^{16} memory elements of 16 bit each, one for every memory address implemented inside the top level entity in the form of signals. The top level entity, IITB_RISC, has a clock and reset input, along with some more inputs (as described) to read the instruction codes.

WORKING:

The top level entity is used sequentially to read instructions into the memory block.

If the **read_instruction** input is true, then the **instruction** input code is read into the memory block , an internal signal **ins_pc** keeps track of the memory address at which the next instruction is to be stored.

If the **read_instruction** input is false, the instruction (according to the execution program counter kept track of by **pc** signal) is executed. The execution happens in phases over multiple cycles (signal **PHASE** keeps track).

To execute an instruction, we maintain a signal **STATE** which is 0 initially. For state 0, we read the **opcode** into a signal. A process that acts whenever **opcode** changes sets the value of **STATE** corresponding to a particular instruction. For some instructions we have the same **STATE** value (addition and nand) and the process handling **opcode** decides whether to set the **STATE** to the desired value or 0 (implying go to next instruction) after looking at C and Z flags.

Now that the value of **STATE** is set, we are ready to begin execution of the instruction. The execution happens in phases. We begin with **PHASE** = 1where we read the operands. In **PHASE** = 2, (and onwards) we execute whatever we are required to do. In the last **PHASE** we set **PHASE** = 1 and increment program counter (register 7). This way, the instruction is executed one phase per clock cycle.

The signals **carry** and **zero** keep track of the carry and zero flags respectively.