EE 6313 Advanced Microprocessors
Fall 2018 Project 2

CACHE CONTROLLER

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Project:

The goal of this project is to determine the best architecture for a cache controller that interfaces to a 16-bit microprocessor that is used for signal processing. While the microprocessor is general purpose in design and performs several functions, it is desired to speed up certain signal processing functions, such as those calculating the eigenvalues and eigenvectors of a system.

It has been assumed that the DRAM data bus is limited to 16 bits in width. The code performs two mathematical functions, 1) Finds Lower & upper Triangular Matrices of a 256 X 256 Positive Definite Matrix using Cholesky decomposition method. 2) Finds the Least-squares solution for a given column matrix. It has been assumed that matrices are located in the 16MB DRAM which has to be interfaced with Cache controller. It determines the best architecture for the 256 kB cache by simulating the behavior of cache controller by incrementing counters for each memory access, Cache hit & cache Miss. The metric being used to evaluate the best performance is the total access time required to run the choldc() followed by the cholsl() routine, including the time required to flush the pipeline after the least-squares solution is computed. By calling Write Memory or Read memory functions at appropriate places, it is possible to determine exactly how memory is accessed. The three degrees of freedom in the design are n-way set associativity, burst length, and write

strategy (write-back or write-through). It has been assumed that the miss penalty is 90ns (for first memory access) and 15ns for subsequent accesses in the same SDRAM word line and the cache hit time is 1ns. Performance has been calculated as a function of set size (n-way), number of cache lines, block size, and write strategy (write-back allocate, write-through allocate, and write-through non-allocate). It determines which 3 configurations result in the best performance out of n-way associativity of 1, 2, 4, 8, and 16 and burst lengths of 1, 2, 4, and 8 are evaluated for all 3 write strategies (60 permutations).

IMPORTANT DETAILS

- All the matrix inputs to the Cholesky Functions [choldc() and cholsl()] are defined in a separate header file named “input.h” .
- Input matrix a[256][256], pointer to input matrix *ptr[256] (“row pointer array”), b[256], p[256], x[256], counters i, j and k, sum are assumed to be stored in memory [SDRAM].
- The input parameters to the Cholesky Functions, double pointer a, array pointers x, b, p and matrix size i.e. n are assumed to be stored in general purpose registers.
- Positive Definite symmetric matrix a(256X256) & random column vector(256) are generated in MATLAB.
- Result of Cholesky least square function i.e. resultant column vector x[256] is verified with the MATLAB output & corresponding MATLAB code is included in the submitted folder.
- Best case and worst case obtained from the results are shown with the help of charts.

FORMULA FOR AVERAGE MEMORY ACCESS TIME(AMAT):

AMAT = (Read_CacheToCPU_Count X 1nsec) +

(Rd_RdMemToCache_Count X (90+(BL-1)15)nSec)

(Rd_WrBack_Dirty_Count X (90+(BL-1)15)nSec) +

MAX(Write_Through_Memory_Count X 90Sec ,

Write_Cache_Time) + FlushTime

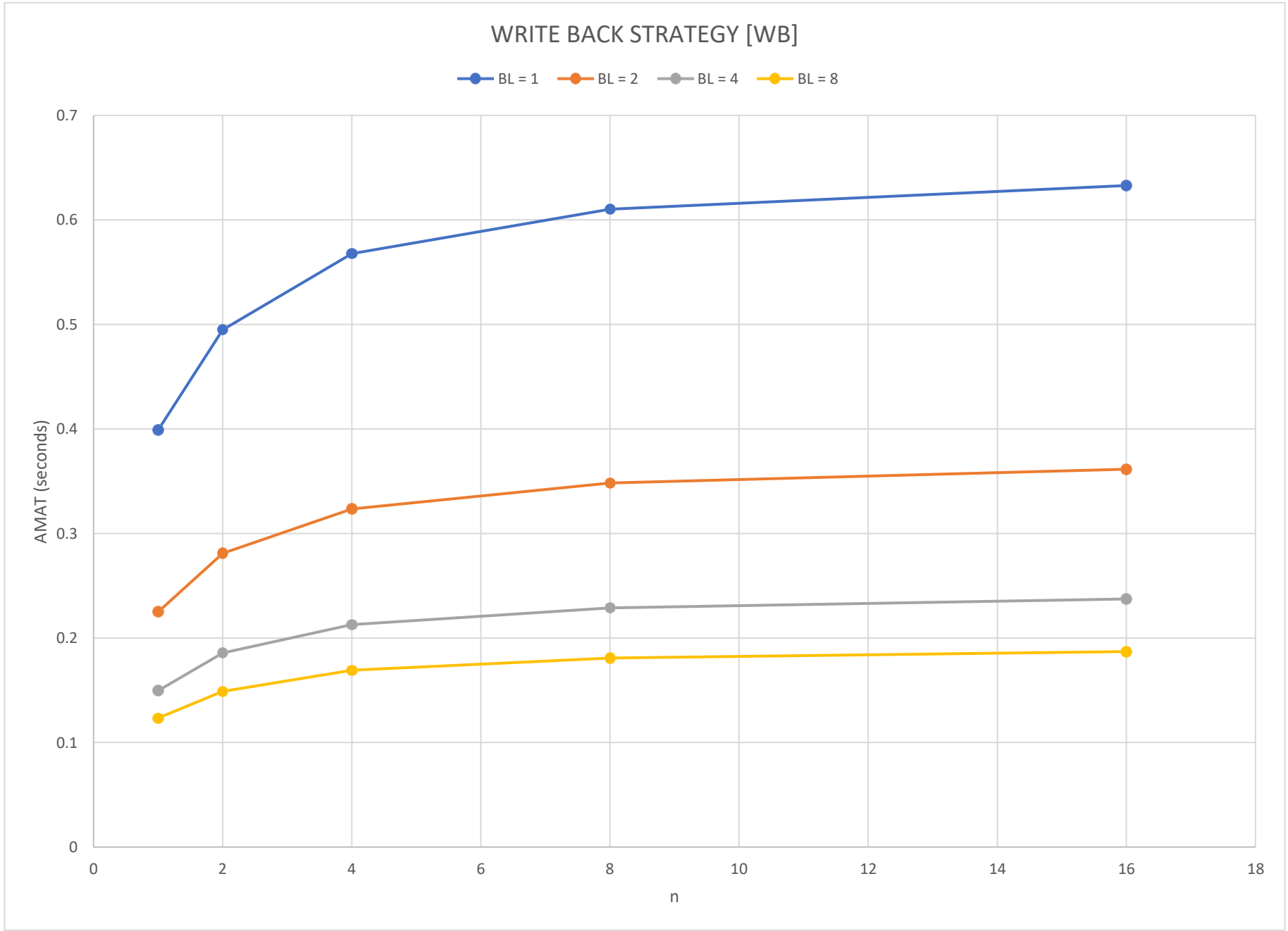
Where,

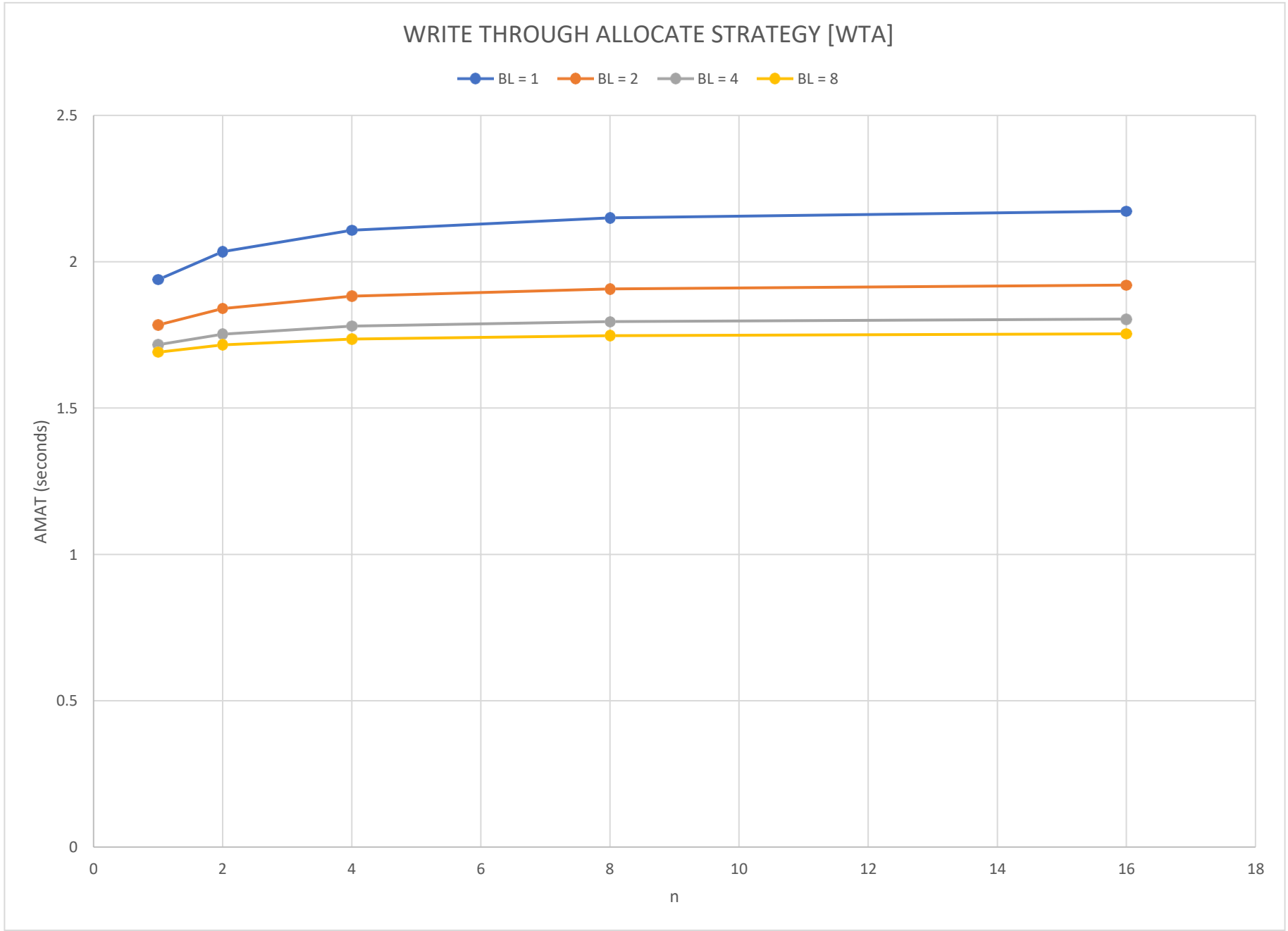
Write_Cache_Time = (Write_CputoCache_Count X 1nsec) +

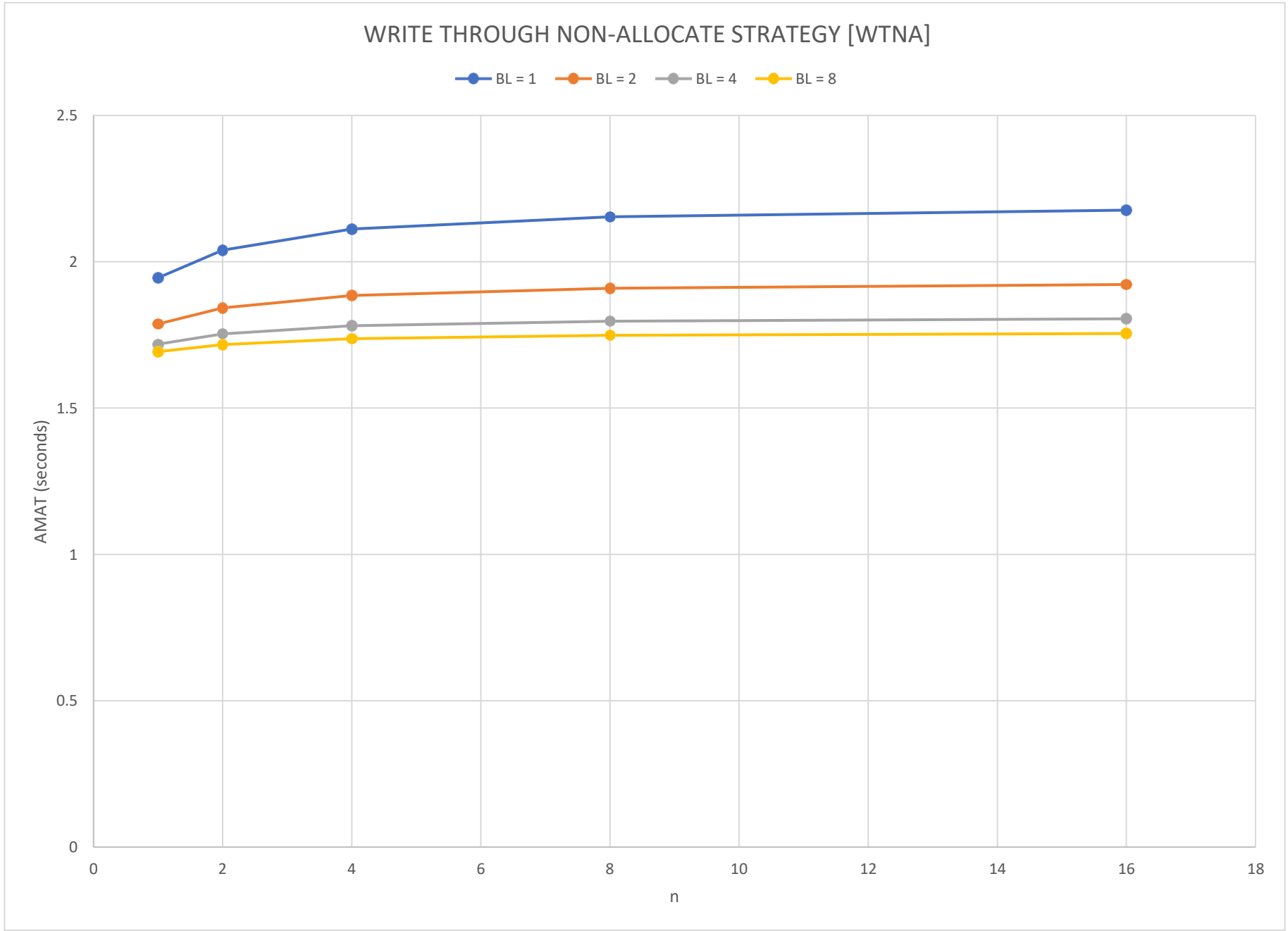
(Wr_RdMemToCache_Count X (90+(BL-1)15)nSec)

(Wr_WrBack_Dirty_Count X (90+(BL-1)15)nSec)

CASE	BEST	WORST
AMAT (seconds)	0.123351436	2.176093056
n	1	16
BL	8	1
STRATEGY	WB	WTNA


WRITE BACK STRATEGY [WB]
BL = 1
BL = 2
BL = 4
BL = 8
AMAT (seconds)
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
2
4
6
8
10
12
14
16
18
n


WRITE THROUGH ALLOCATE STRATEGY [WTA]
BL = 1
BL = 2
BL = 4
BL = 8
AMAT (seconds)
2.5
2
1.5
1
0.5
0
0
2
4
6
8
10
12
14
16
18
n


WRITE THROUGH NON-ALLOCATE STRATEGY [WTNA]
BL = 1
BL = 2
BL = 4
BL = 8
AMAT (seconds)
2.5
2
1.5
1
0.5
0
0
2
4
6
8
10
12
14
16
18
n