Experiment #3

I. To study sampling techniques and the effect of low pass filter.

II. To study pulse code modulation (PCM) and demodulation

III. To study data encoding and decoding techniques

EXPERIMENT NO. 3 (I)

NAME

Signal samplings and their reconstruction

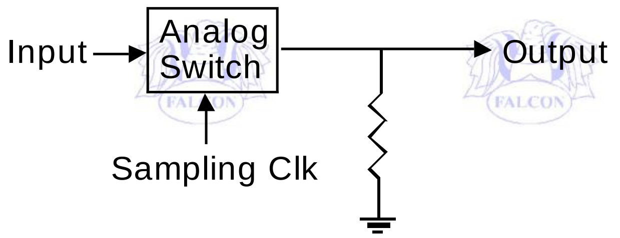
OBJECTIVES

To study different types of signal samplings and their reconstruction:

A. Natural Sampling
B. Sample and Hold
C. Flat top sampling

THEORY

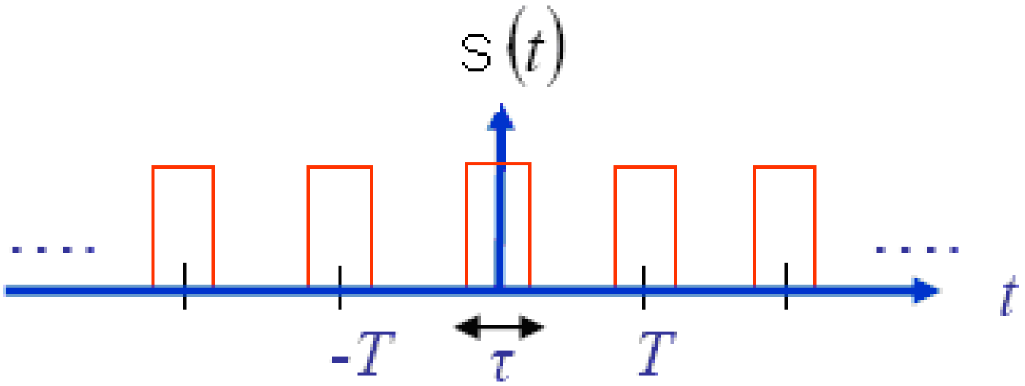
Natural Sampling

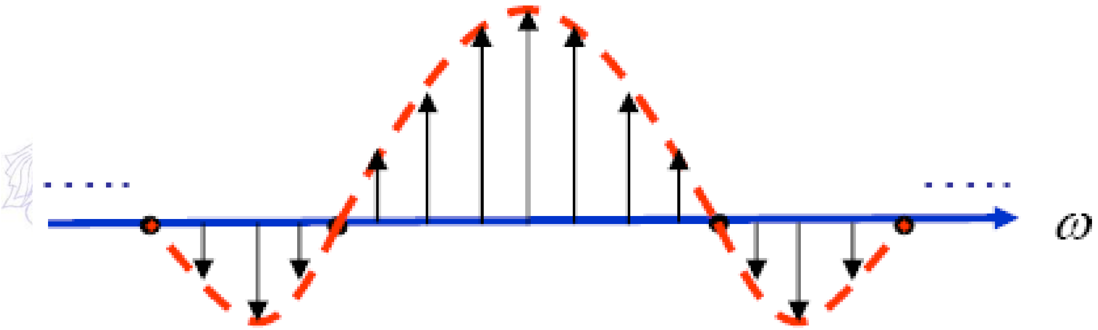


Here, the sampling waveform S (t) consists of a train of pulses having duration τ and it is separated by the sampling time T_s. The baseband signal is m (t), and the sampled signal S (t) m (t) is shown in the figure. Observe that the sampled signal consists of a sequence of pulses varying amplitude whose tops are not flat but follow the waveform of the signal m (t).

With natural sampling, as with instantaneous sampling, a signal sampled at the Nyquist rate may be reconstructed exactly by passing the samples through an ideal low-pass filter with cutoff at the frequency f_m, where f_m is the highest frequency spectral component of the signal. To prove this, we note that the sampling waveform S (t) is given by:

$$S(t) = \tau / T_s + 2\tau / T_s (C_1 \cos 2\prod t / T_s + C_2 \cos 2 * 2\prod t / T_s + \ldots.) \qquad \ldots\ldots\ldots\ldots\ldots\ldots.. \text{(i)}$$





With the constant C_n given by

$$C_n = \frac{\sin(n\prod\tau / T_S)}{n\prod\tau / T_S} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(ii)}$$

The sampled base band signal S (t) m (t) is for $T_s = 2f_M$,

$$S(t)m(t) = \tau\ / T_s\, m(t) + 2\tau\ / T_s\, [m(t)\, C_1 \cos 2\prod(2f_M)t\ +\ m(t)\, C_2 \cos 2\prod(4f_M)t\ +\ldots] \ldots. \text{(iii)}$$

Therefore, as in instantaneous sampling, a low-pass filter with cutoff at f_M will deliver an output signal $s_o(t)$ given by

$$s_o(t) = \tau\ / T_s\, m(t) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(iv)}$$

With samples of finite duration, it is not possible to completely eliminate the crosstalk generated in a channel, sharply band limited to a bandwidth f_c. If N signals are to be multiplexed, then the maximum sample duration is $\tau = T_s / N$. It is advantageous, for the purpose of increasing the level of the output signal, to make τ as large as possible. For (a), as it is seen in Eq. (iv), $s_o(t)$ increases with τ. However, to help suppress crosstalk, it is ordinarily required that the samples be limited to a duration much less than T_s / N. The result is a large guard time between the end of one sample and the beginning of the next.

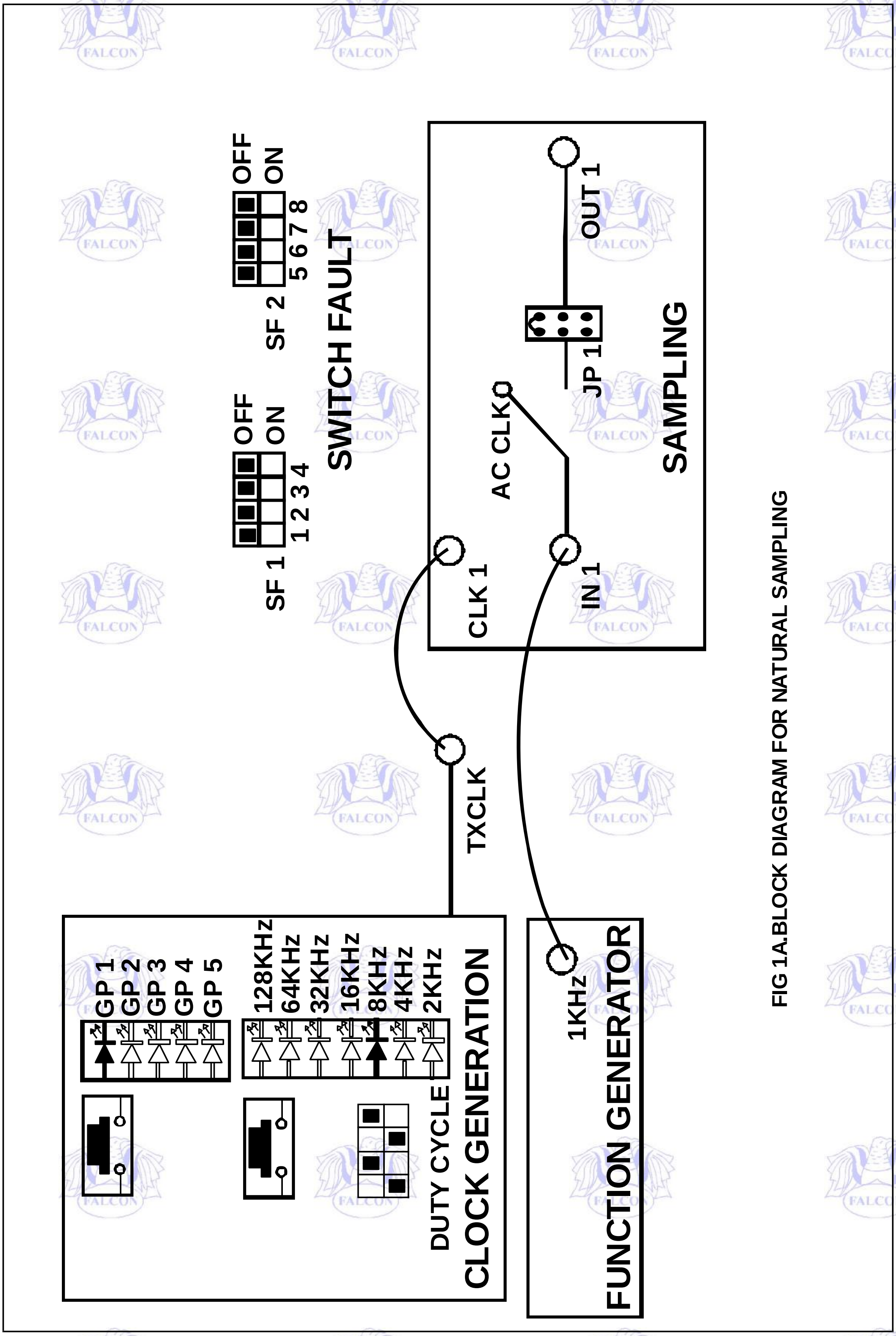
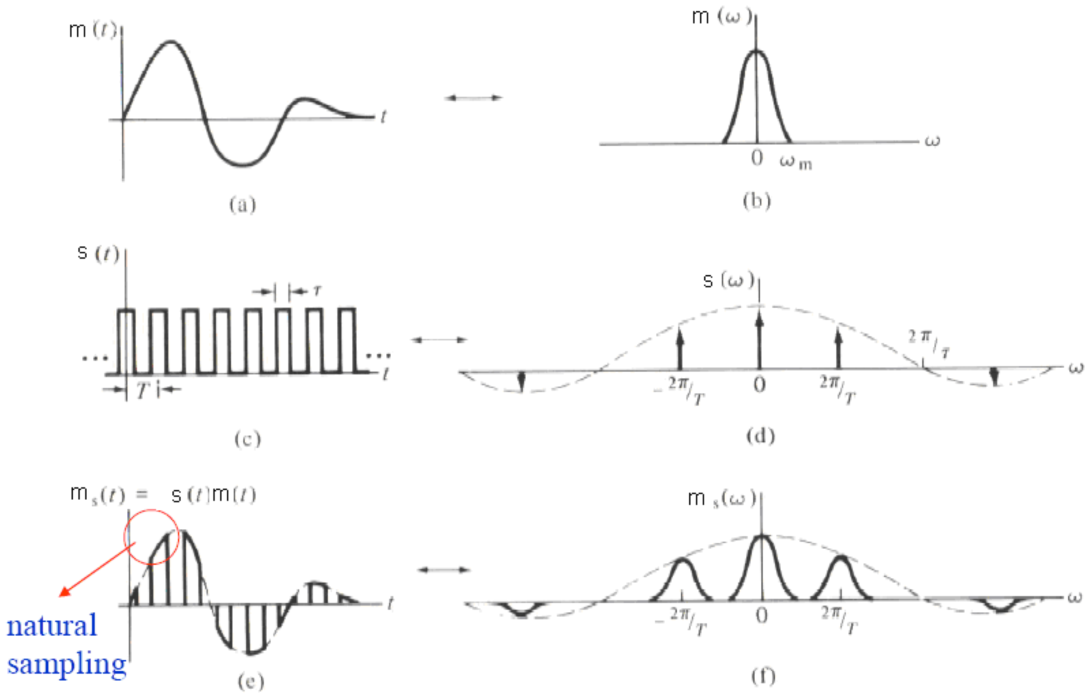


FIG 1A.BLOCK DIAGRAM FOR NATURAL SAMPLING



Natural sampling of a band-limited signal.

EQUIPMENTS

DCS-B kit
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All The Switch Faults In Off Position.

A. NATURAL SAMPLING AND ITS RECONSTRUCTION

PROCEDURE

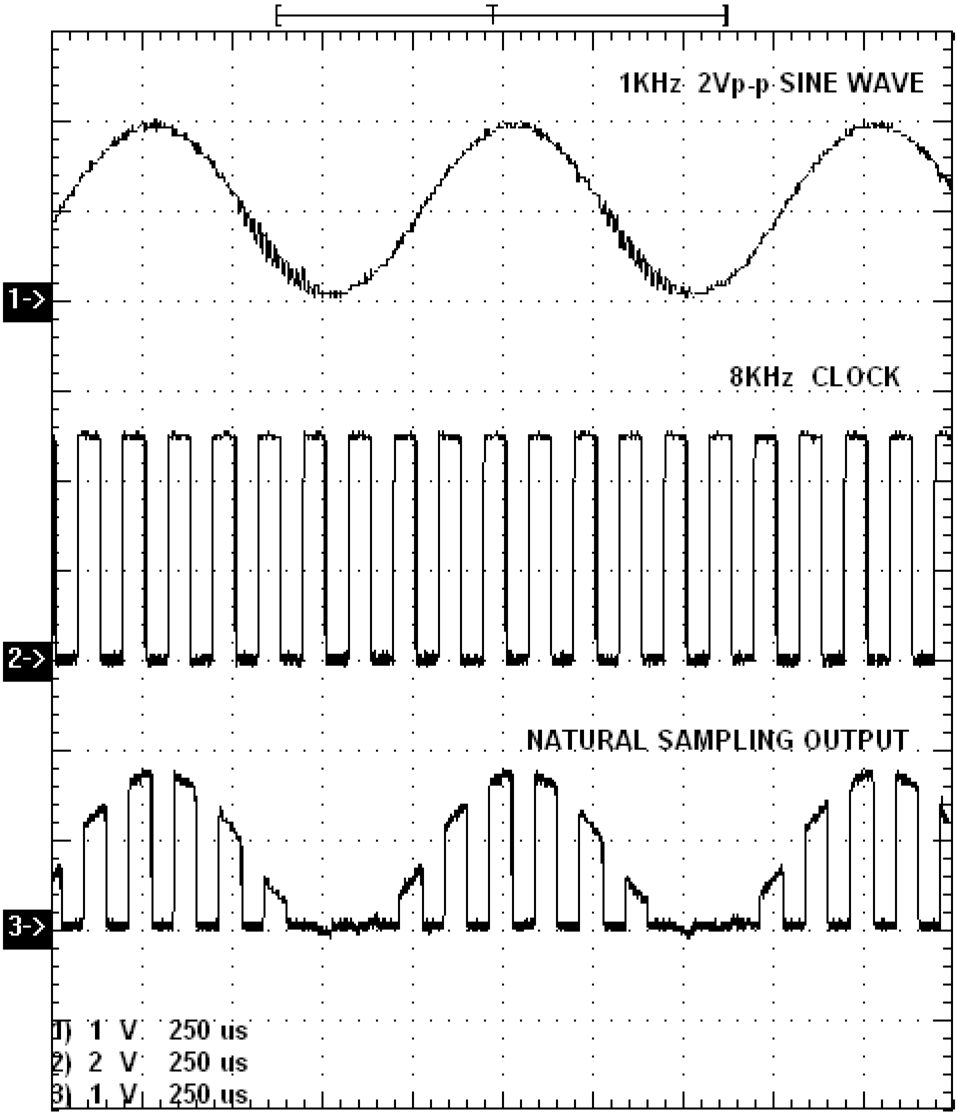
- Ensure that group 1 (**GP1**) clock is selected in the Clock generation section. Selection is done with the help of switch **S1.** Observe the corresponding LED indication.
- Select the sampling clock of frequency 8 KHz using the switch **S2** and observe the corresponding LED indication.
- Adjust the duty cycle of the sampling clock to 50% using Dipswitch **S10** as shown in the block diagram. Sampling clock is available at **TX CLK** post.
- The signal under test, which is in our case, is a sine wave of 1 KHz or 2 KHz, which is available at posts 1 KHz, and **2 KHz** in the Function Generator section.
- Adjust the amplitude of the 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Connect **TX CLK** post to **CLK 1** post and **1 KHz** sine wave to **IN1** post of the Sampling section. To observe the Natural sampling effect, short the jumper **JP1** to **first** position and check the signal at the **OUT1** post of the sampling section.

OBSERVATIONS

- Pressing Switch S1 to select Group1 (GP1) is indicated by corresponding LED.
- Observed that the natural sampled signal consists of a sequence of pulses of varying amplitude whose tops are not flat but follow the waveform of the signal to be sampled. With natural sampling, a signal sampled at the Nyquist rate may be reconstructed by passing the samples through an ideal Low-pass filter.
- Pressing Switch S2 to select sampling frequency of 8 KHz is indicated by corresponding LED.
- Observe the Sampling clock at **TX CLK** post test point.
- Observe the signal under test, i.e. a sine wave, at posts 1 KHz and 2 KHz in the Function Generator section.
- Observe the adjustment in the Amplitude of 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Observe the Natural Sampling effect at the **OUT1** post of the sampling section.

CONCLUSION

Observed that the natural sampled signal consists of a sequence of pulses of varying amplitude whose tops are not flat but follow the waveform of the signal to be sampled. With natural sampling, a signal sampled at the Nyquist rate may be reconstructed by passing the samples through an ideal Low-pass filter.



NATURAL SAMPLING

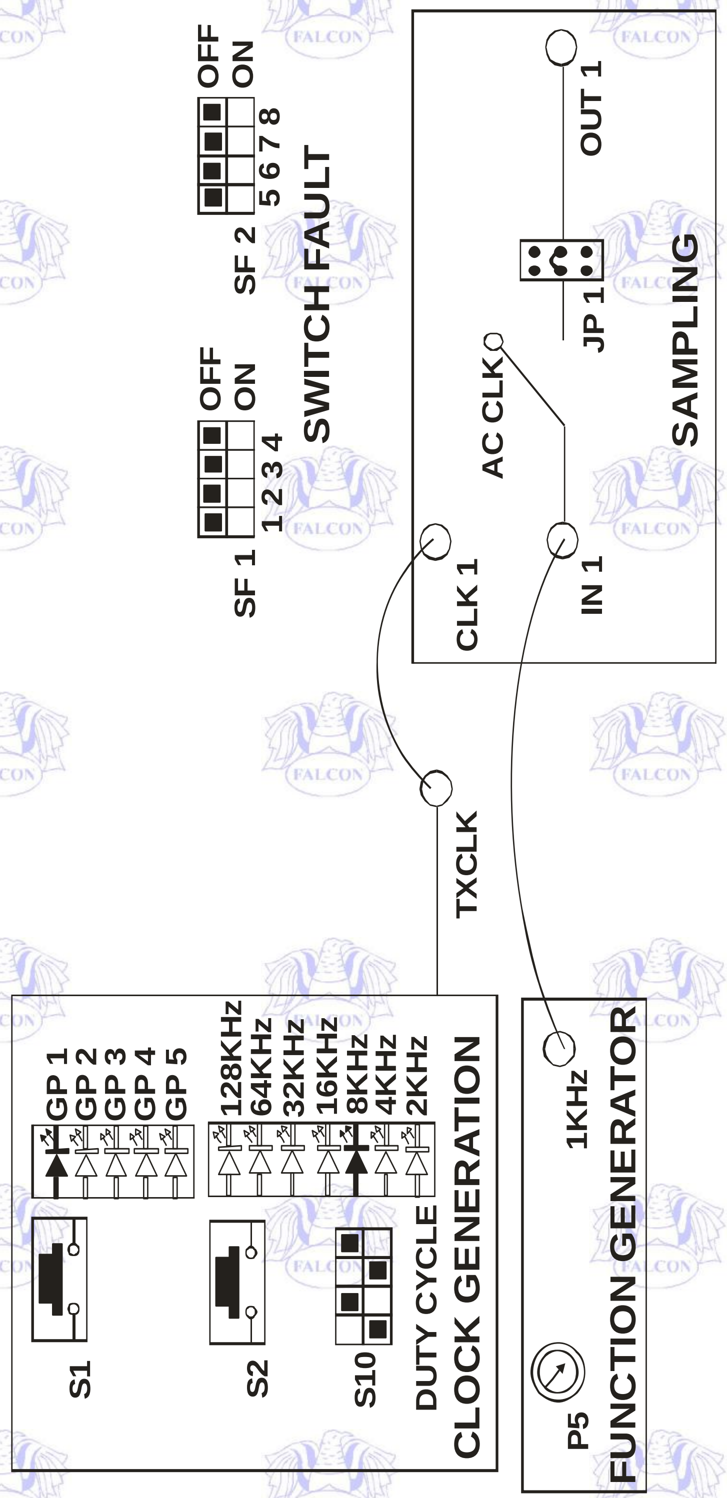
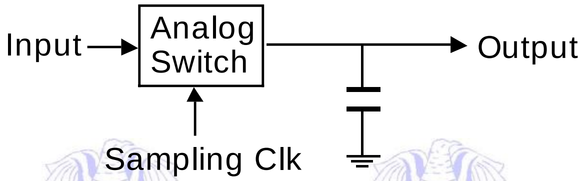
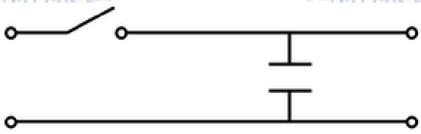


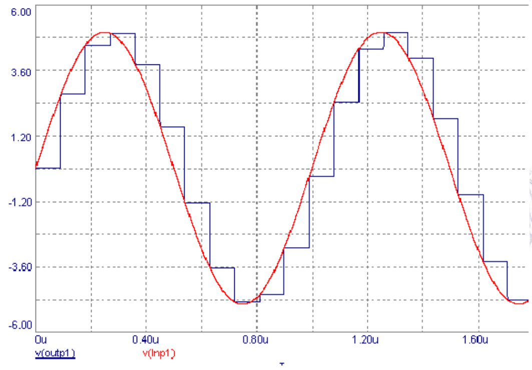
FIG 1B.BLOCK DIAGRAM FOR SAMPLE AND HOLD

B. SAMPLE AND HOLD AND ITS RECONSTRUCTION



In electronics, a sample and hold circuit is used to interface real world, changing analogue signals to a subsequent system such as an analog-to-digital converter. The purpose of this circuit is to hold the analogue value steady for a short time while the converter or other following system performs some operation that takes a little time.
In most circuits, a capacitor is used to store the analogue voltage and an electronic switch or gate is used to alternately connect and disconnect the capacitor from the analog input. The rate at which this switch is operated is the sampling rate of the system.





PROCEDURE

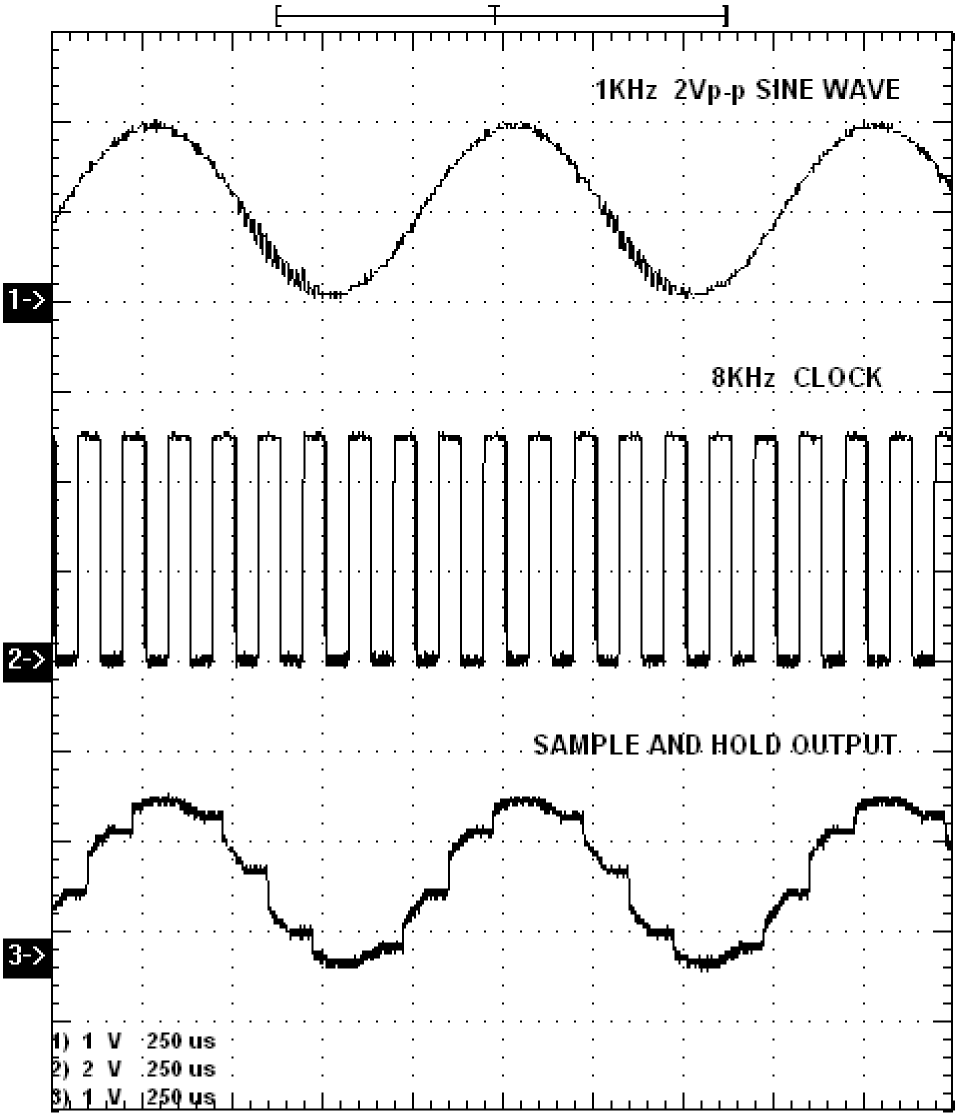
- Ensure that group 1 (**GP1**) clock is selected in the Clock generation section. Selection is done with the help of switch **S1**, observe the corresponding LED indication.
- Select the sampling clock of frequency 8 KHz using the switch **S2** and observe the corresponding LED indication.
- Adjust the duty cycle of the sampling clock to 50% using DIP switch **S10** as shown in the block diagram. Sampling clock is available at **TX CLK** post.
- The signal under test, which in our case is a sine wave of 1 KHz or 2 KHz is available at posts **1 KHz** and **2 KHz** in the Function Generator section.
- Adjust the amplitude of the 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Connect **TX CLK** post to **CLK 1** post and **1 KHz** sine wave to **IN1** post of the Sampling section.
- To observe the Sample and Hold effect, short the jumper **JP1** to **Second** position and check the signal at the **OUT1** post of the sampling section.

OBSERVATIONS

- Pressing Switch S1 to select Group1 (GP1) is indicated by corresponding LED.
- Pressing Switch S2 to select sampling frequency of 8 KHz is indicated by corresponding LED.
- Observe the Sampling clock at **TX CLK** post test point.
- Observe the signal under test, i.e. a sine wave, at posts 1 KHz and 2 KHz in the Function Generator section.
- Observe the adjustment in the Amplitude of 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Observe the Sample & Hold effect at the **OUT1** post of the sampling section.

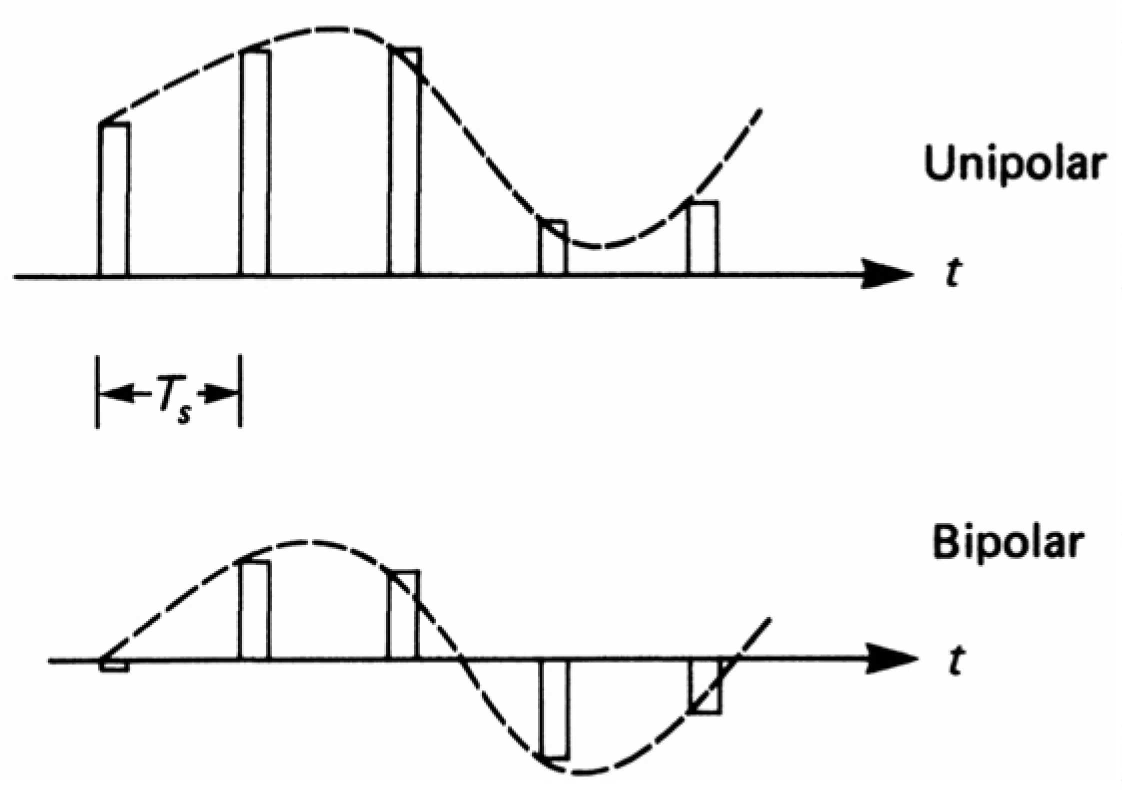
CONCLUSION

In Sample and Hold, we can observe that during on time of Clock capacitor C charges abruptly to a voltage proportional to the sample value and during OFF time of the clock capacitor holds this voltage until the operation is repeated for next sample.



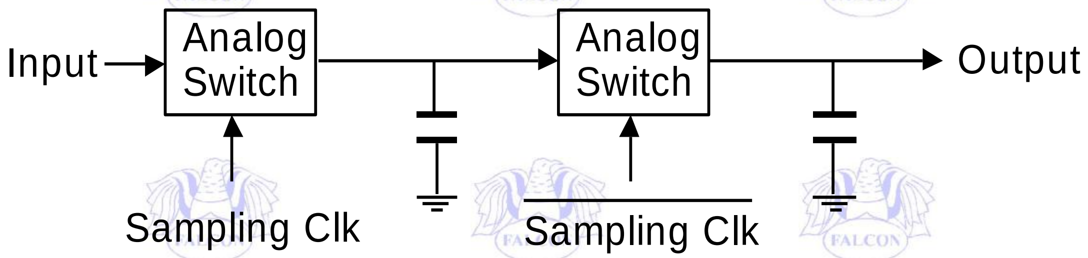
SAMPLE AND HOLD

To illustrate the effect of flat-top sampling, let us assume that the signal m(t) has a flat spectral density equal to M_o over its entire range from o to f_M, as shown



in the figure. The form of the transform of the instantaneously sampled signal is shown in the figure.
The sampling frequency $f_s = 1/T_s$ is assumed large enough to allow for a guard band between the spectrum of the base band signal and the DSB-SC signal with carrier f_s. The spectrum of the flat-top sampled signal is shown in the figure. A low-pass filter reconstructs the original signal.

C. FLAT TOP SAMPLING AND ITS RECONSTRUCTION



A flat-top pulse has constant amplitude established by the sample value of the signal at some point within the pulse interval. Flat-top sampling simplifies the design of the electronic circuitry used to perform the sampling operation.
To show the extent of the distortion, consider the signal m (t) having a Fourier transform M (jω). The transform of the sampled signal for flat-top sampling is determined by considering that the flat-top pulse can be generated by passing the instantaneously

sampled signal through a network which broadens a pulse of duration dt (an impulse) into a pulse of duration τ. The transform of a pulse of unit amplitude and width dt is

F [impulse of strength dt at t = 0] = dt ……….. (i)

The transform of a pulse and unit amplitude is

Sin (ωt/2)[pulse, amplitude = 1,extending from t = -τ /2 to t = τ /2] = τ -------(ii)…. (ωt/2)
Hence the transfer function of the network is

$$H(j\omega) = \frac{\tau \sin(\omega t/2)}{dt \quad (\omega t/2)} \quad \ldots\ldots \text{(iii)}$$

Let the signal m (t), with the transform M (jω), be band limited to f_M and be sampled at the Nyquist rate or faster. Then in the range of 0 to f_M the transform of the flat-topped sampled signal is given by the product H (jω) (jω) or from Eq. (i), (ii) an τ sin (ωt/2)

PROCEDURE

- Ensure that group 1 (**GP1**) clock is selected in the Clock generation section. Selection is done with the help of switch **S1.** Observe the corresponding LED indication.
- Select the sampling clock of frequency 8 KHz using the switch **S2** and observe the corresponding LED indication.
- Adjust the duty cycle of the sampling clock to 50% using DIP switch **S10** as shown in the block diagram. Sampling clock is available at **TX CLK** post.
- The signal under test, which in our case is a sine wave of 1 KHz or 2 KHz is available at posts **1 KHz** and **2 KHz** in the Function Generator section.
- Adjust the amplitude of the 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Connect **TX CLK** post to **CLK 1** post and **1 KHz** sine wave to **IN1** post of the Sampling section.
- To observe the Flat-top sampling effect, short the jumper **JP1** to **FT** position and check the signal at the **OUT1** post of the sampling section.
- Repeat the above procedure from steps 5 to 7 using 2 KHz as an input signal.

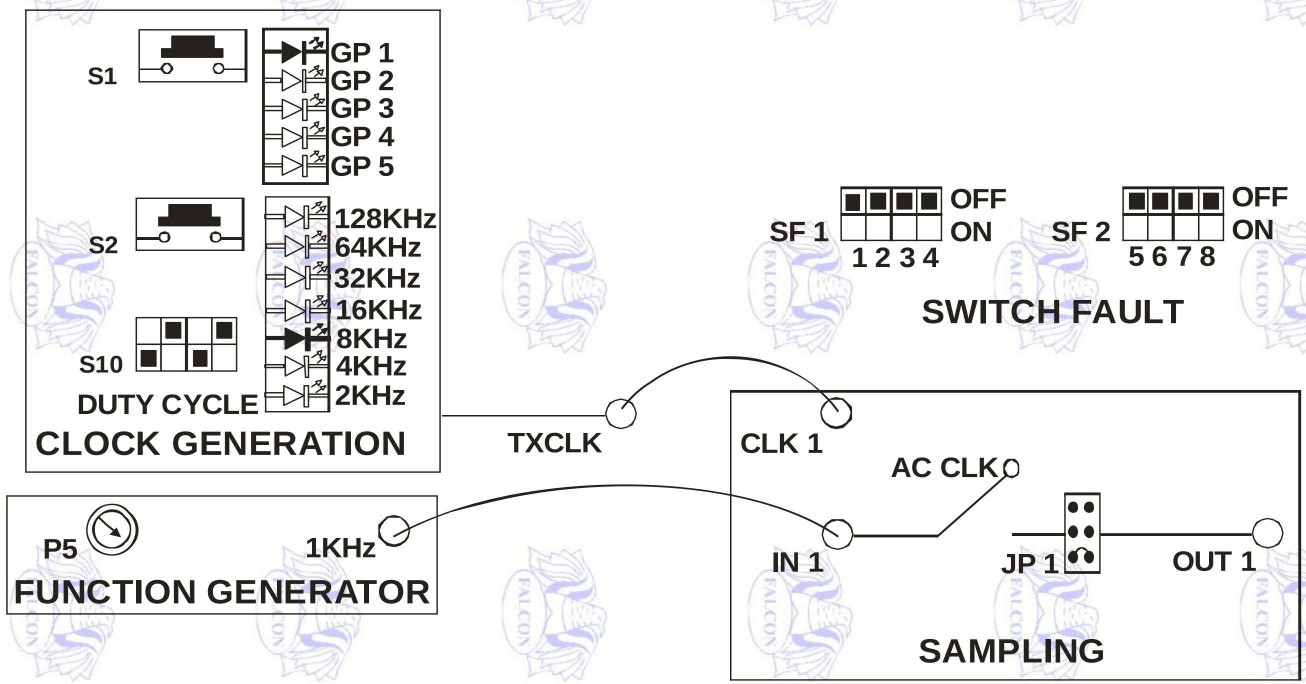


FIG 1C.BLOCK DIAGRAM FOR FLAT-TOP SAMPLING

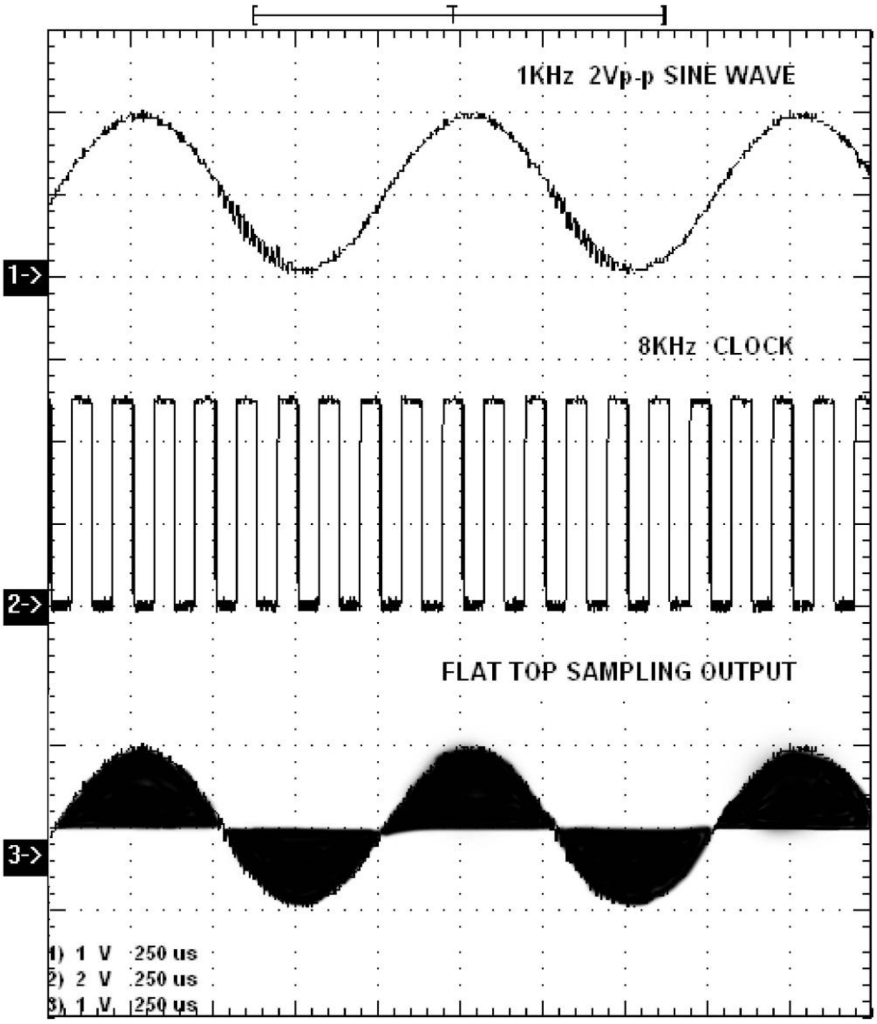
OBSERVATIONS

- Pressing Switch S1 to select Group1 (GP1) is indicated by corresponding LED.
- Pressing Switch S2 to select sampling frequency of 8 KHz is indicated by corresponding LED.
- Observe the Sampling clock at **TX CLK** post test point.
- Observe the signal under test, i.e. a sine wave, at posts 1 KHz and 2 KHz in the Function Generator section.
- Observe the adjustment in the Amplitude of 1 KHz and 2KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Observe the Flat-Top Sampling effect at the **OUT1** post of the sampling section.

CONCLUSION

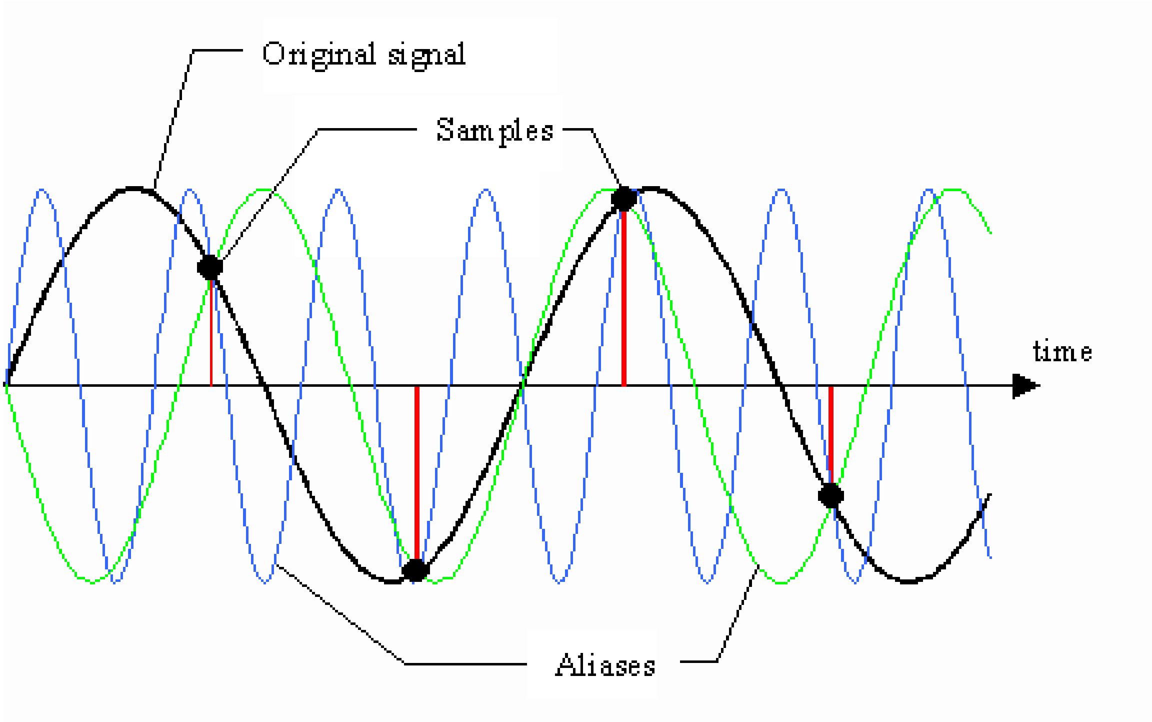
In Flat top sampling, we arbitrarily sampled the signal at the beginning of the pulse. In sampling of this type the original analog signal cannot be recovered exactly by simply passing the samples through an ideal Low pass filter. However, the distortion need not be large. Flat Top sampling has the merit that it simplifies the design of the electronic circuitry used to perform the sampling operation.

Comparing the reconstructed output of 2^{nd} order Low Pass Butterworth Filter for all the three types of sampling, it is observed that the output of the sample and hold is the best as compared to the output of natural sampling and the output of the flat top sampling.

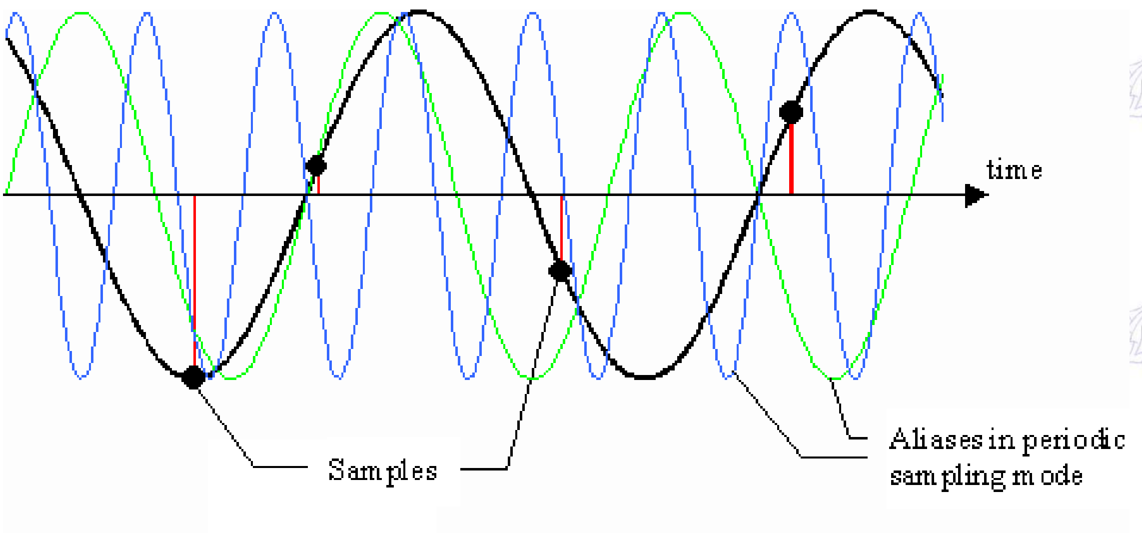


Flat Top Sampling

Illustration of the aliasing effect taking place in the case of periodic sampling



Only one sine function goes exactly through the no uniformly spaced sample values:



NAME

Effect of Various Sampling Frequencies & Duty Cycles

OBJECTIVES

To study the effect of different sampling frequencies on the sampling and reconstructed signal:
A. Study the Effect of Different Sampling Frequencies
B. Study the Effect of Duty Cycles

THEORY

When the continuous analog signal is sampled at a frequency F, the resulting discrete signal has more frequency components than the analog signal. To be precise, the frequency components of the analog signal are repeated at the sample rate. That is, in the discrete frequency response they are seen at their original position and are also seen centered around +/- F and around +/- 2F, etc. How many samples are necessary to ensure that we are preserving the information contained in the signal? If the signal contains high frequency components, we will need to sample at a higher rate to avoid losing information that is in the signal. In general, to preserve the full information in the signal, it is necessary to sample at twice the maximum frequency of the signal. This is known as the Nyquist rate. The Sampling Theorem states that a signal can be exactly reproduced if it is sampled at a frequency F, where F is greater than twice the maximum frequency in the signal.
What happens if we sample the signal at a frequency that is lower than the Nyquist rate? When the signal is converted back into a continuous time signal, it will exhibit a phenomenon called aliasing. Aliasing is the presence of unwanted components in the reconstructed signal. These components were not present when the original signal was sampled. In addition, some of the frequencies in the original signal may be lost in the reconstructed signal. Aliasing occurs because signal frequencies can overlap if the sampling frequency is too low. Frequencies "fold" around half the sampling frequency - which is why this frequency is often referred to as the folding frequency.
Sometimes, the highest frequency components of a signal are simply noise, or do not contain useful information. To prevent aliasing of this frequency, we can filter out these components before sampling the signal. Because we are filtering out high frequency components and allowing lower frequency components through, this is known as low-pass filtering.

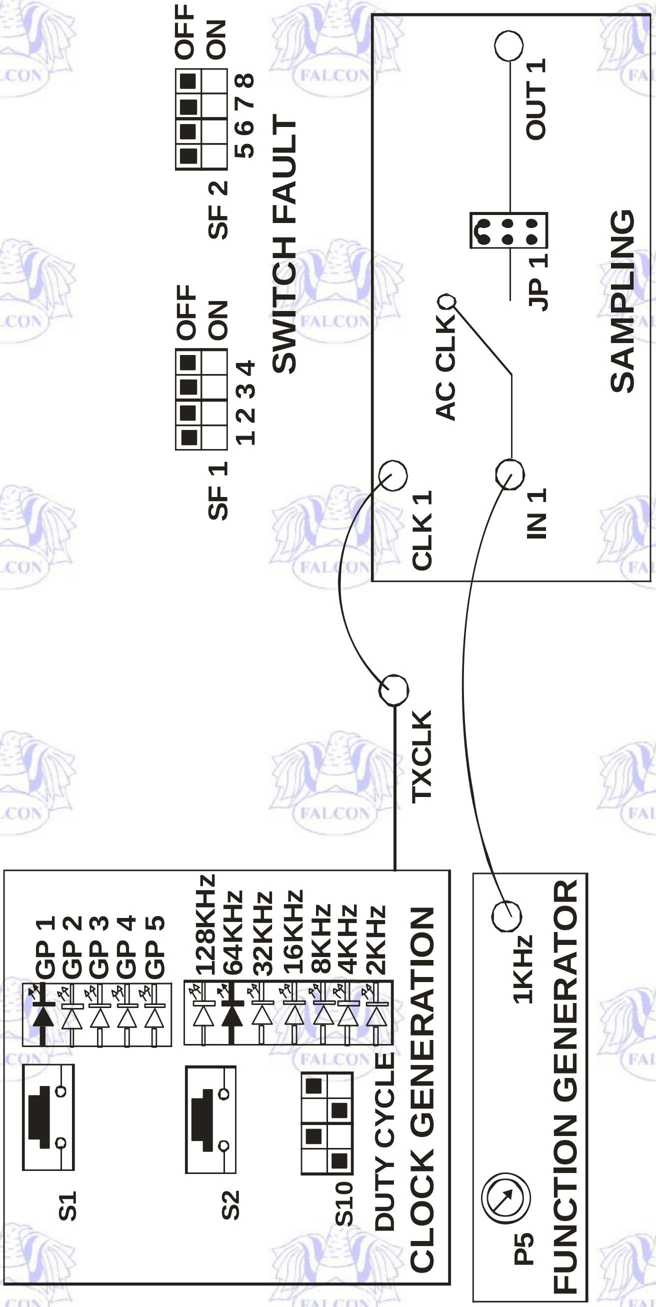


FIG 2A.BLOCK DIAGRAM FOR OBSERVING THE EFFECT OF SAMPLING FREQUENCY

EQUIPMENTS

DCS-B kit
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope

NOTE: Keep All The Switch Faults In Off Position.

A. EFFECT OF SAMPLING FREQUENCY

PROCEDURE

- Ensure that group 1 (**GP1**) clock is selected in the Clock generation section. Selection is done with the help of switch **S1** observe the corresponding LED indication.
- Select the sampling clock of frequency 8 KHz using the switch **S2** and observe the corresponding LED indication.
- Adjust the duty cycle of the sampling clock to 50% using DIP switch **S10** as shown in the block diagram.
- Adjust the amplitude of the 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Connect **TX CLK** post to **CLK 1** post and **1 KHz** sine wave to **IN1** post of the Sampling section.
- Short the jumper **JP1** to **first** position and check the signal at the **OUT1** post of the sampling section.
- Now select the sampling clock of frequency 64 KHz using the switch **S2,** observe the corresponding LED indication.
- Observe its effect at **OUT1** post of the sampling section.
- Similarly, observe the variation in the sampling output by varying the sampling frequencies from 64 KHz to 2 KHz.
- Repeat the above procedure for different sampling techniques.

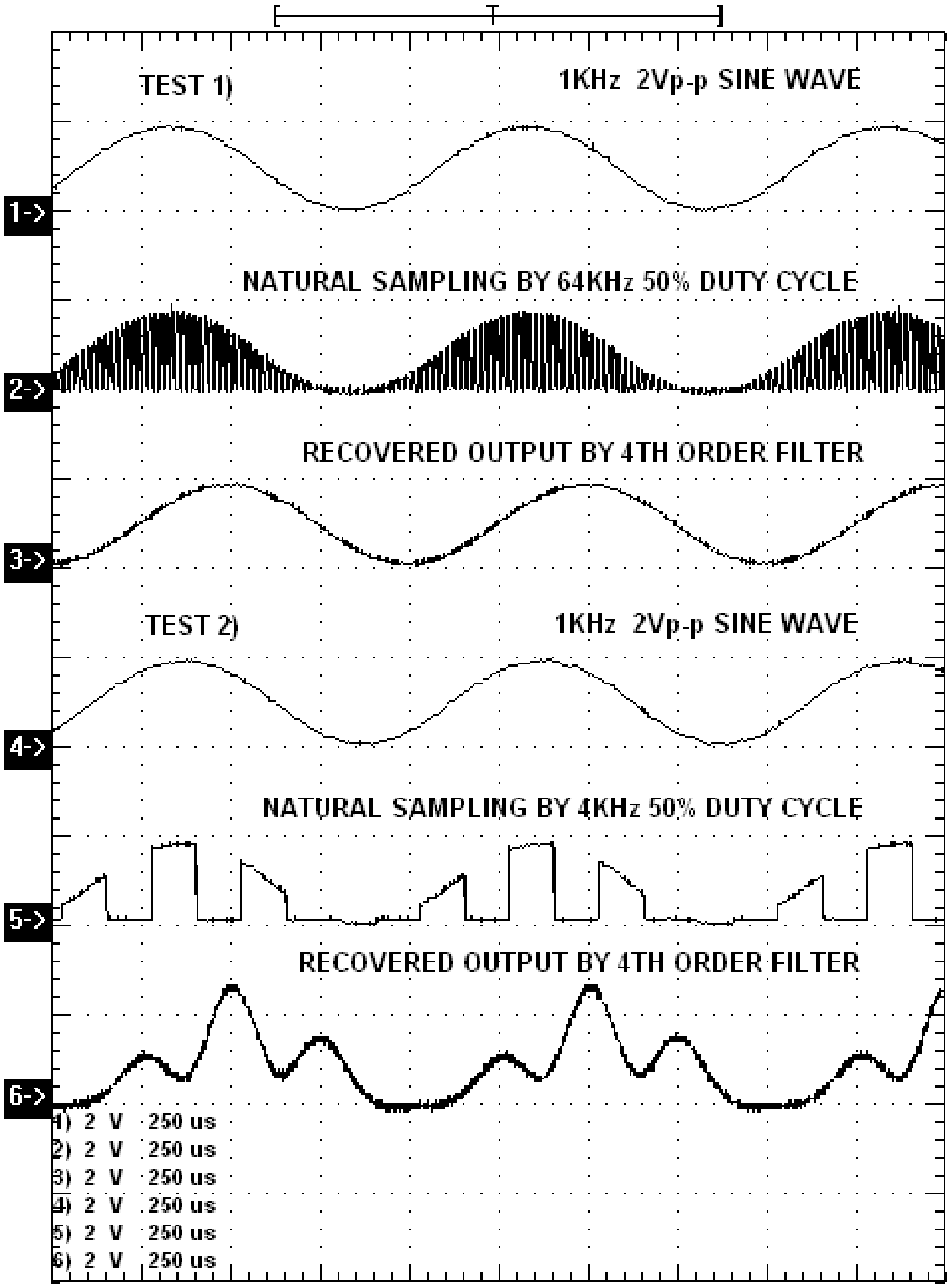
OBSERVATION

- Pressing Switch S1 to select Group1 (GP1) is indicated by corresponding LED.
- Pressing Switch S2 to select sampling frequency of 8 KHz is indicated by corresponding LED.
- Observe the Sampling clock at **TX CLK** post test point.
- Observe the signal under test, i.e. a sine wave, at posts 1 KHz and 2 KHz in the Function Generator section.
- Observe the adjustment in the Amplitude of 1 KHz and 2 KHz sine wave to 2Vpp using pot **P5** and **P6** respectively.
- Observe the Natural Sampling effect at the **OUT1** post of the sampling section.
- Pressing Switch S2 to select sampling frequency of 64 KHz is indicated by corresponding LED.
- Observe its effect at **OUT1** post of the sampling section.

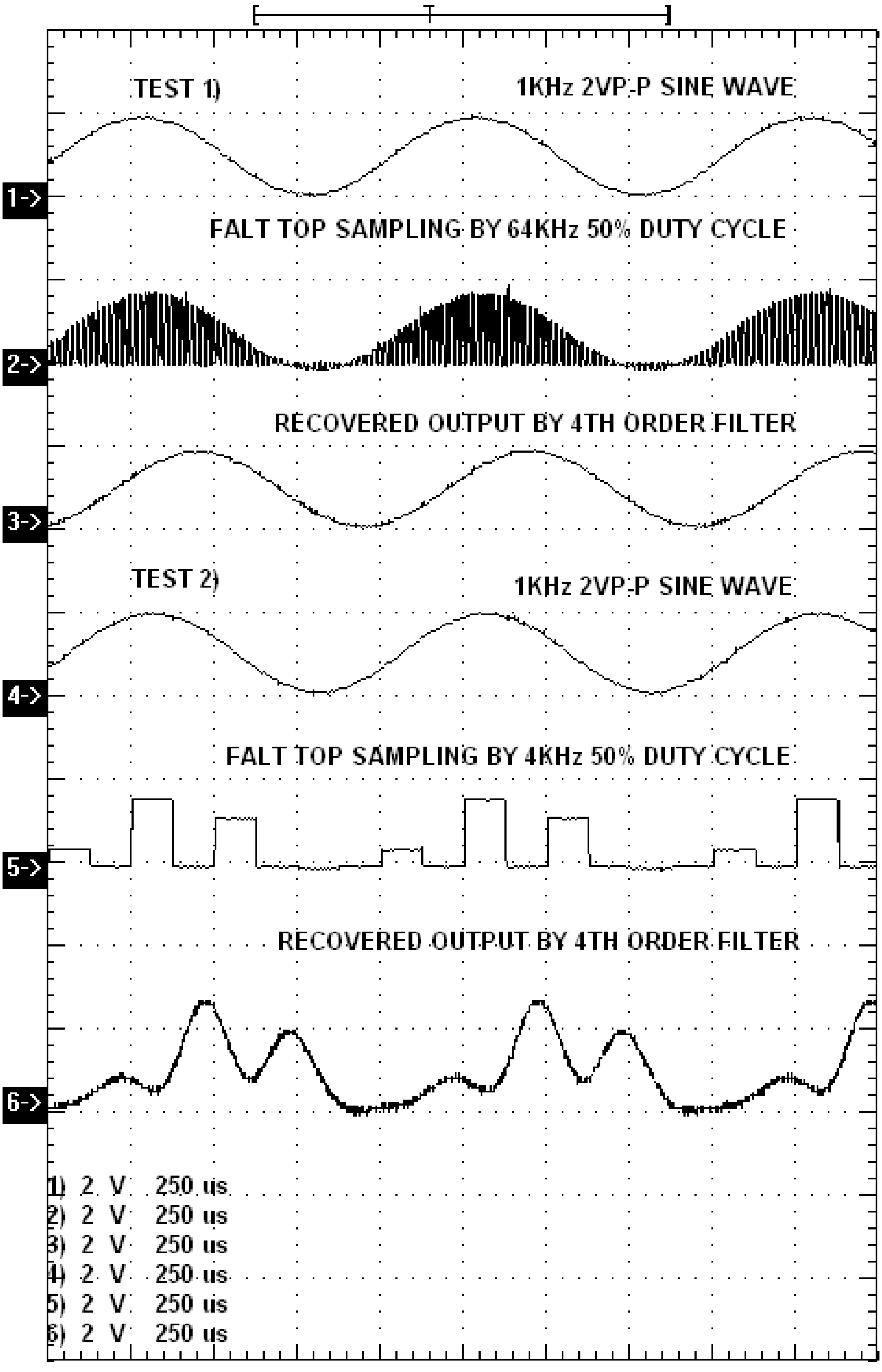
- Similarly, observe the variation in the sampling output by varying the sampling frequencies from 64 KHz to 2 KHz.

CONCLUSION

From the above observations we conclude that when the sampling frequency isincreased the reconstructed output is less distorted and almost original signal isReconstructed.For a sampling frequency of 2 KHz, only 2 samples of the 1 KHz signal are taken, whereas that for a sampling frequency of 8 KHz, 8 samples of 1 KHz signal is taken.Hence, as the number of samples taken of the signal increases, the distortion of the Reconstructed signal decreases. As per the Nyquist Criterion, at least two samples are required for the reconstruction of the signal. If the Nyquist Criterion is not satisfied, or if the signal is not band limited, then spectral overlap, called “aliasing” occurs, causing higher frequencies to show up at lower frequencies in the recovered message.



EFFECT OF SAMPLING FREQUENCY ON NATURAL SAMPLING



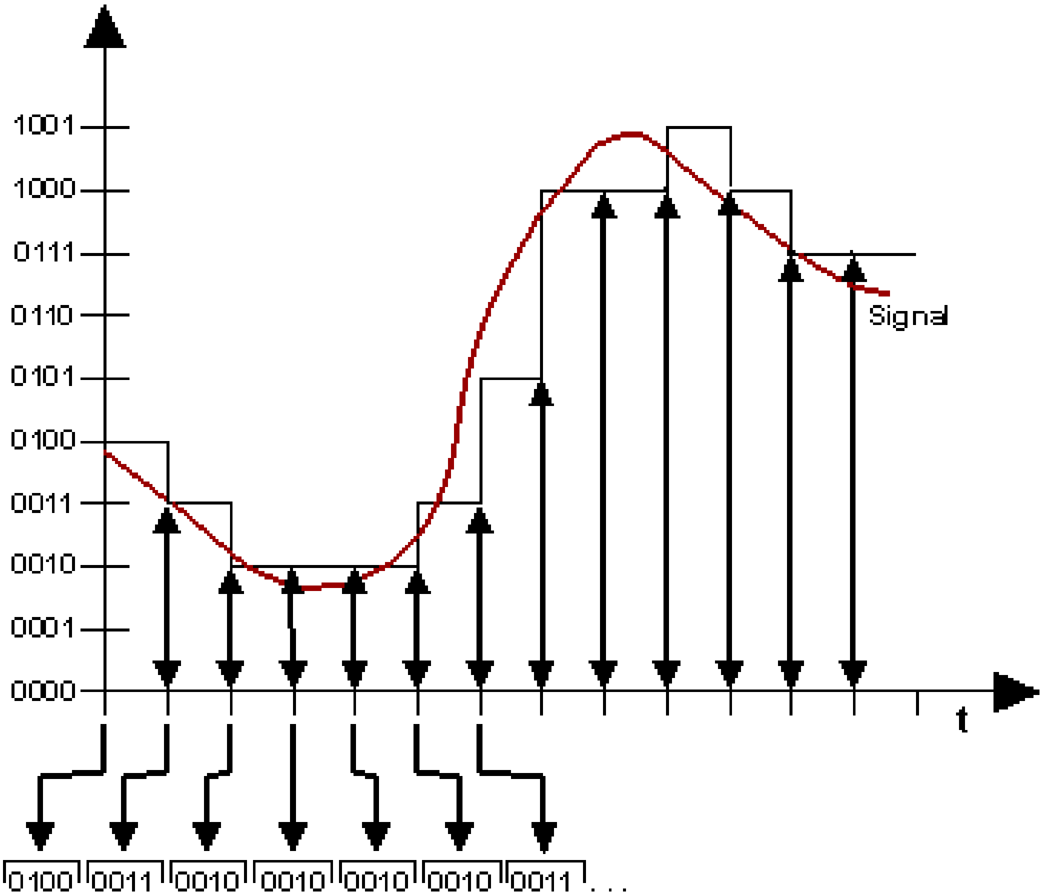
EFFECT OF SAMPLING FREQUENCY ON FLAT TOP SAMPLING

EXPERIMENT NO. 3 (II)

OBJECTIVES

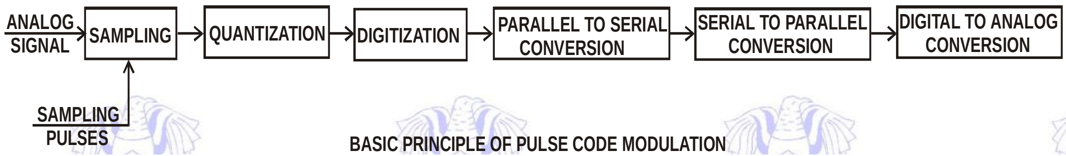
To study the Pulse Code Modulation Technique:

THEORY

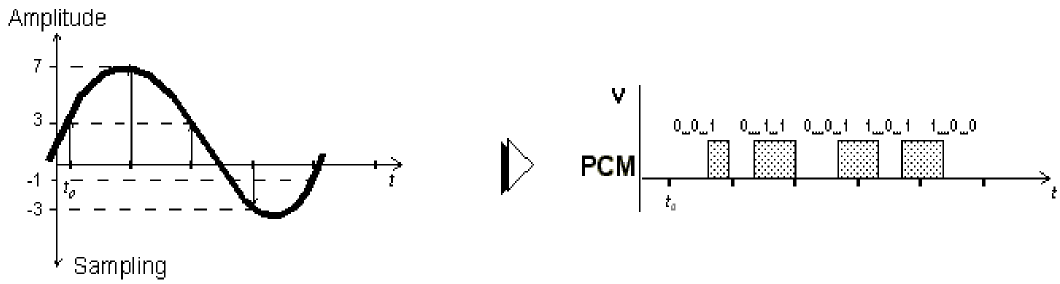


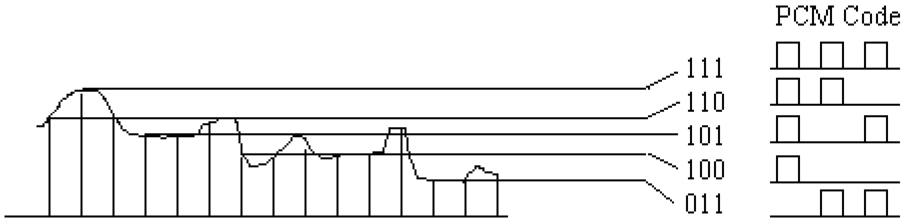
Basic Principle of PCM

The analog signal is sampled at a rate more than the Nyquist rate. Through the process of sampling, a PAM signal is generated. The signal is then quantized and digitized. The parallel data word available after the analog to digital conversion is converted to a serial data stream after coding and it is sent through the channel. This coded data stream is said to be PCM coded data and is transmitted serially by the PCM transmitter.



BASIC PRINCIPLE OF PULSE CODE MODULATION





Quantization

Quantization refers to the process of approximating the continuous set of values in the image data with a finite (preferably small) set of values. It refers to the fact that only certain levels of signal are recognized and transmitted. The input to a quantizer is the original data and the output is always one among a finite number of levels. These levels are decided to accommodate the whole range of amplitudes of the input signal. The signal is then digitized by using an A to D converter. In fact, the quantization is done by this converter. The output of A to D converter may be in binary form or in any other digital code such as excess-3, binary, gray, BCD etc. For giving distinct codes to eight levels, 3-bit binary code will be necessary.

In actual practice, there can be more than 8 levels, say 256 levels. In such a case, an 8-bit code will be generated for each sample. These bits are converted to serial bit stream and these bits are transmitted one after the other.

There are two types of quantization - Scalar Quantization and Vector Quantization. In scalar quantization, each input symbol is treated separately in producing the output; while in vector quantization the input symbols are clubbed together in groups called vectors and processed to give the output. This clubbing of data and treating them as a single unit, increases the optimality of the vector quantizer, but at the cost of increased computational complexity. Here, we'll take a look at scalar quantization.

A quantizer can be specified by its input partitions and output levels (also called reproduction points). If the input range is divided into levels of equal spacing, then the quantizer is termed as a Uniform Quantizer, and if not, it is termed as a Non-Uniform Quantizer. A uniform quantizer can be specified easily by its lower bound and the step size. Also, implementing a uniform quantizer is easier than a non-uniform quantizer. Take a look at the uniform quantizer shown below. If the input falls between n*r and (n+1)*r, the quantizer outputs the symbol n.

On the receiver side, the serial to parallel converter collects and groups the pulses for one sample. If the transmitter generates an 8-bit code per sample then the serial to parallel converter collects 8 pulses of the serial bit stream and passes this 8-bit code to the digital to analog converter. This is done in synchronization.

Fast Mode With Sine Wave

EQUIPMENTS

DCS-B kit
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope
Power connection cables

NOTE: The PCM experiments have two modes of operation i.e. fast mode and slow mode. In fast mode the transmission clock has a frequency of 250 KHz and in the slow mode the transmission clock has a frequency of 32Hz.
The slow mode is used to observe the various data patterns generated during PCM generation and transmission on the LED indications.
In fast mode, sinusoidal signal as well as DC level signal is used as input for PCM generation and its study. In slow mode, only DC level is used for PCM generation.

PROCEDURE

- Ensure that group 3 (**GP3**) clock is selected in the clock generation section. Selection is done with the help of switch **S1**, observe the corresponding LED indication.
- Keep the jumper **JP3** at the fast mode position.
- The selected clock of frequency 230 KHz will be available at the **TXCLK** post.
- Connect **250Hz** signal having voltage around 4V from the Function generator section to the **ADC IN** post of the A/D converter.
- Keep switch **S12** in the **NONE** parity mode and observe the corresponding LED indication.
- Observe the analog to digitally converted bits on the corresponding LED indication (**B0** to **B6**) in the A/D Converter section.
- Observe the Pseudo random bit sequence at the test point marked **PRBS OUT**.
- **TX DATA** post shows multiplexed data having PRBS and PCM data.
- To recover the analog signal from the PCM data at the **TX DATA** post, connect it to the **RX DATA** post.

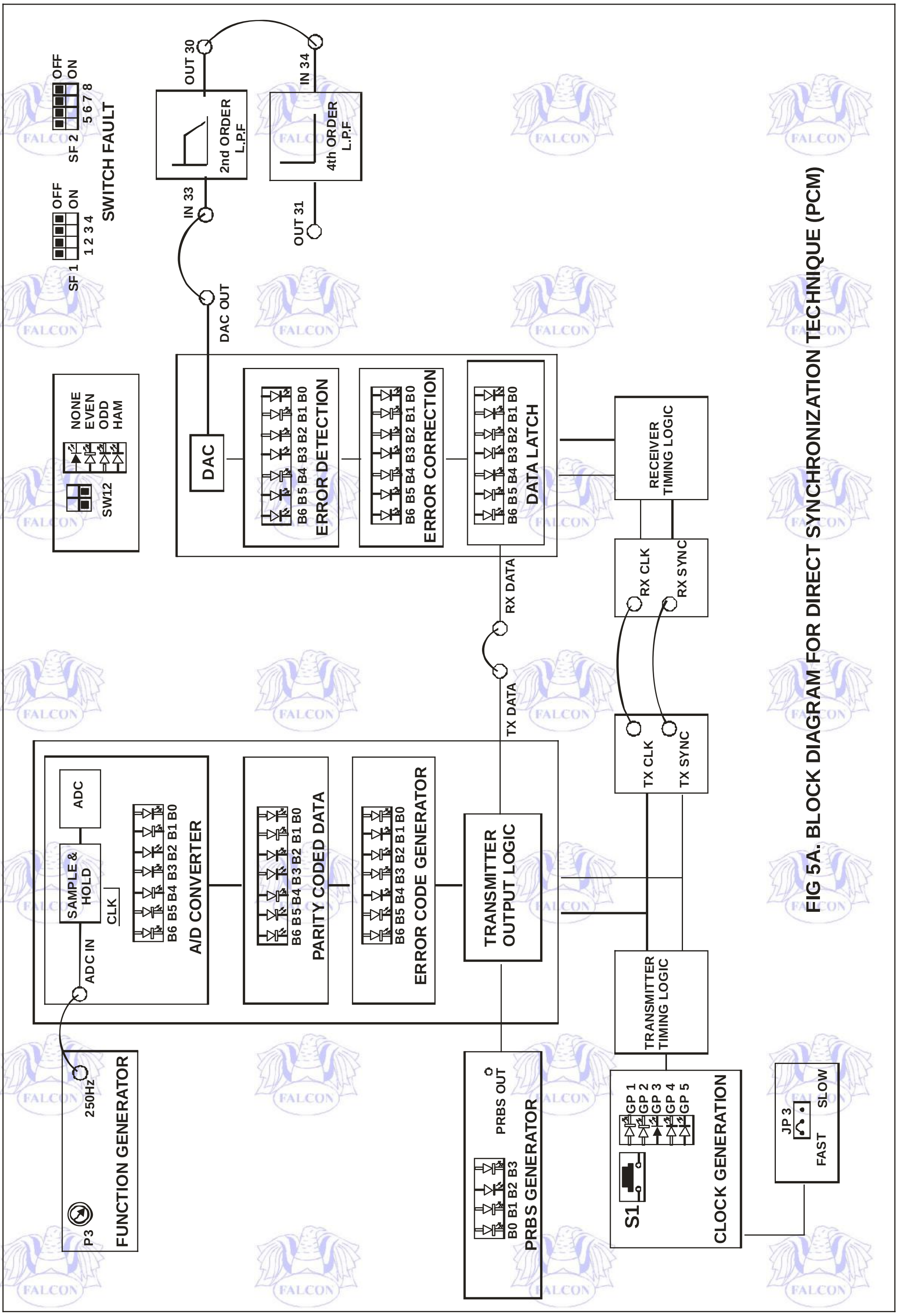


FIG 5A. BLOCK DIAGRAM FOR DIRECT SYNCHRONIZATION TECHNIQUE (PCM)

A. Using Direct Synchronization Technique (TX CLK &TX SYNC Are Transmitted to the Receiver)

PROCEDURE

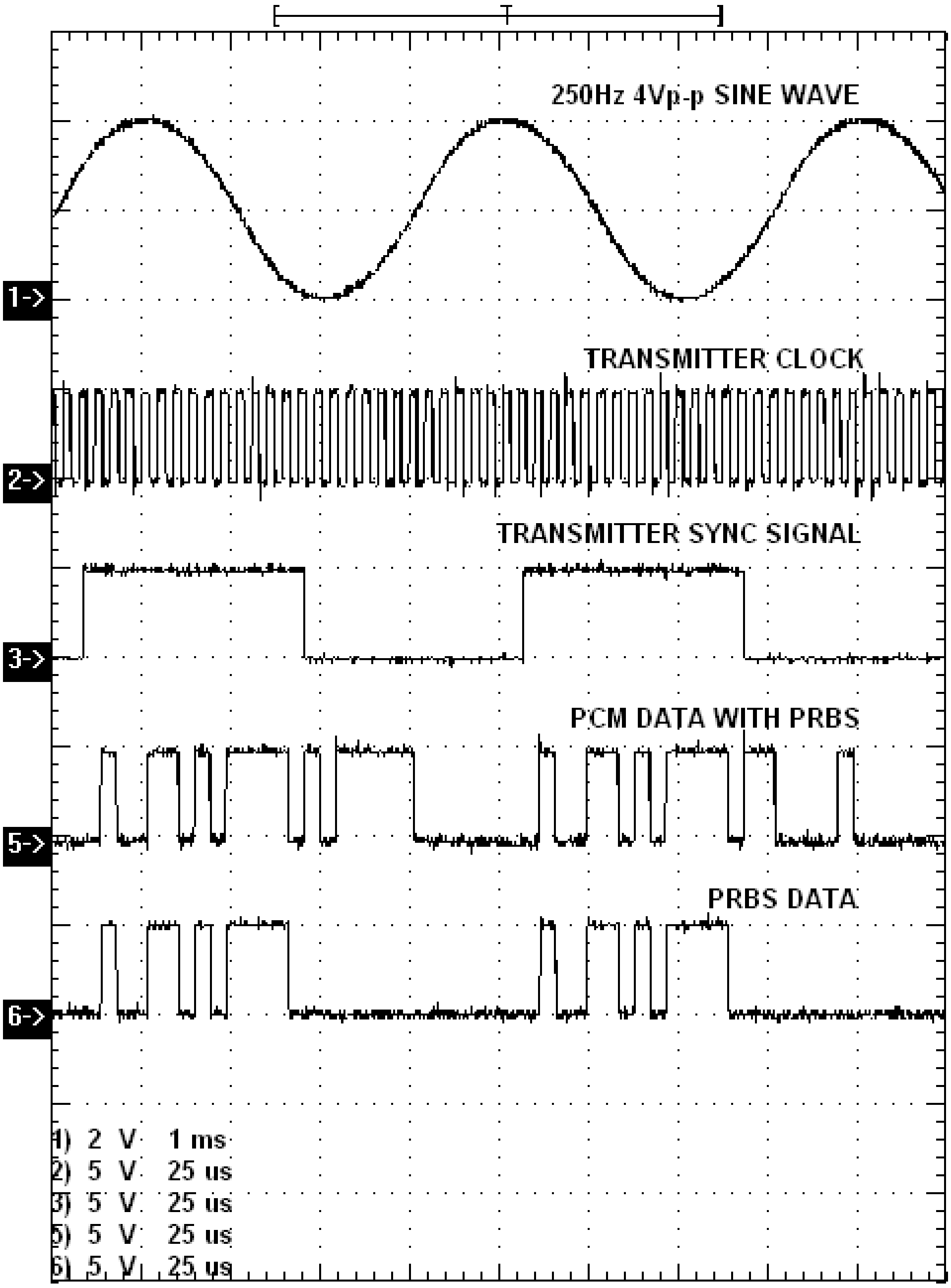
- To provide the timing and synchronization information to the receiver section, connect **TX CLK** post to **RX CLK** post and **TX SYNC** to **RX SYNC** post.
- The serial data is converted to the parallel data & directly observed on the corresponding LED indication at the Data Latch section.
- Observe the D/A converted data at the **DAC OUT** post.
- Connect the **DAC OUT** post to the **IN33** post of the 2nd order LPF. Connect **OUT 30** post of 2nd order LPF to **IN34** post of 4^{th} order LPF.
- Observe the recovered signal at the **OUT31** post of the 4^{th} order LPF.

OBSERVATIONS

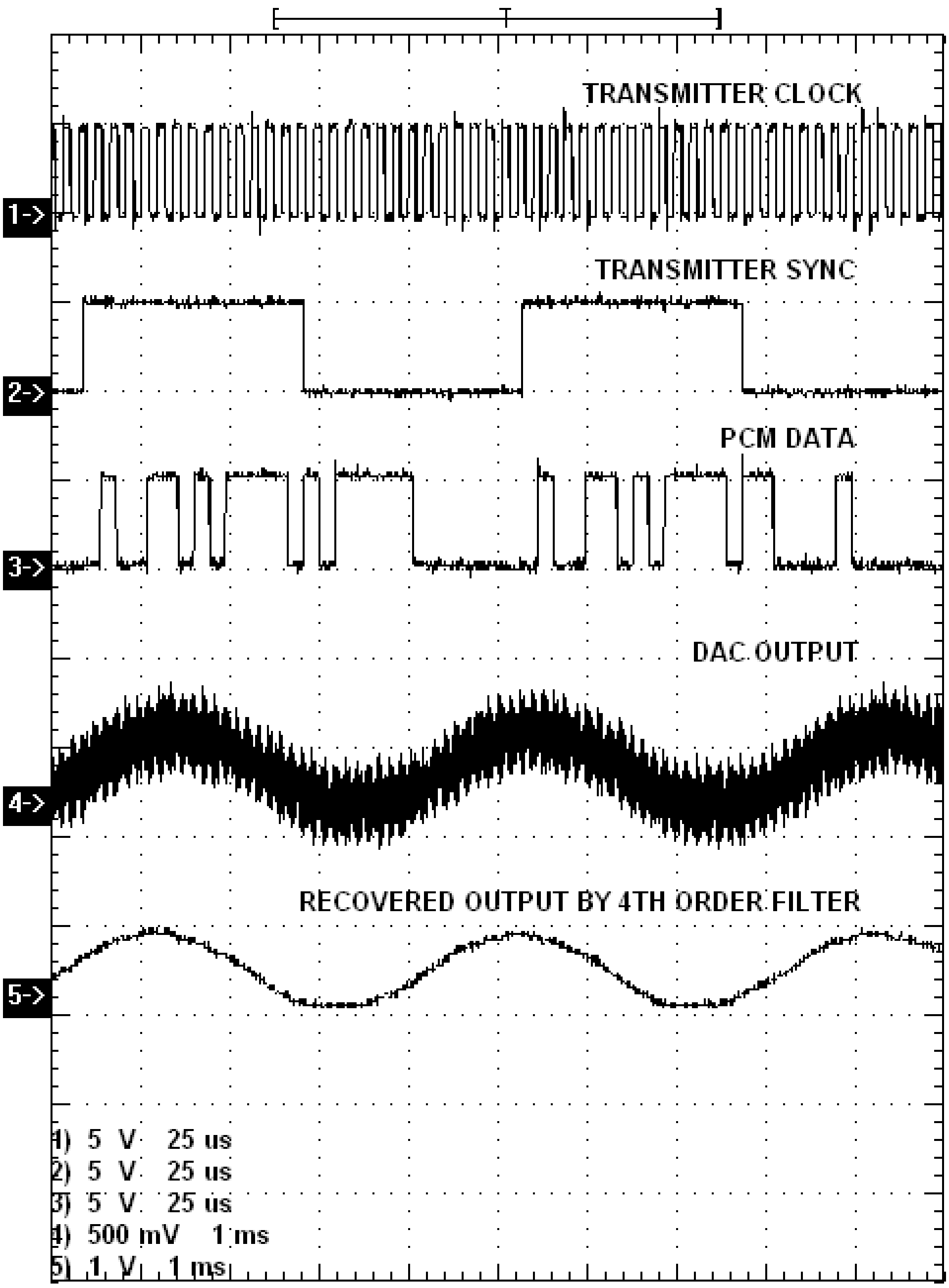
- Input signal
- PCM Data **TX DATA**, **TXCLK**, **TXSYNC**
- PRBS data **PRBS OUT**
- **RXCLK**, **RXSYNC**, **RXDATA**
- **DAC OUT**
- Received signal **OUT 31**

CONCLUSION

At the receiver side, the 4^{th} order low pass butterworth filter is used as a reconstruction unit, which reproduces the signals (sine wave and DC signal levels) same as that of the transmitter side. In this case, it is observed that the reconstructed sine wave has a good linearity.



PCM MODULATION



PCM DEMODULATION USING DIRECT SYNCHRONIZATION TECHNIQUE

EXPERIMENT NO. 3 (III)

NAME

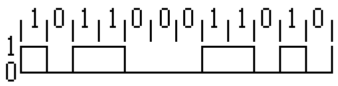
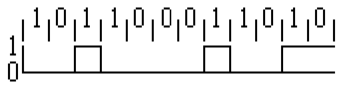
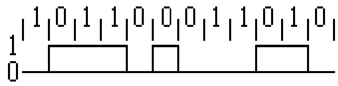
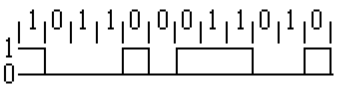
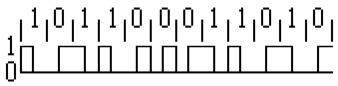
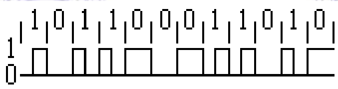
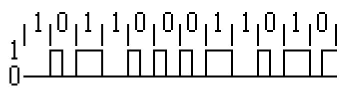
Study of Various Data Encoding and Decoding Techniques

OBJECTIVES

To study the NRZ-L, NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S DATA coding & decoding.

THEORY

ENCODING SCHEMES:

Code Name	Binary Code	Code Definition
NRZ-L		Non-Return-to-Zero Level "One" is represented by one level "Zero" is represented by another level lower the one but not zero.
NRZ-M		Non-Return-to-Zero Mark "One" is represented by a change in level "Zero" is represented by no change in level.
NRZ-S		Non-Return-to-Zero Space "One" is represented by no change in level "Zero" is represented by change in level.
NRZ-I		Non-Return-to-Zero Inverse "One" is represented by no change in level "Zero" is represented by change in level.
Bi-Phase-L		Bi-Phase Level (Split Phase) Level change occurs at the beginning of every bit period "One" is represented by a "One" level with transition to the "Zero" level "Zero" is represented by a "Zero" level with transition to the "One" level.
Bi-Phase-M		Bi-Phase Mark Level change occurs at the beginning of every bit period "One" is represented by a midbit level change "Zero" is represented by no midbit level change.
Bi-Phase-S		Bi-Phase Space Level change occurs at the beginning of every bit period "One" is represented by no midbit level change "Zero" is represented by a midbit level change.

Once the carrier is recovered, the data can be detected by comparing the phase of the received modulated carrier with the phase of the reference carrier.

NON - RETURN TO ZERO signal are the easiest formats that can be generated. These signals do not return to zero with the clock. The frequency component associated with these signals are half that of the clock frequency. The following data formats come under this category. Non-return to zero encoding is commonly used in slow speed communications interfaces for both synchronous and asynchronous transmission. Using NRZ, logic 1 bit is sent as a high value and logic 0 bit is sent as a low value.

A) Non-Return to zero - LEVEL - NRZ-L
B) Non-Return to zero - MARK - NRZ-M
C) Non-Return to zero - SPACE - NRZ-S

A) NON-RETURN TO ZERO - LEVEL (NRZ-L):
This is the most extensively used waveform in digital logics. The data format is very simple where all ‘ones’ are represented by `high’ and all `zeros’ by `low’. The data format is directly available at the output of all digital data generation logics and hence very easy to generate. Here, all the transitions take place at the rising edge of the clock.

B) NON-RETURN TO ZERO - MARK (NRZ-M):
These waveforms are extensively used in magnetic tape recording. In this data format, all ‘ones’ are marked by change in levels and all “zeros’ by no transitions and the transitions take place at the rising edge of the clock.

C) NON-RETURN TO ZERO - SPACE (NRZ-S),
This type of waveform is marked by change in levels for `zeros’ and no transition for `ones’ and the transitions take place at the rising edge of the clock. This format is also used in magnetic tape recording.

D) UNIPOLAR AND BIPOLAR:
Unipolar signals are those signals, which have transition between 0 to +VCC. Bipolar signals are those signals, which have transition between +VCC to -VCC.

THE CODING OF BASIC DATA NRZ-L INTO NRZ-M AND NRZ-S FORMAT CAN BE UNDERSTOOD BY REFERING TO THE CIRCUIT DESCRIPTION MANUAL AND THE WAVEFORMS.

For the decoding the NRZ coded data, firstly the clock is recovered from the incoming coded data by using Phase Locked Loop techniques on kit DCL-06. Waveforms show the data stream and clock using a typical NRZ-L protocol. In this data format, ‘ones’ are represented by highs and ‘zeros’ are represented by lows. In the data stream, it should be guaranteed that continuously more than 5 zeros or 5 ones should not occur in succession while transmitting data.
This ensures that the slowest rate of changes will then be a frequency corresponding to one-twelfth clock. The fastest rate of change of frequency will correspond to one-half of the clock frequency with alternate one and zeroes occurring in the data stream.
This phase -encoded -group consists of:
a) Biphase - Level (Popularly known as Manchester Coding)
b) Biphase - Mark
c) Biphase - Space

These schemes are used in magnetic recording, optical communications and in satellite links. These phase encoded signals are special because they are composed of both the in phase and out of phase components of the clock.

A) BIPHASE-LINE CODING (BIPHASE-L) - (MANCHESTER CODING):
With the Biphase-L, `one' is represented by a half bit wide pulse, positioned during the first half of the bit interval and a `zero' is represented by a half bit wide pulse positioned during the second half of the bit interval.

B) BIPHASE MARK CODING (BIPHASE-M):
With the Biphase-M, a transition occurs at the beginning of every bit interval. A `one' is represented by a second transition, half bit later, whereas a zero has no second transition.

C) BIPHASE SPACE CODING (BIPHASE -S):
With a Biphase-S, a transition occurs at the beginning of every bit interval. A `zero' is marked by a second transition, one half bit later; `one' has no second transition.

The coding of basic data NRZ-L into Biphase-L, Biphase-M, and Biphase-S format can be understood easily by referring to circuit diagram and Waveforms.
Biphase-Line Coding is a synchronous clock coding technique used by the OSI physical layer (in LAN) to encode the clock and data of a synchronous bit stream. In this technique, the actual binary data to be transmitted over the cable are not sent as a sequence of logic 1's and 0's (known technically as Non Return to Zero (NRZ)). Instead, the bits are translated into a slightly different format that has a number of advantages over the use of straight binary encoding (i.e. NRZ).
Biphase-Line Coding follows the rules shown below:

Original	Data Value Sent
Logic 0	0 to 1 (upward transition at bit centre)
Logic 1	1 to 0 (downward transition at bit centre)

Example of Biphase-Line Coding:
The pattern of bits " 0 1 1 1 1 0 0 1 " encodes to " 01 10 10 10 10 01 01 10".
Another more curious example is the pattern " 1 0 1 0 1 etc" which encodes to "10 01 10 01 10 " which could also be viewed as "1 00 11 00 11 0 ". Thus, for a 10 Mbps Ethernet LAN, the preamble sequence encodes to a 10 MHz square wave.
The recovery circuit of Biphase coded signal is quiet simple as compared to NRZ or URZ signals because the bi-phase signals have one transition per cycle of the clock, irrespective of the transmitted data. So these signals ensure sufficient number of transitions in the data stream. But, one disadvantage in bi-phase signals is that they do not provide phase continuity in the transmitted data stream.

A) RETURN TO ZERO SIGNALS:
These signals are called “Return to Zero signals”, since they return to `zero' with the clock. In this category, there is only one data format, i.e., the unipolar return to zero (URZ).
In the URZ a `one' is represented by a half bit wide pulse and a `zero' is represented by the absence of a pulse.

EQUIPMENTS

DCS-B kit
Connecting Chords
Power supply
20 MHz Dual Trace Oscilloscope
Power connection cables

A. NRZ-L, NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S CODING & DECODING

PROCEDURE

- Ensure that the group 4 (**GP4**) clock is selected in the Clock Generation section. Selection is done with the help of switch **S1.** Observe the corresponding LED indication.
- Observe the transmitter clock of frequency **250 KHz** at **TXCLK** post.
- Set the data pattern using switch **S4** as shown in the block diagram.
- Observe the 8-bit data pattern at **S DATA** post.
- Connect **S DATA** to **IN16** post and **TXCLK** to **CLK2** post of the Encoded Data section.
- Observe the encoded data at the **OUT10** post of the Encoded Data section. Selection of the different encoded data's are done using switch **S3**. The selected encoded data is indicated on the corresponding LED indication in the Encoded Data section.
- Connect **OUT10** to **IN27** post of the Decoded Data section.
- Observe the recovered clock at **REC.CLK2** test point of the Decoded Data section.
- Observe the decoded data at **OUT23** post of the Decoded Data section.
- We can observe the decoded data as per the selected encoded data.

OBSERVATIONS

Transmitter Clock	**Txclk**
Simulated Data	**Sdata**
Encoded Data	**Out 10**
Ami Encoded Data	**Out 11**
Recovered Clock	**Rec.Clk2**
Decoded Data	**Out 23**
Ami Decoded Data	**Out 22**
Bipolar Data	**Out 6**
Unipolar Data	**Out 7**

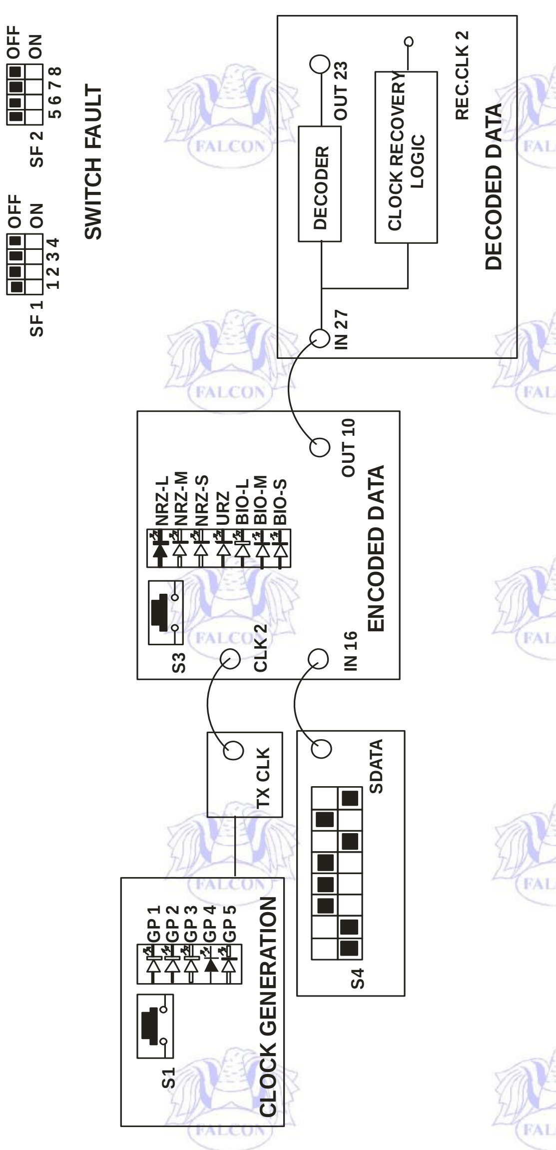
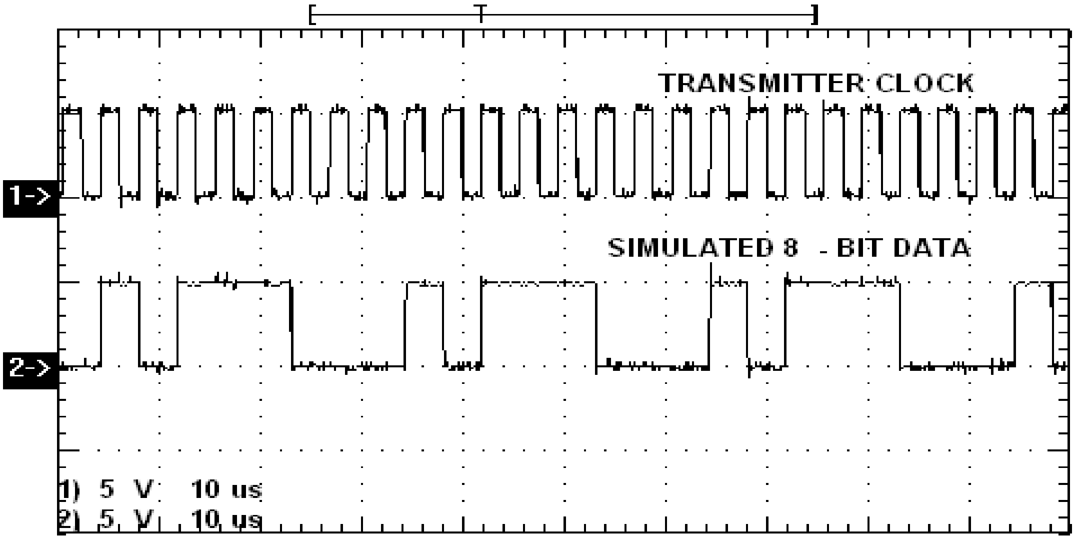
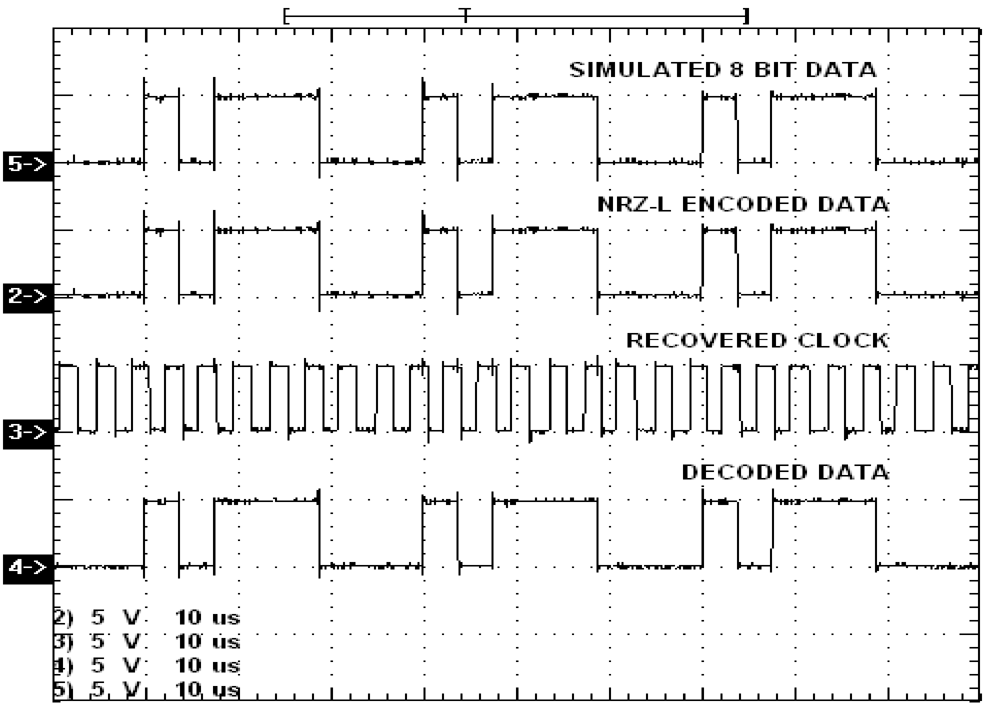


FIG 8A.BLOCK DIAGRAM FOR DATA CODING AND DECODING TECHNIQUES (NRZ-L, NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S)

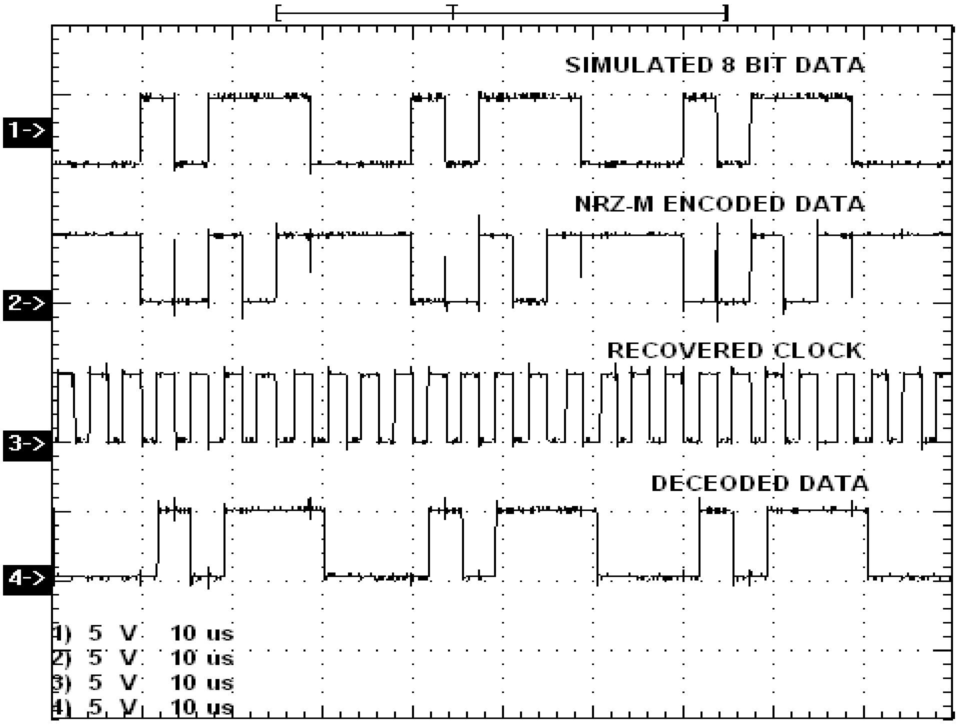
CONCLUSION

The NRZ-L, NRZ-M, NRZ-S, URZ, BIO-L, BIO-M, BIO-S coded signals have a frequency component, that is equal to half the frequency of the coding (reference) clock. The recovered data and clock is observed to have a very small phase lag with respect to the transmitted data and clock.

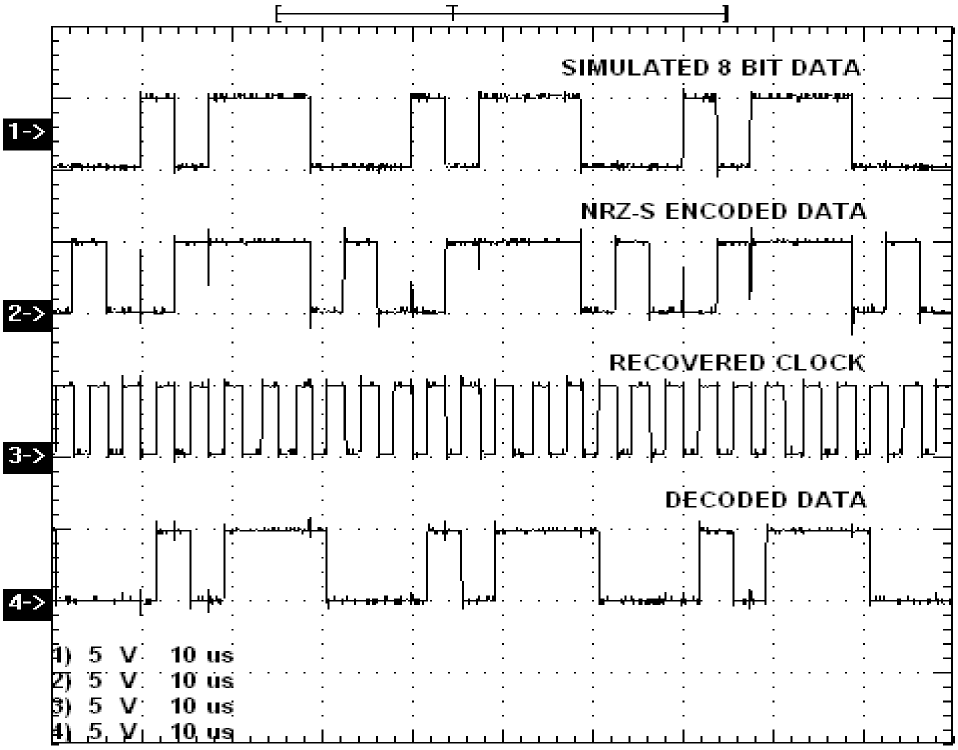




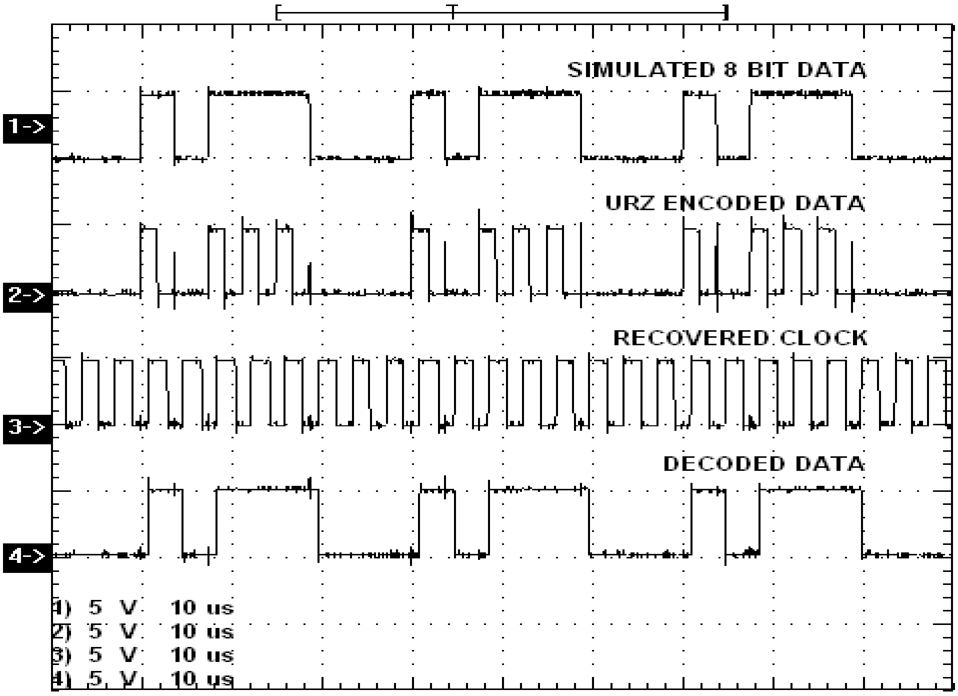
NRZ-L Encoding And Decoding



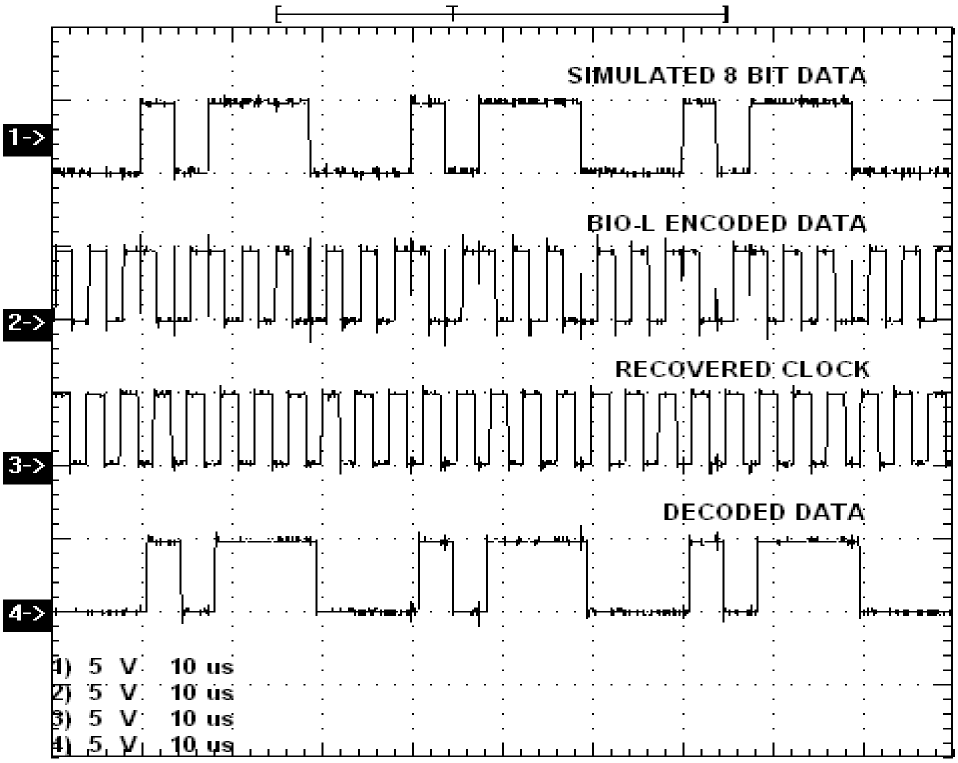
NRZ-M Encoding And Decoding



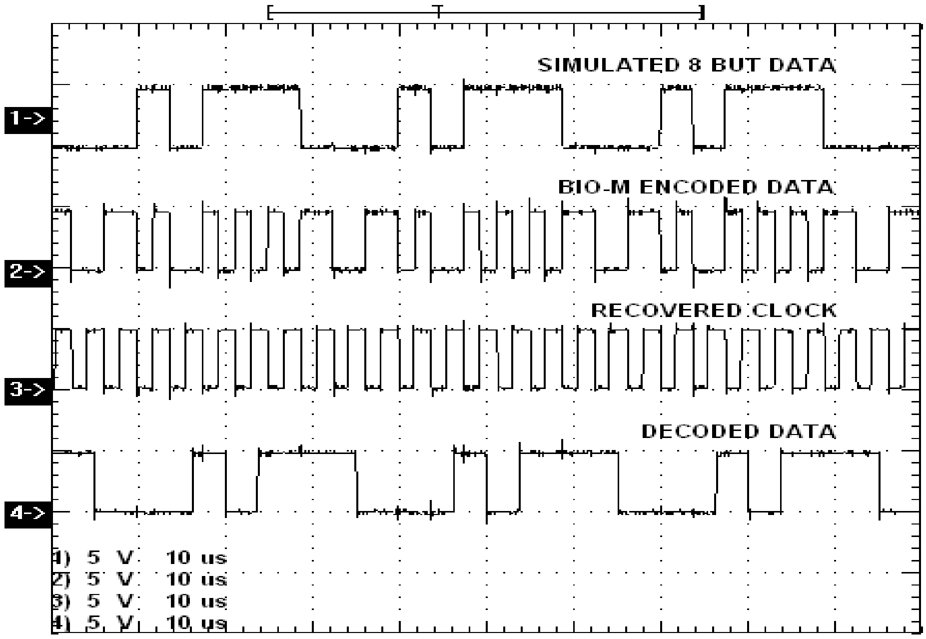
NRZ-S Encoding And Decoding



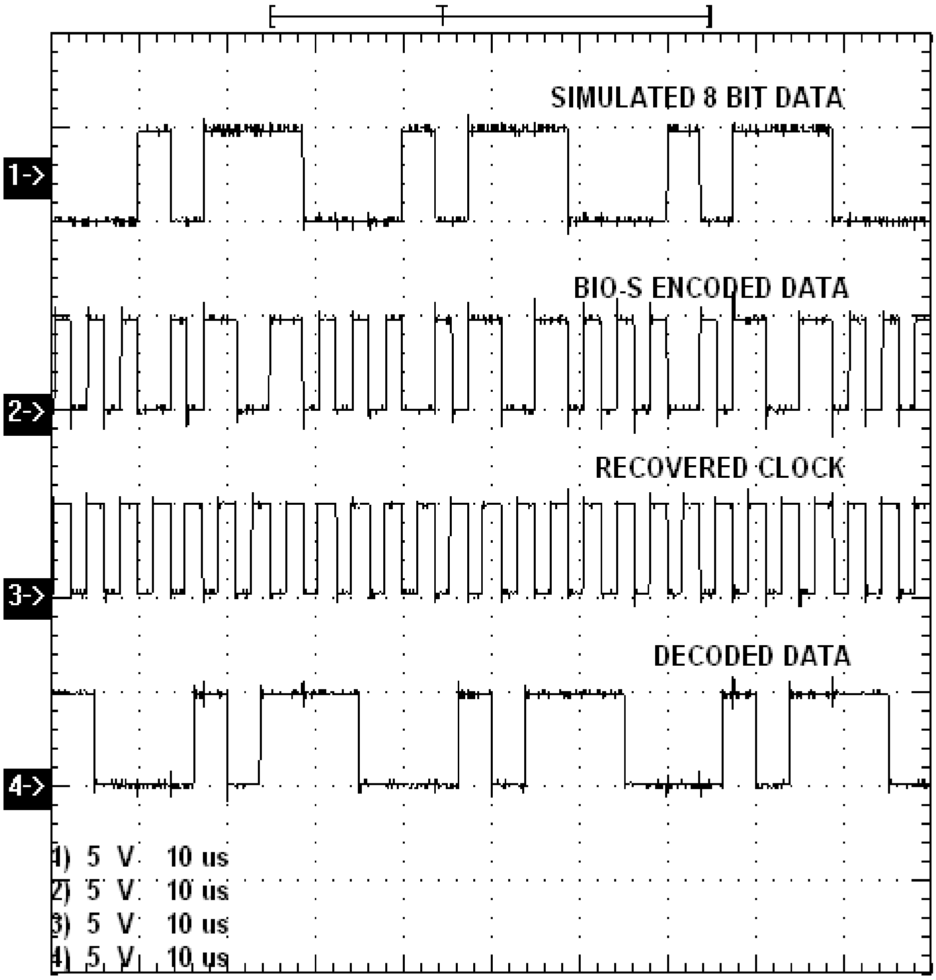
URZ Encoding And Decoding



BIO-L Encoding And Decoding



BIO-M Encoding And Decoding



BIO-S Encoding And Decoding

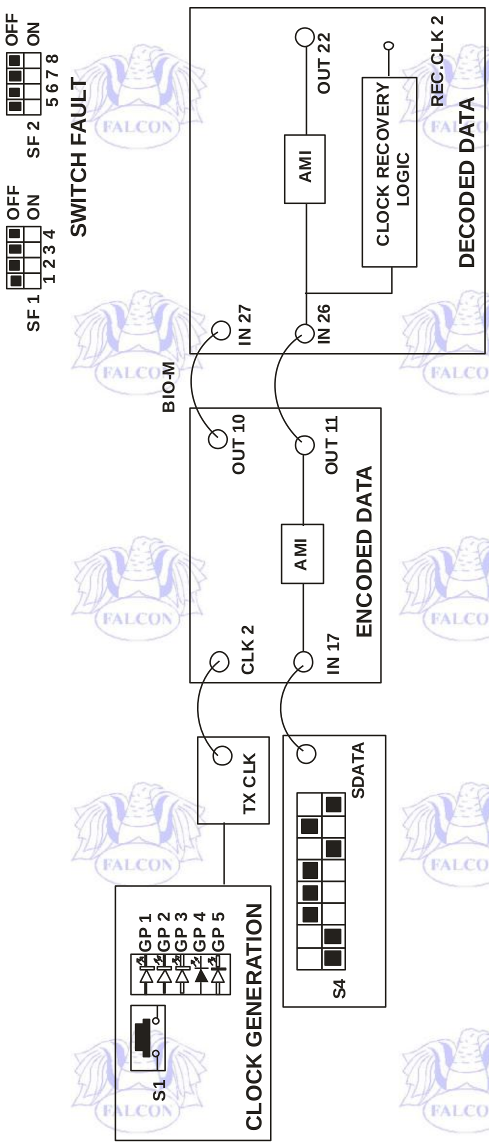


FIG 8B.BLOCK DIAGRAM FOR DATA CODING AND DECODING TECHNIQUES (AMI)

Optional Experiments (B, C, and, D):-

B. Ami Encoding and Decoding

THEORY

Multilevel Signals

Multilevel signals use three or more levels of voltages to represent the binary digits, `one' and `zero' - instead of the normal `highs' and `lows'

Return to zero - Alternative Mark Inversion (RZ - AMI) is the most commonly used multilevel signal This coding scheme is most often used in telemetry systems. In this scheme, `ones' are represented by equal amplitude of alternating pulses, which alternates between +5V and -5V. These alternating pulses return to 0 volt, after every half bit interval. The `zeros' are marked by the absence of pulses.

The coding of basic data NRZ-L into URZ and RZ-AMI format can be understand easily by referring to circuit diagram and Waveforms.

For decoding the URZ coded data, first of all, the clock is recovered from the incoming coded data by using phase locked loop techniques. Since the URZ signal has a frequency component equal to the clock, the bi-directional monoshot and / OR the gate should be eliminated in this application.

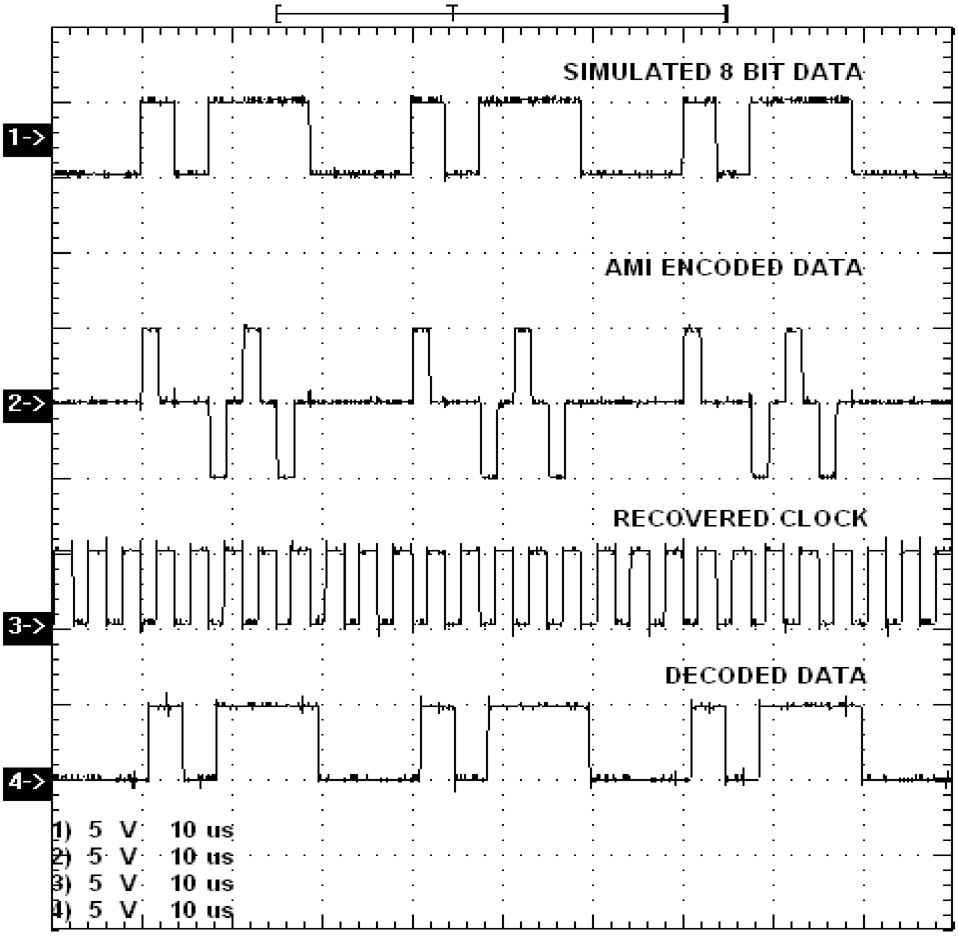
For recovery of clock from RZ-AMI, first the RZ-AMI should be converted to URZ by standard techniques. Then the clock is recovered.

Refer the circuit diagram and waveforms for the decoding techniques.

- Ensure that group 4 (**GP4**) clock is selected in the Clock Generation section. Selection is done with the help of switch **S1**.
- Observe the transmitter clock of frequency **250 KHz** at **TXCLK** post.
- Set the data pattern using switch **S4** as shown in the block diagram.
- Observe the 8-bit data pattern at **S DATA** post.
- Connect **S DATA** to **IN17** post and **TXCLK** to **CLK2** post of the Encoded Data section.
- Observe the AMI encoded data at the **OUT11** post of the Encoded Data section.
- Connect **OUT11** to **IN26** post of the Decoded Data section.
- For clock recovery connect **OUT 10** post of Encoded Data section to **IN 27** post of data decoder section.
- Select **BIO-M** data Using Switch S3 and observe the corresponding LED indication..
- Observe the decoded AMI data at the **OUT22** post of the Decoded Data section.

CONCLUSION

The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.



AMI Encoding And Decoding

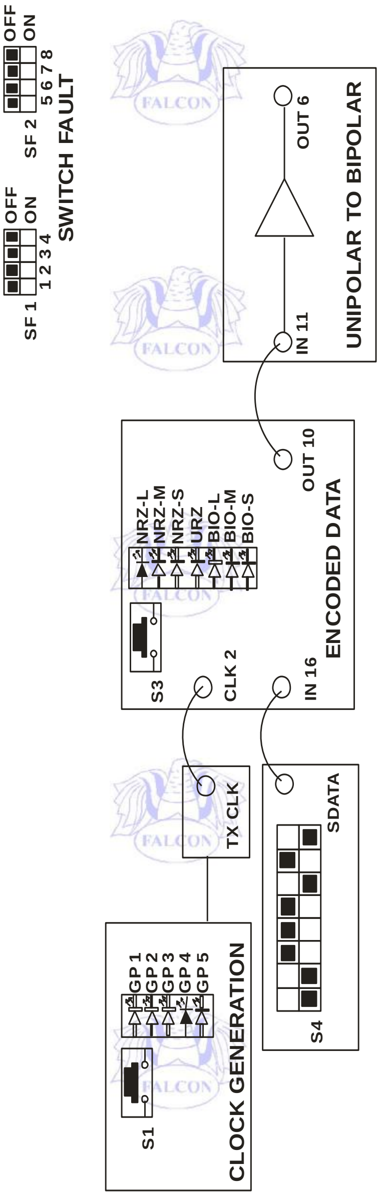


FIG 8C.BLOCK DIAGRAM FOR UNIPOLAR TO BIPOLAR

C. UNIPOLAR TO BIPOLAR

PROCEDURE

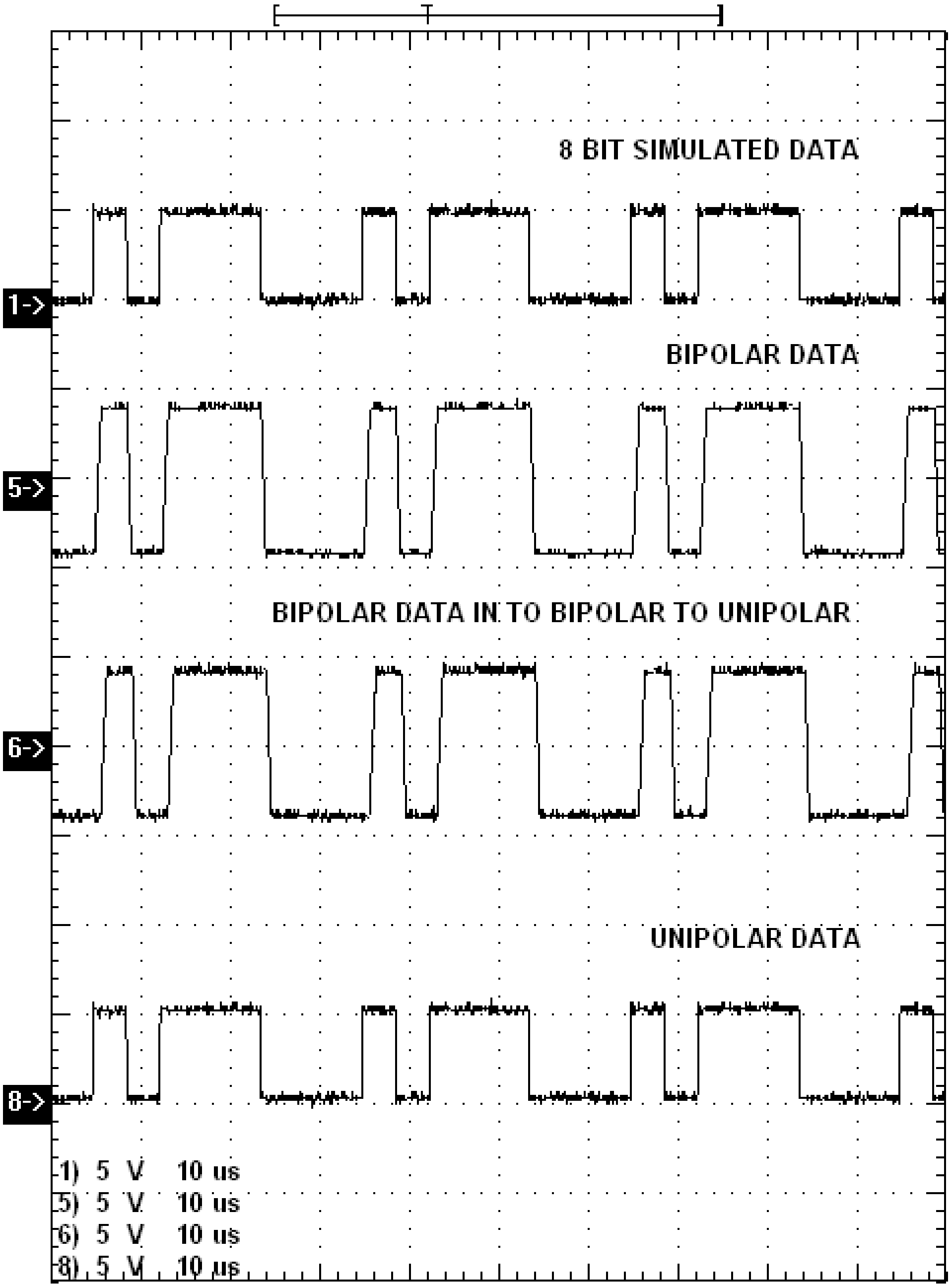
- Ensure that the group 4 (**GP4**) clock is selected in the clock generation section. Selection is done with the help of switch **S1.** Observe the corresponding LED indication.
- Observe the transmitter clock of frequency **250 KHz** at **TXCLK** post.
- The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.
- Set the data pattern using switch **S4** as per the given block diagram.
- Observe the 8-bit data pattern at **S DATA** post.
- Connect **SDATA** to **IN16** post and **TXCLK** to **CLK2** post of the AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.
- Encoded Data section.
- Select NRZ-L data with the help of the switch **S2** and observe the corresponding LED indication in the Encoded Data section.
- Connect **OUT10** post of the Encoded Data section to the **IN11** post of the Unipolar to Bipolar section.
- Observe the Bipolar data at the **OUT6** post of the Unipolar to Bipolar section.
- The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.
- The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.
- The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique.

CONCLUSION

In Unipolar to Bipolar technique NRZ-L data which is unipolar (between GND and +5V) is translated into bipolar (+5V and –5V)

AMI, UNIPOLAR TO BIPOLAR AND BIPOLAR TO UNIPOLAR ENCODING

The AMI coded signal have alternate pulse of +5V and -5V for half bit interval when data bit is ONE. In decoding clock is recovered from incoming data bit using PLL technique



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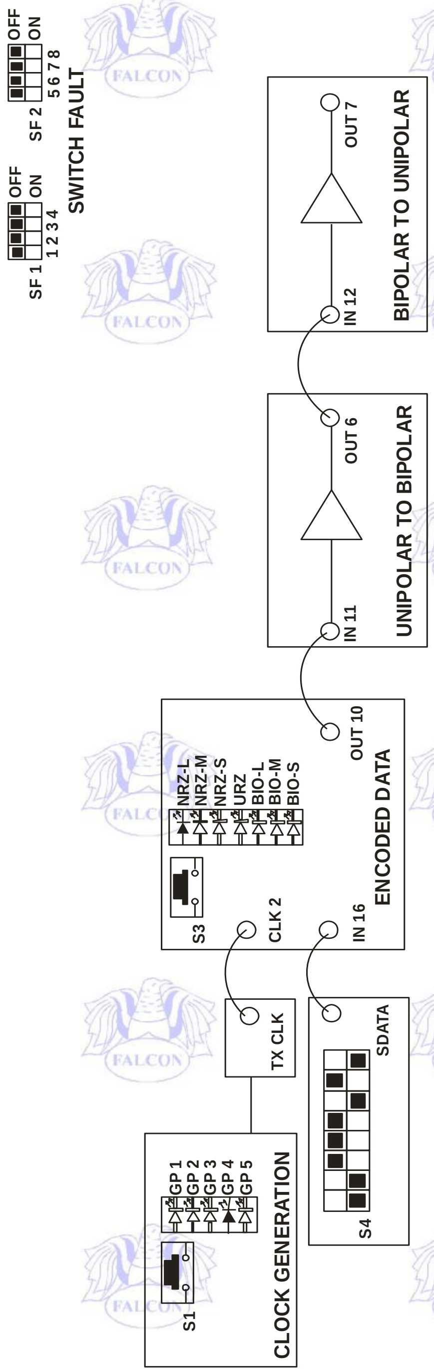

FIG 8D.BLOCK DIAGRAM FOR BIPOLAR TO UNIPOLAR

D. Bipolar To Unipolar

PROCEDURE

- Ensure that the group 4 (**GP4**) clock is selected in the clock generation section. Selection is done with the help of switch **S1** and observes the corresponding LED indication.
- Observe the transmitter clock of frequency **250 KHz** at **TXCLK** post.
- Set the data pattern using switch **S4** as per the given block diagram.
- Observe the 8-bit data pattern at **S DATA** post.
- Connect **SDATA** to **IN16** post and **TXCLK** to **CLK2** post of the Encoded Data section.
- Select NRZ-L data with the help of the switch **S2** and observe the corresponding LED indication in the Encoded Data section.
- Connect **OUT10** post of the Encoded Data section to **IN12** post of the Bipolar to Unipolar section.
- Observe the Bipolar data at the **OUT7** post of Bipolar to Unipolar section.

CONCLUSION

In Bipolar to Unipolar technique bipolar data (+5V and –5V) is converted back into NRZ-L data, which is Unipolar. (Between GND and +5V)