EEL2020 Digital Design Lab Report

# Sem II AY 2023-24

|  |  |  |
| --- | --- | --- |
| **Experiment No.** | **:** | **03** |
| **Name** | **:** | **Dhyey Findoriya** |
| **Roll No.** | **:** | **B22EE024** |
| **Partner Name (Roll Number)** | **:** | **Dheeraj Dhakad(B22EE023)** |

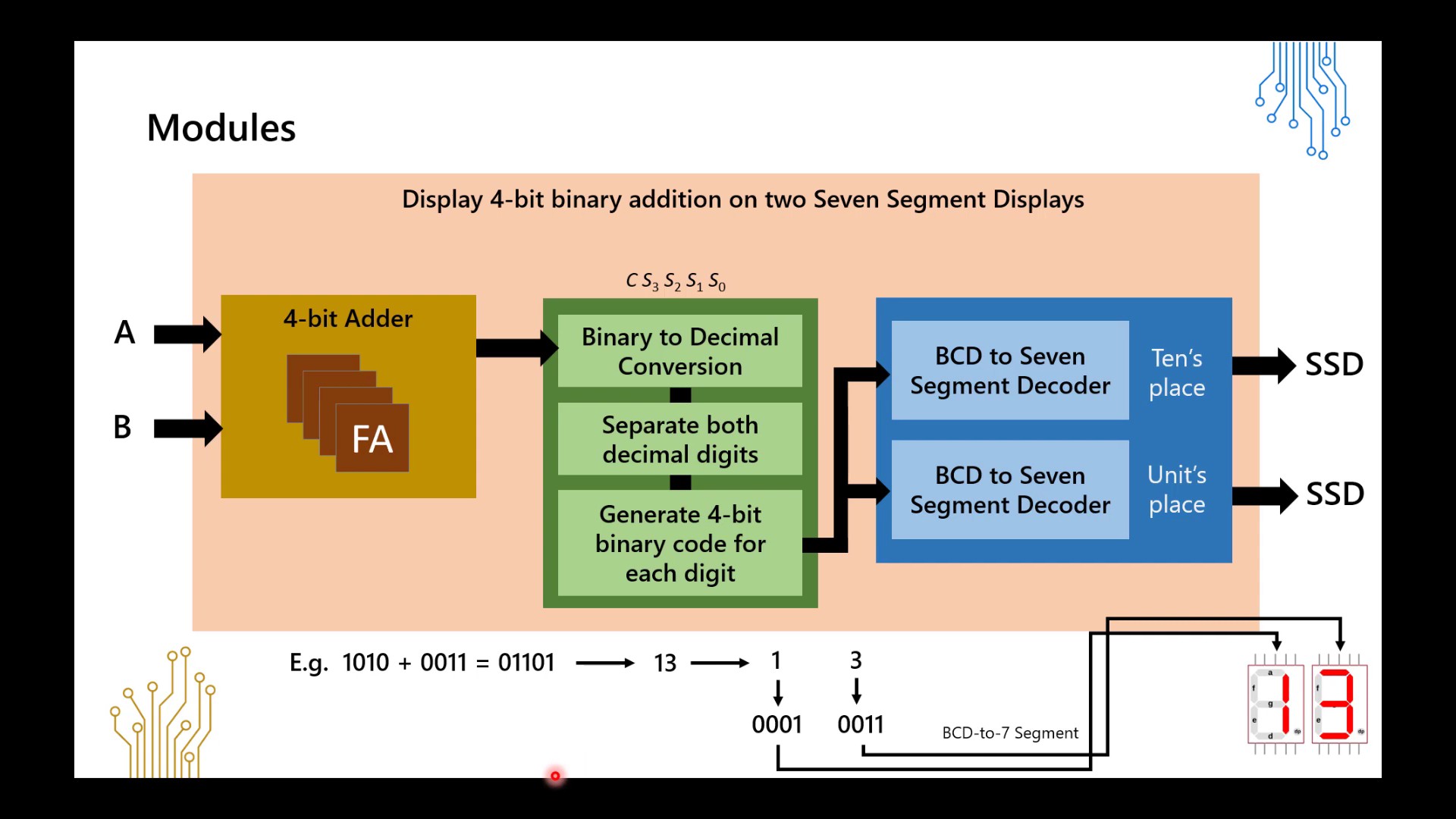
**Objective**

Simulate and implement the 4-bit adder on the PYNQ-Z2 board and display the 2-digit decimal sum on two seven-segment displays

# Logic Design

This experiment is carried out by using a carry ripple 4-bit adder, which takes two 4-bit BCDs as input and generates output as 5-bit sum.

The units and tens place of the output are extracted from the decimal representation of sum.Both units and tens digits are then sent to separate BCD to seven-segment decoders and displayed on separate seven-segment displays.



# Source Description

* Design source

Module name: fourbitadd\_display (add\_display.v)

Input ports: [3:0]A, [3:0]B; Output ports: [6:0] SSD\_tens, [6:0] SSD\_ones;

* Constraint ﬁle

The **PYNQ-Z2 v1.0.xdc** ﬁle was updated with the following changes:-

|  |  |  |  |
| --- | --- | --- | --- |
| **Ports**  (from Verilog module) | **Designation**  (Input/Output) | **PYNQ Component Type** (Button/LED/Switch etc. along with number, eg. LD01, BTN2, etc.) |  |
| **SSD\_ones[0]** | **Output** | JA1\_P | Y18 |
| **SSD\_ones[1]** | **Output** | JA1\_N | Y19 |
| **SSD\_ones[2]** | **Output** | JA2\_P | Y16 |
| **SSD\_ones[3]** | **Output** | JA2\_N | Y17 |
| **SSD\_ones[4]** | **Output** | JA3\_P | U18 |

|  |  |  |  |
| --- | --- | --- | --- |
| **SSD\_ones[5]** | **Output** | JA3\_N | U19 |
| **SSD\_ones[6]** | **Output** | JA4\_P | W18 |
| **SSD\_tens[0]** | **Output** | JB1\_P | W14 |
| **SSD\_tens[1]** | **Output** | JB1\_N | Y14 |
| **SSD\_tens[2]** | **Output** | JB2\_P | T11 |
| **SSD\_tens[3]** | **Output** | JB2\_N | T10 |
| **SSD\_tens[4]** | **Output** | JB3\_P | V16 |
| **SSD\_tens[5]** | **Output** | JB3\_N | W16 |
| **SSD\_tens[6]** | **Output** | JB4\_P | V12 |

The RPI\_Addon.xdc file was updated with the following changes:-

|  |  |  |  |
| --- | --- | --- | --- |
| **Ports**  **(from Verilog module)** | **Designation**  **(Input/Output)** | **RPI Component Type**  **(Button/LED/Switch etc., along with the number, e.g. LD01, BTN2, etc.)** | **Pin Conﬁguration**  **(from the RPI User Manual)** |
| A[0] | Input | SWE | C20 |
| A[1] | Input | SWF | Y8 |
| A[2] | Input | SWG | A20 |
| A[3] | Input | SWH | W9 |
| B[0] | Input | SWA | V6 |
| B[1] | Input | SWB | Y6 |
| B[2] | Input | SWC | B19 |
| B[3] | Input | SWD | U7 |

* Simulation source Testbench for:-

1) A = 0011; B = 0101; *(3 + 5 = 8)*

2) A = 1100; B = 1010; *(12 + 10 = 22)*

3) A = 0111; B = 1001; *(7 + 9 = 16)*

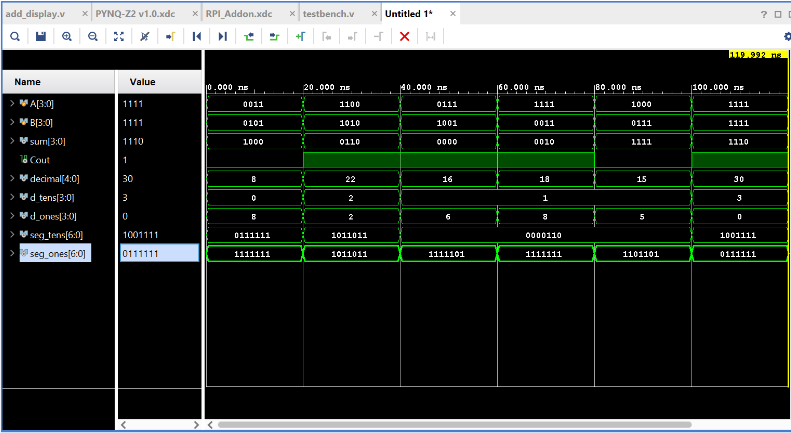
4) A = 1111; B = 0011; *(15 + 3 = 18)*

5) A = 1000; B = 0111; *(8 + 7 = 15)*

6) A = 1111; B = 1111; *(15 + 15 = 30)*

has been included as a simulation source “testbench.v”.

# Simulation Results (Timing diagram)



*Verifying diagram with table:-*

1.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  | 1 | 1 | 1 |  |
| A = 3 |  | 0 | 0 | 1 | 1 |
| B = 5 |  | 0 | 1 | 0 | 1 |
| Sum | Cout-0 | 1 | 0 | 0 | 0 |

(01000)2 = (8)10

2.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  |  |  |  |  |
| A = 12 |  | 1 | 1 | 0 | 0 |
| B = 10 |  | 1 | 0 | 1 | 0 |
| Sum | Cout-1 | 0 | 1 | 1 | 0 |

(10110)2 = (22)10

3.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  | 1 | 1 | 1 |  |
| A = 7 |  | 0 | 1 | 1 | 1 |
| B = 9 |  | 1 | 0 | 0 | 1 |
| Sum | Cout-1 | 0 | 0 | 0 | 0 |

(10000)2 = (16)10

4.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  | 1 | 1 | 1 |  |
| A = 15 |  | 1 | 1 | 1 | 1 |
| B = 3 |  | 0 | 0 | 1 | 1 |
| Sum | Cout-1 | 0 | 0 | 1 | 0 |

(10010)2 = (18)10

5.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  |  |  |  |  |
| A = 8 |  | 1 | 0 | 0 | 0 |
| B = 7 |  | 0 | 1 | 1 | 1 |
| Sum | Cout-0 | 1 | 1 | 1 | 1 |

(01111)2 = (15)10

6.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  | 1 | 1 | 1 |  |
| A = 15 |  | 0 | 0 | 1 | 1 |
| B = 15 |  | 0 | 1 | 0 | 1 |
| Sum | Cout-0 | 1 | 0 | 0 | 0 |

(11110)2 = (30)10

# Elaborated Design

**PYNQ Working Video** (to be recorded during lab session)

*Insert Video Link (GC) - https://drive.google.com/file/d/19d2vnWV5smnZuvhyExPhnIRy-RzY0VSU/view*

# List of Attachments

DD Expt-3.zip contains-1) add\_display.v (which is the source code for HDL)

2) testbench.v (which contains the code of sample to test)