EEL2020 Digital Design Lab Report

# Sem II AY 2023-24

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| --- | --- | --- |
| **Experiment No.** | **:** | **04** |
| **Name** | **:** | **Dhyey Findoriya** |
| **Roll No.** | **:** | **B22EE024** |
| **Partner Name (Roll Number)** | **:** | **Dheeraj Dhakad (B22EE023)** |

**Objective**

To make a BCD Adder/Subtractor circuit and record its functioning and simulate its working on Vivado.

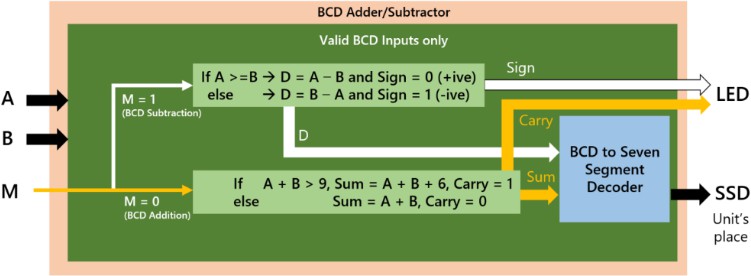
# Logic Design

This circuit performs either addition or subtraction of two 4-bits binary input based on a separate input M, if M=0 then addition and if M=1 then subtraction. The input numbers are limited to max (1001)2 i.e.,9.

The sign (in case of subtraction) and carry (in case of addition ) are shown by the same LD0. While the BCD difference or sum is shown on a 7-segment display.

In case the addition value exceeds 9, the binary representation of the sum is obtained at the 4 least significant bits by adding 610(=01102) to the addition value.

Difference is obtained by subtracting the smaller value from the larger one. The sign is assigned based on whether the first input was the smaller value or not.



# Source Description

* Design source
  1. **Module name:** add\_sub [BCD\_addition\_subtraction.v]
  2. **Input ports:** A, B, M; **Output ports:** SSD 7-bit vector [seg\_out], LED bit [M];
* Constraint file

The **PYNQ-Z2 v1.0.xdc** file was updated with the following changes:-

|  |  |  |  |
| --- | --- | --- | --- |
| **Ports**  (from Verilog module) | **Designation**  (Input/Output) | **PYNQ Component Type** (Button/LED/Switch etc. along with number, eg. LD01, BTN2, etc.) | **Pin Configuration**  (from the PYNQ user manual) |
| **seg\_out[0]** | **Output** | JA1\_P | Y18 |
| **seg\_out[1]** | **Output** | JA1\_N | Y19 |
| **seg\_out[2]** | **Output** | JA2\_P | Y16 |
| **seg\_out[3]** | **Output** | JA2\_N | Y17 |
| **seg\_out[4]** | **Output** | JA3\_P | U18 |
| **seg\_out[5]** | **Output** | JA3\_N | U19 |
| **seg\_out[6]** | **Output** | JA4\_P | W18 |
| **c\_out\_sign[0]** | **Output** | LD0 | R14 |
| **M** | **Input** | SW0 | M20 |

The RPI\_Addon.xdc file was updated with the following changes:-

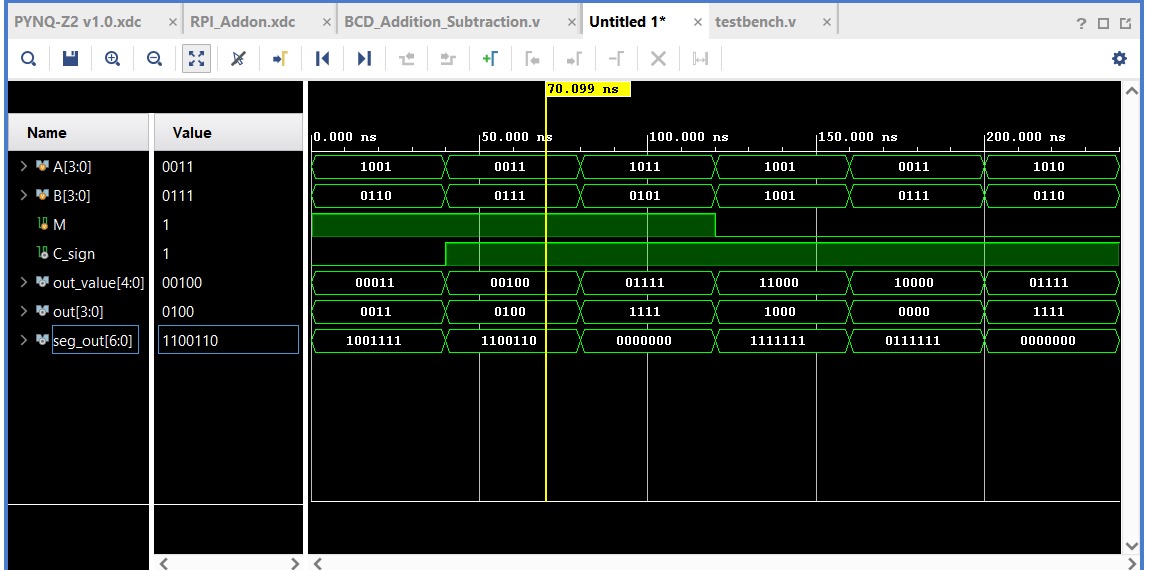
|  |  |  |  |
| --- | --- | --- | --- |
| **Ports**  **(from Verilog module)** | **Designation**  **(Input/Output)** | **RPI Component Type**  **(Button/LED/Switch etc., along with the number, e.g. LD01, BTN2, etc.)** | **Pin Configuration**  **(from the RPI User Manual)** |
| A[0] | Input | SWE | C20 |
| A[1] | Input | SWF | Y8 |
| A[2] | Input | SWG | A20 |
| A[3] | Input | SWH | W9 |

|  |  |  |  |
| --- | --- | --- | --- |
| B[0] | Input | SWA | V6 |
| B[1] | Input | SWB | Y6 |
| B[2] | Input | SWC | B19 |
| B[3] | Input | SWD | U7 |

* Simulation source

Testbench has been included as a simulation source “testbench.v”. And the resulting diagram is shown below:

# Simulation Results (Timing diagram)



*Verifying diagram with table:-*

## M = 0;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  |  |  |  |  |
| A = 9 |  | 1 | 0 | 0 | 1 |
| B = 9 |  | 1 | 0 | 0 | 1 |
| Sum | Cout = 1 | 1 | 0 | 0 | 0 |

(10010)2 = (18)10

## M = 0;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  |  |  |  |  |
| A = 3 |  | 0 | 0 | 1 | 1 |
| B = 7 |  | 0 | 1 | 1 | 1 |
| Sum | Cout = 1 | 0 | 0 | 0 | 0 |

(01010)2 = (10)10

## M = 0;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Carry |  |  |  |  |  |
| A = 10 |  | 1 | 0 | 1 | 0 |
| B = 6 |  | 0 | 1 | 1 | 0 |
| Sum | Cout = 0 | 1 | 1 | 1 | 1 |

Invalid becoz of A = 10

## M = 1;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| B = 6 | 0 | 0 | 1 | 1 | 0 |
| One’s complement of B | 1 | 1 | 0 | 0 | 1 |
| Carry | 1 |  |  |  |  |
| A = 9 | 0 | 1 | 0 | 0 | 1 |
| Two’s complement of B | 1 | 1 | 0 | 1 | 1 |
| diff | Sign = 0 | 0 | 0 | 1 | 1 |

(00011)2 = (3)10

## M = 1;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| B = 7 | 0 | 0 | 1 | 1 | 1 |
| One’s complement of B | 1 | 1 | 0 | 0 | 0 |
| Carry | 1 |  |  |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A = 3 | 0 |  | 0 | 1 | 1 |
| Two’s complement of B | 1 | 1 | 0 | 0 | 1 |
| diff | Sign = 1 | 0 | 1 | 0 | 0 |

(00100)2 = (4)10

## M = 1;

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| B = 5 | 0 | 0 | 1 | 0 | 1 |
| One’s complement of B | 1 | 1 | 0 | 1 | 0 |
| Carry |  |  |  |  |  |
| A = 11 | 0 | 1 | 0 | 1 | 1 |
| Two’s complement of B | 1 | 1 | 0 | 1 | 1 |
| diff | Sign = 0 | 1 | 1 | 1 | 1 |

Invalid due to A = 11

**PYNQ Working Video** (to be recorded during lab session)

**Insert Video Link (GC) -[Video\_link(B22EE024)](https://drive.google.com/file/d/1K0-Xk_MGH2RFBEbiLdVh7mUK1NuWhJPP/view)**

# List of Attachments

DD Expt-04.zip contains-

1. bcd\_adder\_subtractor.v (which is the source code for HDL)
2. testbench.v (which contains the code of sample to test)