

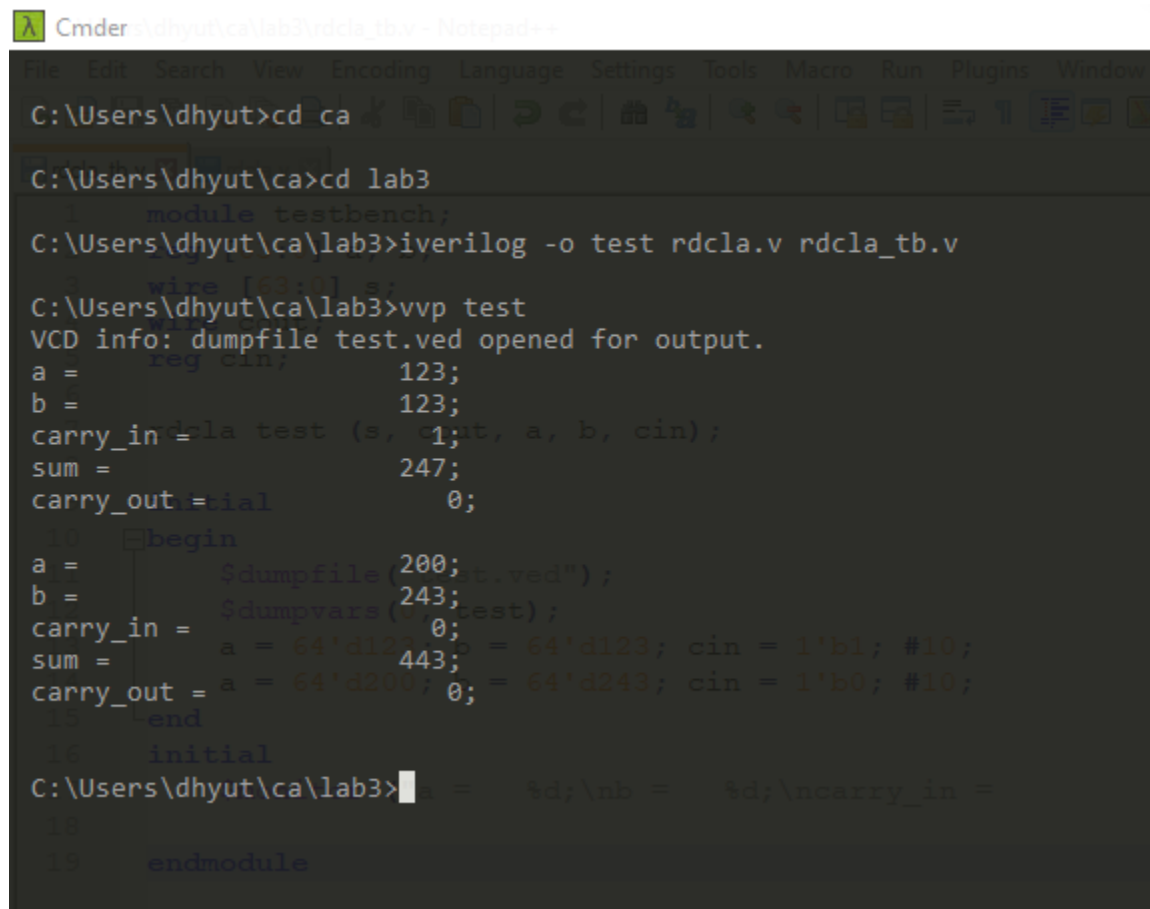
Computer Architecture Practice - COM307P

Lab - 3

64-Bit Recursive Doubling based carry lookahead adder

Done by : N Sree Dhyuti - CED19I027

Output :



```
Cmder C:\Users\dhyut\ca\lab3\rdcla_tb.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window
C:\Users\dhyut>cd ca
C:\Users\dhyut\ca>cd lab3
C:\Users\dhyut\ca\lab3>iverilog -o test rdcla.v rdcla_tb.v
C:\Users\dhyut\ca\lab3>vvp test
VCD info: dumpfile test.ved opened for output.
a = 123;
b = 123;
carry_in = 1;
sum = 247;
carry_out = 0;
10 begin
a = $dumpfile(200; test.ved");
b = $dumpvars(243; test);
carry_in = 0;
sum = a = 64'd123; b = 64'd123; cin = 1'b1; #10;
carry_out = a = 64'd200; b = 64'd243; cin = 1'b0; #10;
15 end
16 initial
C:\Users\dhyut\ca\lab3> a = %d;\nb = %d;\ncarry_in =
18
19 endmodule
```

THE END
