Computer Architecture Practice - COM307P

Lab - 5

Processor Register File

Done by: N Sree Dhyuti - CED19I027

Output:

```
λ Cmder
C:\Users\dhyut>cd ca
C:\Users\dhyut\ca\lab5>iverilog -o uut prf.v prf_tb.v
VCD info: dumpfile uut.ved opened for output.
RD = 0, WR = 1, rst = 0, EN = 1, clk = 1
RD = 1, WR = 0, rst = 0, EN = 1, clk = 1
C:\Users\dhyut\ca\lab5>
```