

①

Shift	Content after each shift	Serial Input
0 th (initial)	1011	101101
1 st	1101	10110
2 nd	0110	1011
3 rd	1011	101
4 th	1101	10
5 th	0110	1
6 th	1011	0

② (a) t_{pd} of each FF = 50 ns
 t_{pd} of each AND gate = 20 ns
 For a synchronous counter of any no. of bits,
 Total delay $\geq t_{pd}(\text{FF}) + t_{pd}(\text{AND gate})$

$$\text{Total delay} \geq (50 + 20) \text{ ns}$$

$$T_{\text{clock}} \geq 70 \text{ ns}$$

$$\frac{1}{T_{\text{clock}}} \leq \frac{1}{70 \text{ ns}}$$

$$f_{\text{clock}} \leq \frac{1}{70} \text{ ns} = 14.285 \times 10^6 \text{ Hz}$$

$$f_{\text{clock}} \leq 14.285 \text{ MHz}$$

$$\boxed{f_{\text{max}} = 14.285 \text{ MHz}}$$

For a MOD-16 ripple counter,

$$f_{\text{max}} = \frac{1}{4} \times \frac{1}{t_{pd} \text{ of FF}} \quad (\text{as it has 4 flipflops})$$

$$f_{\text{max}} = \frac{1}{4 \times 50 \times 10^{-9}} = 5 \text{ MHz}$$

\therefore The f_{max} of 4-bit synchronous counter is greater than the f_{max} of a MOD-16 ripple counter.

(b) To convert a MOD-16 ripple counter to a MOD-32 counter, we should add one more flip flop.

Already a MOD-16 counter will have 4 FF's.

So, adding one more will make it count from 0 to 31

(c) As all the flip flops and other gates function simultaneously or parallelly to each other, adding of FF's will not change the tpd & also the f_{max} ,

So, f_{max} of MOD-32 ripple counter = f_{max} of MOD-16 ripple counter

$$f_{max} \text{ of MOD-32 ripple counter } = 14.28 \text{ MHz}$$

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STATE TABLE

	Present State			Next State			Inputs (D-FF)		
	A	B	C	A	B	C	D _A	D _B	D _C
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	1
2	0	1	0	0	0	0	0	0	0
3	0	1	1	1	0	1	1	0	1
4	1	0	0	X	X	X	X	X	X
5	1	0	1	1	1	1	1	1	1
6	1	1	0	X	X	X	X	X	X
7	1	1	1	0	1	0	0	1	0

Now, using K-maps, we find

D_A, D_B, D_C in terms of present state values of A, B, C

For D_A

A \ BC	00	01	11	10
0	0	0	1	0
1	X	1	0	X

$$D_A = A\bar{B} + \bar{A}BC$$

$$= A\bar{B} + BC$$

$$D_A = A + BC$$

$$D_A = A + BC$$

For D_B

A \ BC	00	01	11	10
0	0	1	0	0
1	X	1	1	X

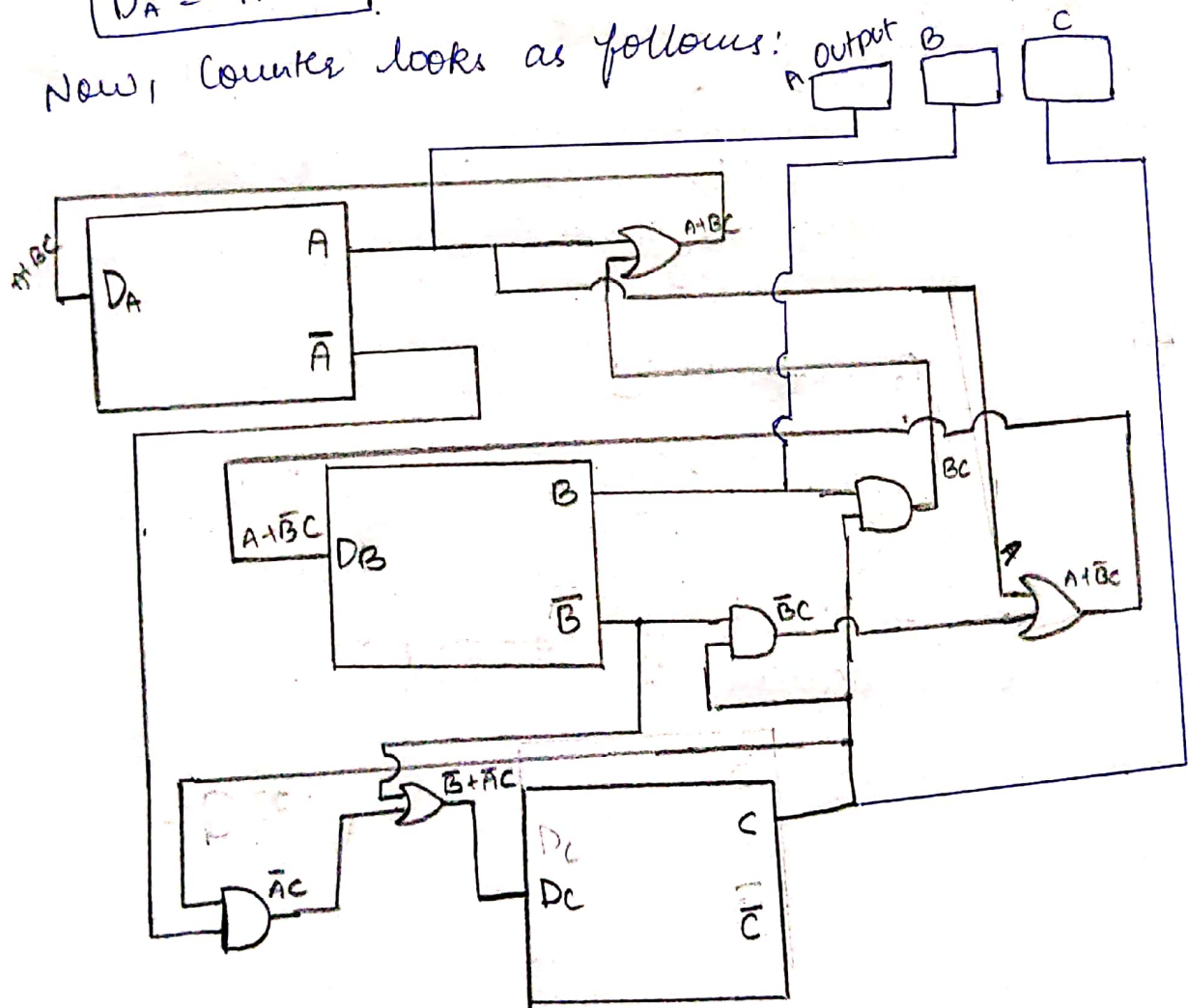
$$D_B = A + \bar{B}C$$

For D_C

A \ BC	00	01	11	10
0	1	1	1	0
1	X	1	0	X

$$D_C = \bar{B} + \bar{A}C$$

Now, Counter looks as follows:



④ (a) Truth table of M-F flip flop

M	F	Q_n	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1 0	0	0	X
1	0	1	X
1	1	0	0
1	1	1	0

} set

} Toggles

} Don't Care / Not allowed

} reset

using Kmap for Q_{n+1}

M \ Q_n				
	00	01	11	10
0	1	1	0	1
1	X	X	0	0

$$Q_{n+1} = \bar{F} + F \bar{M} Q_n$$

$$Q_{n+1} = \bar{F} + \bar{M} Q_n$$

$\therefore Q_{n+1} = \bar{F} + \bar{M} Q_n$ is the characteristic equation for the given M-F flip flop

(b)

Q	Q_{n+1}	M	F
0	0	1	1
0	1	0	X
1	0	X	1
1	1	0	0

⑤ Aim: To construct a circuit that

- ⑤ Aim: To construct a circuit that finds the 10's complement of a BCD digit.
- sol digit \Rightarrow we should construct it for 0-9

Truth table:

Truth table BCD equivalent of input					BCD equivalent of 10's complement				
digit	I_3	I_2	I_1	I_0	10's complement	O_3	O_2	O_1	O_0
0	0	0	0	0	8 10	1	0	1	0
1	0	0	0	1	8 9	1	0	0	1
2	0	0	1	0	8 8	1	0	0	0
3	0	0	1	1	8 7	0	1	1	1
4	0	1	0	0	6 6	0	1	1	0
5	0	1	0	1	6 5	0	1	0	1
6	0	1	1	0	5 4	0	1	0	0
7	0	1	1	1	5 3	0	0	1	1
8	1 1	0	0	0	2 2	0	0	1	0
9	1	0	0	1	2 1	0	0	0	1

remaining all cases are dontcare cases
using Kmaps

For O_0

$I_3 I_2 \backslash I_1 I_0$	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	1	X	X

$$O_0 = I_0$$

For O_1 ,

$I_3 I_2$ \ $I_1 I_0$	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

$$O_1 = \bar{I}_0 \bar{I}_1 + I_0 I_1$$

For O_2 ,

$I_3 I_2$ \ $I_1 I_0$	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

$$O_2 = I_2 \bar{I}_1 + \bar{I}_3 \bar{I}_2 I_1 I_0 + \bar{I}_3 I_2 I_1 \bar{I}_0$$

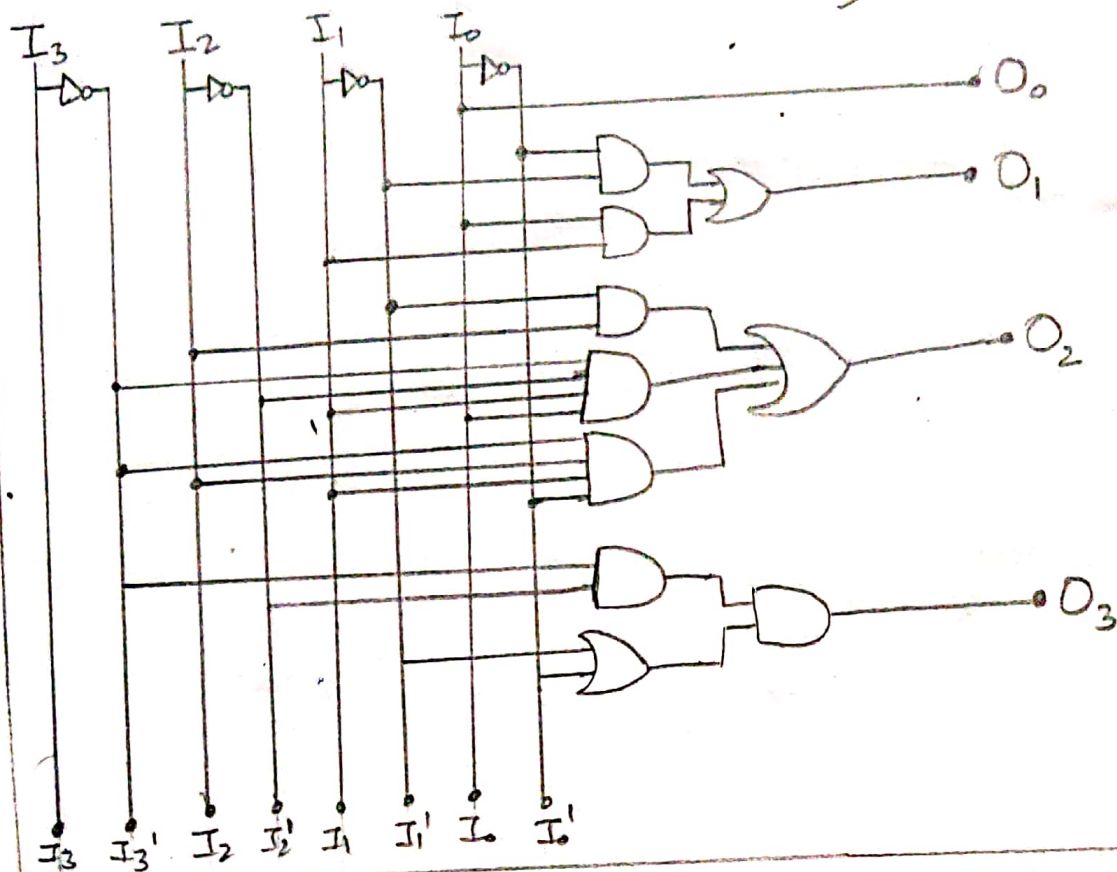
~~For O_3~~

For O_3

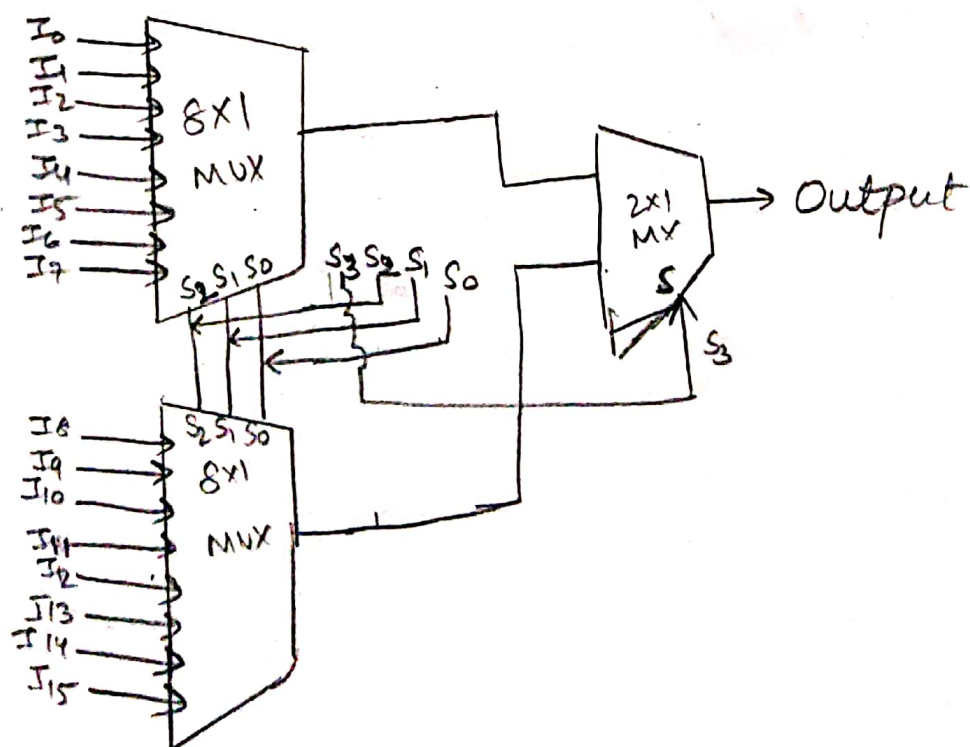
$I_3 I_2$ \ $I_1 I_0$	00	01	11	10
00	1	1	0	1
01	0	0	0	0
11	X	X	X	X
10	0	0	X	X

$$\begin{aligned} O_3 &= \bar{I}_3 \bar{I}_2 \bar{I}_1 + \bar{I}_3 \bar{I}_2 I_0 \\ &= \bar{I}_3 \bar{I}_2 (\bar{I}_1 + I_0) \end{aligned}$$

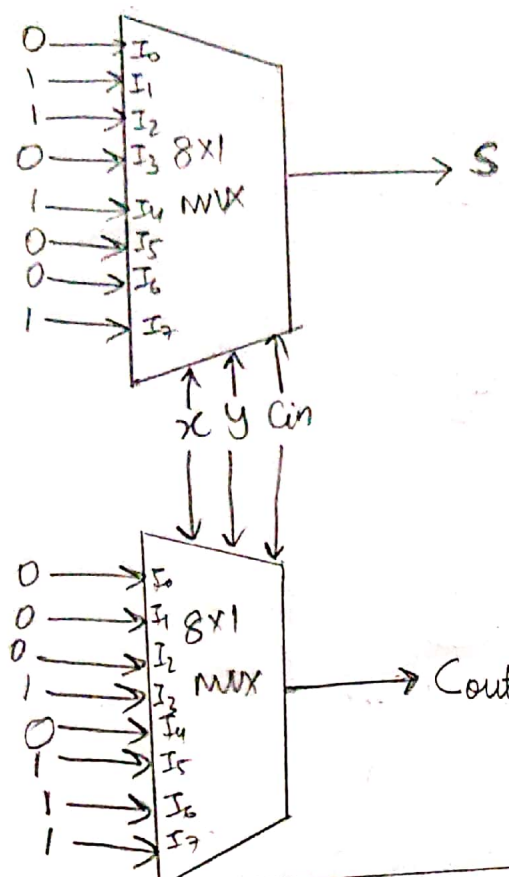
Now, ~~as we~~ from the eqns of O_0, O_1, O_2, O_3 ,
we get the circuit as follows:



6. 16x1 multiplexer using two 8x1 multiplexers & one 2x1 multiplexer
Let S_0, S_1, S_2 be the select lines



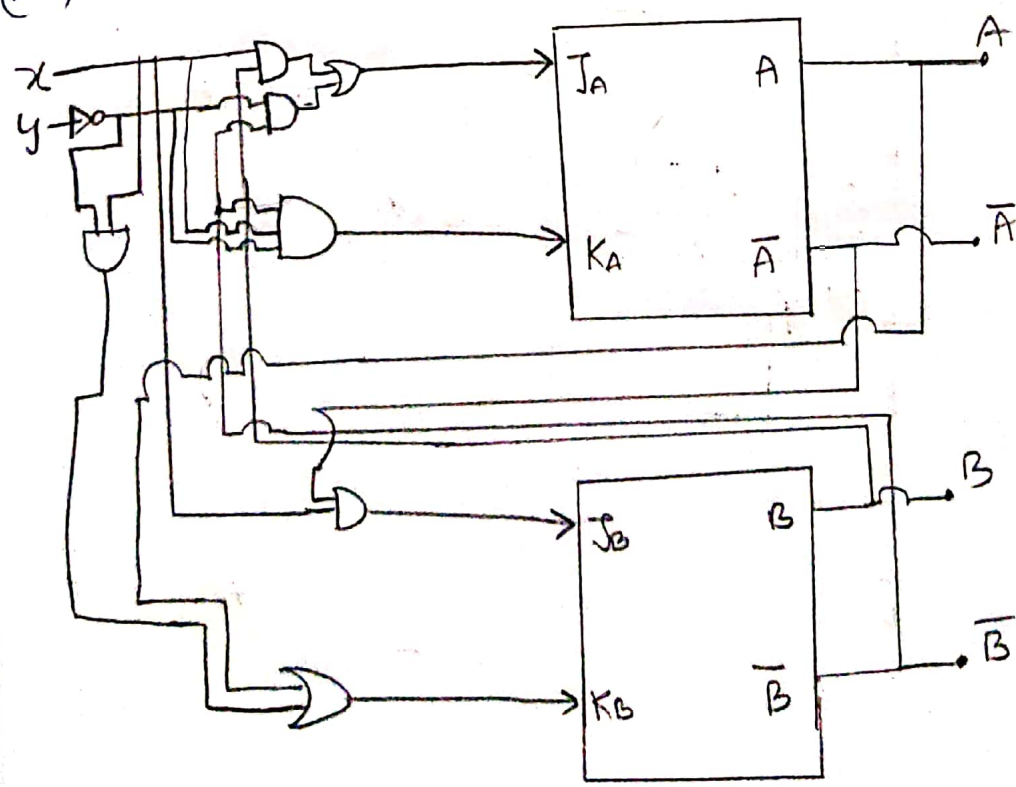
7 (a)



X	Y	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

8 Input equations are
 $J_A = Bx + B'y'$ $K_A = B'xy'$
 $J_B = A'x$ $K_B = A + xy'$
 $Z = Ax'y' + Bxy'$

(a)



(b)

Present state		Inputs		Next state		Output	FF inputs ^{inputs}			
A	B	x	y	A	B	Z	J _A	J_A K _A	J _B	K _B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	1
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	1	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	0	1	0	0	1

(c) K-map for next state A

AB \ xy	00	01	11	10
00	1			1
01			1	1
11	1	1	1	1
10	1	1	1	

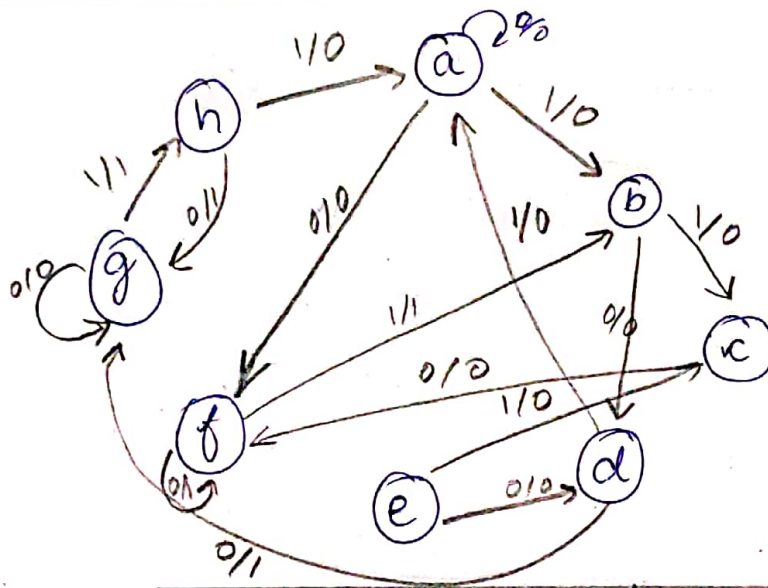
$$A_{t+1} = A\bar{x} + Bx + Ay + \bar{A}\bar{B}\bar{y}$$

for next state of B

AB \ xy	00	01	11	10
00			1	1
01	1	1	1	
11				
10				

$$B_{(t+1)} = \bar{A}\bar{B}x + \bar{A}B\bar{x} + \bar{A}By$$

(9) a)

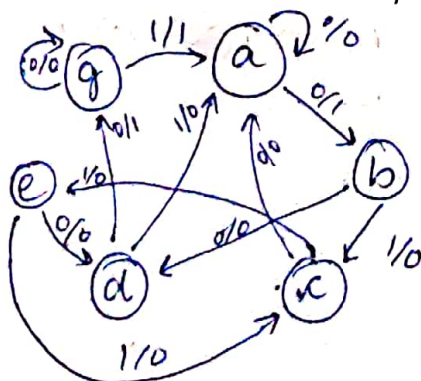


(b)

PS	NS		Output	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	d	c	0	0
c	a	e	0	0
d	g	a	1	0
e	d	c	0	0
g	g	a	0	1

(remove f & h)

(c)



(d)

PS	x	NS	Output
a	0	a	0
a	1	b	0
b	1	c	0
c	1	e	0
e	0	c	0
c	0	a	0
a	1	b	0
b	0	d	0
d	0	g	1
g	1	a	1
a	1	b	0

output: 00000000110