DACD LAB EXPERIMENT 10

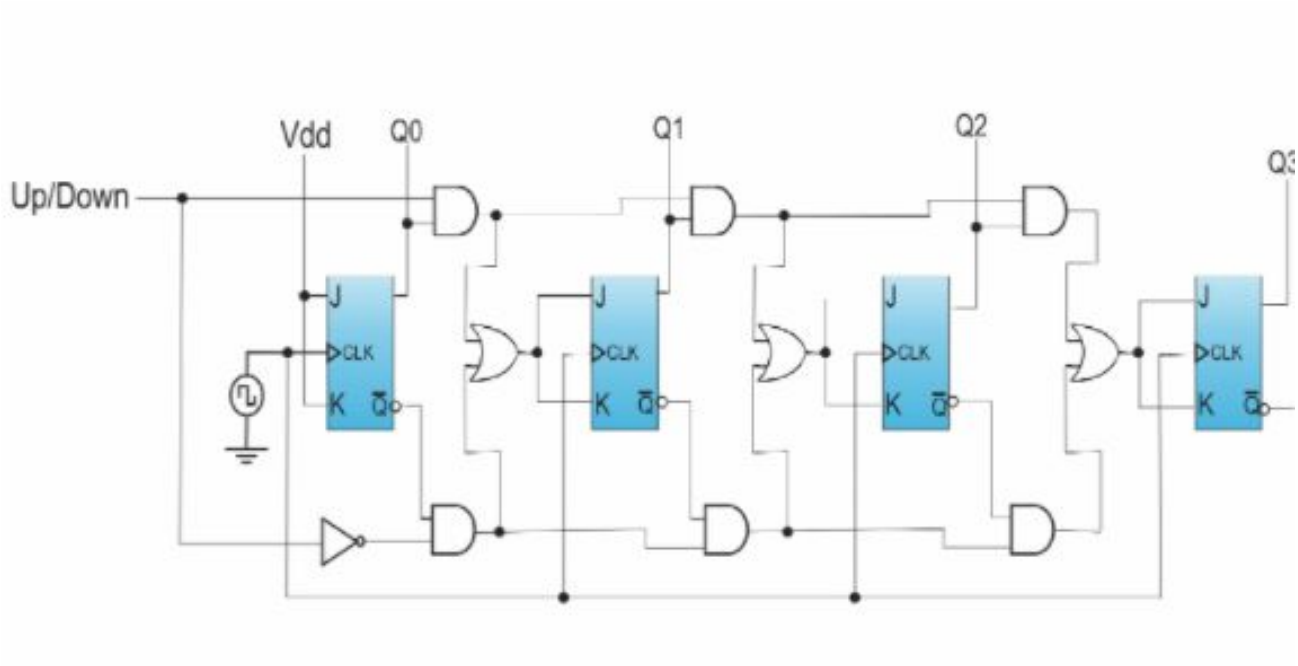
due : 26-10-2020

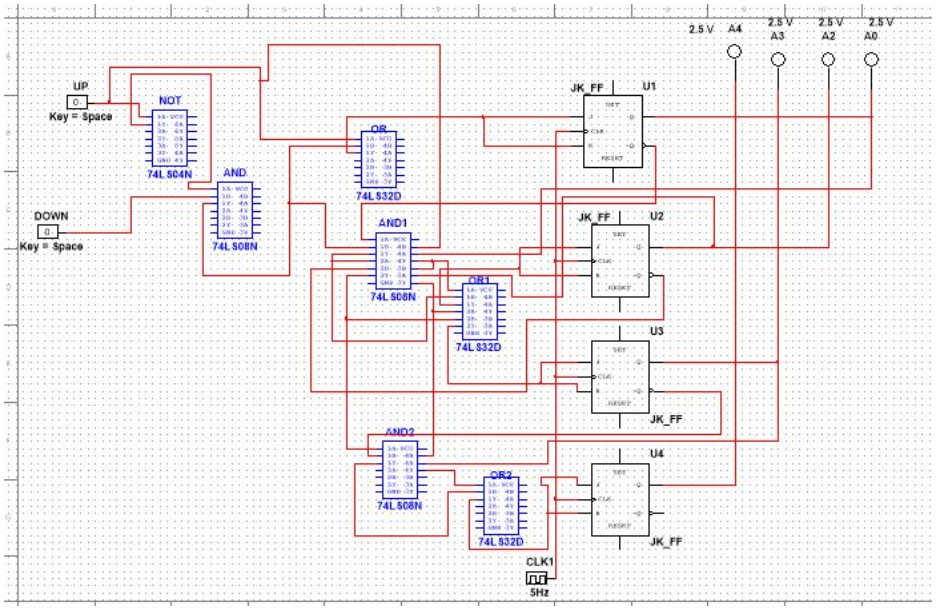
Design an 4-bit synchronous up-down counter

4-bit synchronous counters are circuits that give outputs from 0-15 while up-counting and 15-0 while down-counting.

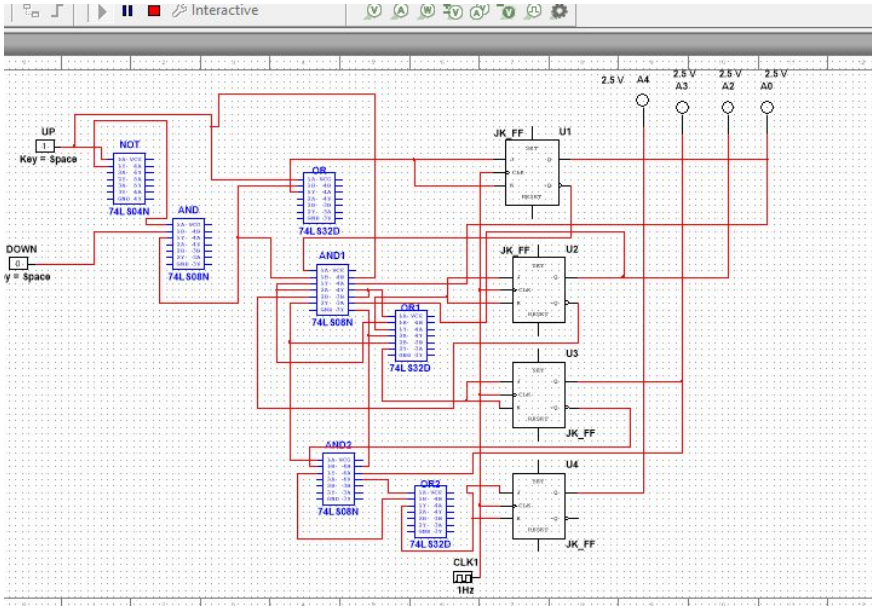
We can do this using JK or T flip flops .
Each output (Q) of Flip Flop will represent each binary digit of the numbers we want to count.
Basic logic is that , we set the Flip flops in such a way that they change their values from 0 to 1 or 1 to 0 in a particular time period .
Each output will have different frequency of changing of 0 to 1 or 1 to 0.
These outputs change in such a way that all together, all the outputs represent numbers from 0-15 (for up) or 15-0(for down) in an order.

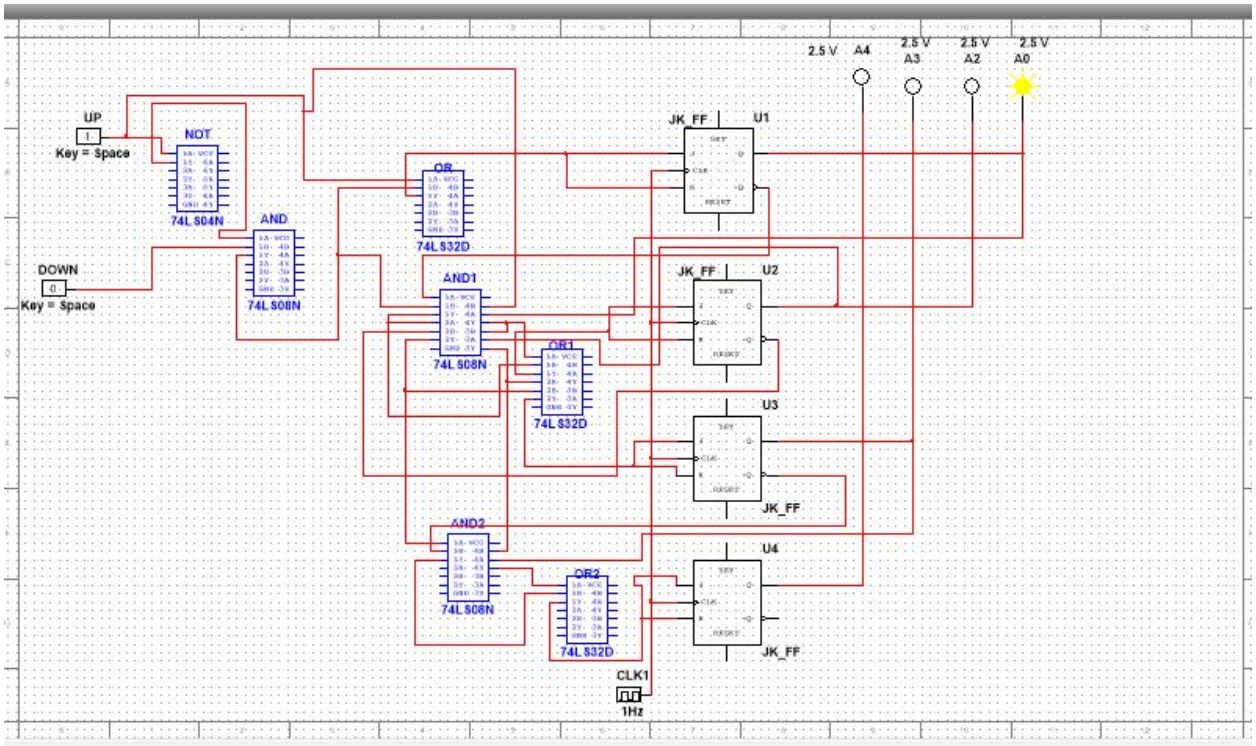
Logical diagram for 4-bit up down synchronous counter is given below





Up-counting
(initially 0)





Next it becomes 1 and so on..

For down counting it changes from 15-0