CS540 Practice Assignment 4

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1 Tasks

1. Determine the cache configuration for your machine. (use /usr/local/papi/bin/mem_info)
2. Run cache.c and analyze (try to determine cache configuration from access times).
3. Run cache.c with PAPI
4. Run cache.c with cachegrind
5. Run cache.c with dinero and explore different cache configurations.
6. Create memory trace for matrix multiplication for the Cache simulator (cache.map and explore miss rate with different cache configurations.)

2 Results

2.1 Cache configuration for `float.cs.drexel.edu`

```
$ ./papi_mem_info
Memory Cache and TLB Hierarchy Information.
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TLB Information.
  There may be multiple descriptors for each level of TLB
  if multiple page sizes are supported.

L1 Instruction TLB:
  Page Size:            2048 KB
  Number of Entries:       7
  Associativity:        Full

L1 Instruction TLB:
  Page Size:            4096 KB
  Number of Entries:       7
  Associativity:        Full

L1 Data TLB:
  Page Size:               4 KB
  Number of Entries:      64
  Associativity:           4

L1 Data TLB:
  Page Size:            2048 KB
  Number of Entries:      32
  Associativity:           4

L1 Data TLB:
  Page Size:            4096 KB
  Number of Entries:      32
  Associativity:           4

L1 Instruction TLB:
  Page Size:               4 KB
  Number of Entries:      64
  Associativity:           4


Cache Information.

L1 Data Cache:
  Total size:             32 KB
  Line size:              64 B
  Number of Lines:       512
  Associativity:           8

L1 Instruction Cache:
  Total size:             32 KB
  Line size:              64 B
  Number of Lines:       512
  Associativity:           4
```

```
L2 Unified Cache:
   Total size:             256 KB
   Line size:               64 B
   Number of Lines:       4096
   Associativity:            8

L3 Unified Cache:
   Total size:           12288 KB
   Line size:               64 B
   Number of Lines:     196608
   Associativity:           16
```

mem_info.c PASSED

2.2 Comparisons of `cache.c`