Tabelas de Sinais									
ADD									
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5				
write_pc	0	0	0	0	1				
read_data_memory	0	0	1	0	0				
write_data_memory	0	0	0	0	1				
read_instruction_memor	1	1	0	0	0				
write_reg_instruction	0	0	0	0	0				
cotrol_pop	0	0	0	0	0				
control_push	0	0	0	0	0				
control_immediat	0	0	0	0	0				
write_reg	0	0	0	1	0				
read_reg	0	1	0	0	0				
alu_function	0	0	0	0	0				
control_branch	0	0	0	0	0				
control_return	0	0	0	0	0				
		SUB							
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5				
	0		0	0					
write_pc	0	0	0	0	1				
read_data_memory	0	0	1	0	0				
write_data_memory	0	0	0	0	1				
					0				
read_instruction_memor write_reg_instruction	0	0	0	0					

cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	0	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

MUL								
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5			
	0	0	0	0	1			
write_pc read_data_memory	0	0	0	0	0			
write_data_memory	0	0	0	0	1			
read_instruction_memor	1	1	0	0	0			
write_reg_instruction	0	0	0	0	0			
cotrol_pop	0	0	0	0	0			
control_push	0	0	0	0	0			
control_immediat	0	0	0	0	0			
write_reg	0	0	0	1	0			
read_reg	0	1	0	0	0			
alu_function	0	0	0	0	0			
control_branch	0	0	0	0	0			
control_return	0	0	0	0	0			
		DIV						

Estado 2

Estado 3

Estado 4

Estado 5

Estado 1

write_pc	0	0	0	0	1
read_data_memory	0	0	1	0	0
write_data_memory	0	0	0	0	1
read_instruction_memor	1	1	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	0	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

AND								
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5			
write no	0	0	0	0	1			
write_pc read_data_memory	0	0	1	0	0			
write_data_memory	0	0	0	0	1			
read_instruction_memor	1	1	0	0	0			
write_reg_instruction	0	0	0	0	0			
cotrol_pop	0	0	0	0	0			
control_push	0	0	0	0	0			
control_immediat	0	0	0	0	0			
write_reg	0	0	0	1	0			
read_reg	0	1	0	0	0			

	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5		
OR OR							
control_return	0	0	0	0	0		
control_branch	0	0	0	0	0		
alu_function	0	0	0	0	0		

	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5			
write_pc	0	0	0	0	1			
read_data_memory	0	0	1	0	0			
write_data_memory	0	0	0	0	1			
read_instruction_memor	1	1	0	0	0			
write_reg_instruction	0	0	0	0	0			
cotrol_pop	0	0	0	0	0			
control_push	0	0	0	0	0			
control_immediat	0	0	0	0	0			
write_reg	0	0	0	1	0			
read_reg	0	1	0	0	0			
alu_function	0	0	0	0	0			
control_branch	0	0	0	0	0			
control_return	0	0	0	0	0			

NOT								
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5			
write_pc	0	0	0	0	1			
read_data_memory	0	0	1	0	0			
write_data_memory	0	0	0	0	1			

read_instruction_memor	1	1	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	0	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

CMP CMP							
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5		
write_pc	0	0	0	0	1		
read_data_memory	0	0	1	0	0		
write_data_memory	0	0	0	0	1		
read_instruction_memor	1	1	0	0	0		
write_reg_instruction	0	0	0	0	0		
cotrol_pop	0	0	0	0	0		
control_push	0	0	0	0	0		
control_immediat	0	0	0	0	0		
write_reg	0	0	0	1	0		
read_reg	0	1	0	0	0		
alu_function	0	0	0	0	0		
control_branch	0	0	0	0	0		
control_return	0	0	0	0	0		

ADDI

	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5
write_pc	0	0	0	0	1
read_data_memory	0	0	1	0	0
write_data_memory	0	0	0	0	1
read_instruction_memor	1	1	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	1	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

SUBI								
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5			
write_pc	0	0	0	0	1			
read_data_memory	0	0	1	0	0			
write_data_memory	0	0	0	0	1			
read_instruction_memor	1	1	0	0	0			
write_reg_instruction	0	0	0	0	0			
cotrol_pop	0	0	0	0	0			
control_push	0	0	0	0	0			
control_immediat	0	0	1	0	0			

write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

		ADDI			
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5
write_pc	0	0	0	0	1
read_data_memory	0	0	1	0	0
write_data_memory	0	0	0	0	1
read_instruction_memor	1	1	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	1	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

ANDI							
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5		
write_pc	0	0	0	0	1		

read_data_memory	0	0	1	0	0
write_data_memory	0	0	0	0	1
read_instruction_memor	1	1	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	1	0	0
write_reg	0	0	0	1	0
read_reg	0	1	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

ORI						
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5	
write_pc	0	0	0	0	1	
read_data_memory	0	0	1	0	0	
write_data_memory	0	0	0	0	1	
read_instruction_memor	1	1	0	0	0	
write_reg_instruction	0	0	0	0	0	
cotrol_pop	0	0	0	0	0	
control_push	0	0	0	0	0	
control_immediat	0	0	1	0	0	
write_reg	0	0	0	1	0	
read_reg	0	1	0	0	0	
alu_function	0	0	0	0	0	
control_branch	0	0	0	0	0	
control_return	0	0	0	0	0	

Estado 1 Estado 2	Estado 3	Estado 4	Estado 5
write_pc 0 0 read_data_memory 0 0 write_data_memory 0 0 read_instruction_memor 1 1 write_reg_instruction 0 0 cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	Estado 3	Estado 4	Fotodo F
write_pc 0 0 read_data_memory 0 0 write_data_memory 0 0 read_instruction_memor 1 1 write_reg_instruction 0 0 cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	Estado 3	Estado 4	Fotodo F
read_data_memory			ESIAGO 5
read_data_memory 0 0 write_data_memory 0 0 read_instruction_memor 1 1 write_reg_instruction 0 0 cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	0	0	
read_instruction_memor 1 1 write_reg_instruction 0 0 cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	1	0	
write_reg_instruction 0 0 cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	0	0	(
cotrol_pop 0 0 control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	0	0	(
control_push 0 0 control_immediat 0 1 write_reg 0 0 read_reg 0 1	0	0	(
control_immediat 0 1 write_reg 0 0 read_reg 0 1	0	0	(
write_reg 0 0 read_reg 0 1	0	0	(
read_reg 0 1	0	0	(
	0	1	(
alu_function 0 0	0	0	(
	1	0	(
control_branch 0 0	0	0	(
control_return 0 0	0	0	
SW			
SVV			
Estado 1 Estado 2	Estado 3	Estado 4	Estado 5
write_pc 0 0	0	0	
read_data_memory 0 0	0	0	
write_data_memory 0 0	0	1	
read_instruction_memor 1 1	0	0	

write_reg_instruction

cotrol_pop	0	0	0	0	0
control_push	0	0	0	0	0
control_immediat	0	1	0	0	0
write_reg	0	0	0	0	1
read_reg	0	1	0	0	0
alu_function	0	0	1	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0

		CALL			
	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5
write_pc	0	0	0	0	1
read_data_memory	0	0	0	0	0
write_data_memory	0	0	0	0	0
read_instruction_memor	1	0	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	0	0	0	0
control_push	0	1	0	0	0
control_immediat	0	0	0	0	0
write_reg	0	0	0	0	0
read_reg	0	0	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0
		RET			

	Estado 1	Estado 2	Estado 3	Estado 4	Estado 5
write_pc	0	0	0	0	1
read_data_memory	0	0	0	0	0
write_data_memory	0	0	0	0	0
read_instruction_memor	1	0	0	0	0
write_reg_instruction	0	0	0	0	0
cotrol_pop	0	1	0	0	0
control_push	0	0	0	0	0
control_immediat	0	0	0	0	0
write_reg	0	0	0	0	0
read_reg	0	0	0	0	0
alu_function	0	0	0	0	0
control_branch	0	0	0	0	0
control_return	0	0	0	0	0