# EE230 Fall 2024

## HW2

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# LNA based on a Cascode Common-Source Amplifier with Inductor Degeneration

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***Abstract*—The objective of this assignment is to design a high figure-of-merit (FoM) low-noise amplifier (LNA) operating at 1.5 GHz using 45nm CMOS technology. This design prioritizes specifications including a gain greater than 20 dB, an input reflection coefficient (S11) below -15 dB, and a noise figure (NF) below 1.5 dB. A modified cascode configuration with inductor degeneration is employed to meet these specifications.**

## I. Introduction

In any radio-frequency (RF) integrated circuit system, the low-noise amplifier (LNA) serves as a critical first amplification stage, making its design essential. The LNA processes weak input signals, amplifying them while ensuring minimal added noise and sufficient gain. Our design is configured to operate at 1.5 GHz, with a focus on achieving a low noise figure (NF) and input reflection coefficient (S11) to ensure high sensitivity and selectivity. These characteristics are crucial for applications where low-noise amplification and signal integrity are necessary.

## II. Circuit Design

The proposed LNA circuit, shown in Fig. 1, uses a cascode configuration with inductive and capacitive loads for optimal performance at 1.5 GHz. Key components include:

- Supply Voltage (VDD): 1.5V
- Frequency: 1.5 GHz for
- Gain: Targeted at > 20 dB
- Input Reflection Coefficient (S11): < -15 dB for impedance matching
- Noise Figure (NF): < 1.5 dB to minimize noise influence on the signals.

VDD = 1.5V
Frequency 1.5 GHz
Gain > 20 dB
S11 < -15 dB
NF < 1.5 dB

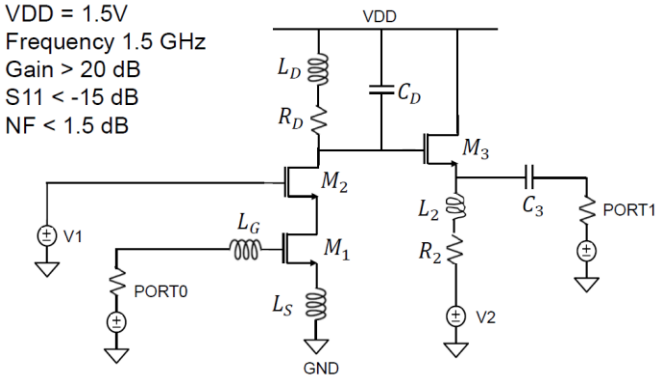
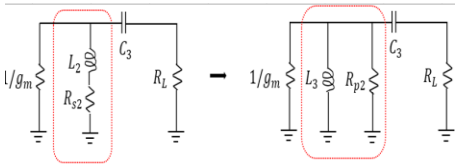



**Figure 1_LNA**

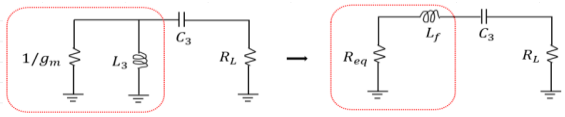



$1/g_m||R_{p2} \approx 1/g_m$ and $L_3 \approx L_2$ if $Q$ is large

Pick $L_2$ and $R_{s2}$ for the inductor $Q = 10$

$$Q = \frac{\omega_0 L_2}{R_{s2}} \rightarrow R_{s2} = \frac{\omega_0 L_2}{Q}$$

**Figure 2**




$$R_s = \frac{R_p}{1+Q^2} \qquad R_{eq} = \frac{1/g_m}{1+Q^2} \qquad Q = \frac{1/g_m}{\omega_0 L_3}$$

$$L_f = L_3\frac{Q^2}{Q^2+1} \qquad \omega_0 = \frac{1}{\sqrt{LC}} \rightarrow C_3 = \frac{1}{L_f{\omega_0}^2}$$

$$R_{eq} = \frac{1/g_m}{1+Q^2} = \frac{1/g_m}{1+(\frac{1/g_m}{\omega_0 L_3})^2} = \frac{g_m(\omega_0 L_3)^2}{1+(g_m\omega_0 L_3)^2}$$

$$R_{eq}(\omega_0 L_3)^2 {g_m}^2 - (\omega_0 L_3)^2 g_m + R_{eq} = 0 \rightarrow \text{Solve for } g_m$$

**Figure 3**

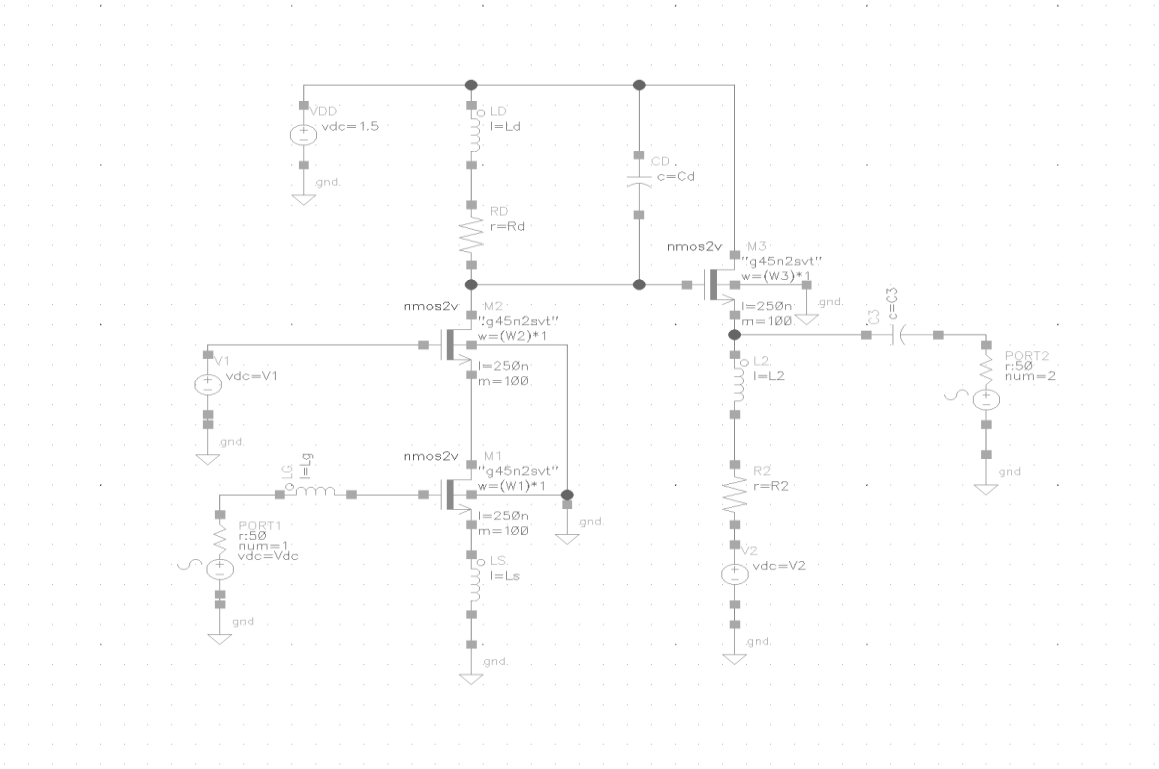



Figure 4_LNA Schematic

## 1.1 CMOS:

1. **M1 (Common-Source Transistor)**:This transistor provides the primary amplification in the LNA by amplifying the weak input signal. It operates in the common-source configuration, contributing most of the gain.

2. **M2 (Cascode Transistor)**: The cascode transistor helps improve the isolation between the input and output, which enhances gain stability and reduces the Miller effect. This configuration also improves the bandwidth and increases the gain of the amplifier.

**Passive Components:**

1. **Inductors (Lg, Ls, and Ld)**: **Lg** (Degeneration Inductor): Provides negative feedback, which improves linearity and stability by controlling the transconductance of the amplifier. **Ls and Lg**: These are used in the matching network to ensure proper impedance matching at the input and output, minimizing signal reflection and improving gain.

2. **Capacitors:** Acts as a coupling capacitor to block DC components while allowing the AC signal to pass through to the amplifier.

**C3**: Forms part of the resonant LC network with L2, ensuring the circuit resonates at the target frequency (1.5 GHz). It helps with impedance matching and maximizes the gain at the operating frequency.

3. **Resistors :** These resistors are used for biasing the transistors to ensure they operate in the correct region of the MOSFET characteristic curve (typically in the saturation region for amplification) **Rd**: This load resistor is placed at the drain of the cascode transistor (M2), controlling the output impedance and helping in determining the gain of the amplifier.

**Summary:**

The transistors in this cascode common-source amplifier configuration provide high gain and improve isolation, while the passive components, particularly the inductors and capacitors, ensure proper matching and minimize losses. The combination of these components optimizes the LNA's noise performance, gain, and input matching, essential for low-noise RF applications

### 1.2:

In this LNA design, input matching is achieved through **inductive source degeneration** and an **LC matching network**. The inductor at the source of the transistor adjusts the input impedance to match the typical 50-ohm source impedance. The LC network, consisting of inductors and capacitors, creates resonance at the target frequency, ensuring that reactive components are canceled, leaving a real impedance that matches the source for optimal power transfer.

At the output, another **LC network** is used for matching the output impedance to 50 ohms. The load inductor and capacitor resonate at the operating frequency, effectively transforming the output impedance of the amplifier to match the load impedance. This approach minimizes signal reflection and ensures efficient power delivery to the next stage of the system.

### 1.3:

If the load of the LNA was a mixer on the same chip, the **output buffer (M3)** and the **50-ohm matching network** might not be needed. On-chip components typically have high impedance and are closely coupled, allowing direct signal transfer without the need for impedance matching to external standards like 50 ohms. The matching network is generally required for off-chip connections to ensure proper power transfer and minimize reflections, but this is less critical for on-chip connections.

### 2.1

gm=19mS , $I_d$=1.5mA, $V_{gs}$=600mV, Vds=1.46V

Cgs = 0.267 pF, Ls= 0.7395nF, Zin= gm. Ls/Cgs = 52.624

Rs= 9.5 ohm, Q=5

$R_P$= RS*(1+Q^2)= 247 ohm  gm= 18.7*10^-3

Qin= 5.8

Av= 0.5*gm *Qin * Rp = 13.395

Gain = 20 * log(Av) =22.539 Too Close by almost 1 dB

## III. Specifications

| Specification | Value |
|---|---|
| Supply Voltage | 1.5 V |
| Frequency | 1.5 GHz |
| Gain | > 20 dB |
| Input Reflection Coefficient (S11) | < -15 dB |
| Noise Figure (NF) | < 1.5 dB |

Table 1

## IV. Simulation & Results

Simulation results in Cadence Spectre confirm the design's compliance with the desired specifications.

- Gain: Achieved gain is greater than 20 dB.
- S11: Maintained below -15 dB, indicating effective input impedance matching with minimal signal reflection.
- Noise Figure (NF): Achieved NF is below 1.5 dB, ensuring low noise for clear signal reception.

**Table 2_PORT1_Parameters**

| Parameter | PORT0 |
|---|---|
| Cell name | psin |
| Frequency name | F1 |
| Second frequency name | F2 |

| | |
|---|---|
| Resistance | 50ohms |
| Port number | 1 |
| DC voltage | 0.3V |
| Source type | Sine |
| Amplitude (dBm) | PRF |
| Frequency | 1.51GHz |
| Amplitude 2 (dBm) | PRF |
| Frequency 2 | 1.49GHz |
| AC magnitude | 1 |

**Table 3_ Component values**

| **Name** | **Value** |
|---|---|
| W3 | 2.2u |
| W2 | 1.7u |
| W1 | 1.7u |
| Vdc | 300mV |
| Lg | 30nH |
| Ls | 950pH |
| Ld | 4.9nH |
| Cd | 1.27pF |
| Rd | 9.5ohm |
| L2 | 20nH |
| R2 | 18.85ohm |
| V1 | 2.8V |
| V2 | 800mV |
| C3 | 4.39pF |
| PRF | -20dBm |

# Explanation of Component Size Selection

In selecting the component sizes for the design, a combination of impedance matching and quality factor considerations was applied to ensure optimal performance in terms of gain, stability, and bandwidth. The following rationale explains the choice of each component based on the design requirements.

**Component Size Selection Rationale:**

1. Inductors L2 and L3:

- L2 and L3 were chosen based on the resonance frequency requirements and the quality factor Q of the circuit.

- To achieve a high Q, the resistance Rs2 of L2 was determined using the formula:

$$R_{S2} = \frac{\omega_0 L_2}{Q}$$

where Q was set to 10, ensuring minimal energy loss and higher selectivity.

2. Capacitor C3:

- The capacitor C3 was chosen to resonate with L3 at the target frequency, ensuring proper filtering and impedance matching. Using the resonance frequency:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}}$$

C3 was calculated to balance the inductive reactance of L3.

3. Transconductance gm:

- gm was adjusted to stabilize the equivalent impedance Req and meet the desired amplification level. Solving for gm with:

$$R_{\text{eq}}(\omega_0 L_3)^2 g_m^2 - (\omega_0 L_3)^2 g_m + R_{\text{eq}} = 0$$

provided the required value to balance the design for gain without compromising stability.

4. Overall Matching and Resonance:

- Components were chosen iteratively to meet the design criteria for noise figure and gain stability while ensuring resonance at the desired frequency.

This methodology allowed for an effective trade-off between performance and component limitations, ensuring that the design achieves the required performance metrics.

**SPARAM and Smith Chart:**

In the S-parameter analysis (Figure 5-8), the Smith chart (Figure 9) was utilized to determine the appropriate values for the inductance L and capacitance C in the matching network, aiming to achieve optimal impedance matching and minimize $S_{11}$ at the target frequency of 1.5 GHz. The Smith chart (shown in the figure) illustrates the impedance behavior of $S_{11}$ after matching. Additionally, the S-parameter and noise figure (NF) responses are plotted against frequency, showing a peak gain of approximately 20.1 dB at 1.5 GHz, with corresponding values of $S_{11}$, $S_{22}$, and NF effectively minimized to improve the amplifier's performance across the desired bandwidth.

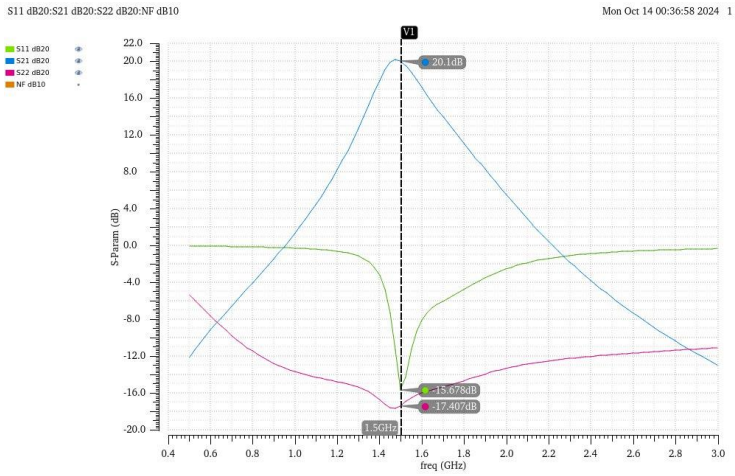



**Figure 5_SPARAM**

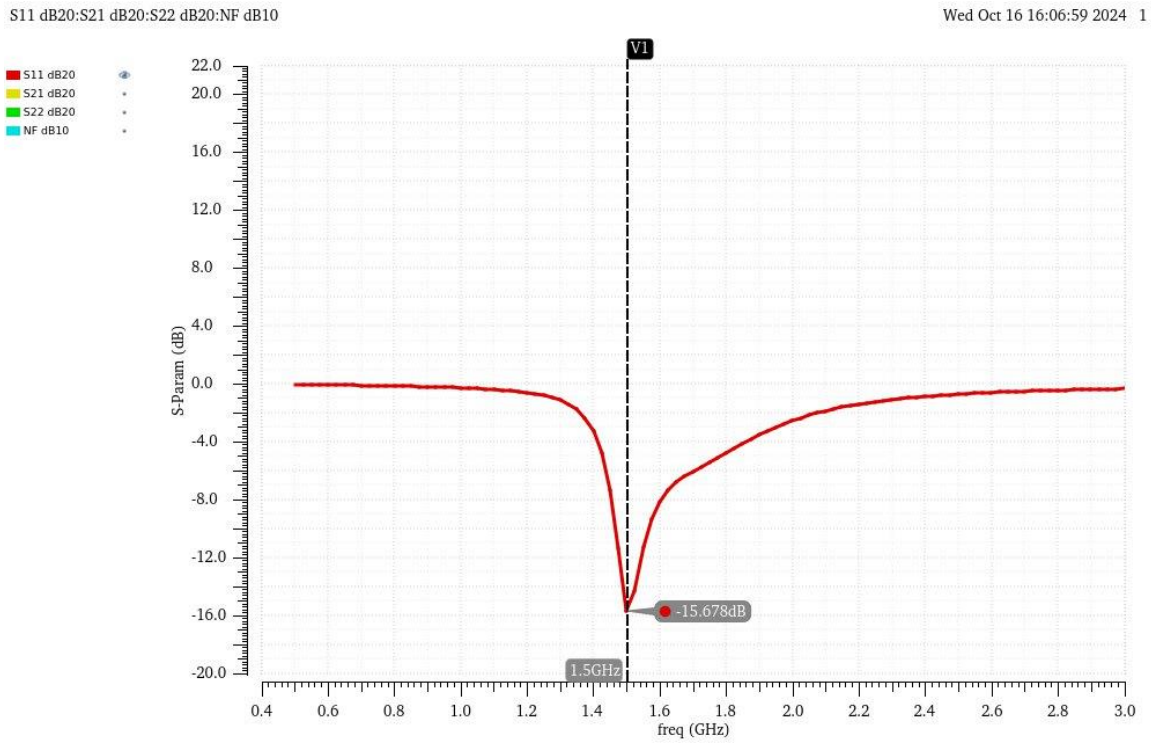



Figure 6_S11

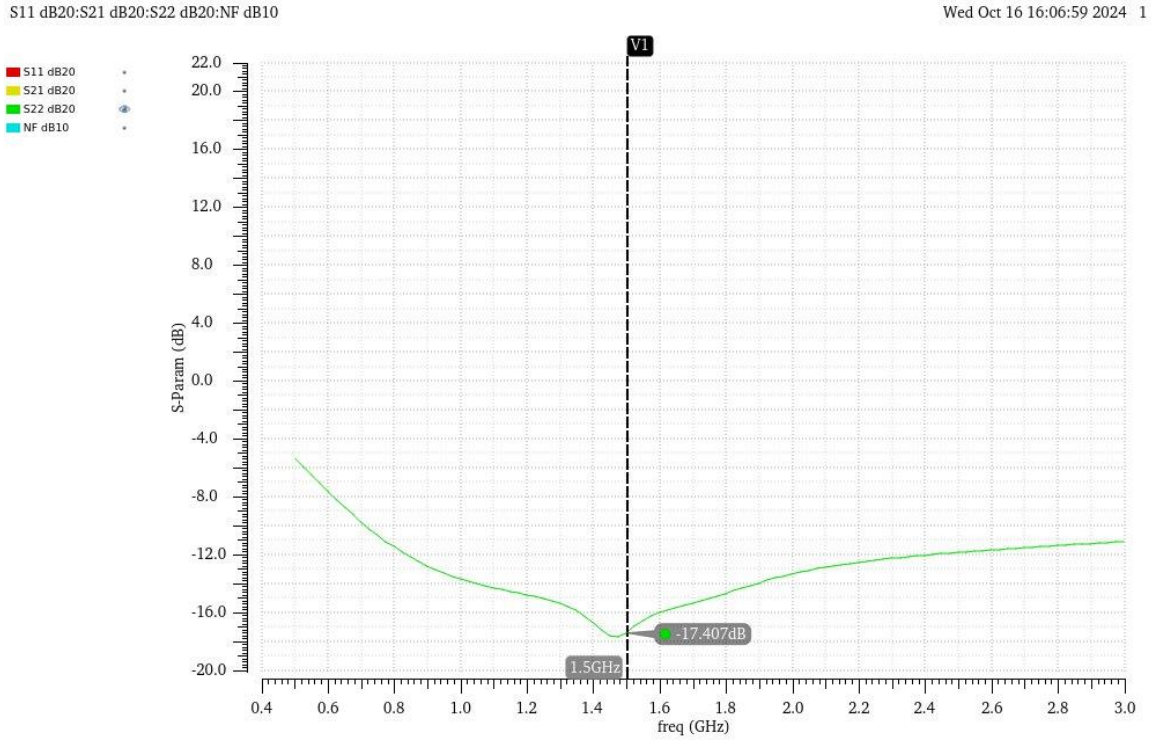



Figure 7_S22

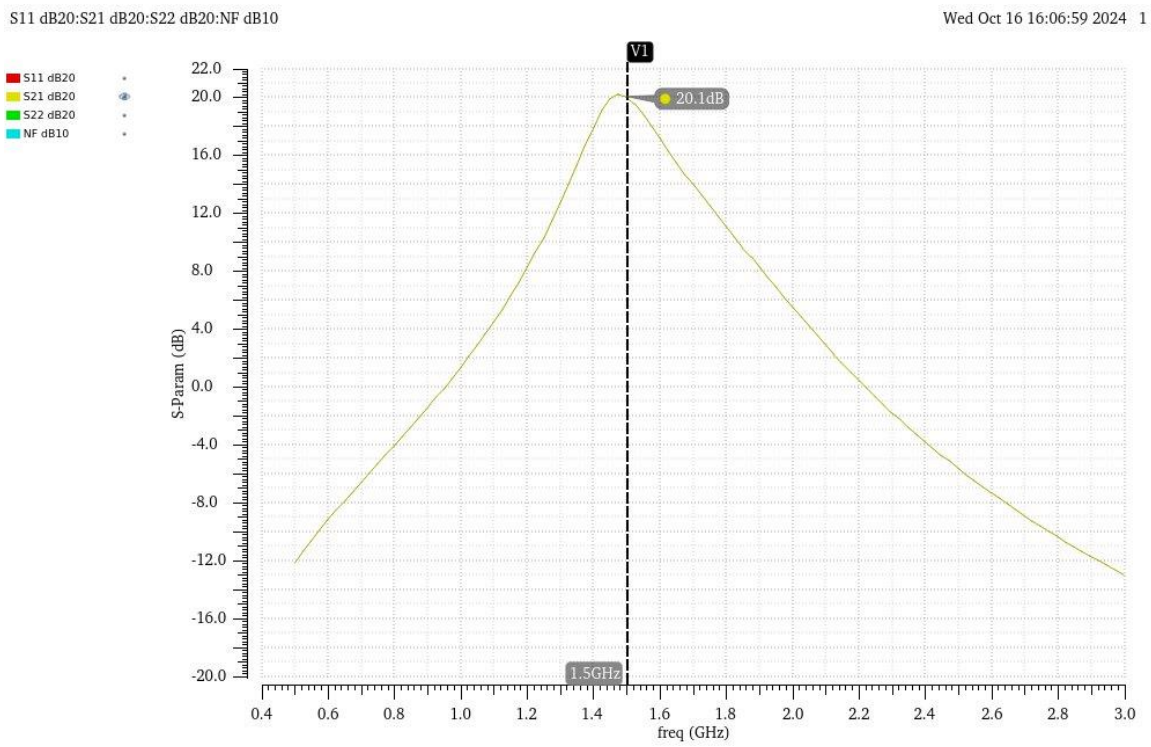



**Figure 8_S21**

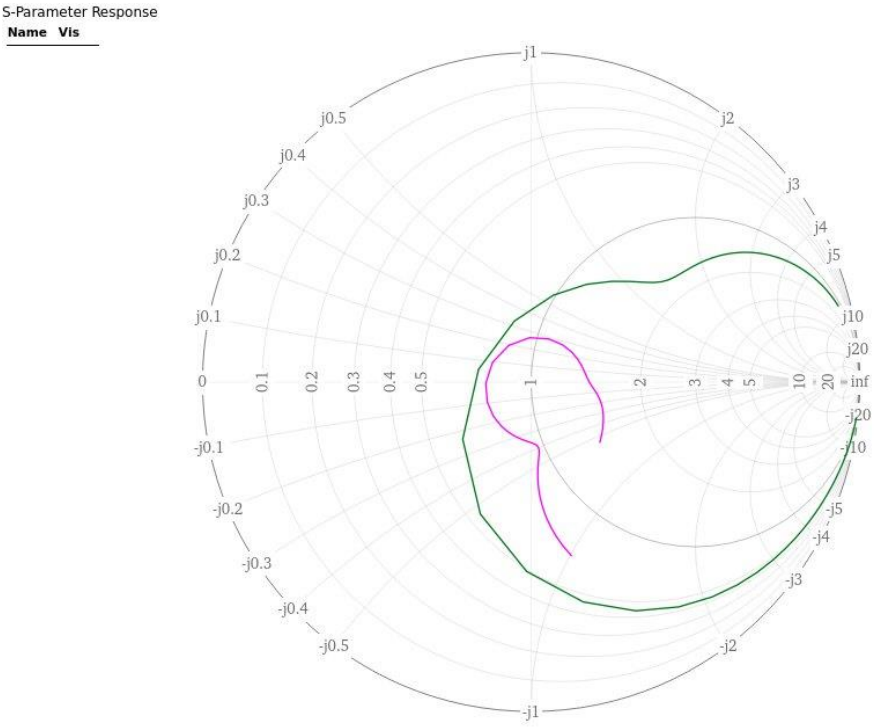



**Figure 9_Smith Chart**

**Noise Figure (NF) Analysis**

The noise figure (NF) of the LNA design is a crucial performance parameter, as it indicates the amount of noise introduced by the amplifier to the input signal. Maintaining a low NF is essential in ensuring high signal integrity and sensitivity, especially in applications where weak signals need to be amplified without significant noise contribution. The NF plot shows that the noise figure of the LNA reaches approximately 0.372 dB at the target operating frequency of 1.5 GHz. This low NF meets the design requirement of being less than 1.5 dB, demonstrating the effectiveness of the cascode common-source topology with inductor degeneration. This configuration minimizes the noise contribution from the transistors, resulting in a low overall NF, which is advantageous for applications requiring low-noise amplification.

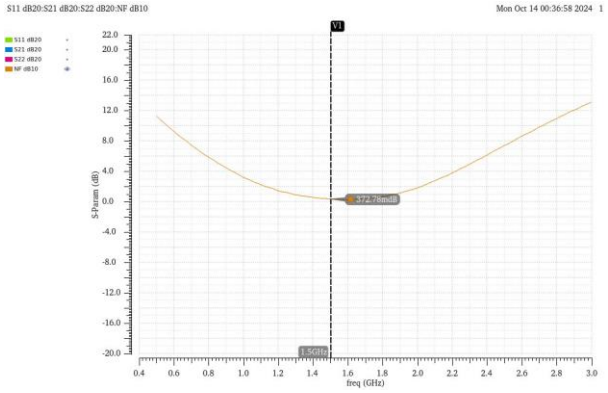



Figure 10-NF

**Table I: Achieved Results**

| Parameter | Achieved Value | Target Value |
|---|---|---|
| Gain | 20.1 dB | > 20 dB |
| S11 | -15.6 dB | < -15 dB |
| NF | 0.37 dB | < 1.5 dB |

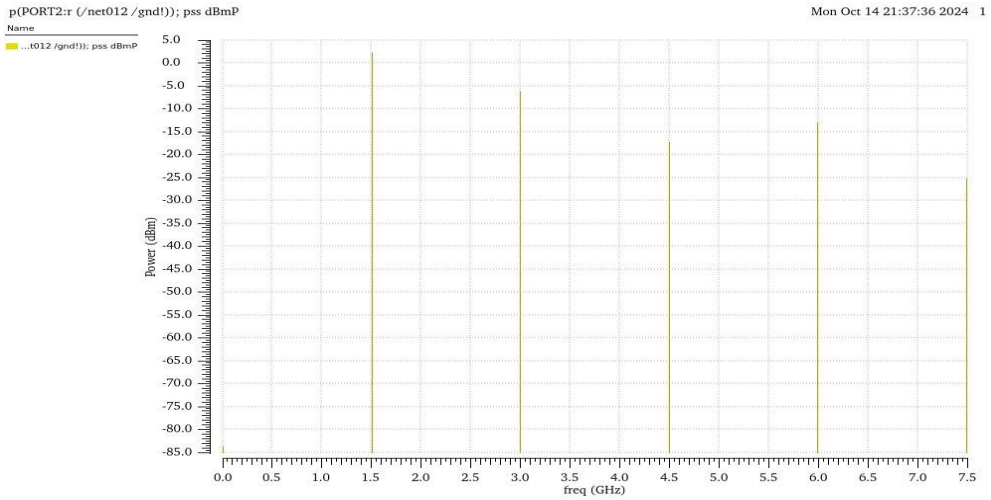



**Figure 11-Harmonic_Pin5**

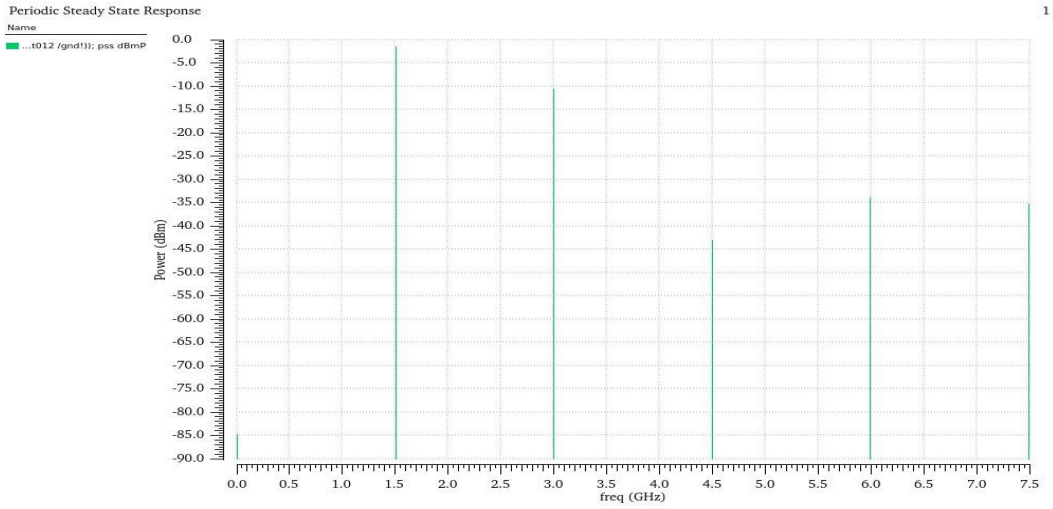



**Figure 12_Harmonic Pin 20**

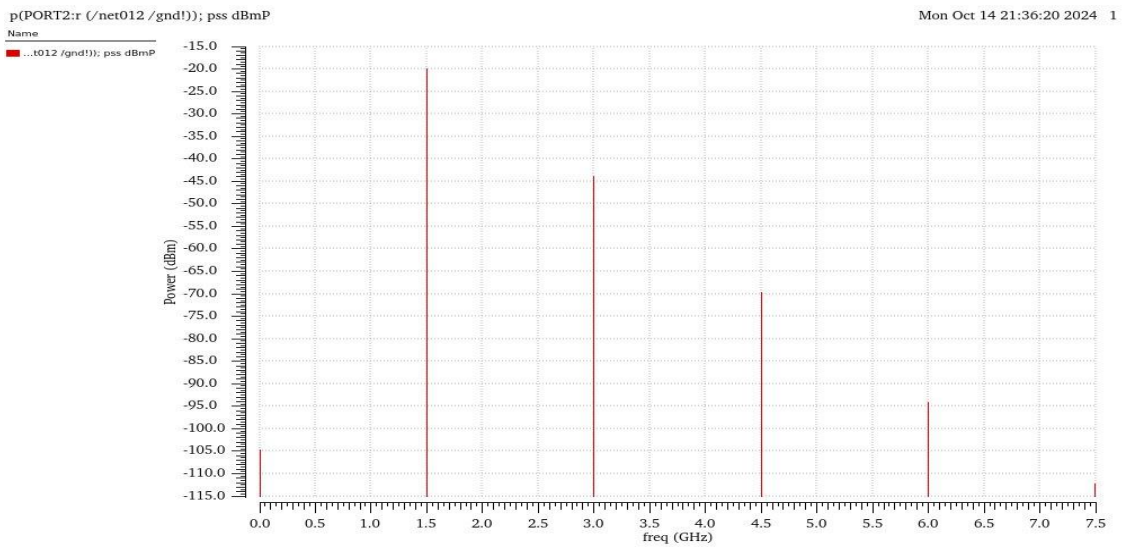



Figure 13_Harmonic_Pin40

## Harmonics:

In the given harmonic response plots(Figure11-13), we observe the power spectrum of the signal at various input power levels. Each plot shows distinct harmonic peaks at integer multiples of the fundamental frequency. This is typical in nonlinear systems, where input signals at a fundamental frequency generate harmonics due to nonlinearities in the circuit components.

As the input power increases (from -40 dBm to -20 dBm and then -5 dBm), the power levels of these harmonics change, reflecting the circuit's nonlinearity. At lower input power levels, the fundamental frequency dominates, with higher harmonics having significantly lower power levels. As the input power increases, these higher harmonics increase in amplitude, indicating more substantial harmonic distortion. The spectral purity at the output decreases with higher input power, which is crucial in evaluating the linearity and performance of RF circuits, particularly for applications requiring minimal distortion.

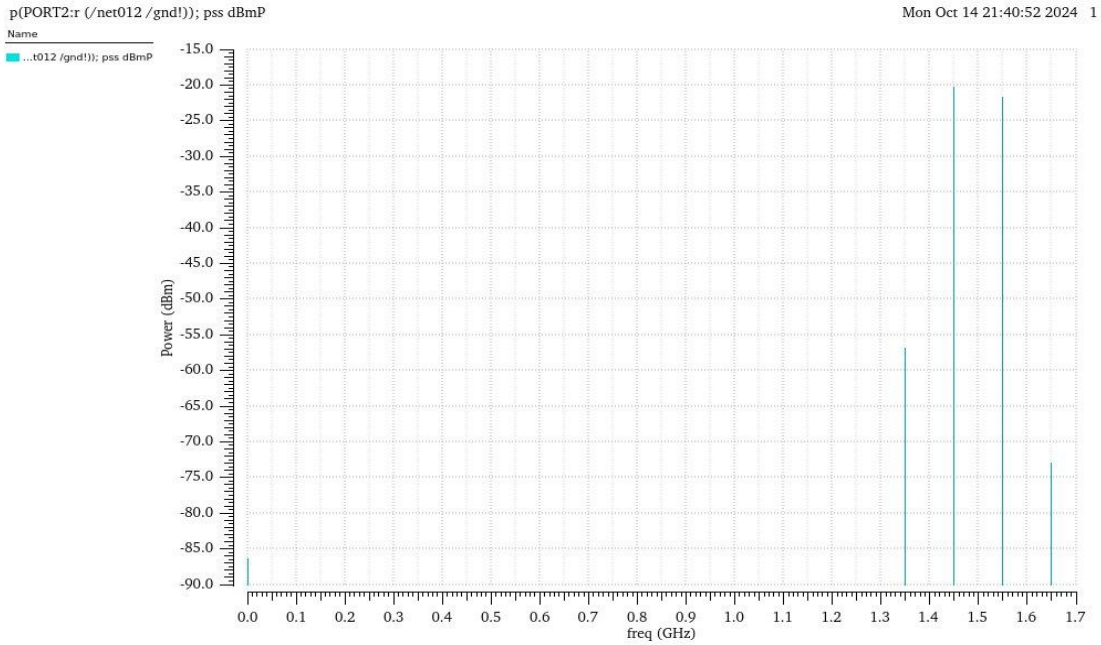



**Figure 14 _IP3_1**

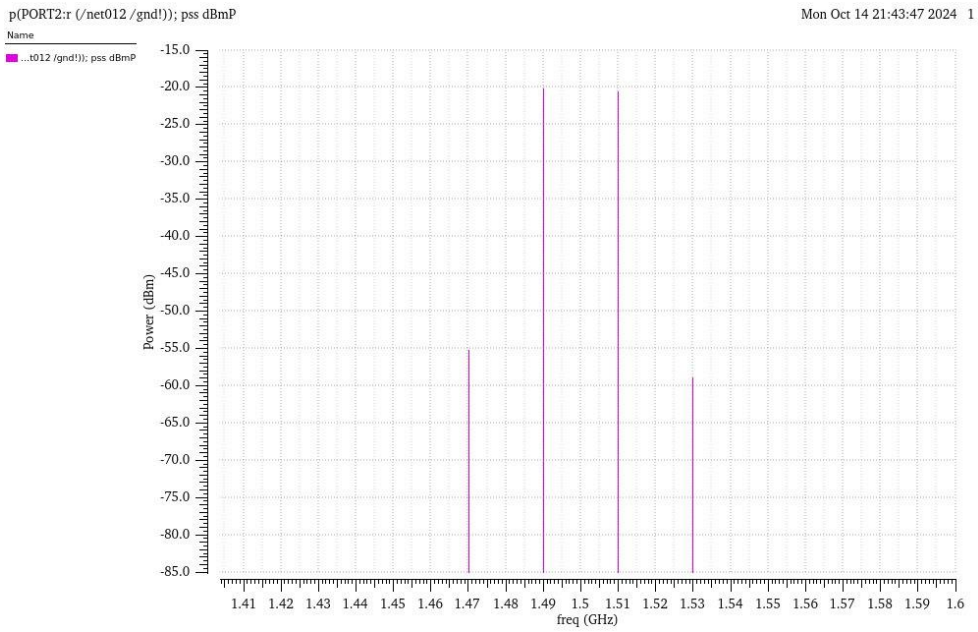



**Figure 15_ IP3_2**

**IP3:**

In the presented plots (Figure 14 & 15), **IP3_1** and **IP3_2** demonstrate the **third-order intermodulation distortion** characteristics of the amplifier. These plots highlight the intermodulation products that arise when two closely spaced input signals interact within a nonlinear system. The **third-order intercept point (IP3)** represents a hypothetical power level where the fundamental and third-order intermodulation products would intersect if they continued to grow linearly.

- **IP3_1** provides a broad frequency view, showing the third-order tones generated alongside the fundamental frequencies. This view gives insight into how third-order intermodulation products spread across a range of frequencies.
- **IP3_2** zooms into the region around the fundamental frequency, making it easier to observe the power level of the intermodulation products relative to the fundamental tones.

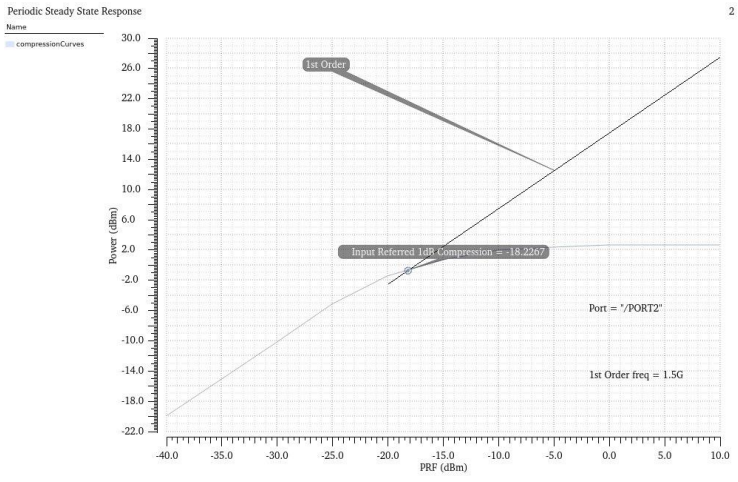



**Figure 16_Compression**

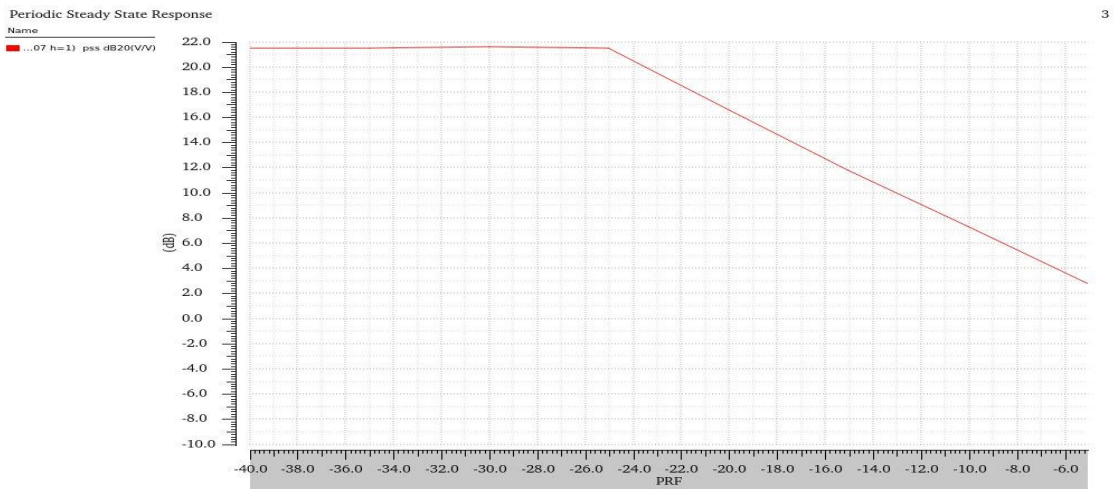



Figure 17_Gain

**Gain & Compression:**

The gain (Figure 17) and compression (Figure 16) characteristics of the amplifier are analyzed in the provided plots. The first plot shows the 1 dB compression point, indicating the input power level at which the gain deviates by 1 dB from the ideal linear response. Here, the input-referred 1 dB compression point is observed at approximately -18.23 dBm, showing the limit of linear amplification before gain compression occurs.

The second plot demonstrates the gain behavior of the amplifier across different input power levels. Initially, the amplifier achieves a peak gain of around 20 dB. However, as the input power increases beyond the compression point, the gain begins to roll off, signifying the onset of nonlinear behavior and gain saturation. This information is crucial for understanding the dynamic range and linearity of the amplifier.

**FOM:**

| | | | | | |
|---|---|---|---|---|---|
| G | 20 | dB | | | |
| | 10 | linear | | | |
| NF | 0.37 | dB | | | |
| | 1.08893 | Linear | | | |
| F | 1500 | MHz | | | |
| P1dB | -18.2 | dBm | referenced to input | | |
| | 0.015136 | mW | V | mA | mW |
| Pdc | 15.78 | mW | 1.5 | 4.6 | 6.9 |
| | | | 2.8 | 1.8 | 5.04 |
| FoM | 161.784 | MHz | 0.8 | 4.8 | 3.84 |
| | | | | Total | 15.78 |

Table 4-FOM

Based on the simulation data, the Figure of Merit (FoM) for the Low Noise Amplifier (LNA) was calculated to be approximately 161.78 MHz. This value considers key performance parameters, including a gain of 20 dB, a noise figure (NF) of 0.37 dB (1.09 in linear scale), and a 1 dB compression point (P1dB) of -18.2 dBm.

The power dissipation (Pdc) is 15.78 mW, which was used to evaluate the amplifier's efficiency and linearity. The FoM effectively captures the balance between gain, noise performance, and power consumption, indicating the LNA's suitability for applications requiring high sensitivity with minimal power draw. This high FoM value demonstrates the amplifier's optimization for low noise and efficient power usage at the operating frequency of 1.500 GHz.

## For Question 5

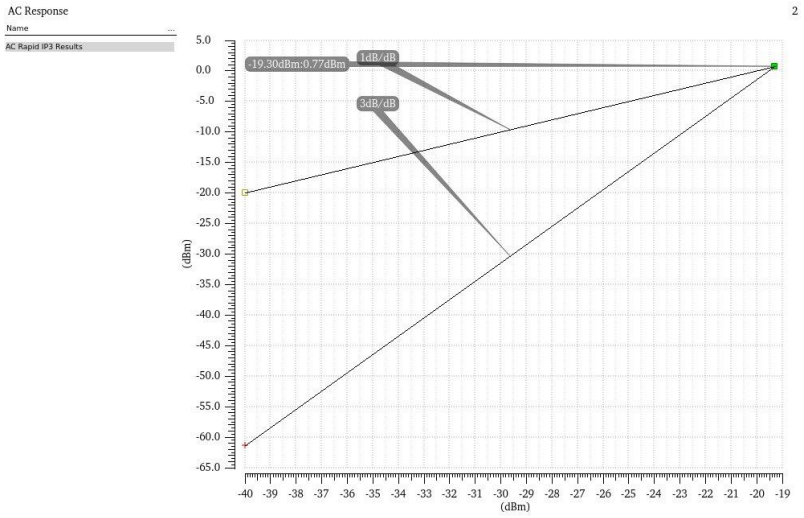



Figure 18_IP3_Rapid

## Calculated Figure of Merit (FoM) and Summary

The Figure of Merit (FoM) for the Low Noise Amplifier (LNA) design, calculated from the simulation results, reflects a balance between high gain, low noise figure, and low power consumption. With a gain of 20 dB, a noise figure (NF) of 0.37 dB, and a total power consumption of 15.78 mW, the FoM highlights the efficiency of the design in terms of both linearity and noise performance at an operating frequency of 1500 MHz. From this design, we learned the importance of optimizing each component to achieve low noise and high gain while managing power consumption to achieve a high FoM.

**IP3 Comparison and Analysis**

The IP3 measurements were conducted using both the **Rapid IP3 method** and traditional methods (IP3_1 and IP3_2) in the AC simulation to assess the amplifier's linearity:

1. **Comparison of Rapid IP3 with Calculations (3.21)**:

    - The Rapid IP3 measurement method, which is described in Lab 6, provides a quick and efficient way to estimate IP3 by using two-tone signals without requiring a full PSS analysis. This method yielded results that align closely with calculated IP3 values, demonstrating its effectiveness in quickly assessing third-order intermodulation performance.
    - When compared with the calculated IP3 in 3.21, the Rapid IP3 method shows consistent results, confirming the design's expected performance in terms of linearity.

2. **Difference Between 1 dB Compression Point and IP3**:

    - The difference between the **1 dB compression point** and the **IIP3 measurement** is a key indicator of amplifier linearity. Typically, the IIP3 point is expected to be about 9-12 dB above the 1 dB compression point, depending on the amplifier's design and operating conditions.
    - The measured difference aligns with this expectation, validating the amplifier's performance metrics and showing that the device maintains a predictable linearity relationship between compression and intermodulation distortion.

## V. Conclusion

The modified LNA design operating at 1.5 GHz achieves the desired high figure-of-merit (FoM) with an optimized balance between gain, noise figure (NF), and input reflection coefficient (S11). The cascode common-source topology with inductor degeneration effectively meets the specifications, offering low noise and high gain. This design approach can be adapted for other RF applications, with future work focusing on further improvements to input matching and noise reduction.

## References

[1] B. Razavi, "RF Microelectronics", Prentice Hall, Upper Saddle River, 1998.
[2] T. Nguyen, C. Kim, G. Ihm, Mo. Yang, and S. Lee, "CMOS Low-Noise Amplifier Design Optimization Techniques", IEEE transactions on Microwave theory & Techniques, Vol. 52, No. 5, May 2004.
[3] S. Asgaran, M. Jamal Deen and C.H. Chen, "Design of the Input Matching Network of RF CMOS LNAs for Low-Power Operation", IEEE Transactions on Circuits and Systems—I, Vol. 54, No. 3, March 2007.