Physical Techniques for Chip-Backside IC Debug in Nanotechnologies

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Editor's note:
Physical failure analysis remains indispensable for final defect confirmation, but is increasingly difficult due to semiconductor technology advances with smaller feature sizes, many metal layers, and flip-chip packaging. This article reports on how, despite an uphill battle, constant innovations keep physical failure analysis going.

—Erik Jan Marinissen, NXP Semiconductors

In recent IC technologies, physical techniques supporting functional circuit analysis must access the active information through the chip's backside.[1] For this purpose, the device typically receives a global polishing preparation. In most cases, mechanical stability and heat-sink requirements limit the minimum remaining silicon substrate thickness to 50 to 100 microns, or *moderate silicon thickness*.

The penetration depth of particle beams is orders of magnitude smaller, so the previously successful electron or ion beam microscopy derivatives using voltage contrast, such as electron-beam probing (EBP), do not apply under these circumstances. Bulk silicon, however, is transparent to light if photon energies are smaller than the Si band gap of 1.1 eV—that is, the near-infrared (IR) regime.

When the circuit design needs to be modified, engineering samples with the new circuit concept increase the confidence level for new mask production. Those engineering samples can be produced by physical cutting and rewiring of the existing circuit using focused-ion beam (FIB), the *circuit edit* technique. CE also must be performed through the chip's backside. The key to backside CE is milling local trenches to the bottom level of the shallow trench isolation (STI), leaving an ultrathin layer of silicon (approximately 300 nm) for active device function, similar to SOI (silicon on insulator). This preparation technique, expanded to planes of up to 0.03 mm^2, offers a new breakthrough approach of physical functional-analysis techniques. Although the circuit remains fully functional, the active volume is small enough to interact with high-energy photons or particle beams applied through the chip's backside.

In this article, we present and evaluate a survey of these analysis techniques for functional analysis and resolution potential. We also discuss the CE technique valid for nanotechnology ICs that is based on the formation of local trenches using the bottom of STI as an endpoint for FIB milling. This process enables the breakthrough application of nanoscale analysis techniques to a fully functional circuit through the chip's backside. Several applications demonstrate how powerful this approach can be.

Backside access functional analysis

Global polishing of bulk silicon is a high-yield process as long as a moderate thickness of 50 to 100 microns remains. The preferred interactive medium of functional-analysis techniques in this case is near-IR optics, with photon energies smaller than the silicon energy band gap of 1.1 eV, corresponding to wavelengths of 1.1 microns and higher. Three main dynamic approaches have been established: time-resolved photon emission (TRE), laser voltage probing (LVP), and laser stimulation techniques (see Figure 1).

Table 1 compares LVP and TRE to EBP, the reference front-side access technique. We did not include laser stimulation in this comparison, because there is not just one single technique. There is such a

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large variety of signal generation and data access techniques that covering it fully would require a survey of its own.

TRE

Photon emission is the standard functional-analysis technique of semiconductor devices because it occurs in an MOS transistor without any further stimulus when a considerable number of carriers gain kinetic energy high enough to relax by emitting photons.[2] This is happening in CMOS digital circuits mainly during the signal pattern's rise and fall time. Although this dynamic light signal is faint, TRE is a powerful, reliable, and easy-to-interpret technique with low risk of artifacts and time resolution in the 10-ps regime.[3]

Owing to the low signal level, it is necessary to integrate the signal over several samples. Because the waveform is not reproduced in full but the signal represents only the short switching pulses, trigger stability and jitter are critical.[4] TRE intensity decreases nonlinearly with supply voltage,[5] but recent studies indicate that the resulting signal-to-noise ratio (SNR) challenge of recent IC technologies might not be too severe.[6] Thus far, the emission's spectral information has only been marginally used in analysis. A more detailed understanding of device physics and the mechanisms of photon emission could change this.

LVP

When an IR laser illuminates the active devices through the chip's backside, the reflected light is modulated by active device operation in the parts per million (ppm) range. This signal has been proven to be linearly correlated to the voltage applied to the device, and the waveform of a signal pattern passing the node can be reproduced, very similar to EBP.[7] Originally, the signal was attributed to electrical fields in the device due to free-carrier dynamics (the Franz-Keldysh Effect). Recent investigations using device simulation have correlated the signal to pure free-carrier-absorption dynamics by space charge modulation,[8] which allows simpler modeling of the effect. The time resolution is in the same range as TRE. Due to the waveform reproduction, we can still obtain the signal pattern information when trigger stability is problematic. Probe placement might not be trivial when local interference is affecting the signal level.

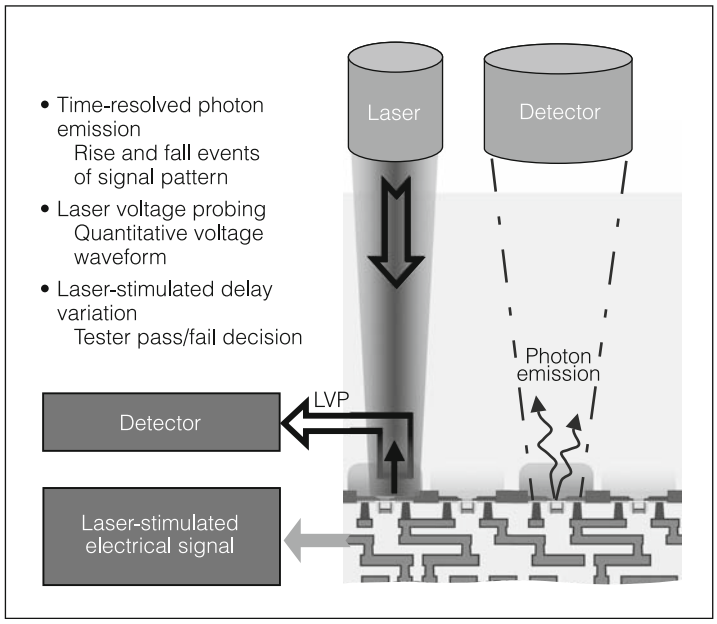

Figure 1. Optical probing and stimulation techniques. (LVP: laser voltage probing.)

Table 1. Comparison between LVP, time-resolved photon emission (TRE), and electron-beam probing (EBP).

Criterion	LVP (IDS 2K)	TRE	EBP (IDS 10K)
Spatial resolution (SR)	0.7 μm	0.25 μm (SILs)	100 nm
Bandwidth	About 10 GHz	About 6 GHz	About 9 GHz
Acquisition time	1 to 10 min	1 min to 24 hr	1 to 10 min
Voltage accuracy	Probe point dependent	No	Quantitative
Voltage linearity	Qualitative	No	Good
Sensitivity to supply voltage	Linear	Complex	Linear
Invasiveness	Slight or none	None	None
Sample preparation	Decapsulation and thinning	Decapsulation and thinning	Decapsulation
Trigger cycle	5 μs to about 10 ms	Any	Any
Node access	Any SR limited	Any SR limited	Top two layers interconnect
Waveform reproduction	Good to SR limited	No waveform	Good

* SIL: solid immersion lens.

Table 2. Derivatives of photonic and thermal laser stimulation.

Circuit	Static techniques	Dynamic techniques
Photoelectric laser stimulation (PLS)	Optical beam-induced current (OBIC)	Laser-assisted device alteration (LADA)
	Light-induced voltage alteration (LIVA)	Shmoo variation, delay variation
Thermal laser stimulation (TLS)	Optical-beam-induced resistivity change (OBIRCH)	Resistive interconnect localization (RIL)
	Thermally induced voltage alteration (TIVA)	Soft-defect localization (SDL), shmoo variation
	Seebeck effect imaging (SEI), thermoelectric voltage	Delay variation

Although LVP has been available for a long time, it hasn't developed a whole lot since TRE was introduced, because TRE offered far more straightforward data access. With the in-depth investigation of the interaction mechanisms, and a new product generation using polarized light, LVP might become increasingly attractive again, especially because it offers some robustness to IC clock instabilities.

Laser stimulation

Scanning IR lasers with several hundred megawatts can stimulate electrical-signal alteration either by local heat conversion of the absorbed light modulating electrical parameters—thermal laser stimulation (TLS)[9]—or by the photocurrent induced into the signal path if photon energies reach the silicon band gap level and electron hole pairs are generated. This process is called photoelectric laser stimulation (PLS).

Because it is possible to alter electrical-circuit behavior in various ways, many techniques employ the laser stimulation principle. Table 2 gives an overview of the most common techniques used for statically and dynamically driven circuits. This article concentrates on techniques for dynamic circuit analysis. The results of dynamic laser stimulation can be obtained either by employing a pass/fail condition with the tester under stimulation (shmoo variation) or by directly evaluating the signal pattern variation. A systematic overview on the laser stimulation for static techniques is available,[10] but not for dynamic circuit operation (which is why some of the techniques listed in Table 2 seem to overlap), and some possible options have not been published yet.

An effective analysis uses an already established test signal path of a soft-failing device that is driven below a critical temperature, and the laser raises the illuminated area above the critical level. Such a shmoo variation using TLS results in a resistive interconnect localization (RIL) if the soft defect is located in interconnect levels, or a soft defect localization (SDL) when active devices are affected.[11] Photoelectric laser stimulation (PLS) causes similar effects.

The other group of techniques obtain the signal pattern directly, like laser-assisted device alteration (LADA) or delay variation.[12,13] In a transistor, the effects of PLS and TLS on the output current must be studied in detail for correct evaluation.[10] In general, if PLS is enabled by selection of the proper laser wavelength, it usually prevails over TLS. Laser stimulation's time resolution and required trigger quality depend on the signal extraction procedure. In laser stimulation, we can apply a large variety of stimulation and read-out opportunities, and the overall potential of this approach is not exhausted yet by far.

Nanoscale potential

Maximum microscopic resolution is the light wavelength referring to a repeating structure's length, or *pitch*. A pitch consists of a minimum of two features, so the minimum resolved feature is smaller by a factor of 2. Realistic pitch resolution is approximately 800 nm, or 400-nm feature size. But feature sizes are rapidly shrinking with technology innovation. Solid immersion lenses (SILs) make bulk silicon a part of the microscope and increase resolution theoretically by the refraction index of silicon, $n_{Si} = 3.5$. Features of 200 nm have been resolved using SILs.[14]

As technologies progress further into the nanometer range, even with SILs, IR techniques can localize only the area of interest but not the exact device. In addition, it is increasingly inevitable that scanning probe techniques and derivatives will identify the critical node in the nanoscale regime. Nanoprobing uses the contacts to the active structures under investigation.[15,16] Physical- or chemical-preparation techniques must be applied from the chip's front side to open the probing areas; such techniques typically attack the interconnect layers.

This process is time-consuming and risky. If the failing transistor cannot be found in the final

measurement, the problem might have been removed with the backend, leaving no second chance for other failure analysis techniques.

Backside circuit edit

The challenge for FIB-based CE today is access through the chip's backside, which requires circuit cut-and-paste operations much closer to the active layers than global preparation techniques can provide. A trenching process using a FIB with a coaxial IR optical microscope removes bulk silicon down to the bottom level of STI. This process involves three steps (see Figure 2): After applying a global polishing technique, we identify the region of interest with the IR microscope. Then, after a special FIB cleaning procedure, a $200 \times 200\ \mu m^2$ wide trench is milled until the operator stops on the n-well level. The end point becomes visible because of a voltage contrast between the n-wells and the substrate due to the built-in potential of the pn junction.[17] Next, a smaller local trench is milled until the STI becomes visible as imaging contrast—lower secondary electron emission of SiO_2—and the preparation ends.

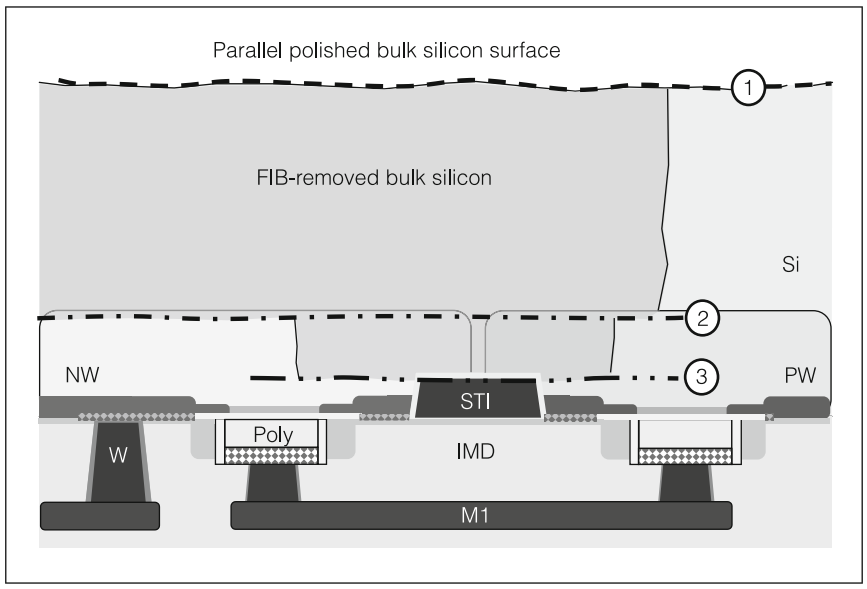

Figure 2. Focused-ion beam (FIB) preparation for backside circuit edit. (IMD: intermetal dielectric; M1: metal 1; NW: n-well; Poly: highly doped polycrystalline silicon; PW: p-well; W: tungsten.)

This way, the active device material is reduced down to 300 nm to 400 nm (the depth of the STI trenches), and the chip is ready for the actual edit process: the milling of narrow trenches for the cuts and contact holes.[18]

This backside FIB process offers several more opportunities to edit the circuit than the front-side process: The technique to the endpoint of the contact trenches on the silicide interface, which is only 300 nm below the trench to STI, is meanwhile established.[19] This allows contact with any source and drain area on the chip, even those that have not been contacted on the IC interconnect level. All the functional nodes are represented at the active device level. Figure 3 illustrates a typical backside CE.

Any CE contact can be performed using the contact to silicide (CtS) process; only cut operations still have to be performed by trenching deeper into metal interconnects. The lower aspect ratio for CtS compared to contacts to metal lines (see the right side of Figure 3) is very fortunate since it reduces the contact resistance, which is the critical parameter for nanoscale applications. With current platinum deposition, contacts on silicide have resistivities below 60 $\Omega/\mu m^2$. Typical contact sizes of $1 \times 0.2\ \mu m^2$ end up with 300Ω resistance per contact, which is considerably lower than field-effect transistor (FET) channel resistances of several kilohms,[20] and is acceptable for most CE and probing tasks. When SOI technologies are considered, the contact height will be reduced by a factor of 3, reducing resistance further. Using advanced

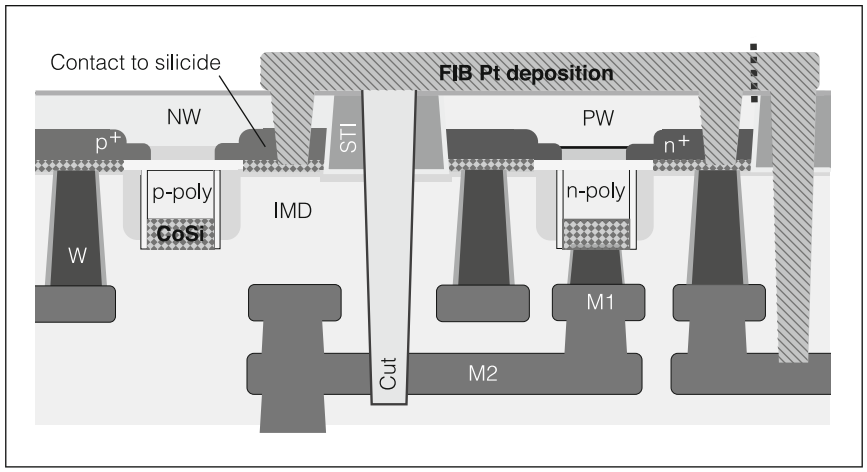

Figure 3. Variety of FIB contacts using ultrathin silicon (UTS).

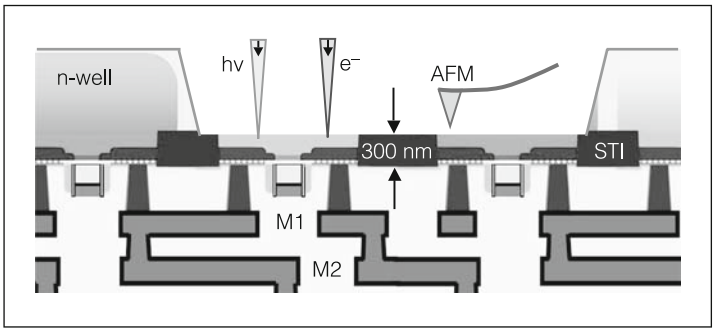

Figure 4. Probing techniques using ultrathin silicon (UTS) to improve spatial resolution.

Table 3. Comparison of resolution potential of functional-analysis techniques though moderate silicon and UTS.

Techniques	Resolution	Potential	Status
IR optical through bulk Si	400 nm	200 nm (SIL)	Standard technique
IR optical through UTS	200 nm	100 nm (SIL)	Future concept
UV through UTS	100 nm	< 50 nm (SIL)	Future concept
Electron-beam on UTS	100 nm	10 to 20 nm	Demonstrated
Nanoprobing on UTS	50 nm	10 nm	Demonstrated

conductor deposition materials such as molybdenum might offer further improvement potential.

Taking into account state-of-the-art FIB resolution performance, this backside CE technique is fully suitable for technology scaling well into the nanometer regime.

An invasiveness study of backside CE processing using intentionally enlarged trench sizes down to the STI level resulted in almost unchanged single device and circuitry performance during regular processing.[18] This study also showed that a wide FIB trench to the n-well level can be performed with remarkable coplanarity to the chip levels. A planarity mismatch of less than 200 nm on 250-micron trench expansion or 0.08% deviation is state of the art. With such a process, a new base plane can be created for the application of analysis techniques through the backside of ultrathin silicon (UTS).

Functional IC analysis through UTS backside

The FIB preparation routines developed for CE through the chip's backside produce a back surface of an ultrathin active-device volume, maintaining full IC functionality. The back surface of the remaining ultrathin active volume can now be regarded as a completely new worktop for physical techniques to access fully functional circuits. This innovative concept opens a short path to device interaction for analysis techniques with improved resolution potential (see Figure 4), which Table 3 summarizes.

Nanoprobing can now be performed on a fully functional circuit, avoiding the risks of parallel polishing from the IC front side. Furthermore, we can reconsider particle-beam techniques, such as EBP, with the resolution potential of an electron microscope for IC analysis at a higher technical level. Optical techniques can be shifted to far smaller wavelengths with the respective resolution improvement, because no bulk silicon has to be passed anymore.

In the case of substantial power consumption in the IC's area of interest, solutions for proper heat dissipation paths still need to be developed.

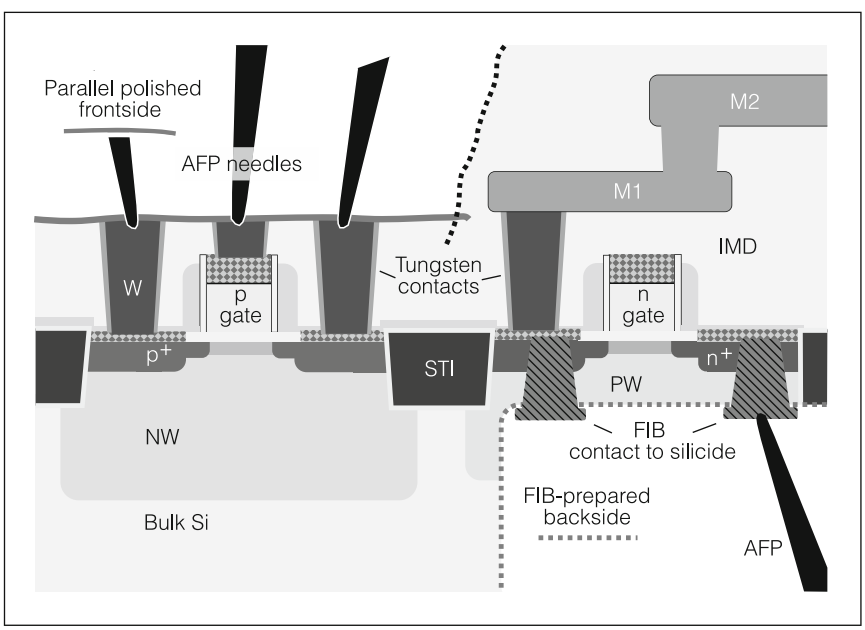

Figure 5. Principle of nanoscale atomic force probing (AFP) on a parallel polished sample (left) and on a backside FIB-prepared sample (right).

Nanoprobing on UTS

Nanoprobing on UTS can be achieved using FIB-created contacts, because of their low resistance and small geometries. Figure 5 shows a comparison between front-side and

backside nanoprobing. The main advantage of the new backside approach is that the interconnect layers no longer must be removed. For characterization of single devices, some cuts might be necessary to separate the transistors from their environment,[20] but full-circuit functionality can be reestablished easily by using simple conductor deposition.

EBP on UTS

The interaction opportunities through UTS expand to particle beams as well. Then, high-resolution probing or stimulation with electron beams returns to the IC debug toolkit. Schlangen et al. demonstrate that switching information on lower metal lines is transferred to the back surface—capacitive-coupled voltage contrast (CCVC).[21] Additionally, the full active-device area can be used to pick up node waveforms (see Figure 6) based on the modulation of the floating body potential. In this way, the pulsed electron beam's spot size can be as big as the full transistor body, which is always larger than the smallest metal lines by a factor of 3 to 5, and the resolution requirements become more relaxed. Furthermore, this method offers all the advantages that front-side EBP did: fast signal acquisition, linear V_{DD} signal scaling, and superior SNR.[22]

Figure 7 shows first results measured with a 10-year-old EBP, clearly resolving 90-nm technology.[23] Considering the latest improvements in scanning electron microscopy (SEM), especially for applications enforcing a low acceleration voltage, this technique should be suitable for scaling further into the nanometer regime.

Optical techniques on UTS

On UTS, visible and even UV light may be used to stimulate the devices, instantly improving resolution even without SIL. In addition, short wavelength SIL solutions are within reach. Stimulating a sufficient photocurrent in small active volumes as in SOI devices requires light of short absorption ranges. Only UTS provides the condition for such a stimulation.

Another problem is that the stimulation character in multimaterial active volumes will be increasingly more related to strain technologies. Stimulation, as

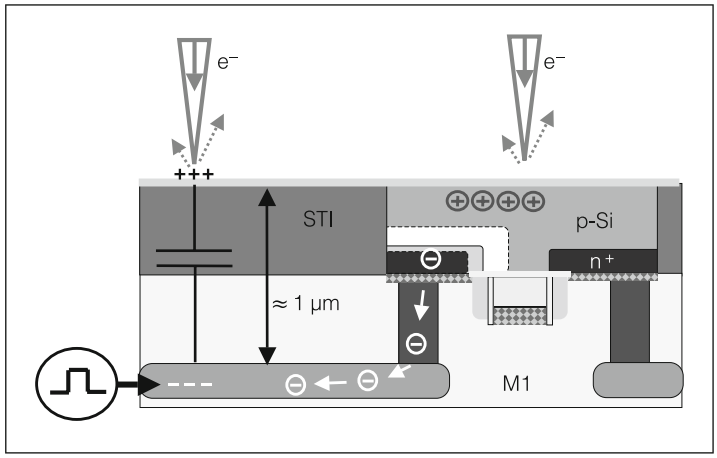

Figure 6. Backside EBP targeting M1 or directly measuring on the field-effect transistor (FET) floating body. (STI: shallow trench isolation.)

performed today with photon energies near the Si band gap, has hardly predictable absorption properties for Ge compounds used for straining and mobility enhancement. Using shorter wavelengths on UTS, we can clearly define absorption properties independent of the semiconductor material. If the laser beam can be blocked when scanning across active areas and only hits the device when over STI, it might be possible

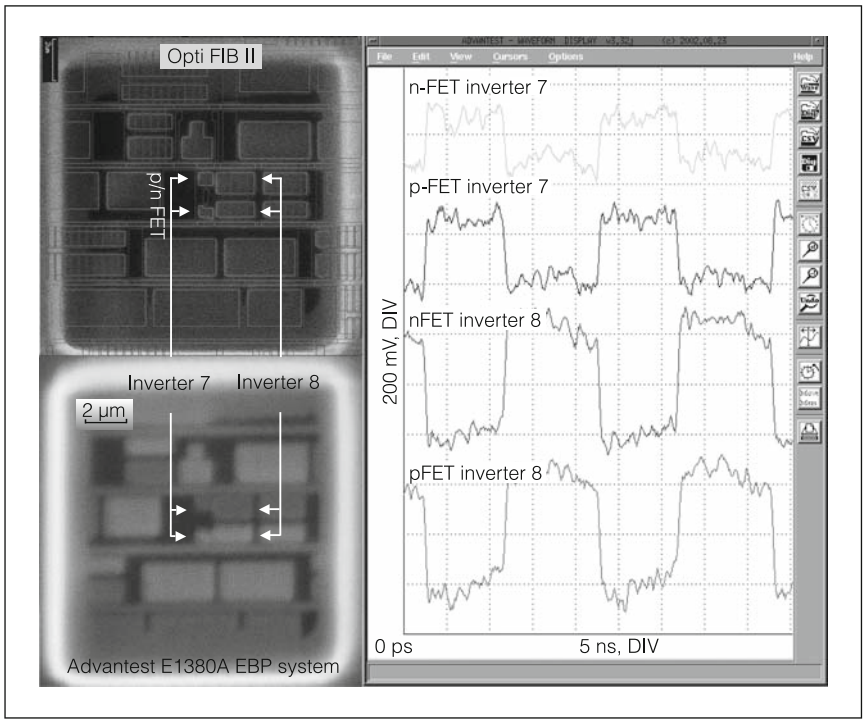

Figure 7. EBP results measured directly on the FET floating body of a 90-nm bulk CMOS after FIB backside prep down to the STI level. (DIV: division.)

to suppress photocurrent generation, so thermal stimulation could then be accomplished with high resolution.

To gain resolution beyond all optical limits, backside EBP and the stimulation of electron-hole-pair generation by electron beam seem to be the most promising techniques.

Well-established IR analysis techniques for IC debug are still powerful and offer various opportunities to localize circuit problems. The potential of these techniques can be put into practice via wisely expanded applications. The only drastic disadvantage is the increasing optical resolution mismatch in nanoscale technologies. CE has established access through the chip's backside with FIB preparation technique processing toward the STI level.

The back surface of the UTS produced for backside CE is full of opportunities for debug of nanoscale devices with the additional advantage that the circuit remains fully functional. UTS analysis potential matches the requirements for several technology generations to come. ■

Acknowledgments

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