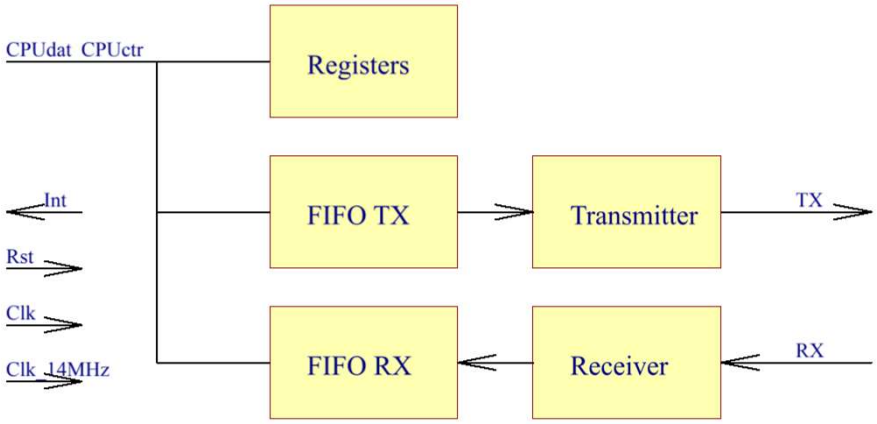
UART (Universal Asynchronous Receiver/Transmitter)

Features

- 8 bit data bus, FIFO buffer for RX and TX line
- 5, 6, 7 or 8 bits per character
- Odd, Even or no parity detection and generation
- 1 stop bit detection and generation
- Baud rate generator from separateclock input
- Transmit, receive, line status interrupts
- All FIFO TX,RX control line thru redgisters



UART Registers		
Address		**Register Name**
0x00	FIFOtx	Write data to trnasmit FIFO
0x00	FIFOrx	Read data from receive FIFO
0x01	CR	CONTROL REGISTER
0x02	FCR	FIFO STATUS/CONTROL REGISTER
0x03	TxCntL	Number of byte in transmit FIFO lower byte
0x04	TxCntH	Number of byte in transmit FIFO high byte
0x05	RxCntL	Number of byte in receive FIFO lower byte
0x06	RxCntH	Number of byte in receive FIFO high byte
0x07	ISR	INTERRUPT STATUS REGISTER
0x08	ESR	Error STATUS REGISTER
0x09	DLL	Clock divisor lath register lower byte
0x0A	DLH	Clock divisor lath register high byte

FIFO TX/RX REGISTER		
bit	**name**	**description**
7-0	**FIFOtx**	Write data to trnasmit FIFO
	FIFOrx	Read data from receive FIFO

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CONTROL REGISTER		
bit	**name**	**description**
2 - 0	**PrTp**	**Parity Type**
		0d: No parity
		1d: Odd parity
		2d: Even parity
		3d: Mark
		4d: Space
3	**RxInt**	**Rx Data Available Interrupt**
		0b: Disable the Receive Data Ready Interrupt
		1b: Enable the Receive Data Ready Interrupt
4	**TxInt**	**Tx Empty Interrupt**
		0b: Disable the Transmit Holding Register Empty Interrupt
		1b: Enable the Receive Line Status Interrupt
5	**RxLineInt**	**Rx Error Status Interrupt**
		0b: Disable the Receive Line Status Interrupt
		1b: Enable the Receive Line Status Interrupt
6	**InLoop**	Internal Loop TX to RX
		1b: TX line internaly connected to RX line
		0b: Disable Internal Loop TX to RX
7	**r**	**recerved**

FIFO STATUS/CONTROL REGISTER		
bit	**name**	**description**
0	**TxFull**	**TX FIFO Full Flag**
		0b: not Full
		1b: Full
1	**TxEmpty**	**TX FIFO Empty Flag**
		0b: not Empty
		1b: Empty
2	**RxFull**	**RX FIFO Full Flag**
		0b: not Full
		1b: Full
3	**RxEmpty**	**RX FIFO Empty Flag**
		0b: not Empty
		1b: Empty
4	**TxClear**	**TX FIFO Clear**
		Writing a 1B into this bit clears the data in transmit FIFO
		bit. A read always returns 0.
5	**RxClear**	**RX FIFO Clear**
		Writing a 1B into this bit clears the data in receive FIFO
		bit. A read always returns 0.
6	**TxComp**	**Tx Complete**
		0b: Tx Shift Register is not empty.
		1b: Tx Shift Register is empty.
7	**r**	**recerved**

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FIFO TX COUNTER REGISTER		
bit	name	description
7 - 0	TxCntL	Number of byte in transmit FIFO lower byte

FIFO TX COUNTER REGISTER		
bit	name	description
7 - 0	TxCntH	Number of byte in transmit FIFO high byte

FIFO RX COUNTER REGISTER		
bit	name	description
7 - 0	RxCntL	Number of byte in receive FIFO lower byte

FIFO RX COUNTER REGISTER		
bit	name	description
7 - 0	RxCntH	Number of byte in receive FIFO high byte

INTERRUPT STATUS REGISTER, reading this register clear Int line and all status Interrupt bit		
bit	name	description
0	RxInt	Rx data availble
1	TxInt	Tx FIFO empty
2	ErrInt	Rx Error Status

Error STATUS REGISTER, reading this register clear all error status bit		
bit	name	description
0	Ovrn	Rx FIFO Overrun
1	Prt	Rx Parity Error
2	Frm	Rx Frame Error
3	Brk	Rx Break Error

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DIVISOR LATCH REGISTER value to corresponding Bbaudrate	
Bbaudrate	**DIVISOR LATCH REGISTER**
9600	768
14400	512
19200	384
28800	256
38400	192
57600	128
76800	96
115200	64
230400	32
460800	16
921600	8
1843200	4

DIVISOR LATCH REGISTER		
bit	**name**	**description**
7 - 0	**DLL**	**Clock divisor lath register lower byte**

DIVISOR LATCH REGISTER		
bit	**name**	**description**
7 - 0	**DLH**	**Clock divisor lath register high byte**