Timer

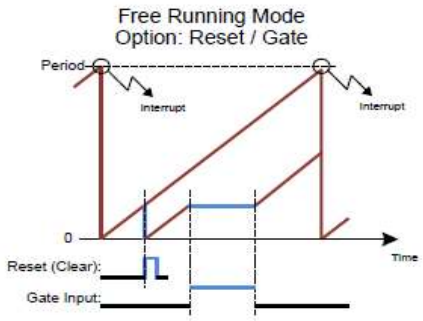
Functionality based on CCU4 unite of Infenion XMC1000 32-bit microcontroller series

For aplication:

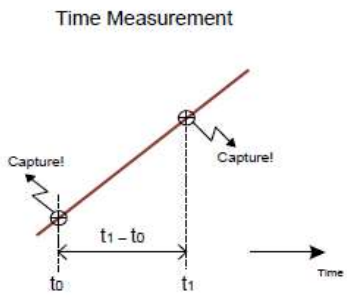
- Simple timer
- Input signal monitoring/conditioning
- Pulse Width Modulation (PWM)

Basic functions:

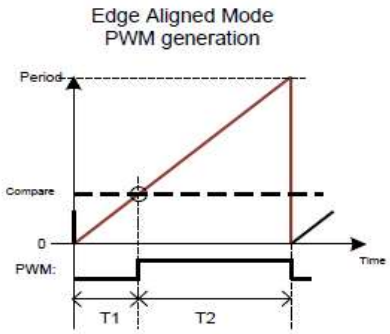
Timer



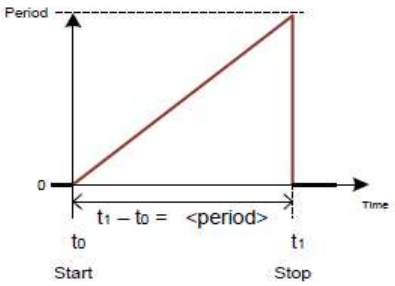
Capture



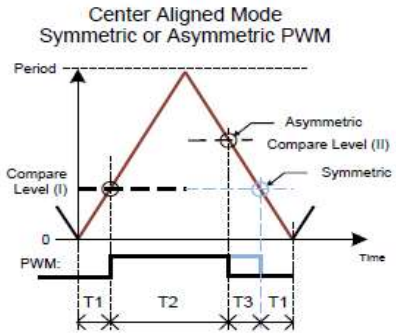
Compare



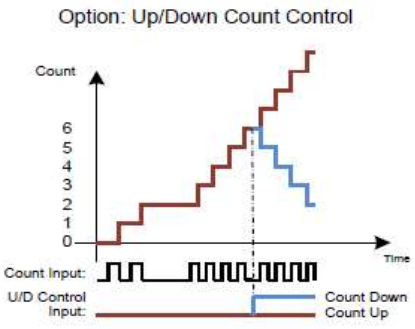
Single Shot

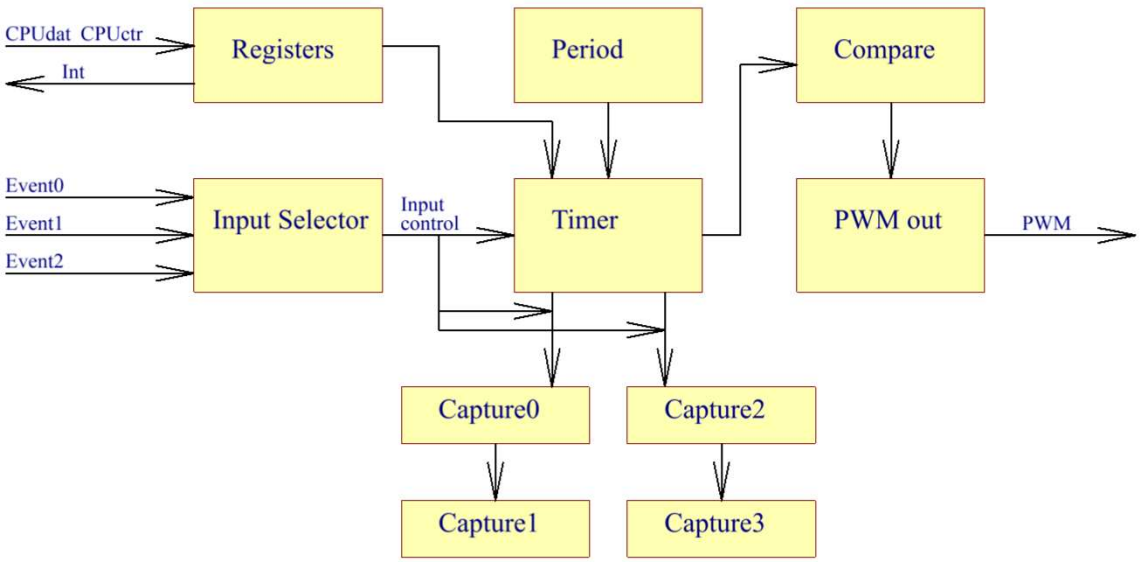


Compare



Counter





Timer Registers		
Address		**Register Name**
0x00	**TRS**	**Timer Run/Clear Setting**
		This register control start, stop, clear of Timer
0x04	**TCFS**	**Timer Capture Flags Status**
		This register containt flags of load state Capture Register 0 - 3
0x08	**TRSt**	**Timer Run Status**
		This register containt current run status, count derection
0x0C	**TMS**	**Timer Mode Setting**
		This register control direction, Timer mode, external control event
0x10	**ECR**	**Event control register**
		This register set selection Edge/Level and setting low pass filter of input Event 0 - 2
0x14	**CMC**	**Event 0 - 2 Connection Matrix Control**
		This register set selection Event 0 - 2 to Start, Stop, Capture… functionality
0x18	**ISR**	**Interrupt Status register**
		This register contains the status of all interrupt sources
0x1C	**IEC**	**Interrupt Enable Control**
		Through this register it is possible to enable or disable the specific interrupt source(s).
0x20	**ISC**	**Interrupt Status Clear**
		Through this register it is possible for the SW to clear a specific interrupt status flag.
0x24	**PLC**	**Passive Level Config**
		This register holds the configuration for the output passive level control.
0x28	**TmVal**	**Timer Value**
		This register contains the current value of the timer
0x2C	**TmPr**	**Timer Period Value**
		This register contains the actual value for the timer period.
0x30	**TmPrSh**	**Timer Shadow Period Value**
		This register contains the value for the timer period that is going to be transferred into the TmPr field when the next shadow transfer occurs.
0x34	**TmCap0**	This register contains the values captured of Timer Value by event Cap0
0x38	**TmCap1**	This register get the values from TmCap0 event Cap0
0x3C	**TmCap2**	This register contains the values captured of Timer Value by event Cap1
0x40	**TmCap3**	This register get the values from TmCap2 by event Cap1
0x44	**TmC1mC0**	This register contains number of tiks between last two Cap0 event
0x48	**TmC3mC2**	This register contains number of tiks between last two Cap1 event
0x4C	**TmCmp**	**Timer Compare Value**
		This register contains the value for the timer comparison.
		Output PWM signal setting by timer Compare Value. bwPWM parametre set number of PWM outputs. All PWM have same frequence from timer period, compare value determine duty cycle.
0x50	**TmCmpSh**	**Timer Shadow Compare Value**
		This register contains the value that is going to be loaded into the TmCmp field when the next shadow transfer occurs.
0x4C + 2*n	**TmCmp(n)**	**Timer Compare Value for "n" PWM output**
0x50 + 2*n	**TmCmpSh(n)**	**Timer Shadow Compare Value for "n" PWM output**

Timer Run/Clear Setting		
bit	**name**	**description**
0	RS	**Timer Run Bit set** Writing a 1B into this field sets the run bit of the timer. Read always returns 0.
1	RC	**Timer Run Bit Clear** Writing a 1B into this field clears the run bit of thetimer. The timer is not cleared. Read always returns 0.
2	TC	**Timer Clear** Writing a 1B into this field clears the timer to 0000H.Read always returns 0.

Timer Run Status		
bit	**name**	**description**
0	TR	**Timer Run Bit set** This field indicates if the timer is running. 0B Timer is stopped 1B Timer is running
1	TCD	**Timer Counting Direction** This filed indicates if the timer is being increment ordecremented 0B Timer is counting up 1B Timer is counting down

Timer Capture Flags Status		
bit	**name**	**description**
0	C0Full	1B Capture 0 register have data, cleared after read Capture 0 reg
1	C1Full	1B Capture 1 register have data, cleared after read Capture 1 reg
2	C2Full	1B Capture 2 register have data, cleared after read Capture 2 reg
3	C3Full	1B Capture 3 register have data, cleared after read Capture 3 reg

Timer Mode Setting		
bit	**name**	**description**
0	**TCM**	**Timer Counting Mode** 0B Edge aligned mode 1B Center aligned mode Note: When using an external signal to control the counting direction, the counting scheme is
1	**SShM**	**Single shot mode** This field controls the single shot mode. This is applicable in edge and center aligned modes. 0B Single shot mode is disabled 1B Single shot mode is enabled
2	**CCM**	**Capture Compare Mode** This field indicates in which mode the slice is operating. The default value is compare mode. The capture mode is automatically set by the HW when an external signal is apped to a capture trigger. 0B Compare Mode 1B Capture Mode

3	**STC**	**Shadow Transfer on Clear** Setting this bit to 1B enables a shadow transfer when a timer clearing action is performed.
5:4	**CCC**	**Clear on Capture Control** 00B Timer is never cleared on a capture event 01B Timer is cleared on a capture event into capture registers 0 and 2. (When SCE = 1B, Timer is always cleared in a capture event) 10B Timer is cleared on a capture event into capture registers 1 and 3. (When SCE = 1B, Timer is always cleared in a capture event) 11B Timer is always cleared in a capture event.
7:6	**StpFC**	**Extended Stop Function Control** This field controls the extended functions of the external Stop signal. 00B Clears the timer run bit only (default stop) 01B Clears the timer only (flush) 10B Clears the timer and run bit (flush/stop) 11B Reserved Note: When using an external up/down signal the flush operation sets the timer with zero if the counter is counting up and with the Period value if the counter is being decremented.
8	**StrFC**	**Extended Start Function Control** This field controls the extended functions of theexternal Start signal. 0B Sets run bit only (default start) 1B Clears the timer and sets run bit (flush/start) Note: When using an external up/down signal the if the counter is being incremented and with the Period value if the counter is being
9	**CCE**	**Continuous Capture Enable** 0B The capture into a specific capture register is done with the rules linked with the full flags 1B The capture into the capture registers is always done regardless of the full flag status (even if the register has not been read back).
10	**EMS**	**External Modulation Synchronization** Setting this bit to 1B enables the synchronization of the external modulation functionality with the PWM period. 0B External Modulation functionality is not synchronized with the PWM signal 1B External Modulation functionality is synchronized with the PWM signal

Event control register		
bit	**name**	**description**
1:0	**E0ES**	**Event 0 Edge Selection** 00B No action 01B Signal active on rising edge 10B Signal active on falling edge 11B Signal active on both edges
3:2	**E1ES**	**Event 1 Edge Selection**
5:4	**E2ES**	**Event 2 Edge Selection**

6	**E0LS**	**Event 0 Level Selection** 0B Active on HIGH level 1B Active on LOW level
7	**E2LS**	**Event 2 Level Selection**
8	**E3LS**	**Event 3 Level Selection**
10:9	**E0FC**	**Event 0 Low Pass Filter Configuration** This field sets the number of consecutive counts for needs to remain stable for this number of counts Clk, so that a level/transition is accepted. 00B LPF is disabled 01B 3 clock cycles 10B 5 clock cycles 11B 7 clock cycles
12:11	**E1FC**	**Event 1 Low Pass Filter Configuration**
14:13	**E2FC**	**Event 2 Low Pass Filter Configuration**

Event 0 - 2 Connection Matrix Control		
bit	**name**	**description**
1:0	**StrtS**	**External Start Functionality Selector** Selects the Event that is going to be linked with theexternal start functionality. 00B External Start Function deactivated 01B External Start Function triggered by Event 0 10B External Start Function triggered by Event 1 11B External Start Function triggered by Event 2
3:2	**StpS**	**External Stop Functionality Selector** Selects the Event that is going to be linked with theexternal start functionality. 00B External Start Function deactivated 01B External Start Function triggered by Event 0 10B External Start Function triggered by Event 1 11B External Start Function triggered by Event 2
5:4	**CapS0**	**External Capture 0 Functionality Selector** Selects the Event that is going to be linked with theexternal capture for capture regis 00B External Capture 0 Function deactivated 01B External Capture 0 Function triggered byEvent 0 10B External Capture 0 Function triggered byEvent 1 11B External Capture 0 Function triggered byEvent 2
7:6	**CapS1**	**External Capture 0 Functionality Selector** Selects the Event that is going to be linked with the external capture for capture registers number 1 and 0 (CAP0S) number 3 and 2 (CAP1S) 00B External Capture 0 Function deactivated 01B External Capture 0 Function triggered byEvent 0 10B External Capture 0 Function triggered byEvent 1 11B External Capture 0 Function triggered byEvent 2
9:8	**GatS**	**External Gate Functionality Selector** Selects the Event that is going to be linked with the counter gating function. This function is used to gate the timer increment/decrement procedure. 00B External Gating Function deactivated

		01B External Gating Function triggered by Event 0 10B External Gating Function triggered by Event 1 11B External Gating Function triggered by Event 2
11:10	**UpDwS**	**External Up/Down Functionality Selector** Selects the Event that is going to be linked with the Up/Down counting direction control. 00B External Up/Down Function deactivated 01B External Up/Down Function triggered by Event 0 10B External Up/Down Function triggered by Event 1 11B External Up/Down Function triggered by Event 2
13:12	**LdS**	**External Timer Load Functionality Selector** Selects the Event that is going to be linked with thetimer load function. 00B - External Load Function deactivated 01B - External Load Function triggered by Event 0 10B - External Load Function triggered by Event 1 11B - External Load Function triggered by Event 2
15:14	**CntS**	**External Count Selector** Selects the Event that is going to be linked with the count function. The counter is going to be increment/decremented each time that a specific transition on the event is detected. 00B External Count Function deactivated 01B External Count Function triggered by Event 0 10B External Count Function triggered by Event 1 11B External Count Function triggered by Event 2
17:16	**MdlS**	**External Modulation Functionality Selector** Selects the Event that is going to be linked with theexternal modulation function 00B - Modulation Function deactivated 01B - Modulation Function triggered by Event 0 10B - Modulation Function triggered by Event 1 11B - Modulation Function triggered by Event 2

Interrupt Status register		
bit	**name**	**description This register contains the status of all interrupt sources**
0	**PMup**	**Period Match while Counting Up** 0B Period match while counting up not detected 1B Period match while counting up detected
1	**OMdw**	**One Match while Counting Down** 0B One match while counting down not detected 1B One match while counting down detected
2	**CMup**	**Compare Match while Counting Up** 0B Compare match while counting up notdetected 1B Compare match while counting up detected
3	**CMdw**	**Compare Match while Counting Down** 0B Compare match while counting down notdetected 1B Compare match while counting down detected
4	**Ev0DS**	**Event 0 Detection Status** Depending on the user selection on the , this bit can be set when a rising, falling or both transitions are detected.

		0B Event 0 not detected 1B Event 0 detected
5	**Ev1DS**	**Event 1 Detection Status** 0B Event 1 not detected 1B Event 1 detected
6	**Ev2DS**	**Event 2 Detection Status** 0B Event 2 not detected 1B Event 2 detected

Interrupt Enable Control		
bit	**name**	**Through this register it is to enable or disable the specific interrupt source(s).**
0	**PMupEn**	**Period match while counting up enable** Setting this bit to 1B enables the generation of an interrupt pulse every time a period match while counting up occurs. 0B Period Match interrupt is disabled 1B Period Match interrupt is enabled
1	**OMdwEn**	**One match while counting down enable** Setting this bit to 1B enables the generation of an interrupt pulse every time an one match while counting down occurs. 0B One Match interrupt is disabled 1B One Match interrupt is enabled
2	**CMupEn**	**Compare match while counting up enable** Setting this bit to 1B enables the generation of an interrupt pulse every time a compare match while counting up occurs. 0B Compare Match while counting up interrupt isdisabled 1B Compare Match while counting up interrupt isenabled
3	**CMdwEn**	**Compare match while counting down enable** Setting this bit to 1B enables the generation of an interrupt pulse every time a compare match while counting down occurs. 0B Compare Match while counting down interruptis disabled 1B Compare Match while counting down interruptis enabled
4	**Ev0DSEn**	**Event 0 interrupt enable** Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 0 is detected. 0B Event 0 detection interrupt is disabled 1B Event 0 detection interrupt is enabled
5	**Ev1DSEn**	**Event 1 interrupt enable** Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 1 is detected. 0B Event 1 detection interrupt is disabled 1B Event 1 detection interrupt is enabled
6	**Ev2DSEn**	**Event 2 interrupt enable** Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 2 is detected. 0B Event 2 detection interrupt is disabled 1B Event 2 detection interrupt is enabled

Interrupt Status Clear		
bit	**name**	**Through this register it is for the SW to clear a specific interrupt status flag.**
0	**PMup**	**Period match while counting up clear** Writing a 1B into this field clears the ISR.PMup
1	**OMdw**	**One match while counting down clear** Writing a 1B into this bit clears the ISR.Omdw bit. A read always returns 0.
2	**CMup**	**Compare match while counting up clear** Writing a 1B into this field clears the ISR.CMup bit. A read always returns 0.
3	**CMdw**	**Compare match while counting down clear** Writing a 1B into this bit clears the ISR.CMdw bit. A read always returns 0.
4	**Ev0DS**	**Event 0 detection clear** Writing a 1B into this bit clears the ISR.Ev0DS bit. A read always returns 0.
5	**Ev1DS**	**Event 1 detection clear** Writing a 1B into this bit clears the ISR.Ev1DS bit. A read always returns 0.
6	**Ev2DS**	**Event 2 detection clear** Writing a 1B into this bit clears the ISR.Ev2DS bit. A read always returns 0.

Passive Level Config		
bit	**name**	**This register holds the configuration for the output passive level control.**
bwPWM - 1 : 0	**OPL**	**Output Passive Level of PWM outputs** This field controls the passive level of the output pin. 0B Passive Level is LOW 1B Passive Level is HIGH A write always addresses the shadow register, while a read always returns the current used value.

Timer perepherial module

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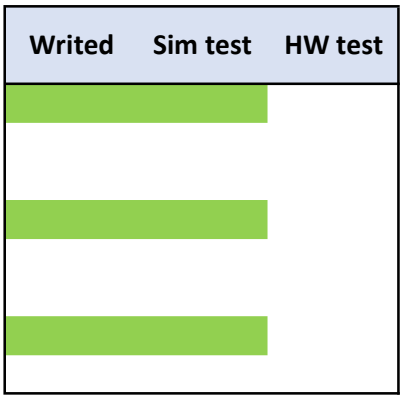

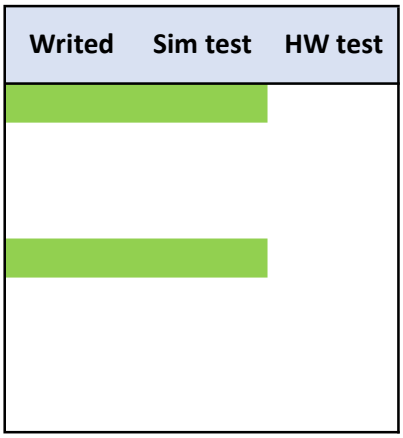

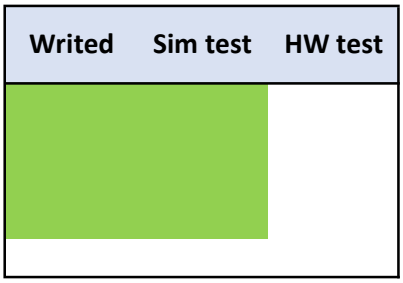

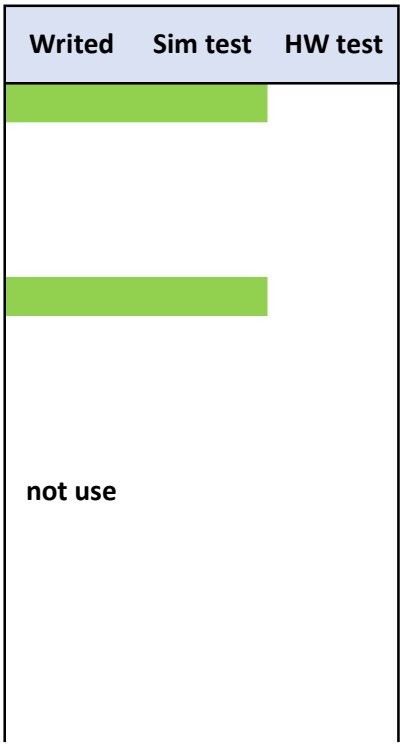

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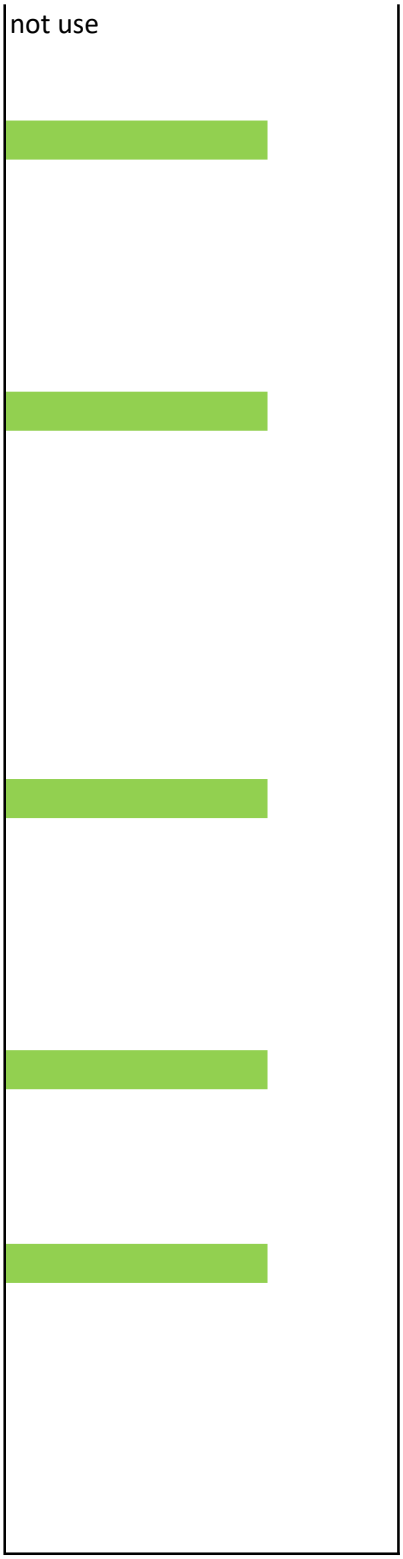

Writed	Sim test	HW test

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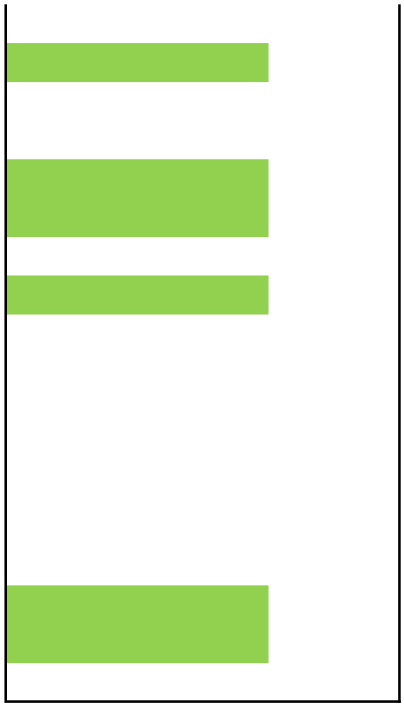

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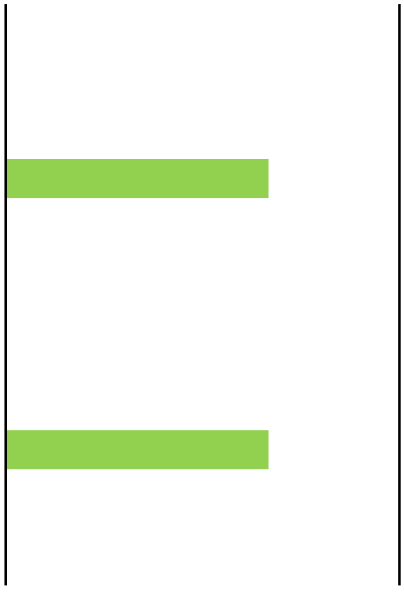
sters number 1 and0 (CAP0S) number 3 and2 (CAP1S)



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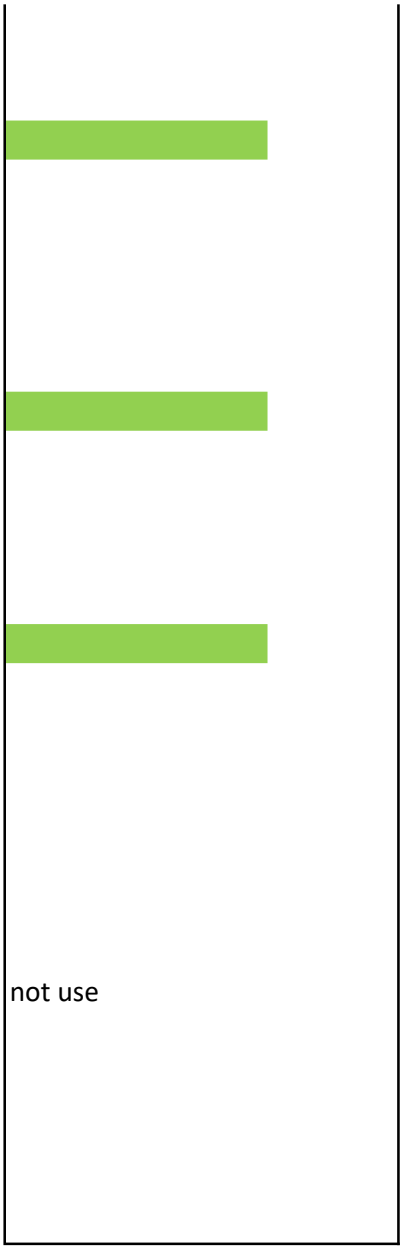

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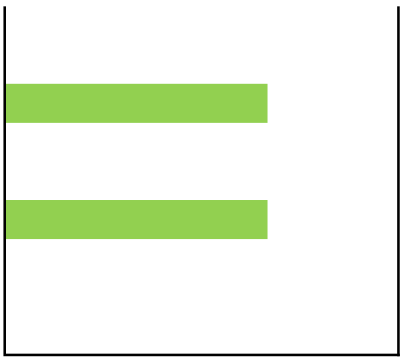

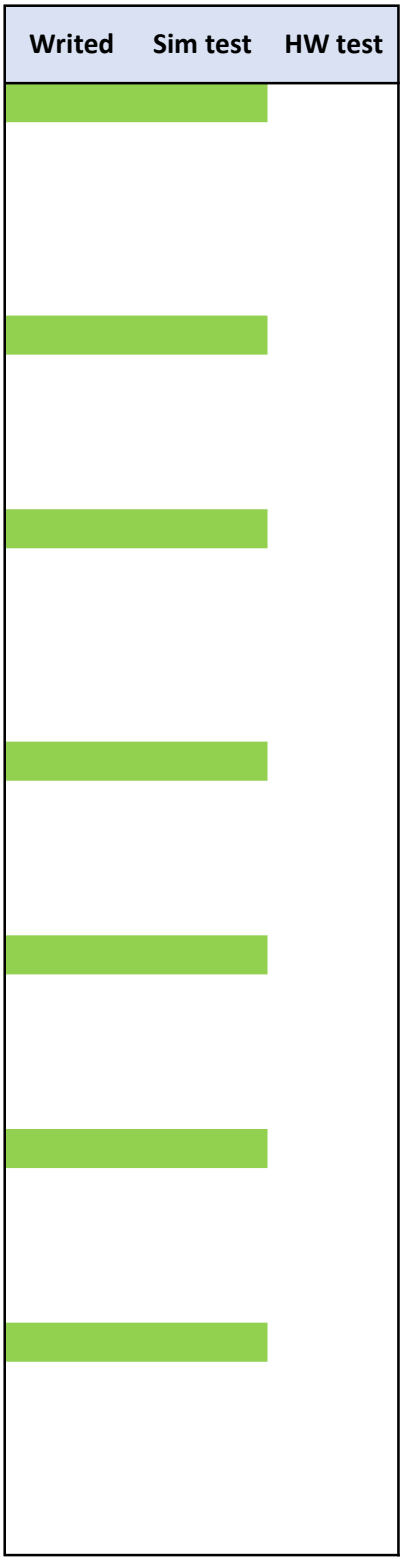

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