

Timer

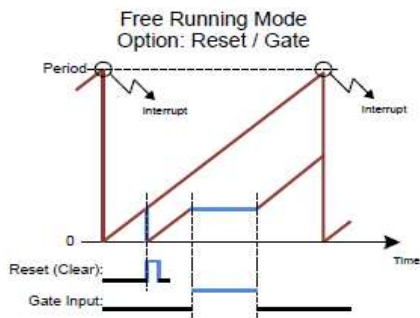
Functionality based on CCU4 unite of Inferion XMC1000 32-bit microcontroller series

For application:

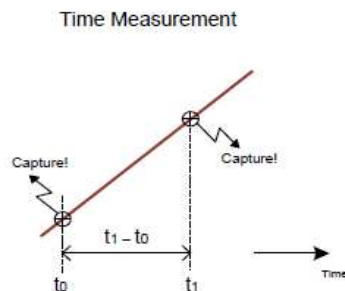
- Simple timer
- Input signal monitoring/conditioning
- Pulse Width Modulation (PWM)

Basic functions:

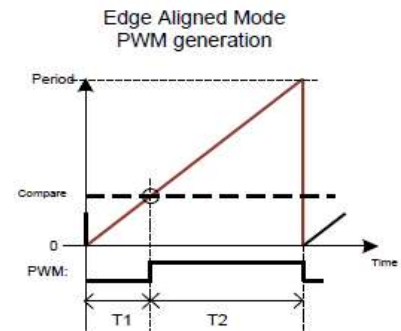
Timer



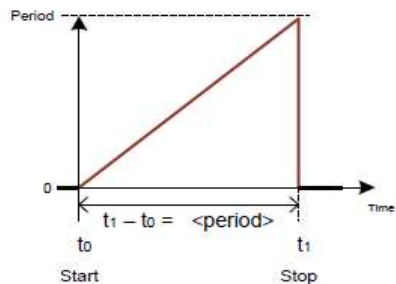
Capture



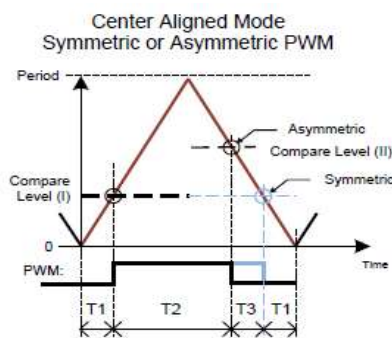
Compare



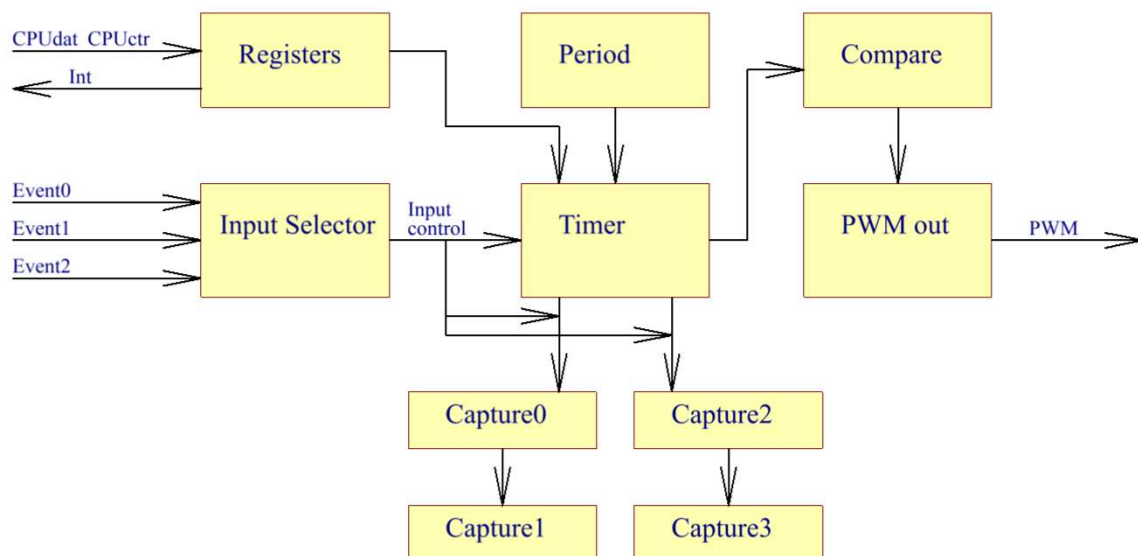
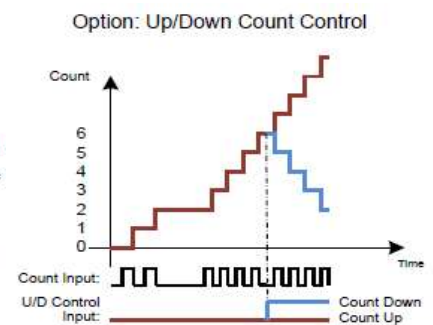
Single Shot



Compare



Counter



Timer Registers		
Address		Register Name
0x00	TRS	Timer Run/Clear Setting This register control start, stop, clear of Timer
0x04	TCFS	Timer Capture Flags Status This register contain flags of load state Capture Register 0 - 3
0x08	TRSt	Timer Run Status This register contain current run status, count direction
0x0C	TMS	Timer Mode Setting This register control direction, Timer mode, external control event
0x10	ECR	Event control register This register set selection Edge/Level and setting low pass filter of input Event 0 - 2
0x14	CMC	Event 0 - 2 Connection Matrix Control This register set selection Event 0 - 2 to Start, Stop, Capture... functionality
0x18	ISR	Interrupt Status register This register contains the status of all interrupt sources
0x1C	IEC	Interrupt Enable Control Through this register it is possible to enable or disable the specific interrupt source(s).
0x20	ISC	Interrupt Status Clear Through this register it is possible for the SW to clear a specific interrupt status flag.
0x24	PLC	Passive Level Config This register holds the configuration for the output passive level control.
0x28	TmVal	Timer Value This register contains the current value of the timer
0x2C	TmPr	Timer Period Value This register contains the actual value for the timer period.
0x30	TmPrSh	Timer Shadow Period Value This register contains the value for the timer period that is going to be transferred into the TmPr field when the next shadow transfer occurs.
0x34	TmCap0	Capture0 register In capture mode this register contains the values captured of Timer Value by event Cap0 When CMC.CntCapS0 set, this register count external event from selected source. When timer run and period is setted, value of TmCap0 writed to TmCap1 and cleared by period match
0x38	TmCap1	This register get the values from TmCap0 event Cap0
0x3C	TmCap2	Capture2 register In capture mode this register contains the values captured of Timer Value by event Cap1 When CMC.CntCapS1 set, this register count external event from selected source. When timer run and period is setted, value of TmCap2 writed to TmCap3 and cleared by period match
0x40	TmCap3	This register get the values from TmCap2 by event Cap1
0x44	TmC1mC0	This register contains number of ticks between last two Cap0 event
0x48	TmC3mC2	This register contains number of ticks between last two Cap1 event
0x4C	TmCmp	Timer Compare Value This register contains the value for the timer comparison. Output PWM signal setting by timer Compare Value. bwPWM parametre set

Timer peripheral module

		number of PWM outputs. All PWM have same frequency from timer period, compare value determine duty cycle.
0x50	TmCmpSh	Timer Shadow Compare Value This register contains the value that is going to be loaded into the TmCmp field when the next shadow transfer occurs.
0x4C + 2*n	TmCmp(n)	Timer Compare Value for "n" PWM output
0x50 + 2*n	TmCmpSh(n)	Timer Shadow Compare Value for "n" PWM output

Timer Run/Clear Setting		
bit	name	description
0	RS	Timer Run Bit set Writing a 1B into this field sets the run bit of the timer. Read always returns 0.
1	RC	Timer Run Bit Clear Writing a 1B into this field clears the run bit of the timer. The timer is not cleared. Read always returns 0.
2	TC	Timer Clear Writing a 1B into this field clears the timer to 0000H. Read always returns 0.

Timer Run Status		
bit	name	description
0	TR	Timer Run Bit set This field indicates if the timer is running. 0B Timer is stopped 1B Timer is running
1	TCD	Timer Counting Direction This field indicates if the timer is being incremented or decremented 0B Timer is counting up 1B Timer is counting down

Timer Capture Flags Status		
bit	name	description
0	C0Full	1B Capture 0 register have data, cleared after read Capture 0 reg
1	C1Full	1B Capture 1 register have data, cleared after read Capture 1 reg
2	C2Full	1B Capture 2 register have data, cleared after read Capture 2 reg
3	C3Full	1B Capture 3 register have data, cleared after read Capture 3 reg

Timer Mode Setting		
bit	name	description
0	TCM	Timer Counting Mode 0B Edge aligned mode 1B Center aligned mode Note: When using an external signal to control the counting direction, the counting scheme is
1	SshM	Single shot mode This field controls the single shot mode.

		<p>This is applicable in edge and center aligned modes.</p> <p>0B Single shot mode is disabled</p> <p>1B Single shot mode is enabled</p>
2	CCM	<p>Capture Compare Mode</p> <p>This field indicates in which mode the slice is operating.</p> <p>The default value is compare mode.</p> <p>The capture mode is automatically set by the HW when an external signal is apped to a capture trigger.</p> <p>0B Compare Mode</p> <p>1B Capture Mode</p>
3	STC	<p>Shadow Transfer on Clear</p> <p>Setting this bit to 1B enables a shadow transfer when a timer clearing action is performed.</p>
5:4	CCC	<p>Clear on Capture Control</p> <p>00B Timer is never cleared on a capture event</p> <p>01B Timer is cleared on a capture event into capture registers 0 and 2. (When SCE = 1B, Timer is always cleared in a capture event)</p> <p>10B Timer is cleared on a capture event into capture registers 1 and 3. (When SCE = 1B, Timer is always cleared in a capture event)</p> <p>11B Timer is always cleared in a capture event.</p>
7:6	StpFC	<p>Extended Stop Function Control</p> <p>This field controls the extended functions of the external Stop signal.</p> <p>00B Clears the timer run bit only (default stop)</p> <p>01B Clears the timer only (flush)</p> <p>10B Clears the timer and run bit (flush/stop)</p> <p>11B Reserved</p> <p>Note: When using an external up/down signal the flush operation sets the timer with zero if the counter is counting up and with the Period value if the counter is being decremented.</p>
8	StrFC	<p>Extended Start Function Control</p> <p>This field controls the extended functions of the external Start signal.</p> <p>0B Sets run bit only (default start)</p> <p>1B Clears the timer and sets run bit (flush/start)</p> <p>Note: When using an external up/down signal the if the counter is being incremented and with the Period value if the counter is being</p>
9	CCE	<p>Continuous Capture Enable</p> <p>0B The capture into a specific capture register is done with the rules linked with the full flags</p> <p>1B The capture into the capture registers is always done regardless of the full flag status (even if the register has not been read back).</p>
10	EMS	<p>External Modulation Synchronization</p> <p>Setting this bit to 1B enables the synchronization of the external modulation functionality with the PWM period.</p> <p>0B External Modulation functionality is not synchronized with the PWM signal</p> <p>1B External Modulation functionality is synchronized with the PWM signal</p>

Event control register		
bit	name	description
1:0	E0ES	Event 0 Edge Selection 00B No action 01B Signal active on rising edge 10B Signal active on falling edge 11B Signal active on both edges
3:2	E1ES	Event 1 Edge Selection
5:4	E2ES	Event 2 Edge Selection
6	E0LS	Event 0 Level Selection 0B Active on HIGH level 1B Active on LOW level
7	E2LS	Event 2 Level Selection
8	E3LS	Event 3 Level Selection
10:9	E0FC	Event 0 Low Pass Filter Configuration This field sets the number of consecutive counts for needs to remain stable for this number of counts Clk, so that a level/transition is accepted. 00B LPF is disabled 01B 3 clock cycles 10B 5 clock cycles 11B 7 clock cycles
12:11	E1FC	Event 1 Low Pass Filter Configuration
14:13	E2FC	Event 2 Low Pass Filter Configuration

Event 0 - 2 Connection Matrix Control		
bit	name	description
1:0	StrtS	External Start Functionality Selector Selects the Event that is going to be linked with the external start functionality. 00B External Start Function deactivated 01B External Start Function triggered by Event 0 10B External Start Function triggered by Event 1 11B External Start Function triggered by Event 2
3:2	StpS	External Stop Functionality Selector Selects the Event that is going to be linked with the external start functionality. 00B External Start Function deactivated 01B External Start Function triggered by Event 0 10B External Start Function triggered by Event 1 11B External Start Function triggered by Event 2
5:4	CapS0	External Capture 0 Functionality Selector Selects the Event that is going to be linked with the external capture for capture register 0. 00B External Capture 0 Function deactivated 01B External Capture 0 Function triggered by Event 0 10B External Capture 0 Function triggered by Event 1 11B External Capture 0 Function triggered by Event 2
7:6	CapS1	External Capture 1 Functionality Selector

		<p>Selects the Event that is going to be linked with the external capture for capture registers number 1 and 0 (CAP0S) number 3 and 2 (CAP1S)</p> <p>00B External Capture 0 Function deactivated</p> <p>01B External Capture 0 Function triggered byEvent 0</p> <p>10B External Capture 0 Function triggered byEvent 1</p> <p>11B External Capture 0 Function triggered byEvent 2</p>
9:8	GatS	<p>External Gate Functionality Selector</p> <p>Selects the Event that is going to be linked with the counter gating function. This function is used to gate the timer increment/decrement procedure.</p> <p>00B External Gating Function deactivated</p> <p>01B External Gating Function triggered by Event 0</p> <p>10B External Gating Function triggered by Event 1</p> <p>11B External Gating Function triggered by Event 2</p>
11:10	UpDwS	<p>External Up/Down Functionality Selector</p> <p>Selects the Event that is going to be linked with the Up/Down counting direction control.</p> <p>00B External Up/Down Function deactivated</p> <p>01B External Up/Down Function triggered by Event 0</p> <p>10B External Up/Down Function triggered by Event 1</p> <p>11B External Up/Down Function triggered by Event 2</p>
13:12	LdS	<p>External Timer Load Functionality Selector</p> <p>Selects the Event that is going to be linked with the timer load function.</p> <p>00B - External Load Function deactivated</p> <p>01B - External Load Function triggered by Event 0</p> <p>10B - External Load Function triggered by Event 1</p> <p>11B - External Load Function triggered by Event 2</p>
15:14	CntS	<p>External Count Selector</p> <p>Selects the Event that is going to be linked with the count function. The counter is going to be increment/decremented each time that a specific transition on the event is detected.</p> <p>00B External Count Function deactivated</p> <p>01B External Count Function triggered by Event 0</p> <p>10B External Count Function triggered by Event 1</p> <p>11B External Count Function triggered by Event 2</p>
17:16	MdIS	<p>External Modulation Functionality Selector</p> <p>Selects the Event that is going to be linked with the external modulation function</p> <p>00B - Modulation Function deactivated</p> <p>01B - Modulation Function triggered by Event 0</p> <p>10B - Modulation Function triggered by Event 1</p> <p>11B - Modulation Function triggered by Event 2</p>
19:18	CntCapS0	<p>External Count to Capture0 reg Selector</p> <p>Selects the Event that is going to be linked with the count function. The Capture0 reg is going to be increment each time that a specific transition on the event is detected.</p> <p>00B External CntCapS0 Function deactivated</p> <p>01B External CntCapS0 Function triggered by Event 0</p> <p>10B External CntCapS0 Function triggered by Event 1</p> <p>11B External CntCapS0 Function triggered by Event 2</p>

21:20	CntCapS1	External Count to Capture2 reg Selector Selects the Event that is going to be linked with the count function. The Capture2 reg is going to be increment each time that a specific transition on the event is detected. 00B External CntCapS1 Function deactivated 01B External CntCapS1 Function triggered by Event 0 10B External CntCapS1 Function triggered by Event 1 11B External CntCapS1 Function triggered by Event 2
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Interrupt Status register			
bit	name	description	This register contains the status of all interrupt sources
0	PMup	Period Match while Counting Up 0B Period match while counting up not detected 1B Period match while counting up detected	
1	OMdw	One Match while Counting Down 0B One match while counting down not detected 1B One match while counting down detected	
2	CMup	Compare Match while Counting Up 0B Compare match while counting up notdetected 1B Compare match while counting up detected	
3	CMdw	Compare Match while Counting Down 0B Compare match while counting down notdetected 1B Compare match while counting down detected	
4	Ev0DS	Event 0 Detection Status Depending on the user selection on the , this bit can be set when a rising, falling or both transitions are detected. 0B Event 0 not detected 1B Event 0 detected	
5	Ev1DS	Event 1 Detection Status 0B Event 1 not detected 1B Event 1 detected	
6	Ev2DS	Event 2 Detection Status 0B Event 2 not detected 1B Event 2 detected	

Interrupt Enable Control		
bit	name	Through this register it is to enable or disable the specific interrupt source(s).
0	PMupEn	Period match while counting up enable Setting this bit to 1B enables the generation of an interrupt pulse every time a period match while counting up occurs. 0B Period Match interrupt is disabled 1B Period Match interrupt is enabled
1	OMdwEn	One match while counting down enable Setting this bit to 1B enables the generation of an interrupt pulse every time an one match while counting down occurs. 0B One Match interrupt is disabled 1B One Match interrupt is enabled

2	CMupEn	Compare match while counting up enable Setting this bit to 1B enables the generation of an interrupt pulse every time a compare match while counting up occurs. 0B Compare Match while counting up interrupt is disabled 1B Compare Match while counting up interrupt is enabled
3	CMdwEn	Compare match while counting down enable Setting this bit to 1B enables the generation of an interrupt pulse every time a compare match while counting down occurs. 0B Compare Match while counting down interrupt is disabled 1B Compare Match while counting down interrupt is enabled
4	Ev0DSEn	Event 0 interrupt enable Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 0 is detected. 0B Event 0 detection interrupt is disabled 1B Event 0 detection interrupt is enabled
5	Ev1DSEn	Event 1 interrupt enable Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 1 is detected. 0B Event 1 detection interrupt is disabled 1B Event 1 detection interrupt is enabled
6	Ev2DSEn	Event 2 interrupt enable Setting this bit to 1B enables the generation of an interrupt pulse every time that Event 2 is detected. 0B Event 2 detection interrupt is disabled 1B Event 2 detection interrupt is enabled

Interrupt Status Clear		
bit	name	Through this register it is for the SW to clear a specific interrupt status flag.
0	PMup	Period match while counting up clear Writing a 1B into this field clears the ISR.PMup
1	OMdw	One match while counting down clear Writing a 1B into this bit clears the ISR.Omdw bit. A read always returns 0.
2	CMup	Compare match while counting up clear Writing a 1B into this field clears the ISR.CMup bit. A read always returns 0.
3	CMdw	Compare match while counting down clear Writing a 1B into this bit clears the ISR.CMdw bit. A read always returns 0.
4	Ev0DS	Event 0 detection clear Writing a 1B into this bit clears the ISR.Ev0DS bit. A read always returns 0.
5	Ev1DS	Event 1 detection clear Writing a 1B into this bit clears the ISR.Ev1DS bit. A read always returns 0.
6	Ev2DS	Event 2 detection clear Writing a 1B into this bit clears the ISR.Ev2DS bit. A read always returns 0.

Passive Level Config		
bit	name	This register holds the configuration for the output passive level control.
bwPWM - 1 : 0 OPL		
Output Passive Level of PWM outputs This field controls the passive level of the output pin. 0B Passive Level is LOW 1B Passive Level is HIGH A write always addresses the shadow register, while a read always returns the current used value.		