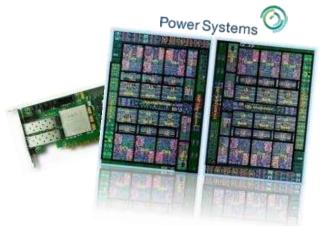


# CAPI SNAP Education Series: User Guide

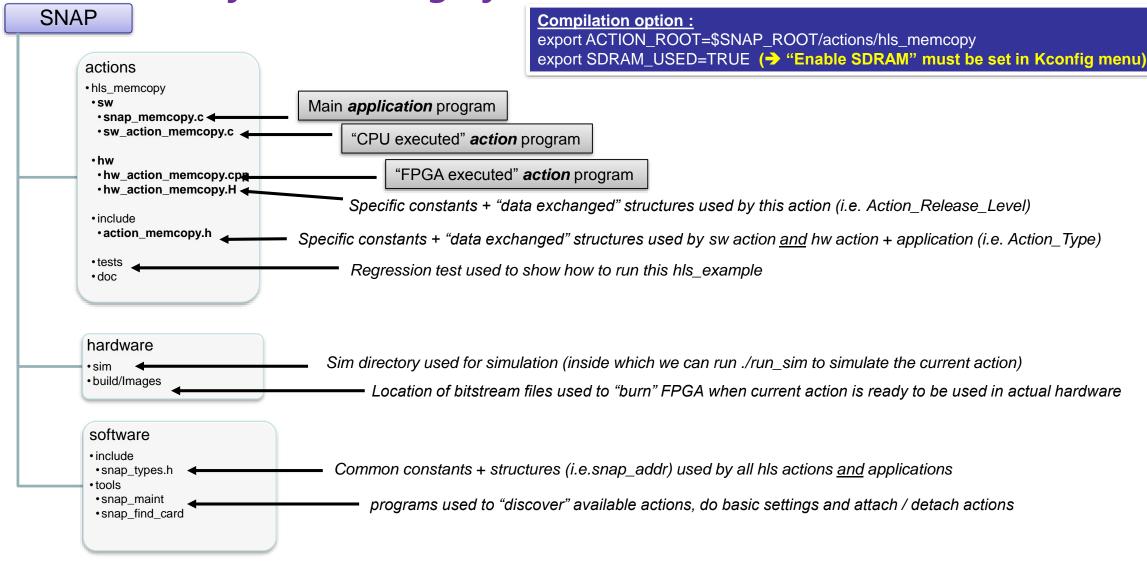
# CAPI SNAP Education hls\_memcopy : howto? V2.3











### **Action overview**

**<u>Purpose:</u>** Transferring data between different resources :

- host memory,
- DDR,
- NVMe (soon)

### When to use it:

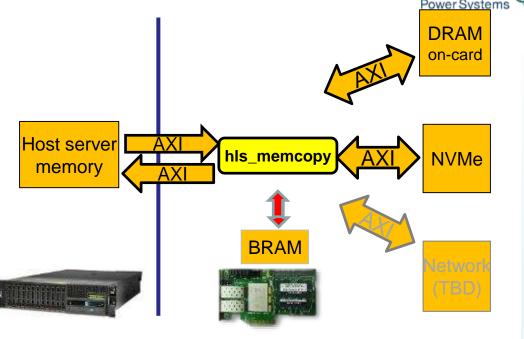
- Understand Basic access to different interfaces
- Memcopy benchmarking

### **Memory management:**

- Application is managing address of Host memory and DDR
- Action is testing if size of transfer is greater than DRAM size (see constants)
- Size of buffer (BRAM) used to copy data can be configured (see constants)

### **Known limitations:**

- HLS requires transfers to be 64 byte aligned and a size of multiples of 64 bytes
- DDR simulation model reads will return wrong values if non 64 bytes words or non initialized words are read (this is due to the simulation model only)



**CAPI SNAP Enabled Card** 

# Action usage (1/2)



```
Usage: ./snap_memcopy [-h] [-v, --verbose] [-V, --version]

-C, --card <cardno> can be (0...3)

-i, --input <file.bin> input file.

-o, --output <file.bin> output file.

-A, --type-in <CARD_DRAM, HOST_DRAM, ...>.

-a, --addr-in <addr> address e.g. in CARD_RAM.

-D, --type-out <CARD_DRAM, HOST_DRAM, ...>.

-d, --addr-out <addr> address e.g. in CARD_RAM.

-s, --size <size> size of data.

-t, --timeout Timeout in sec to wait for done. (10 sec default)

-X, --verify verify result if possible (only CARD_DRAM)

-N, --no irg Disable IROs
```

#### **Example:**

```
export SNAP TRACE=0x0
snap_maint -vv

echo move 4kB from Host to DDR@0x0 and back from DDR@0x0 to Host
rm t2; dd if=/dev/urandom of=t1 bs=1K count=4
SNAP CONFIG=FPGA snap_memcopy -i t1 -D CARD_DRAM -d 0x0
SNAP_CONFIG=FPGA snap_memcopy -o t2 -A CARD_DRAM -a 0x0 -s0x1000

diff t1 t2
  if diff t1 t2 >/dev/null; then echo "RC=$rc file_diff ok"; else
    echo -e "$t RC=$rc file_diff is wrong\n$del"; exit 1;
fi
```

```
Options: (default option in bold)

SNAP_TRACE = 0x0 → no debug trace

SNAP_TRACE = 0xF → full debug trace

SNAP_CONFIG = FPGA → hardware execution

SNAP_CONFIG = CPU → software execution
```

# Action usage (2/2)



#### Different cases that can be run

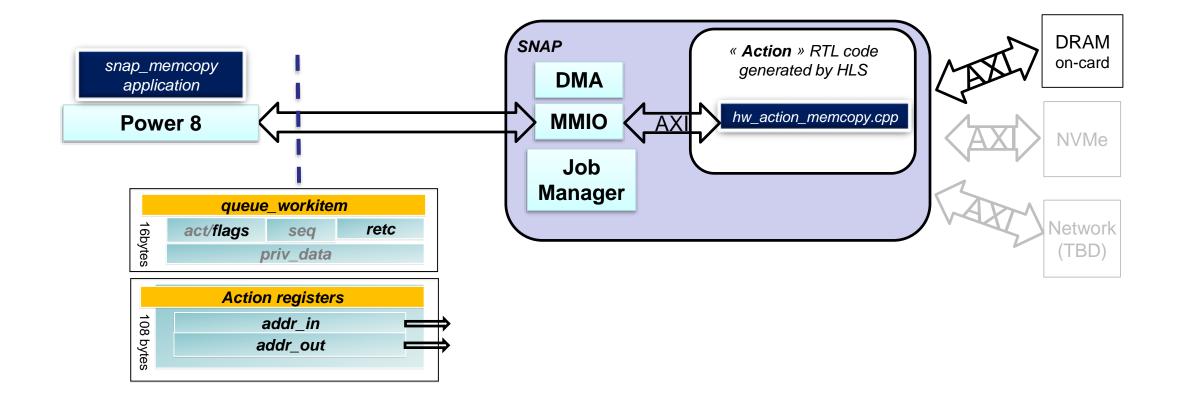
```
snap maint -vv -C0
echo create a 512MB file with random data ...wait...
rm t2; dd if=/dev/urandom of=t1 bs=1M count=512
echo READ 512MB from Host - one direction
snap memcopy -C0 -i t1
echo WRITE 512MB to Host - one direction - (t1!=t2 since buffer is 256KB)
snap memcopy -C0 -o t2 -s0x2000 0000
echo READ 512MB from DDR - one direction
snap memcopy -C0 -s0x2000 0000 -ACARD DRAM -a0x0
echo WRITE 512MB to DDR - one direction
snap memcopy -C0 -s0x2000 0000 -DCARD DRAM -d0x0
Move 4KB from Host to DDR and back to Host and compare
rm t2; dd if=/dev/urandom of=t1 bs=1K count=4
snap memcopy -i t1 -D CARD DRAM -d 0x0
snap memcopy -o t2 -A CARD DRAM -a 0x0 -s0x1000
diff t1 t2
echo same test using polling instead of IRQ waiting for the result
snap memcopy -o t2 -A CARD DRAM -a 0x0 -s0x1000 -N
```

Take in account that running on a simulator is far more slow than an execution on a FPGA:

→ moving 512MB with a simulator is a HUGE challenge. May be just trying 4K should be sufficient!

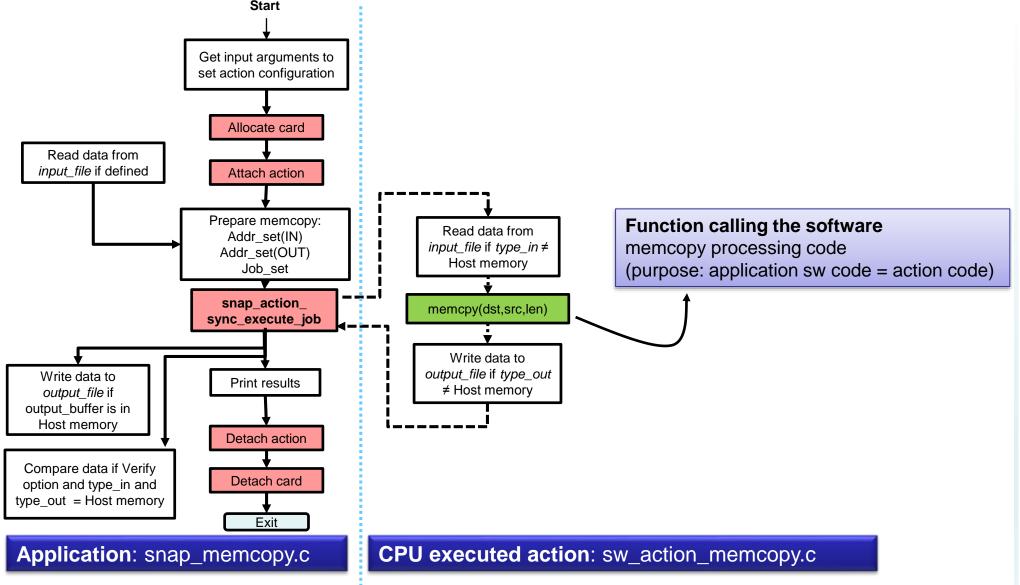
## memcopy registers





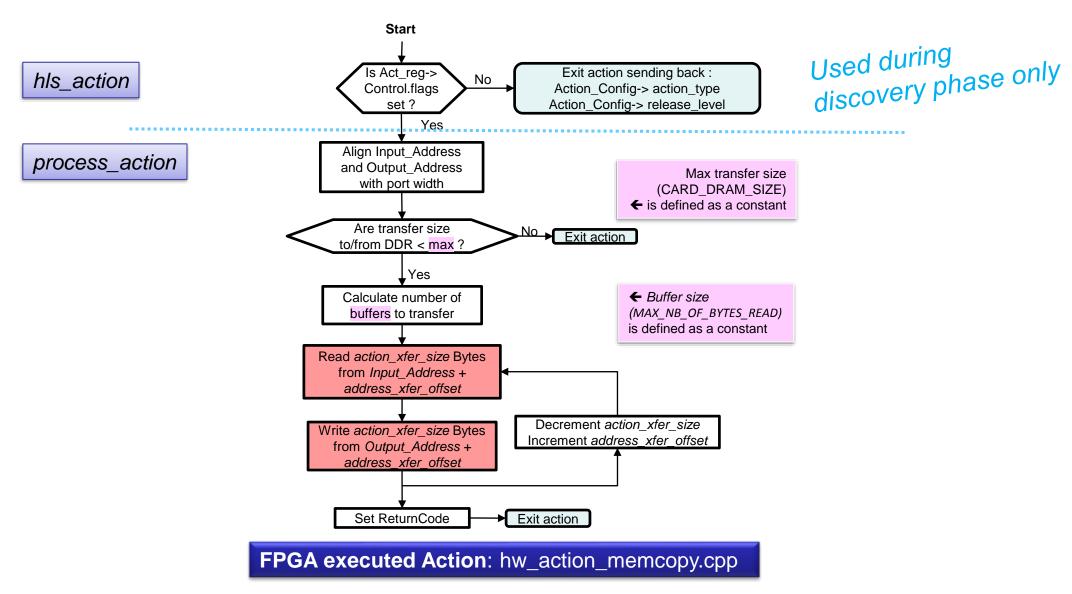
# Application Code + software action code : what's in it?





### Hardware action Code: what's in it?





### **Constants - Ports**



### **Constants:** → \$ACTION\_ROOT = snap/actions/hls\_memcopy

Constant name	Value	Туре	Definition location	Usage
MEMCOPY_ACTION_TYPE	0x10141000	Fixed	\$ACTION_ROOT/include/action_memcopy.h	memcopy ID - list is in snap/ActionTypes.md
RELEASE_LEVEL	0x00000023	Variable	\$ACTION_ROOT/hw/hw_action_memcopy. <b>H</b>	release level – user defined
MAX_NB_OF_BYTES_READ	(256 * 1024)	Variable	\$ACTION_ROOT/hw/hw_action_memcopy. <b>H</b>	Max size in Bytes of the buffer for read/write access
MAX_NB_OF_WORDS_READ	(MAX_NB_OF_BYTES_READ/BPERDW)	Operation	\$ACTION_ROOT/hw/hw_action_memcopy. <b>H</b>	Max size in 64B words of the buffer for read/write access
CARD_DRAM_SIZE	(1 * 1024 *1024 * 1024)	Variable	SACTION ROOT/NW/NW action memcony <b>H</b>	Max size of the DDR - prevents from moving data with a size larger than this value

### **Ports used:**

Ports name	Description	Enabled
	Host memory data bus input Addr : 64bits - Data : 512bits	Yes
dout_gmem	Host memory data bus output Addr : 64bits - Data : 512bits	Yes
d_ddrmem	DDR3 - DDR4 data bus in/out Addr : 33bits - Data : 512bits	Yes
nvme	NVMe data bus in/out Addr : 32bits - Data : 32bits	No (soon)

# **MMIO** Registers



Doad and	l Mrita ara c	oncidored :	from the application / s	oftware cide							7
	g.Control		der is initialized by the S		The action will undate t	the Peturn code a	nd read the flags	value			i i
_	NTROL								he action		-
Simu - WF		If the flags value is 0, then action sends only the action_RO_config_reg   Read@   3   2   1			T T T T T T T T T T T T T T T T T T T	0		Typical Write value		ıl Read value	1
0x3C40	0x100	0x180	sequence flags			short action type	f001_01_00		7		1
x3C41	0x104	0x184	•		ode 0x102/0x104)			)	0x102 - 0x104	SUCCESS/FAILURE	1
)x3C42	0x108	0x188		Priva		c0febabe					
0x3C43	0x10C	0x18C	Private Data				deadbeef				]
											_
action_	_reg.Data	Action sp	ecific - user defined - ne	eed to stay in 108 By	tes						
memco	opy_job_t		e way for application ar			h this set of regist	ers				<u>[</u>
imu - WF	R Write@	Read@	3	2	1	0	Typical	al Write value Typical		l Read value	]
0x3C44	0x110	0x190		in.ad	l <b>dr</b> (LSB)						
0x3C45	0x114	0x194	in.addr (MSB)								
0x3C46	0x118	0x198	in. <b>size</b>								
0x3C47	0x11C	0x19C	in. <b>flags</b> (SR0	in. <b>flags</b> (SRC, DST,) in. <b>type</b> (HOST, DRAM, N\							_
0x3C48	0x120	0x1A0	out.addr (LSB) out.addr (MSB)								
0x3C49	0x124	0x1A4							_		
0x3C4A	0x128	0x1A8	out. <b>size</b>								_
0x3C4B	0x12C	0x1AC	out. <b>flags</b> (SR	RC, DST,)	out. <b>type</b> (HOST	, DRAM, NVME,)					4
Ć A CTIC	0x130	0x1B0	action management			CONAD	DOOT / a atia ma				_
	_	/nw/nw_	_action_memcopy.	.п			_ROOT/actions/	include/nis	_snap.H		
• .	f struct {	Control	/* 10 hydaa */				fstruct {				
	ONTROL			ov#00 */			snapu8_t sat; // short action type snapu8_t flags;				
<pre>memcopy_job_t Data; /* up to 108 bytes */ uint8_t padding[SNAP_HLS_JOBSIZE - sizeof(memcopy_job_t)];</pre>						apu16_t seq;					
	-	aingįSiv <i>P</i>	IP_HLS_JUBSIZE	- sizeoi(memcoj	oy_Job_t)];		apu32_t Retc;				
} action_reg;						snapu64_t Reserved; // Priv_data \$			AP ROOT/softwa	are/include/snap_types.h	
\$ACTION_ROOT/include/action_memcopy.h typedef struct memcopy_job {					} CON	} CONTROL;			edef struct <b>snap_a</b>	. —	
									uint64_t addr;		
									uint32_t size;		
struct snap_addr in; /* input data */					_					snap_addrtype_t	
struct <b>snap_addr</b> out; /* output data */										snap_addrflag_t	t flags;       /* SRC, DST, EXT,
}	memcopy	y_job_t;							} sn	ap_addr_t;	

# **Performances measurements**



### Measurements on cards (512MB memory area transfer)

hls_ı	тетсору	1-direction access					
256KBytes buffer	- 64 access/burst	Read from Host	Write to Host	Read from DDR	Write to DDR		
	Bytes transferred	BW (GBps)	BW (GBps)	BW (GBps)	BW (GBps)		
CAPI1.0:	POWER8 + ADKU3	3.337	3.305	DDR3: <b>10.336</b>	DDR3: <b>9.584</b>		
CAPI1.0:	POWER8 + N250S	3.166	3.569	DDR4: <b>14.854</b>	DDR4: <b>13.524</b>		
CAPI2.0 :	POWER9 + FX609	12.321	14.201	DDR4: <b>14.926</b>	DDR4: <b>14.820</b>		
CAPI2.0:	POWER9 + RCXVUP	12.288	13.120	DDR4: <b>13.520</b>	DDR4: <b>13.487</b>		

#### Latency to access DDR3 memory:

Read: from HLS\_action request to data in HLS: 232ns
Write: from HLS action request to data in DDR: 226ns

#### Latency to access DDR4 memory:

Read: from HLS\_action request to data in HLS: 184ns
Write: from HLS\_action request to data in DDR: 105ns

#### To run these performances, run the following:

```
from snap installation directory, get the card slot number
    snap find card -A <name of the card>
    0 or 1
     ./actions/hls memcopy/tests/test 0x10141000 throughput.sh -C1 -dLONG
or
    snap maint -vvv -C1
    echo create a 512MB file ...wait...
    dd if=/dev/urandom of=t1 bs=1M count=512
     echo READ 512MB from Host
    snap memcopy -C1 -i t1
    echo WRITE 512MB to Host
    snap memcopy -C1 -o t2 -s0x2000 0000
    echo READ 512MB from DDR
    snap memcopy -C1 -s0x2000 0000 -ACARD DRAM -a0x0
    echo WRITE 512MB to DDR
     snap memcopy -C1 -s0x2000 0000 -DCARD DRAM -d0x0
```

# Path of improvements



1. HLS memcpy function waits for the end of the request before starting a new one. Being able to parallelize reads with writes since both ports are independent would increase performance since the DMA is able to pipeline requests.





- V2.0: initial document
- V2.1: new files directory structure applied
- V2.2: changes to have one direction access to get real performances
- V2.3: simplification of paths thanks to new SNAP features updates in documentation Issue#320 circumvention removed