Dian-Lun Lin

https://dian-lun-lin.github.io | https://www.linkedin.com/in/dian-lun-aaron-lin-0ba721117/ | cyc4542000@gmail.com | (+1) 657-657-3479

EDUCATION

University of Wisconsin-Madison *US;* 2024
PhD in Computer Engineering
- Thesis: Task-parallel Heterogeneous Programming System for Logic Simulation, Advisor: Tsung-Wei Huang

National Taiwan University *Taiwan;* 2019
MS in Electrical Engineering
- Thesis: On the Analysis of Network Creation Game with Imperfect Monitoring, Advisor: Ho-Lin Chen
- Teaching: Algorithms (2017 Fall & 2019 Spring)

National Cheng Kung University *Taiwan;* 2017
BS in Electrical Engineering

RESEARCH INTERESTS/SKILLS

Explore high-performance computing techniques to accelerate machine learning, electronic design automation, and other scientific computing applications using modern C++ and SIMD operations.

WORK EXPERIENCE

IBM *WA, US;* Nov. 2025 - present
Research Engineer - Watsonx Data

Intel *OR, US;* Sep. 2024 - Oct. 2025
AI Research Engineer/Scientist at Intel Labs

NVIDIA *Remote, US;* May. 2022 – Aug. 2022
Research Intern at Design Automation Research

NVIDIA *Remote, US;* May. 2021 – Nov. 2021
Research Intern at Design Automation Research

SOFTWARE PROJECTS

1. **Intel ScalableVectorSearch**: a performance library for vector similarity search
   - https://github.com/intel/ScalableVectorSearch
   - I am one of the core developers. I explore innovative high-performance computing technologies and methodologies that can be integrated into SVS. I investigate opportunities for enhancing performance and efficiency, such as inter-query and intra-query parallelism using heterogeneous computing and GPU computing, ensure that the library is both performance-critical and easy to integrate into existing applications.
2. **Taskflow**: A General-purpose Parallel and Heterogeneous Task Programming System
   - https://github.com/taskflow/taskflow (Over 10K GitHub stars)
   - I am one of the core developers. I developed cudaFlow, a significant feature within Taskflow. cudaFlow enables users to harness heterogeneous parallelism by constructing a CPU-GPU task graph. Currently, my focus lies on enhancing Taskflow's capabilities by integrating C++ Coroutines to facilitate multitasking. Additionally, I actively engaged in optimizing Taskflow's runtime performance by leveraging modern C++20 concurrency.
3. **Taro**: Task-based Asynchronous Programming System using C++ Coroutine
   - https://github.com/dian-lun-lin/taro
   - I built Taro which allows users to write coroutines in a task graph while abstracting away complex coroutine management. I also developed a coroutine-aware work-stealing algorithm to support the programming model while minimizing CPU migration overhead. I presented Taro in CppCon 2023.
4. **RTLflow**: From RTL to CUDA - A GPU Acceleration Flow for RTL simulation with Multiple Inputs
   - https://github.com/dian-lun-lin/verilator_rtlflow
   - This is a one-year project cooperated with NVIDIA Design Automation Research. During the collaboration, I organized meetings with NVIDIA and effectively communicated the progress of the work. RTLflow demonstrated over 40 times speedup compared to the existing solutions, making it the most efficient open-source RTL simulator available. Through this project, I received second place at the PACT Student Research Competition 2022.
5. **GenFuzz**: A GPU-accelerated hardware fuzzer
   - https://github.com/dian-lun-lin/GenFuzz
   - With NVIDIA Research collaboration, I built GenFuzz, a GPU-accelerated hardware fuzzer. We showed that GenFuzz running on a single A6000 GPU achieves 80× runtime speed-up when compared to state-of-the-art hardware fuzzers. The work has been published in DAC 2023.

6. **SNIG**: Accelerated Large Sparse Neural Network Inference using Task Graph Parallelism
   - https://github.com/dian-lun-lin/SNIG
   - I developed a powerful inference engine tailored for large sparse neural networks. The implementation outperformed the state-of-the-art baseline by up to 2.3 times on a machine equipped with 4 GPUs. Through this project, I received the champion of the 2020 IEEE HPEC Neural Network Challenge.

AWARDS

1. ACM/IEEE DAC Young Student Fellowship, 2020 & 2021 & 2023 & 2024
2. Second place in ACM/PACT Student Research Competition, 2022
3. ACM ISPD Wafer-Scale Physics Modeling Contest – Honorable Mention, 2021
4. Champion of the IEEE/MIT/Amazon HPEC Large Sparse Neural Network Challenge, 2020
5. Best Master Thesis Nomination, Department of Electrical Engineering, National Taiwan University, 2019
6. Presidential Award, Department of Electrical Engineering, National Cheng Kung University, Fall 2015

CONFERENCE PUBLICATION

1. Wan-Luan Lee, Shui Jiang, **Dian-Lun Lin**, Che Chang, Boyang Zhang, Yi-Hua Chung, Ulf Schlichtmann, Tsung-Yi Ho, and Tsung-Wei Huang, "iG-kway: Incremental k-way Graph Partitioning on GPU," *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2025
2. Wan-Luan Lee, **Dian-Lun Lin**, Cheng-Hsiang Chiu, Ulf Schlichtmann, and Tsung-Wei Huang, "HyperG: Multilevel GPU-Accelerated k-way Hypergraph Partitioner," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025
3. Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, **Dian-Lun Lin**, Yang Sui, Chih-Chun Chang, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "iTAP: An Incremental Task Graph Partitioner for Task-parallel Static Timing Analysis," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025
4. Che Chang, Boyang Zhang, Cheng-Hsiang Chiu, **Dian-Lun Lin**, Yi-Hua Chung, Wan-Luan Lee, Zizheng Guo, Yibo Lin, and Tsung-Wei Huang, "PathGen: An Efficient Parallel Critical Path Generation Algorithm," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, 2025
5. **Dian-Lun Lin**, Tsung-Wei Huang, Joshua San Miguel, and Umit Ogras, "TaroRTL: Accelerating RTL Simulation using Coroutine-based Heterogeneous Task Graph Scheduling", *International European Conference on Parallel and Distributed Computing (Euro-Par),* Madrid, Spain, 2024
6. **Dian-Lun Lin** (co-first author), Boyang Zhang, Che Chang, Cheng-Hsiang Chiu, Bojue Wang, Wan Luan Lee, Chih-Chun Chang, Donghao Fang, and Tsung-Wei Huang, "G-PASTA: GPU Accelerated Partitioning Algorithm for Static Timing Analysis", *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, 2024
7. Wan Luan Lee, **Dian-Lun Lin**, Tsung-Wei Huang, Shui Jiang, Tsung-Yi Ho, Yibo Lin, and Bei Yu, "G-kway: Multilevel GPU-Accelerated k-way Graph Partitioner", *ACM/IEEE Design Automation Conference (DAC),* San Francisco, CA, 2024
8. Che Chang, Tsung-Wei Huang, **Dian-Lun Lin**, Guannan Guo, and Shiju Lin, "Ink: Efficient Incremental k-Critical Path Generation", *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, 2024
9. Shao-Hung Chan, Zhe Chen, **Dian-Lun Lin**, Yue Zhang, Daniel Harabor, Tsung-Wei Huang, Sven Koenig, and Thomy Phan, "Anytime Multi-Agent Path Finding using Operator Parallelism in Large Neighborhood Search", *International Conference on Autonomous Agents and Multi-Agent Systems (AAMAS),* Auckland, New Zealand, 2024
10. Tsung-Wei Huang, Boyang Zhang, **Dian-Lun Lin**, and Cheng-Hsiang Chiu, "Parallel and Heterogeneous Timing Analysis: Partition, Algorithm, and System", *ACM International Symposium on Physical Design (ISPD),* Taiwan, 2024
11. **Dian-Lun Lin**, Yanqing Zhang, Haoxing Ren, Shih-Hsin Wang, Brucek Khailany, and Tsung-Wei Huang, "GenFuzz: GPU-accelerated Hardware Fuzzing using Genetic Algorithm with Multiple Inputs", *ACM/IEEE Design Automation Conference (DAC), US,* 2023
12. Cheng-Hsiang Chiu, **Dian-Lun Lin**, and Tsung-Wei Huang, "Programming Dynamic Task Parallelism for Heterogeneous EDA Algorithms (Invited paper)", *International Conference on Computer-Aided Design (ICCAD),* US, 2023
13. Elmir Dzaka, **Dian-Lun Lin**, Tsung-Wei Huang "Parallel And-Inverter Graph Simulation Using a Task-graph Computing System", *IEEE International Symposium on Parallel and Distributed Processing Workshops (IPDPSW)*, US, 2023
14. **Dian-Lun Lin**, Haoxing Ren, Yanqing Zhang, Brucek Khailany, and Tsung-Wei Huang, "From RTL to CUDA: A GPU

Acceleration Flow for RTL Simulation with Batch Stimulus", *ACM International Conference on Parallel Processing (ICPP)*, France, 2022

15. Cheng-Hsiang Chiu, **Dian-Lun Lin**, and Tsung-Wei Huang, "An Experimental Study of SYCL Task Graph Parallelism for Large-Scale Machine Learning Workloads", *International Workshop of Asynchronous Many-Task systems for Exascale (AMTE),* Portugal, 2021
16. **Dian-Lun Lin** and Tsung-Wei Huang, "Efficient GPU Computation using Task Graph Parallelism", *European Conference on Parallel and Distributed Computing (Euro-Par),* Portugal, 2021
17. **Dian-Lun Lin** and Tsung-Wei Huang, "A Novel Inference Algorithm for Large Sparse Neural Network using Task Graph Parallelism", *IEEE High-performance and Extreme Computing Conference (HPEC),* US, 2020

JOURNAL PUBLICATION

1. Wan-Luan Lee, **Dian-Lun Lin**, Shui Jiang, Cheng-Hsiang Chiu, Yibo Lin, Bei Yu, Tsung-Yi Ho, and Tsung-Wei Huang, "G-kway: Multilevel GPU-Accelerated *k*-way Graph Partitioner using Task Graph Parallelism," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, 2025
2. **Dian-Lun Lin** and Tsung-Wei Huang, "Accelerating Large Sparse Neural Network Inference using GPU Task Graph Parallelism," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 11, pp. 3041-3052, Nov 2022
3. Tsung-Wei Huang, **Dian-Lun Lin**, Chun-Xun Lin, and Yibo Lin, "Taskflow: A Lightweight Parallel and Heterogeneous Task Graph Computing System," *IEEE Transactions on Parallel and Distributed Systems (TPDS)*, vol. 33, no. 6, pp. 1303-1320, June 2022
4. Tsung-Wei Huang, **Dian-Lun Lin**, Yibo Lin, and Chun-Xun Lin, "Taskflow: A General-purpose Parallel and Heterogeneous Task Programming System," *IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems (TCAD)*, vol. 41, no. 5, pp. 1448-1452, May 2022

TALK

1. "A Task Graph-based Programming System for CPU-GPU Heterogeneous Computing", Invited Talk, GPUs for Science Day, NERSC, Oct 2023
2. "Taro: Task-graph-based Asynchronous Programming Using C++ Coroutines", CppCon, Oct 2023
3. "Accelerating Hardware Design Verification: Exploring Simultaneous Execution of Multiple Stimuli with RTLflow and GenFuzz ", Invited Talk, MediaTek Research, June 2023
4. "An Introduction to C++ Coroutines Through a Thread Scheduling Demonstration", Invited Talk, Berkeley National Lab, June 2023
5. "An Introduction to C++ Coroutines Through a Thread Scheduling Demonstration", CppNow, May 2023
6. "RTLflow: A GPU acceleration flow for parallel RTL simulation", ICPP, Aug 2022
7. "G-Fuzz: GPU-accelerated hardware fuzzing", NVIDIA Research, Aug 2022
8. "RTLflow: A GPU acceleration flow for parallel RTL simulation", NVIDIA Research, Apr 2022
9. "cudaFlow: A Modern C++ Programming Model for GPU Task Graph Parallelism", CppCon, Oct 2021
10. "GPU-accelerated RTL simulation", NVIDIA Research, Aug 2021

JOURNAL REVIEWS

1. Parallel Computing (2025)
2. Journal of Computational Science (2025)
3. Applied Soft Computing (2025)
4. Transactions on Architecture and Code Optimization (2024 & 2025)
5. The Journal of Supercomputing (2023 & 2024 & 2024 & 2025)
6. International Journal of Computational Intelligence Systems (2024)
7. Cluster Computing (2024)
8. Operations Research Forum (2024)
9. International Journal of Machine Learning and Cybernetics (2024)
10. Concurrency and Computation: Practice and Experience (2024)
11. IEEE Access (2023)

PROGRAM COMMITTEE

1. CppCon - “The C++ Conference” 2022-2024
2. C++Now - “The C++Now Conference” 2023-2024

INVITED POSTS

1. A Concise Introduction to Coroutines
   - https://www.modernescpp.com/index.php/a-concise-introduction-to-coroutines-by-dian-lun-li/
2. Coroutines: A Scheduler for Tasks
   - https://www.modernescpp.com/index.php/coroutines-a-scheduler-for-tasks-by-dian-lun-li/