Eight Discipline Report (8D Report)

To:	8D report No.:
From:：	RMA claim No.:
CC：	Chicony Power P/N: **A250A001P-FJ01**
	Customer P/N:
Submit date: **2018/12/07**	Product description:
Receive date: **2018/12/07**	

Subject：MOS 參數誤觸 IC 保護 (MOS ciss 參數比 main source 大，導致 turn off 較慢，觸發 IC CMP 保護)
MOS, Ciss, 誤觸保護, Capacitive Mode Protection [MOSFET, IC]

D1.) 問題解決成員:Use Team Approach

主持者 (Team Leader)：

內部成員 (Internal Team Members):

外部成員 (External Team Member):

D2.)問題說明:Problem Description:

(**Note**: Use **who**, **what**, **when**, **where**, **why**, **how**, **how many** to specify the Customer's problem.)

250W Power Shut Down Issue

1. **adapter shut down on production line.**
2. **The phenomenon is:**
   Turn-on the adapter at no load → Connect the NB system (Light load around 0.87A)
   → Adapter latched
3. **If the adapter didn't turn on at no load condition first, the adapter will not shut down.**
4. **Check related protection function of controller, it's not Output: SCP, OVP, OLP,FSP PFC: OVP, UVP, SCP, OLP protection trigged.**

D3.)內部或客戶的暫時解決辦法及實施日期:Implement and Verify Containment Action:

(Note: Internal / external containment action effectiveness and date.**)**

1. **FAE of CPT got this PSU from customer for further analysis.**
2. **CPT send 1pc PSU to customer for exchange.**

D4.)不良原因確認: Define and Verify Root Causes:

(Note: Identify and verify all suspect causes, which needs explain why the problem occurred.**)**

Main control IC (NXP TEA1716T) has build-in CMP (Capacitive Mode Protection) to prevent the operation enter "Capacitive Mode" and the time-out of CMP is 690ns, ±100ns(Checked with NXP).

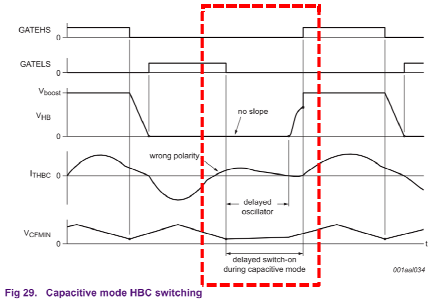
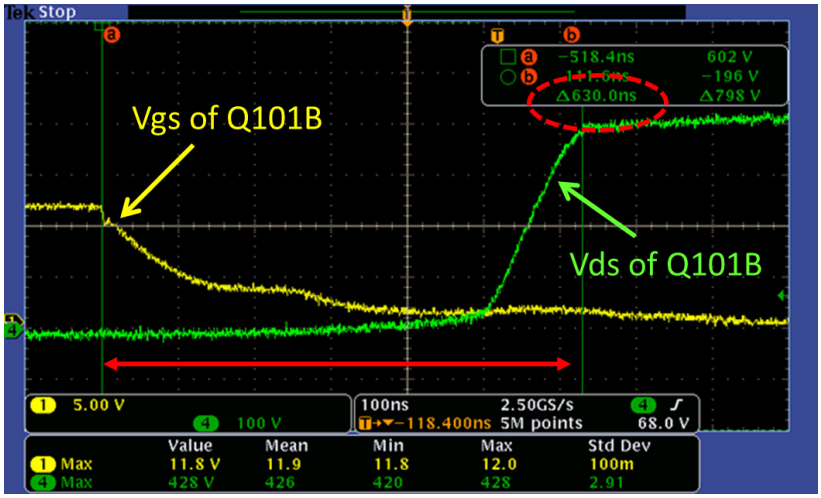
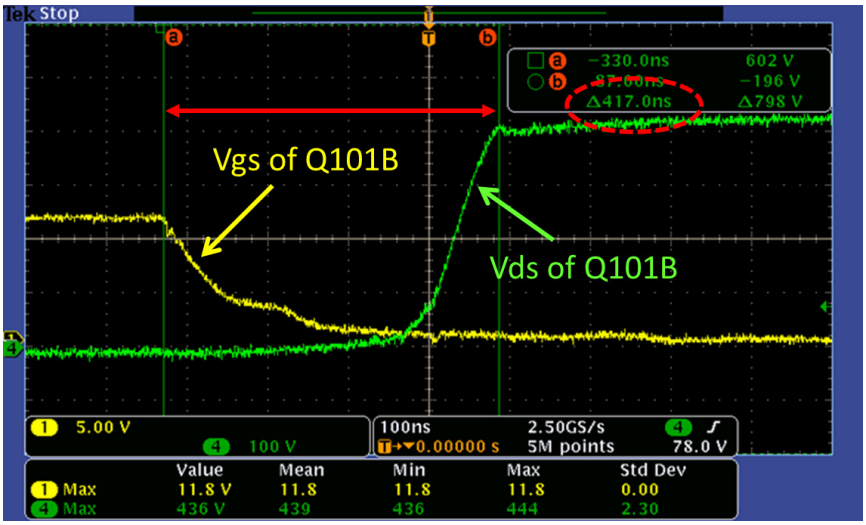


Fig 29. Capacitive mode HBC switching

When the MOSFET is 30A/600V (Toshiba TK31A60W), because of the "capacitance parameter" of MOSFET, when adapter is operating under light load (burst mode) condition, the MOSFET turn off time will too long then trig the CMP function of IC.



When the MOSFET is 20A/600V (Toshiba TK20A60W), because of the "capacitance parameter" of MOSFET, the turn-off time is much shorter and it will not trig CMP function of IC.



6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

TK20A60W

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 300 V, V_{GS} = 0 V, f = 1 MHz	—	1680	—	pF
Reverse transfer capacitance	C_{rss}		—	7	—	
Output capacitance	C_{oss}		—	40	—	
Effective output capacitance	$C_{o(er)}$	V_{DS} = 0 to 400 V, V_{GS} = 0 V	—	70	—	
Gate resistance	r_g	V_{DS} = OPEN, f = 1 MHz	—	1.5	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	25	—	ns
Switching time (turn-on time)	t_{on}		—	50	—	
Switching time (fall time)	t_f		—	6	—	
Switching time (turn-off time)	t_{off}		—	100	—	
MOSFET dv/dt ruggedness	dv/dt	V_{DD} = 0 to 400 V, I_D = 10 A	50	—	—	V/ns

TK31A60W

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 300 V, V_{GS} = 0 V, f = 100 kHz	—	3000	—	pF
Reverse transfer capacitance	C_{rss}		—	9.5	—	
Output capacitance	C_{oss}		—	70	—	
Effective output capacitance	$C_{o(er)}$	V_{DS} = 0 to 400 V, V_{GS} = 0 V	—	123	—	
Gate resistance	r_g	V_{DS} = OPEN, f = 1 MHz	—	2	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	32	—	ns
Switching time (turn-on time)	t_{on}		—	70	—	
Switching time (fall time)	t_f		—	8.5	—	
Switching time (turn-off time)	t_{off}		—	165	—	
MOSFET dv/dt ruggedness	dv/dt	V_{DD} = 0 to 400 V, I_D = 7.7 A	50	—	—	V/ns

Analyze:

The key factors of CMP are:

1. PSU enter Burst Mode: Loading 0.X~2.0A

2. Time-out of CMP of IC: 690ns±100ns (590ns~790ns)

3. The capacitance parameters of MOSFET

TK20A60W				
Items	Min.	Typ.	Max.	Unit
Ciss	1512	1680	1848	pF
Crss	6	7	8	
Coss	36	40	44	
Rg (Internal)	-	1.5	-	Ω
Qg	43	48	53	nC
Vth	2.7	-	3.7	V

TK31A60W				
Items	Min.	Typ.	Max.	Unit
Ciss	2700	3000	3300	pF
Crss	8.5	9.5	10.5	
Coss	63	70	77	
Rg (Internal)	-	2	-	Ω
Qg	85	86	95	nC
Vth	2.7	-	3.7	V

Refer to following formula, the calculated timing of 20A and 30A MOSFET:

260ns + $t_4 = (R_g + R_{g\_app})(C_{gd} + C_{gs})\ln\left(\frac{V_{GS\_APP}}{V_{GP}}\right)$ + $t_{vr} = \frac{Q_{gd\_d}(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{DS\_D} - V_{F\_D})\left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)}$ +

Delayed Oscillator

$t_{if} = (R_g + R_{g\_app})(C_{iss}{}^{at\ V_{DS}})\ln\left(\frac{\left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)}{V_{th}}\right)$ + $t_{vf} = \frac{Q_{gd\_d}(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{DS\_D} - V_{F\_D})\left(V_{GS\_APP} - \left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)\right)}$ = Delay Time

20A MOSFET	30A MOSFET
By calculation: **444ns**	By calculation: **604ns**
By measurement: **427ns**	By measurement: **656ns**

Time-out of CMP of IC: **690ns±100ns (590ns~790ns)**

1. **The power shut down due to the IC CMP function trigged when PSU enter burst mode.**
2. **The time-out of IC CMP function is 690ns±100ns (590ns~790ns)**
3. **Due to different capacitance characteristics between 20A and 30A MOSFET, this issue would be found when using 30A MOSFET**
4. **According to our calculation and measurement, 20A MOSFET will not trig CMP function because of shorter turn off time**
5. **We shipped 260pcs MP revision goods (Use 20A MOSFET) to customer factory and 120pcs PSU on production line, there's no power shut down has been found**
6. **According to above information, we believe use 20A MOSFET is no problem of this model.**

D5.)改善措施:Corrective Action Verification:

(Note: Be make sure the corrective actions is effective in process as well as able to fix the customer complaint problem**)**

Q101A/Q101B uses 20A MOSFET(TK20A60W).

D6.)改善措施實施日期:Implement Permanent Corrective Actions:

(Note: Be provide the phase-in date or lot# of corrective actions **implementation** in process**)**

immediately

D7.)預防再發生措施:Prevent Recurrence:

(Note: Modified the management, operating systems, practices, and procedures to prevent recurrence for the

problems as well as lessons learned cases.)

1. **Check all critical functions not only on "steady-state" but also "transient-state" (EE functions, components stress, EMI…)**
2. **Consider all side-effects when doing any modification → Build-up check list by category, for example:**
   - **Modify MOSFET to lower R_{DSON} for efficiency, thermal performance**
     → Check EMI, on/off timing(LLC) is necessary.
   - **Modify the capacitance of MOSFET D-S for EMI:**
     Check efficiency, thermal is necessary, capacitance more than 200pF is not allow.
3. **Check carefully about the parameter, behavior of critical components (transformer, line filter, MOSFET, IC…)**

D8.)確認並感謝問題解決成員:Check and Congratulate the Team:
(Note: Recognize the collective efforts of the team.**)**

Thanks to you all！！！

Signature **Team Leader**:	
	Name – Title
Signature by Approver:	
	Name-Title