



Eight Discipline Report (8D Report)

To:	8D report No.:
From: : Chicony Power Technology	RMA claim No.:
CC :	Chicony Power P/N: A240A005P
	Customer P/N:
Submit date: 5/18	Product description: 240W
Receive date: 5/18	Defect D/C or Lot No.:
Subject : 客戶端告知有 2pcs 240W 在 DC plug 移除後, 不定期插回系統端會無法充電 (IC, MOSFET)	
D1.) 問題解決成員: Use Team Approach 主持者 (Team Leader) : 內部成員 (Internal Team Members): 外部成員 (External Team Member):	
D2.) 問題說明: Problem Description: <i>(Note: Use who, what, when, where, why, how, how many to specify the Customer's problem.)</i>	

客戶端告知有 2pcs 240W 在 DC plug 移除後, 不定期插回系統端會無法充電,

取回不良品分析, 不良品複製出不良現象, 確認與客訴內容一致

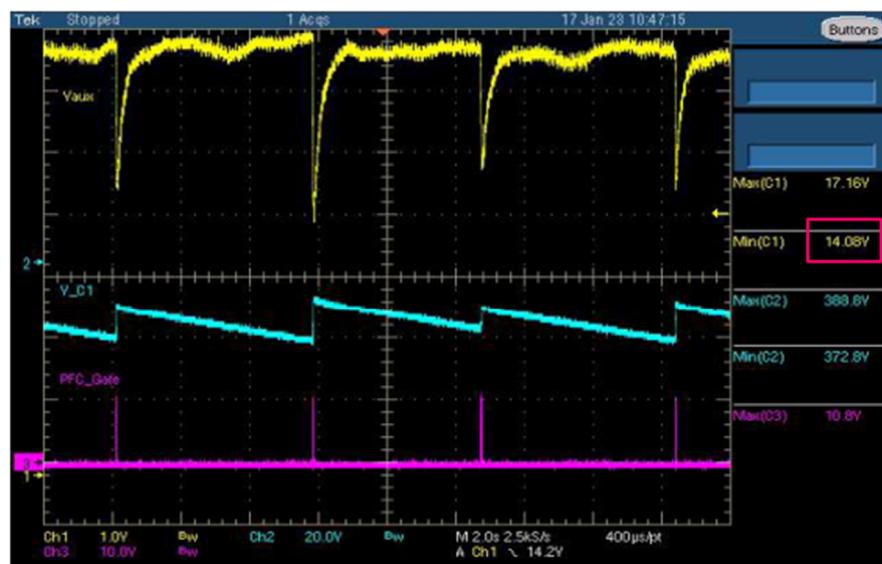
不良現象複製 :

於廠內模擬, Vin=110Vac, DC plug 不接, 放置 3~4 小時後, 產品 Latch 無電壓輸出, AC socket 插拔後可正常, 與客訴內容一致。

不良原因分析 :

DC plug 不接系統且 AC 持續供電時, PSU 運作在 burst mode, IC41(LLC 控制) Vcc 是藉由 C35 提供穩定電壓, 當 IC31(PFC 控制 IC)驅動 Q1&Q2 導通時, 會造成 Vcc 電壓有短暫 drop 發生。若 drop 的電壓進入 IC41 UV Protection 保護範圍時有機會導致產品 Latch

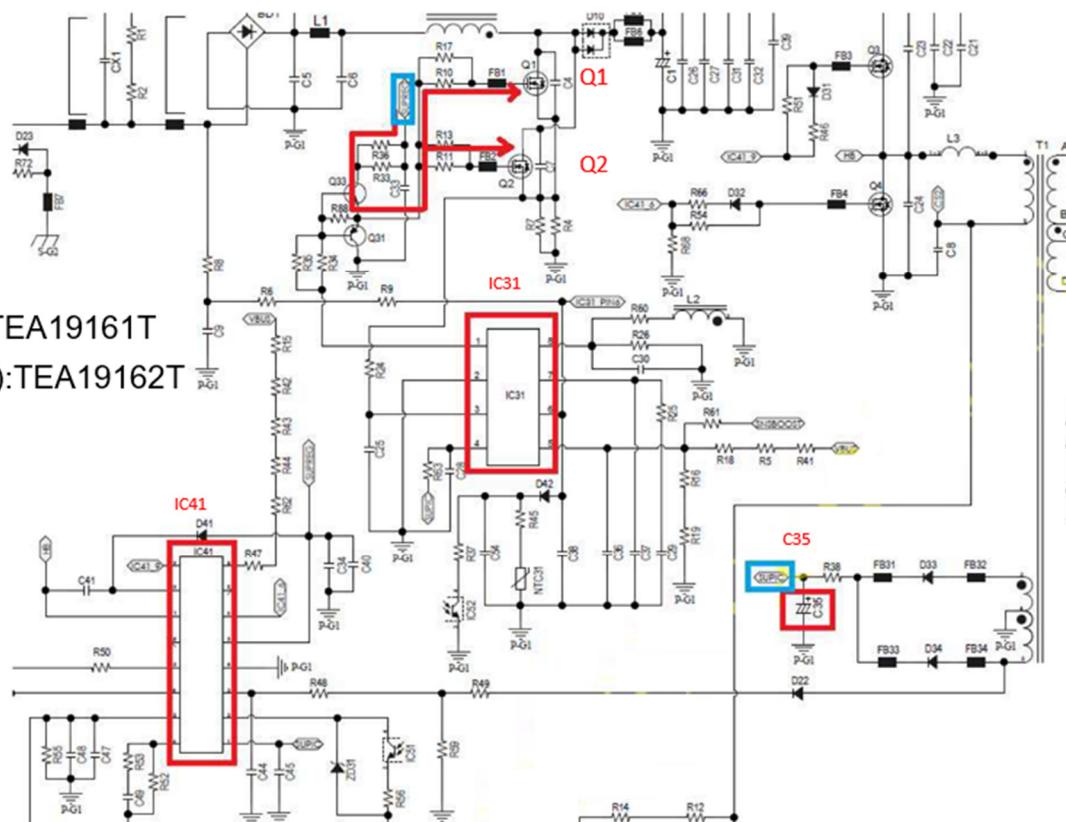
	UV Protection Range	Remark
LLC IC(IC41)	12.7~13.7V	保護點較高
PFC IC(IC31)	8.55~9.45V	



CH1:Vcc CH2:Bulk cap CH3:PFC_Gate

失效分析:

電路如下

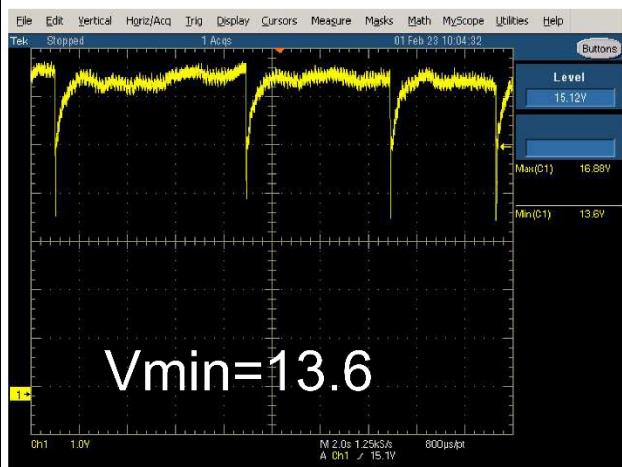




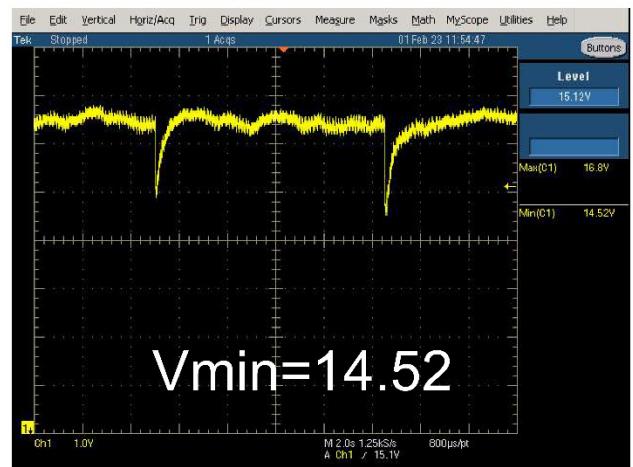
不良品分析

#1 確認不良品 Vaux 電壓表現@ $V_{in_ac}=100 / 220V$, No load

$V_{in_ac}=100V$



$V_{in_ac}=220V$



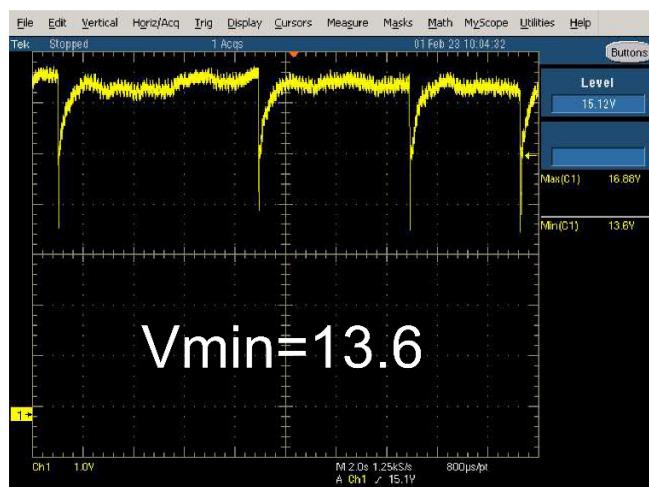
不良品觸發 IC41 Vcc pin UVP 保護功能，造成 no load 待機下 latch

$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC	12.7	13.2	13.7	V
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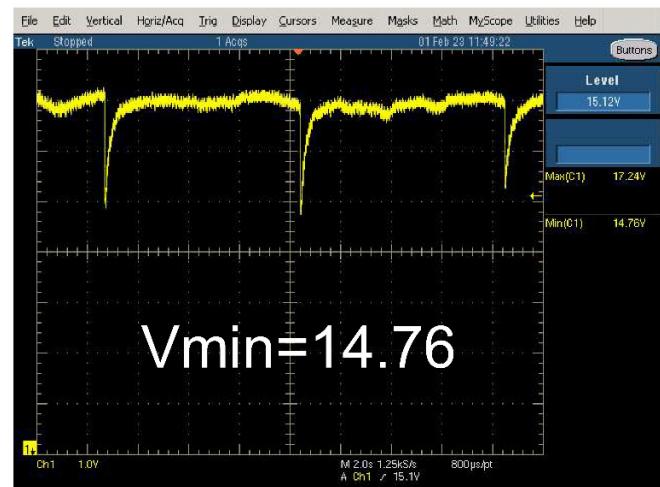
#1 比較良品 和不良品的 Vaux 電壓表現@ $V_{in_ac}=100V$, No load

發現良品與不良品使用不同的 source, 在 $V_{cc min}$ 有差

不良品(Q1/Q2 APEC)



良品(Q1/Q2 AOS)





- Q1/Q2 source 參數比對，APEC Qg 比另外兩家大許多
- 因 240W 線路架構，PFC MOS 驅動透過圖騰柱由Vcc 電壓提供，Qg 越大將導致 PFC MOS 啟動瞬間所需要的能量越大， $Q=CV(Q=Qg, C=Aux Cap, V=\text{電容 drop 電壓的幅度})$ ，所以 Qg 越大將導致 Vcc 電壓 drop 越深。

APEC

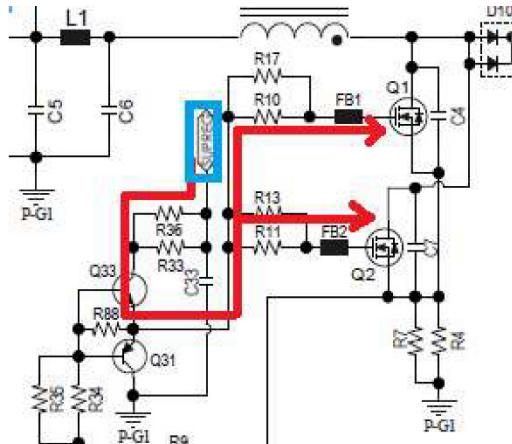
Q_g	Total Gate Charge	$I_D=14A$	-	91	145	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=480V$	-	20	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=10V$	-	42	-	nC
*	Turn on Delay Time	$V=-300V$	-	22	-	ns

IFX

Gate Charge Characteristics		$V_{DD}=400\text{ V}, I_D=16\text{ A}, V_{GS}=0 \text{ to } 10\text{ V}$	-	12	-	nC
Gate to source charge	Q_{gs}		-	18	-	
Gate to drain charge	Q_{gd}		-	53	70	
Gate charge total	Q_g		-	-	-	

AOS

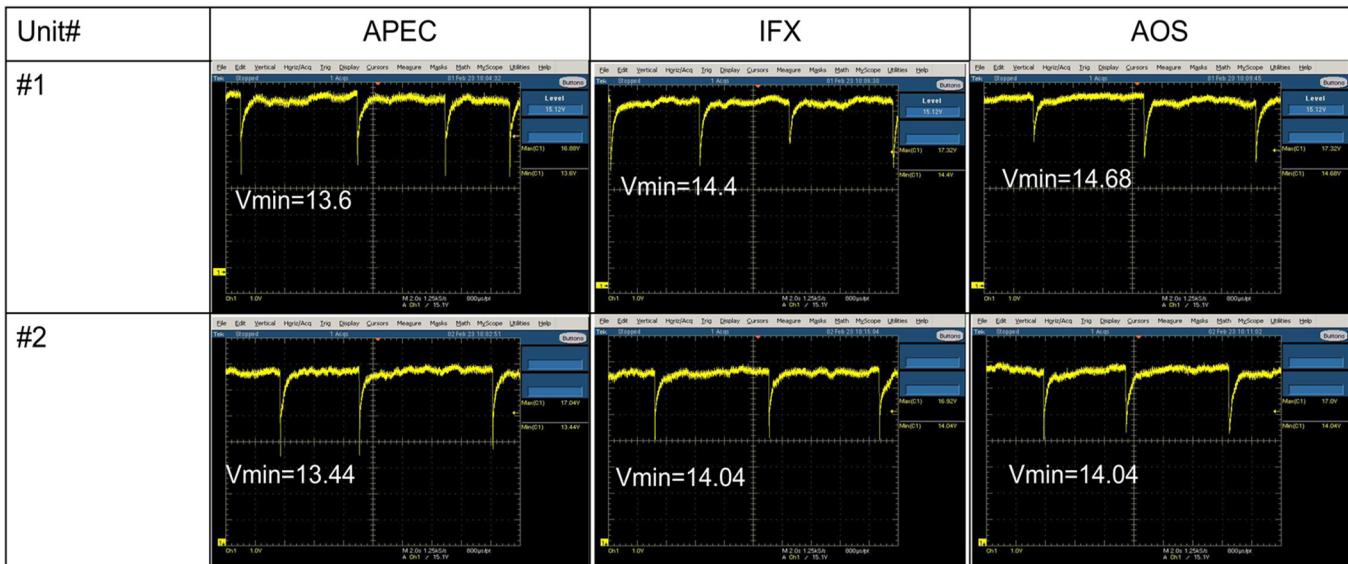
SWITCHING PARAMETERS		$V_{GS}=10\text{V}, V_{DS}=480\text{V}, I_D=14\text{A}$	19	39	60	nC
Q_g	Total Gate Charge		9	19	30	nC
Q_{gs}	Gate Source Charge		4	9	15	nC
Q_{gd}	Gate Drain Charge		-	-	-	



Vendor	$Qg(\text{nC})$
APEC	91~145
IFX	53~70
AOS	19~60



- 將兩台不良品的 Q1 與 Q2 更換為 IFX 與 AOS 確認 Vaux 電壓表現@Vin=100Vac，No Load.
- APEC source 有機會觸發 IC41 Vcc pin UVP，造成 Latch



- 使用不良品 APEC 量測Qg 數據，約落在 90nC

APEC 原廠結果

D/C:	21542F	21929F	22370F	22383F
Symbol	Q_g	Q_g	Q_g	Q_g
Conditions				
	$I_D=14A$, $V_{DD}=480V$, $V_{GS}=10V$			
Units	nC	nC	nC	nC
#1	90.42	90.12	90.86	91.78
#2	90.8	90.08	90.94	91.14
#3	90.7	90.1	90.78	91.57
#4	90.93	90.18	91.47	91.28
#5	90.46	90.22	91.04	91.02
#6	91.12	90.1	91.02	90.77
#7	90.91	90.54	90.88	91.1
#8	91.36	90.4	90.35	91.33
#9	91.25	90.37	90.94	91.1
#10	91.04	89.38	90.54	91.36
#11	90.69	90.1	90.58	91.57
#12	91.39	89.79	91.06	91.46
#13	90.93	90.06	91.5	90.9
#14	91.18	89.33	90.86	91.54
#15	91.09	89.55	90.7	90.9
#16	91.22	89.01	91.12	91.01
#17	91.06	89.78	90.91	91.22
#18	90.83	89.49	90.24	91.12
#19	90.91	89.66	90.53	91.42
#20	91.09	89.23	90.54	90.02
#21	90.74	89.78	90.67	91.26
#22	90.96	89.79	91.33	90.08
#23	90.91	89.6	90.56	90.18
#24	90.78	90.03	90.88	90.26
#25	90.13	90.26	90.46	90.56
#26	90.74	89.74	90.38	90.21
#27	90.43	90.02	90.54	90.14
#28	90.34	89.46	90.34	90.21
#29	90.78	89.82	90.26	90.58
#30	90.78	89.71	90.16	90.74
#31	91.31	89.33	90.56	90.78
#32	90.69	90.42	90.43	90.67



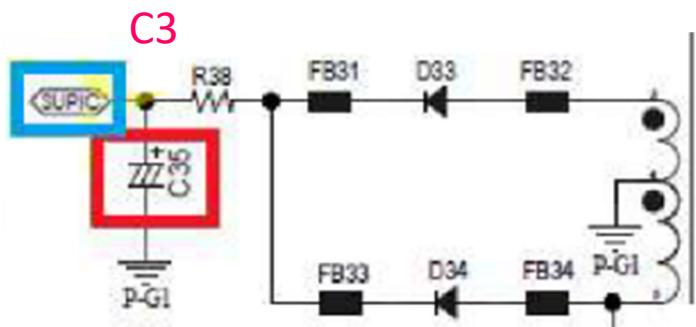
改善對策

AOS New Build Test Plan :

- 取 APEC & AOS 樣品各 30pcs 量測 Vcc (90V/110V/220V), C35 容值改小使其更容易頂到 IC UVP 其數據如下
- 根據量測數據可確認如下訊息：
 - a. 當輸入電壓越高，IC Vcc 測試值越高
 - b. 在 90/110/220V，良品的 Vcc 值均大於 IC UVP 值

APEC	量測VCC				IC UVP
	85V	90V	110V	220V	
1		13.46	13.89	15.21	13.01
2		13.56	14.12	15.04	13.02
3		13.56	14.04	15.55	13.12
4		13.24	13.69	15.77	13.08
5		13.37	13.68	15.68	13.08
6		13.37	13.73	14.85	13.09
7		13.32	13.66	14.64	13.17
8		13.41	13.66	14.6	13.12
9		13.83	13.89	15.8	13.08
10		13.6	13.68	15.25	12.95
11		13.5	13.77	14.88	
12		13.54	14.13	15.48	
13		13.76	13.9	15.32	
14		13.57	14.12	15.6	
15		13.52	14.26	15.72	
16		13.68	13.76	15.12	
17		13.36	13.72	14.69	
18		13.57	13.62	14.91	
19		13.76	14.4	15.26	
20		13.38	13.76	15.09	
21	13.79	13.77	13.88	15.25	
22	13.44	13.49	13.84	15.49	
23	13.68	13.74	13.8	15.32	
24	14.04	14.08	14.12	15.48	
25	14.16	14.15	14.24	15.32	
26	13.38	13.39	13.67	15.1	
27	13.61	13.61	13.72	15	
28	13.34	13.33	13.66	14.88	
29	13.72	13.83	14.49	15.64	
30	13.33	13.37	13.64	14.68	

AOS	量測VCC		
	90V	110V	220V
1	14.05	14.32	15.63
2	14.13	14.33	15.56
3	14.10	14.32	15.26
4	14.08	14.26	15.52
5	14.05	14.21	15.88
6	14.01	14.20	15.64
7	14.00	14.29	15.68
8	14.08	14.36	15.16
9	14.12	14.34	15.29
10	14.17	14.43	15.64
11	14.05	14.22	15.40
12	14.12	14.37	15.40
13	14.07	14.29	15.00
14	14.16	14.36	15.66
15	14.00	14.12	15.68
16	14.02	14.16	15.66
17	14.00	14.15	15.74
18	14.08	14.20	15.23
19	14.09	14.23	15.19
20	14.00	14.24	15.76
21	14.06	14.33	15.50
22	14.13	14.32	15.45
23	14.11	14.24	15.28
24	14.03	14.36	15.41
25	14.06	14.25	15.14
26	14.01	14.20	15.78
27	14.01	14.20	15.73
28	14.08	14.20	15.21
29	14.12	14.31	15.26
30	14.09	14.32	15.73





AOS New Build Test Plan :

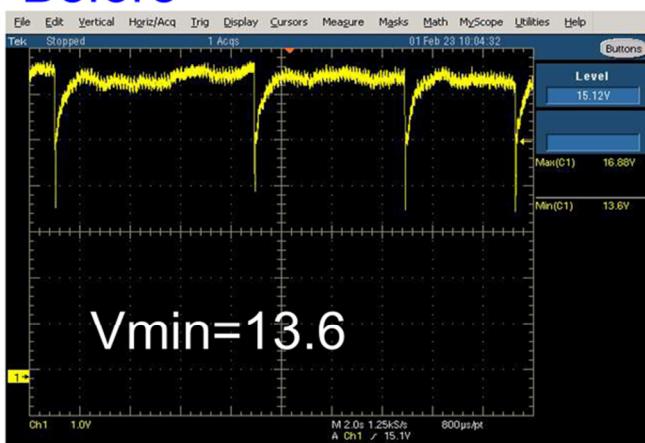
240W adapter with AOS Mosfet test					
項目	測試條件	測試數量	Fail數量	pass數量	不良率
B/I 車架驗證	Input 110Vac@8Hrs,DC 端空置	192	0	192	0.0%
	Input 110Vac@4Hrs,DC 端空置	192	0	192	0.0%
	Input 110Vac@4Hrs,DC 端空置	192	0	192	0.0%
	Total	576	0	576	0.0%
AC source sorting	Input 85Vac@ 60s	2,000	0	2,000	0.0%

*短期抽樣以每批工單取 sampling size 0.5%，以85Vac@ 60s測試條件，每周更新測試結果

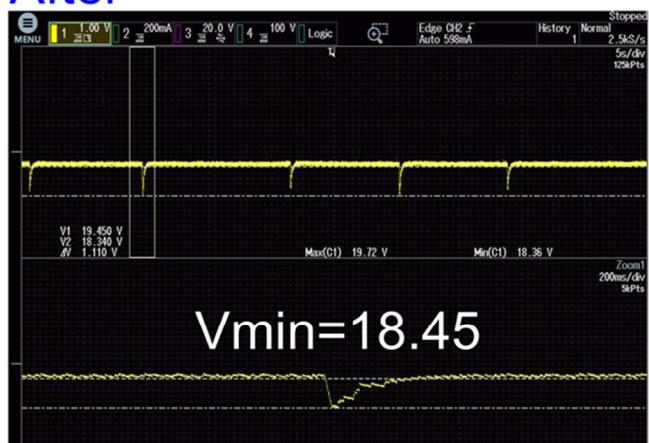
- R38 change from 2ohm to 0ohm
- C35 change from 220uF to 330uF

Vin_ac=100V, No load (APEC source)

Before



After



V _{uvp} (SUPIC)	undervoltage protection voltage on pin SUPIC	12.7	13.2	13.7	V
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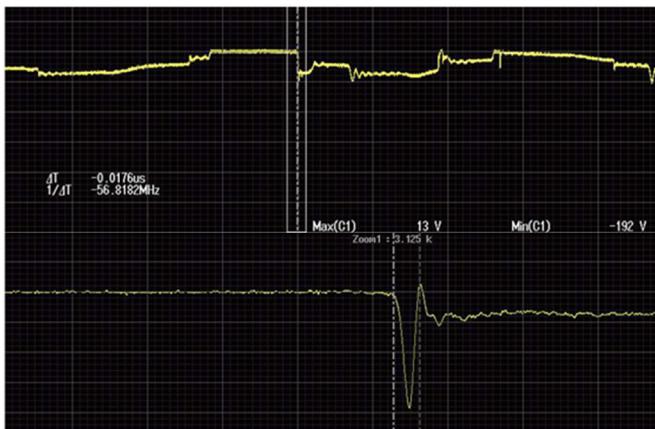


➤ Side Effect

Turn on Delay time (spec < 3S)

D33/D34 Voltage Stress (Voltage Derating=200V*0.95=190V)

Voltage Stress



Turn on delay time(330uF)



V_D34_max=192V

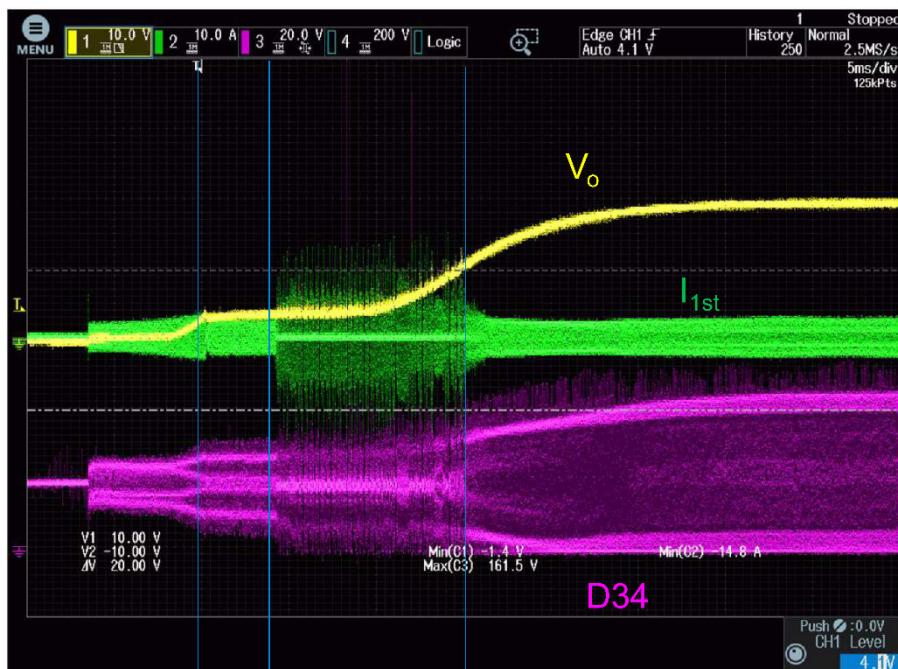
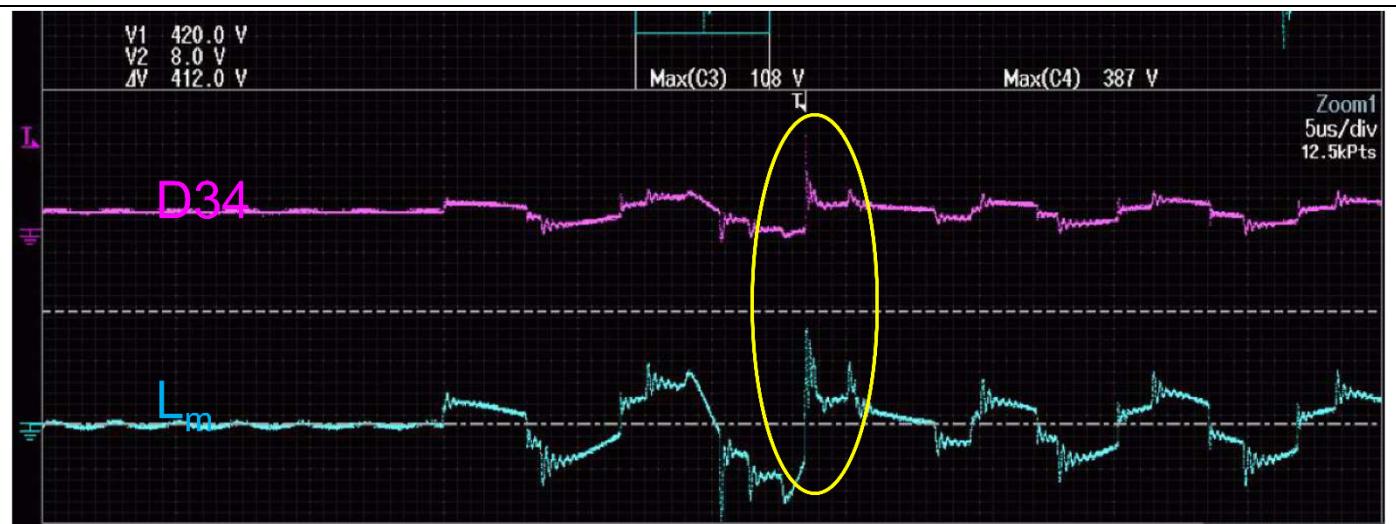
T_on=2.181S

➤ Analysis Stress

由激磁電感上的跨壓可發現D34 上的 spike是由諧振槽透過變壓器耦合到aux 上，

使 D33/D34 造成 spike。





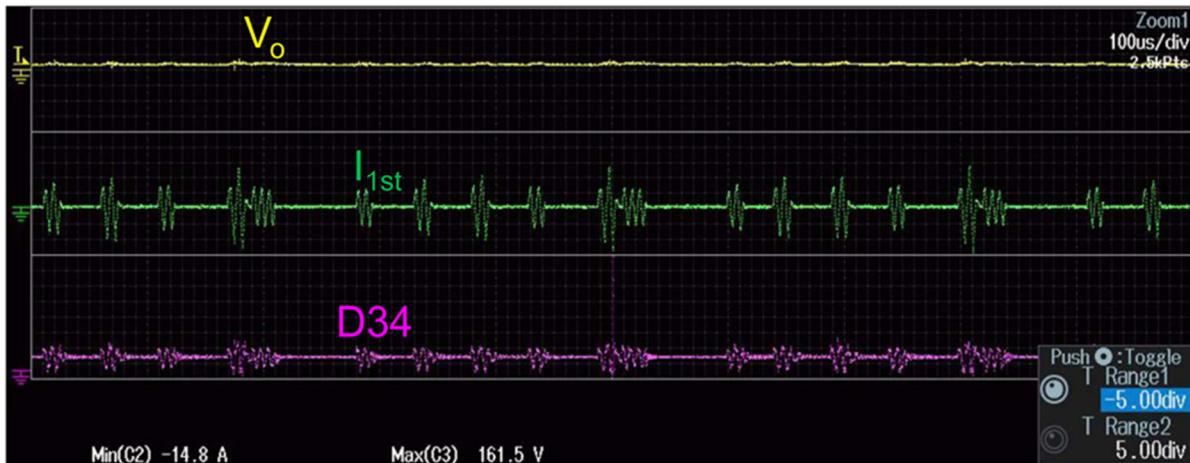
high power mode

burst mode

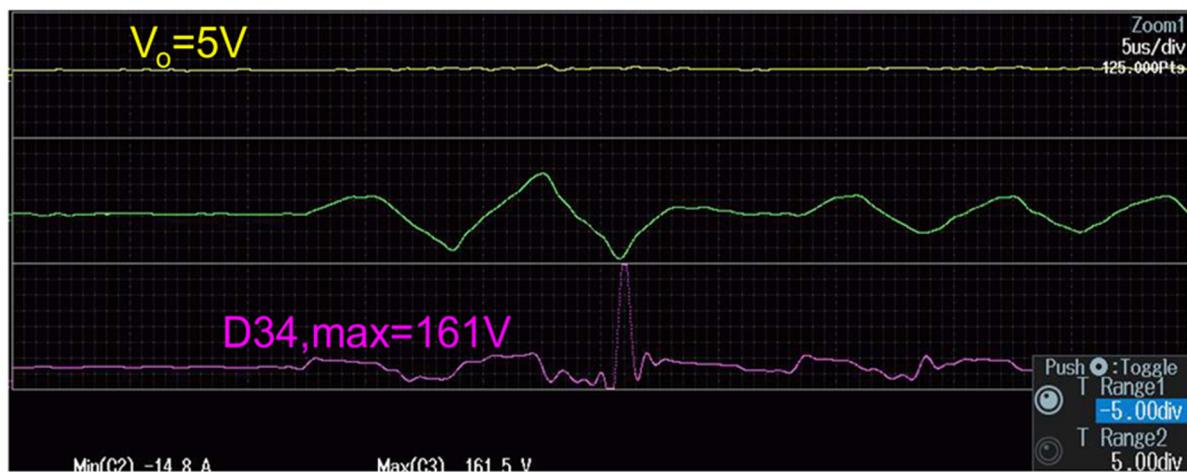
→high power mode



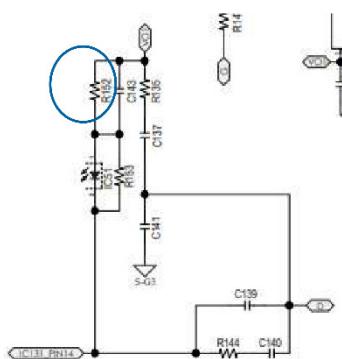
在此區間操作於burst mode ,而每個 cycle 的burst變得不規律

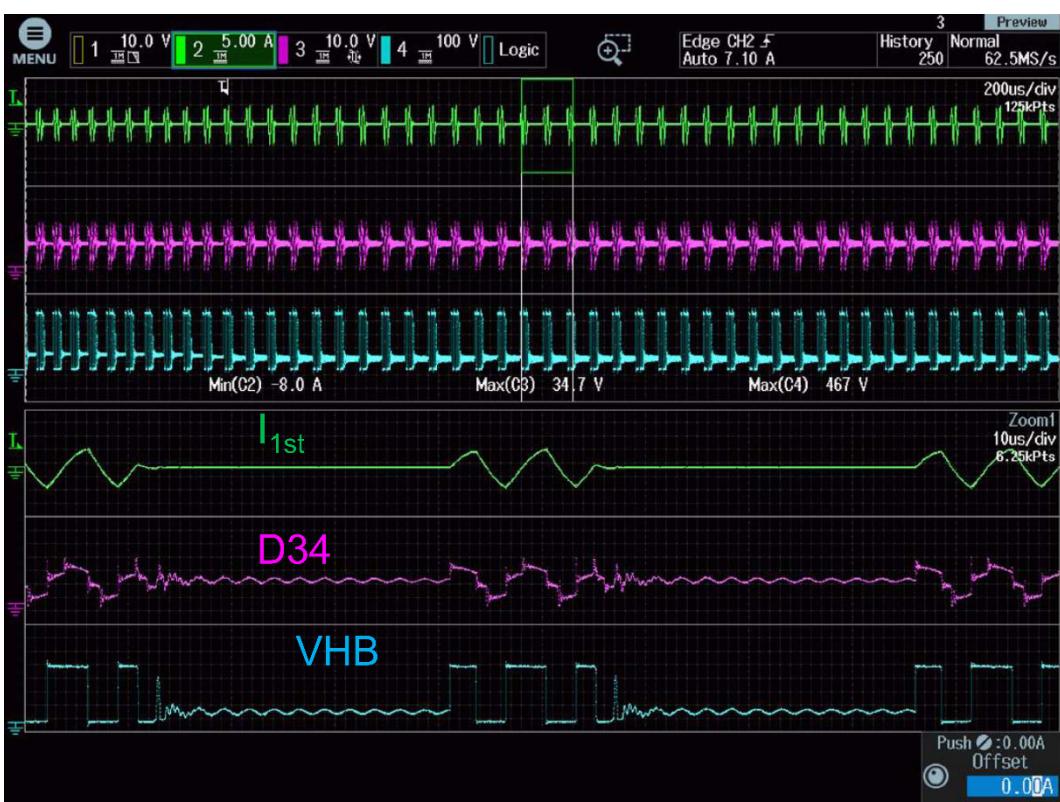
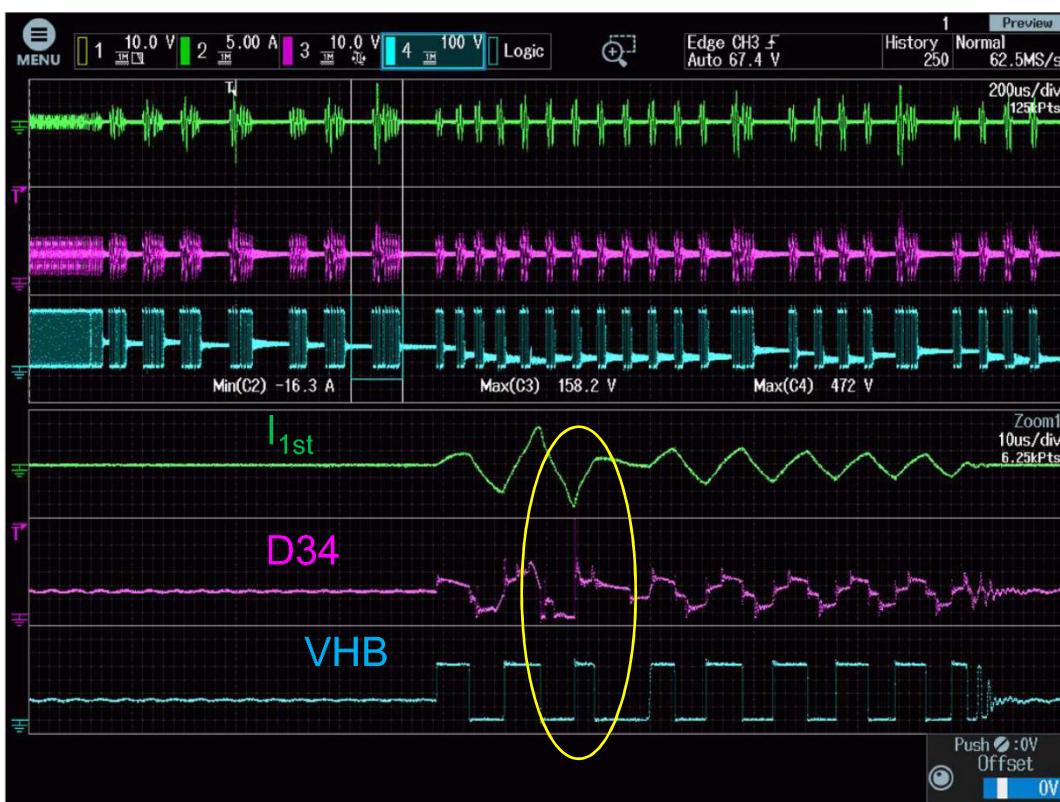


操作於burst mode ,每一叢burst電流都一根較大的電流spike ,與此同時D34也會有電壓spike



R152=1.25k 造成 FB 響應太快，偵測到輸出電壓不足時，瞬間補上能量造成較大的電流 spike ，使 burst mode 不穩定，High/Low side Gate 的 Cycle 不規則，因此調慢響應速度，使 burst mode 穩定，D34/D33 就不會有 spike 。







Final Solution

- R38 change from 2ohm to 0ohm
- C35 change from 220uF to 330uF
- R152 change from 1.25K to 3K

Function Test:

	100Vac/50Hz		240Vac/50Hz	
200% peak load	$V_{o,min} = 18.77V$		$V_{o,min} = 18.75V$	
225% peak load	$V_{o,min} = 18.75V$		$V_{o,min} = 18.77V$	
Dynamic 100Hz (0.05A~full load)	$V_{o,min} = 19.41V$		$V_{o,min} = 19.41V$	

Component De-rating Check :

D33/34 current derating

Location	Vendor	Part No.	Grade	Type	I (A)		Surge current rating (A)	I der. Factor (Steady State)	I der. Factor (Transient State)	I max accepted (A)	I surge accepted current (A)	Measured Current (A)		Calculate Stress Factor			
					Rating	Thermal-Current derating						90Vac Max Load	264Vac Max Load	Derating(%)	Steady State	Transient State	PASS / FAIL
					Steady State	AC on/off (Imax)						Steady State	Input ON/OFF	Steady State	Input ON/OFF		
D33/34	NEXPERIA	BAS316	A	SMD	1	1	30	90%	90%	0.9	27	0.08	0.65	8.00%	2.17%	PASS	

D33/34 voltage derating

Location	Vendor	Part No.	Grade	Max. Rating (V)	der. Factor (Steady state)	der. Factor (Transient state)	V max. accepted (Steady state)	V max. accepted (Transient state)	Measured Voltage (Vmax)				Calculate Stress Factor				
									264Vac / Max Load		264Vac / Min Load		Derating		Steady State	Transient State	PASS / FAIL
									Steady State	Input ON/OFF	Steady State	Input ON/OFF	Steady State	Transient State			
D33/34	NEXPERIA	BAS316	A	200	80%	95%	160	190	56.4	55.2	50	47.5	28.20%	27.60%	PASS		



D3.)內部或客戶的暫時解決辦法及實施日期:Implement and Verify Containment Action:

(Note: Internal / external containment action effectiveness and date.)

安排工廠端作對策驗證,驗證數量 10 台

Date:2022/6/10

D4.)不良原因確認: Define and Verify Root Causes:

(Note: Identify and verify all suspect causes, which needs explain why the problem occurred.)

1. 240W output latch 發生在 no load condition, Root cause 為 PWM 控制 IC 觸發 UVP保護功能導致 Latch.
2. UVP 觸發與PFC 的 MOSFET Qg 參數有關，參數越大 Latch 風險越高
3. Latch 發生在低壓市場，高壓市場無風險
4. HUB 庫存使用最嚴苛的條件，Sorting Condition: 85Vac/60s

D5.)改善措施:Corrective Action Verification:

(Note: Be make sure the corrective actions is effective in process as well as able to fix the customer complaint problem)

改善對策:

- a. 短期對策為更換 AOS source，每批工單按 sample size 0.5% 抽測 85Vac/60s
- b. 長期對策為 R38 change to 0ohm / C35 change to 330uF / R152 change to 3Kohm

風險評估(APEC source):

- a. 2K sorting: 100Vac 不良率 0.8%, 110Vac 不良率為 0.65%, 120Vac 不良率為 0.55%, 220Vac 不良率為 0%.
- b. 依據目前 HUB sorting(85Vac/60s)的結果，使用 APEC source 的不良率約在 1.25%
建立把關量測 SOP，針對新開發機種做把關，同時水平展開確認使用此 IC41 機種不會有 latch 風險

Date:2022/6/10

D6.)改善措施實施日期:Implement Permanent Corrective Actions:

(Note: Be provide the phase-in date or lot# of corrective actions implementation in process)



Immediately

D7.) 預防再發生措施: Prevent Recurrence:

(Note: Modified the management, operating systems, practices, and procedures to prevent recurrence for the problems as well as lessons learned cases.)

Same as D5

D8.) 確認並感謝問題解決成員 : Check and Congratulate the Team:

(Note: Recognize the collective efforts of the team.)

Thanks to you all ! ! !

Signature Team Leader:	Arthur Wu
	Name – Title
Signature by Approver:	Mark Meng
	Name-Title