

Eight Discipline Report (8D Report)

To:	8D report No.:
From: :	RMA claim No.:
CC :	Chicony Power P/N: W045R127P-AX01
	Customer P/N:
Submit date: 2020/10/08	Product description:
Receive date: 2020/10/08	
Subject : CS fail (CS 測試造成輸出電感跨壓上升影響回授運作) [CS 測試] 雜訊, 感抗, 跨壓變化, 迴授影響	
D1.) 問題解決成員: Use Team Approach	
主持者 (Team Leader) : 內部成員 (Internal Team Members): <div style="text-align: right;">外部成員 (External Team Member):</div>	
D2.) 問題說明: Problem Description:	
(Note: Use who, what, when, where, why, how, how many to specify the Customer's problem.) 45W Power CS Issue 搭配客戶系統做 CS 測試時, 發現在 CS 訊號進入 PSU 後會造成輸出電壓 drop, 由 19.6V 掉到 16.6V, 由於輸出電壓太低無法對系統電池充電, 造成系統端出現 AC mode / Battery mode 反覆切換的現象	
D3.) 內部或客戶的暫時解決辦法及實施日期: Implement and Verify Containment Action:	
(Note: Internal / external containment action effectiveness and date.) 1. FAE of CPT got this PSU from customer for further analysis. 2. CPT send 1pc PSU to customer for exchange.	

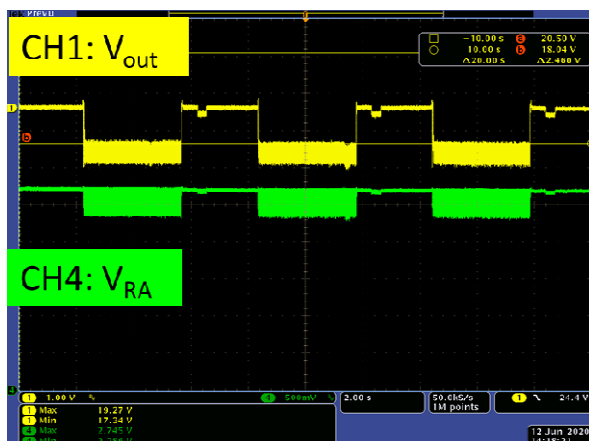
D4.)不良原因確認: Define and Verify Root Causes:

(**Note:** Identify and verify all suspect causes, which needs explain why the problem occurred.)

1. 確認前一版搭系統驗證 CS 測試結果 PASS.
2. 此版本為提升 EMI margin 在二次側輸出端新增 common choke(LF51).
3. 短路 LF51 驗證 CS 測試結果為 PASS.
4. 偵測輸出回授的電壓源由原本的 LF51 後(cable 端), 改接至 LF51 前, CS 測試結果為 PASS.

Common choke(LF51)干擾分析:

1. 當高頻雜訊干擾源竄入正迴路時, 造成 choke 感抗(Impedance)變大, 干擾 TL431 準位異常, 造成輸出異常掉電壓。
2. Choke 的感抗在越高頻時, 感抗會越高, 造成跨壓越大; 所以在高頻條件下, 輸出掉電壓現象會更明顯。
3. 測試 CS 時, 同時量測輸出電壓 與 TL431(R-A)電壓, 由下圖可得知, TL431 被干擾, V_{RA}:2.286V, 此時輸出電壓降至 17.24V

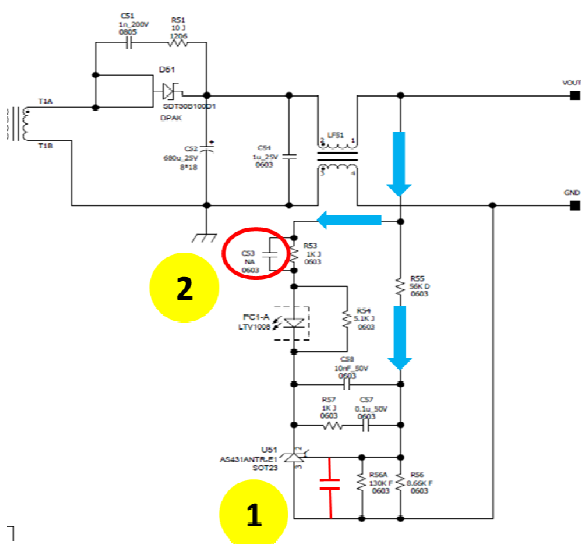


4. TL431 ref pin 增加旁路電容可降低影響

D5.)改善措施:Corrective Action Verification:

(Note: Be make sure the corrective actions is effective in process as well as able to fix the customer complaint problem)

1. 在 TL431 的對地電阻旁並聯電容，可 bypass 高頻雜訊，降低影響。
2. 在 C53 上，增加 33pF 濾波電容降低 TL431 被干擾影響。
3. 偵測電壓回授位置改在 LF51 前



D6.)改善措施實施日期:Implement Permanent Corrective Actions:

(Note: Be provide the phase-in date or lot# of corrective actions **implementation** in process)

immediately

D7.)預防再發生措施:Prevent Recurrence:

(Note: Modified the management, operating systems, practices, and procedures to prevent recurrence for the problems as well as lessons learned cases.)

1. 輸出電壓迴授訊號不要接在輸出 choke 後
2. 若因 layout 限制，在迴授迴路上就要預留電容
3. 所有與迴授線路的相關變更，都必須重新驗證 loop gain、CS、EFT 等項目。

D8.)確認並感謝問題解決成員:Check and Congratulate the Team:

(Note: Recognize the collective efforts of the team.)

Thanks to you all ! ! !

Signature	
Team Leader:	
	Name – Title
Signature by Approver:	
	Name-Title