Eight Discipline Report (8D Report)

To: **Wistron**	8D report No.: **20240301**
From:：**Chicony Power Technology**	RMA claim No.: **N/A**
CC：	Chicony Power P/N: **A090AP06P-DL01**
	Customer P/N: **H2FR2**
Submit date: **2024/5/17**	Product description: **90W Adapter**
Receive date: **2024/3/19**	
Subject：noise issue * 2pcs	

D1.) 問題解決成員:Use Team Approach

主持者 (Team Leader)：**Cf Liu**

內部成員 (Internal Team Members):

RD:Hunter/Benson

PE: Guoqian

IPQC/QE:Chase Cai

MFG: Xiaohui

IE: Yansong

Sales: Steve

外部成員 (External Team Member):

D2.)問題說明:Problem Description:

(**Note**: Use **who**, **what**, **when**, **where**, **why**, **how**, **how many** to specify the Customer's problem.)

12/7 Wistron(CD) feedback that 6pcs E5 90W units fail continuously in their NPI process.

Then till 12/26, more 18pcs failures were found, total 24pcs

DELL P/N: H2FR2, D/C :2021/11/24

Failure Station: B/I* 18pcs, OBA* 6pcs B/I time: 16H

Feedback date	Fail station	PPID
2021/12/7	B/I	CN-0H2FR2CH2001BNA0IKX03
		CN-0H2FR2CH2001BNA0IPX03
		CN-0H2FR2CH2001BN00BLX03
		CN0H2FR2CH2001BNA0IEX03
		CN0H2FR2CH2001BN00BNX03
		CN0H2FR2CH2001BNA0JLX03
2021/12/15		CN0H2FR2CH2001BN00FEX03
		CN0H2FR2CH2001BNA0J4X03
		CN0H2FR2CH2001BN00B5X03
		CN0H2FR2CH2001BN00BXX03
		CN0H2FR2CH2001BNA0IDX03
		CN0H2FR2CH2001BN002XX03
		CN0H2FR2CH2001BN00FDX03
		CN0H2FR2CH2001BNA0JFX03
		CN0H2FR2CH2001BN00DNX03
	OBA	CN0H2FR2CH2001BN00CNX03
		CN0H2FR2CH2001BN0066X03
		CN0H2FR2CH2001BNA0IXX03
		CN0H2FR2CH2001BN001LX03
2021/12/21		CN0H2FR2CH2001BN00BWX03
		CN0H2FR2CH2001BN00ICX03

D3.)內部或客戶的暫時解決辦法及實施日期:Implement and Verify Containment Action:

(Note: Internal / external containment action effectiveness and date.**)**

1. Stop the new build and on hold the stock of all E5 PD 90W model until the issue is clarified clearly.

Owner: PM/Ivy , OBA/Mary Implement date :12/7

DELL P/N	CPT P/N	CPT库存(成品pcs)	Hub库存(pcs)	ship out
H2FR2(E5 PD)	A090AP05P-DL01	0	0	just for control run
	A090AP04P-DL01	817	0	
WRC3R(E5 PD 军规)	A090AP03P-DL01	0	0	0
	A090AP02P-DL01	1148	0	台灣和碩*960pcs(already on hold) Service*95pcs(already on hold)

2. Take the stock to do normal B/I test,

Result :PASS

B/I condition :Input voltage 220V/Full load , Tem:40±5°, B/I time:48hours

Owner: QE/Kitty, MFG/Xiaohui Implement date :12/20

3. Randomly pick 10pcs stock to do Non-operational vibration test then check the function of the product,

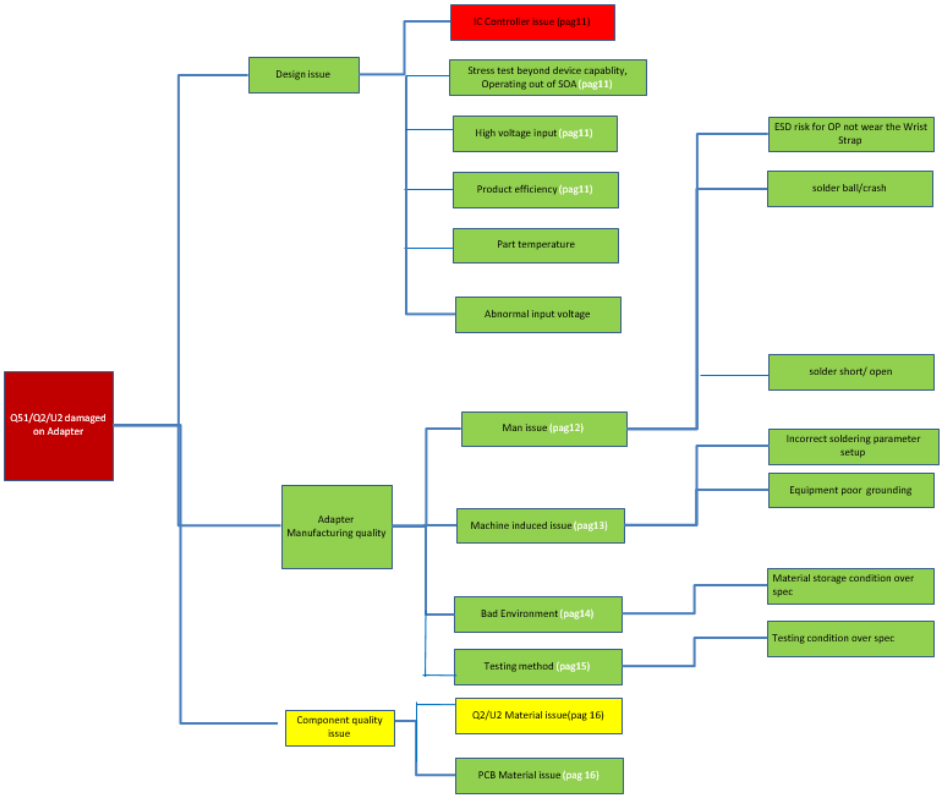
Result: PASS

Owner: DQA/Kobe, PE/Guoqian Implement date:12/21

D4.)不良原因確認: Define and Verify Root Causes:

(Note: Identify and verify all suspect causes, which needs explain why the problem occurred.**)**

Failure tree analysis :



1. By tracking the S/N through by the SFCS , these 3 samples have through all test stations and no abnormity was found.

#01 :

出貨序號 :N0H2FR2CH2001BNA0IKX03 欄寬自動調整

生產條碼	FTTL48N01900081	客戶名稱	
工單	TT2148N019	途程名稱	R-M-NODIPSN
工單類型		生產線別	STO-SHIPPING
料號	A090AP05PDL01X2	規格	
機種	A090AP05PDL01	狀態	PASS complete
版本	N/A	下道工序	
客戶序號1	CN0H2FR2CH2001BNA0IKX03	客戶序號2	

包裝作業資訊 出貨作業資訊

流程 維修 抽驗 重工 物料 錫膏 鋼板 刮刀 組裝物料

工單	料號	客戶料號	生產線別	制程	狀態
TT2148N019	A090AP05PDL01X2		NPI	ICT	OK
TT2148N019	A090AP05PDL01X2		NPI	ACT	OK
TT2148N019	A090AP05PDL01X2		NPI	ASSY	OK
TT2148N019	A090AP05PDL01X2		NPI	PRE-ATE	OK
TT2148N019	A090AP05PDL01X2		NPI	TURN ON	OK
TT2148N019	A090AP05PDL01X2		NPI	HIPOT/GROUNDING	OK
TT2148N019	A090AP05PDL01X2		NPI	FINAL-ATE	OK
TT2148N019	A090AP05PDL01X2		NPI	ICC	OK
TT2148N019	A090AP05PDL01X2		NPI	PACKING	OK
TT2148N019	A090AP05PDL01X2		NPI	QC	OK
TT2148N019	A090AP05PDL01X2		STO-SHIPPING	SHIPPING	OK

#02 :

出貨序號 :N0H2FR2CH2001BNA0IPX03 欄寬自動調整

生產條碼	FTTL48N01900115	客戶名稱	
工單	TT2148N019	途程名稱	R-M-NODIPSN
工單類型		生產線別	STO-SHIPPING
料號	A090AP05PDL01X2	規格	
機種	A090AP05PDL01	狀態	PASS complete
版本	N/A	下道工序	
客戶序號1	CN0H2FR2CH2001BNA0IPX03	客戶序號2	

包裝作業資訊 出貨作業資訊

流程 維修 抽驗 重工 物料 錫膏 鋼板 刮刀 組裝物料

工單	料號	客戶料號	生產線別	制程	狀態
TT2148N019	A090AP05PDL01X2		NPI	ICT	OK
TT2148N019	A090AP05PDL01X2		NPI	ACT	OK
TT2148N019	A090AP05PDL01X2		NPI	ASSY	OK
TT2148N019	A090AP05PDL01X2		NPI	PRE-ATE	OK
TT2148N019	A090AP05PDL01X2		NPI	TURN ON	OK
TT2148N019	A090AP05PDL01X2		NPI	HIPOT/GROUNDING	OK
TT2148N019	A090AP05PDL01X2		NPI	FINAL-ATE	OK
TT2148N019	A090AP05PDL01X2		NPI	ICC	OK
TT2148N019	A090AP05PDL01X2		NPI	PACKING	OK
TT2148N019	A090AP05PDL01X2		NPI	QC	OK
TT2148N019	A090AP05PDL01X2		STO-SHIPPING	SHIPPING	OK

#03 :

出貨序號 :N0H2FR2CH2001BN00BLX03 欄寬自動調整

生產條碼	FTTL48N01800451	客戶名稱	
工單	TT2148N018	途程名稱	R-M-NODIPSN
工單類型		生產線別	STO-SHIPPING
料號	A090AP04PDL01X2	規格	
機種	A090AP04PDL01	狀態	PASS complete
版本	N/A	下道工序	
客戶序號1	CN0H2FR2CH2001BN00BLX03	客戶序號2	

包裝作業資訊 出貨作業資訊

流程 維修 抽驗 重工 物料 錫膏 鋼板 刮刀 組裝物料

工單	料號	客戶料號	生產線別	制程	狀態
T2148N018	A090AP04PDL01X2		NPI	ICT	OK
T2148N018	A090AP04PDL01X2		NPI	ACT	OK
T2148N018	A090AP04PDL01X2		NPI	ASSY	OK
T2148N018	A090AP04PDL01X2		NPI	PRE-ATE	OK
T2148N018	A090AP04PDL01X2		NPI	TURN ON	OK
T2148N018	A090AP04PDL01X2		NPI	HIPOT/GROUNDING	OK
T2148N018	A090AP04PDL01X2		NPI	FINAL-ATE	OK
T2148N018	A090AP04PDL01X2		NPI	ICC	OK
T2148N018	A090AP04PDL01X2		NPI	PACKING	OK
T2148N018	A090AP04PDL01X2		NPI	QC	OK
T2148N018	A090AP04PDL01X2		STO-SHIPPING	SHIPPING	OK

2. Check the production record of the W/O, we total shipped 334pcs to Wistron, detail information as below:

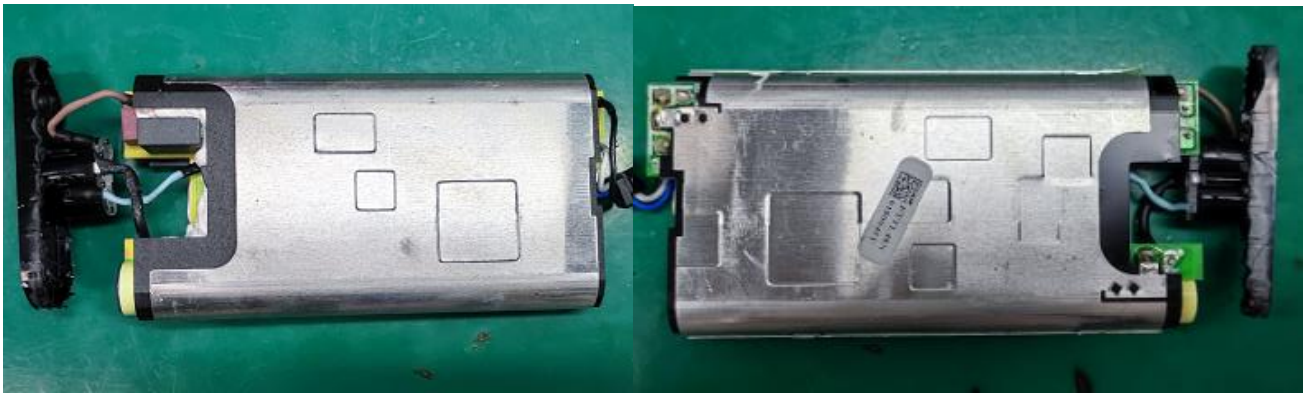
PPID	D/C	W/O	W/O Q'ty	Shipped to Wistron (Q'ty)	CPT process function failure
CN-0H2FR2-CH200-1BN-A0IK	1BN(2021/11/24)	TT2148N019	120	74	0
CN-0H2FR2-CH200-1BN-A0IP	1BN(2021/11/24)				
CN-0H2FR2-CH200-1BN-00BL	1BN(2021/11/24)	TT2148N018	530	260	0

2.Cosmetic inspection :OK

3. Turn on the adapter, all of them have no power that as same as customer feedback.(pic for reference)

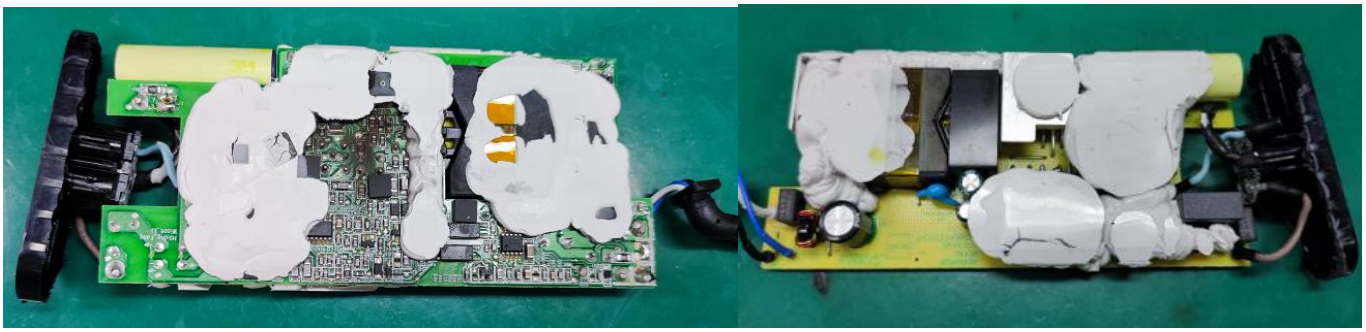
4. Open the case, also no abnormality was found.

#Top side #Bottom side

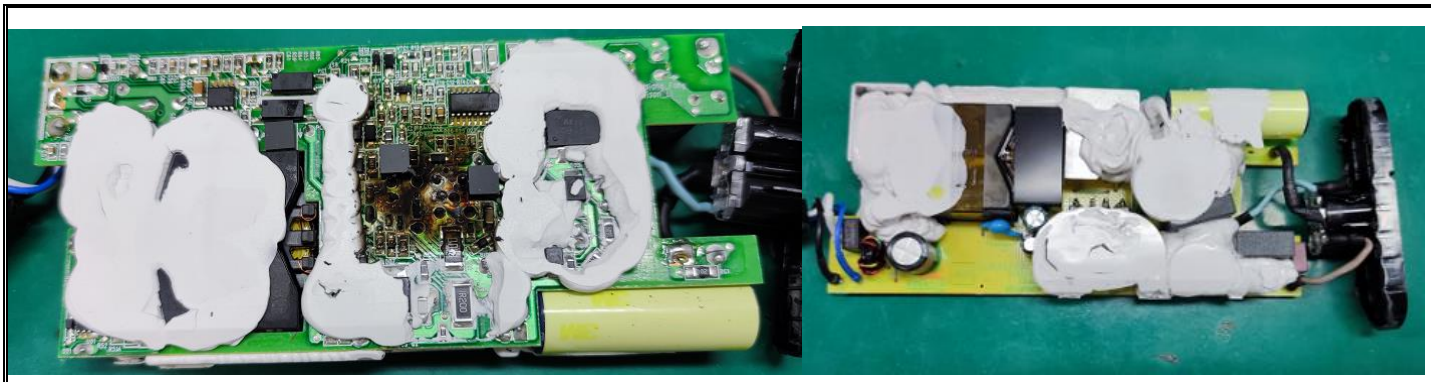


5. Remove the shielding then found the arc trace in below area.

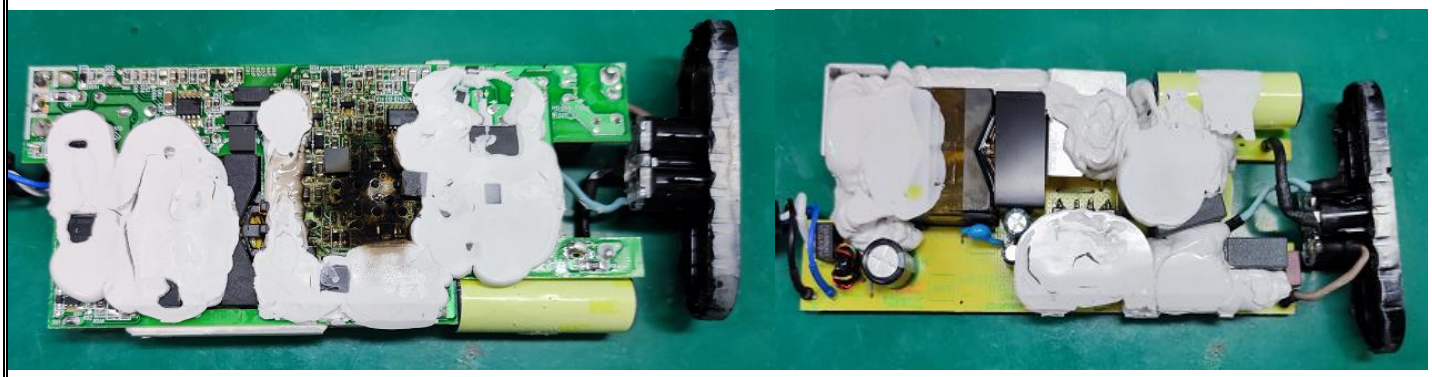
PPID:CN-0H2FR2-CH200-1BN-A0IK-X03



PPID:CN-0H2FR2-CH200-1BN-A0IP-X03



PPID: CN-0H2FR2-CH200-1BN-00BL-X03



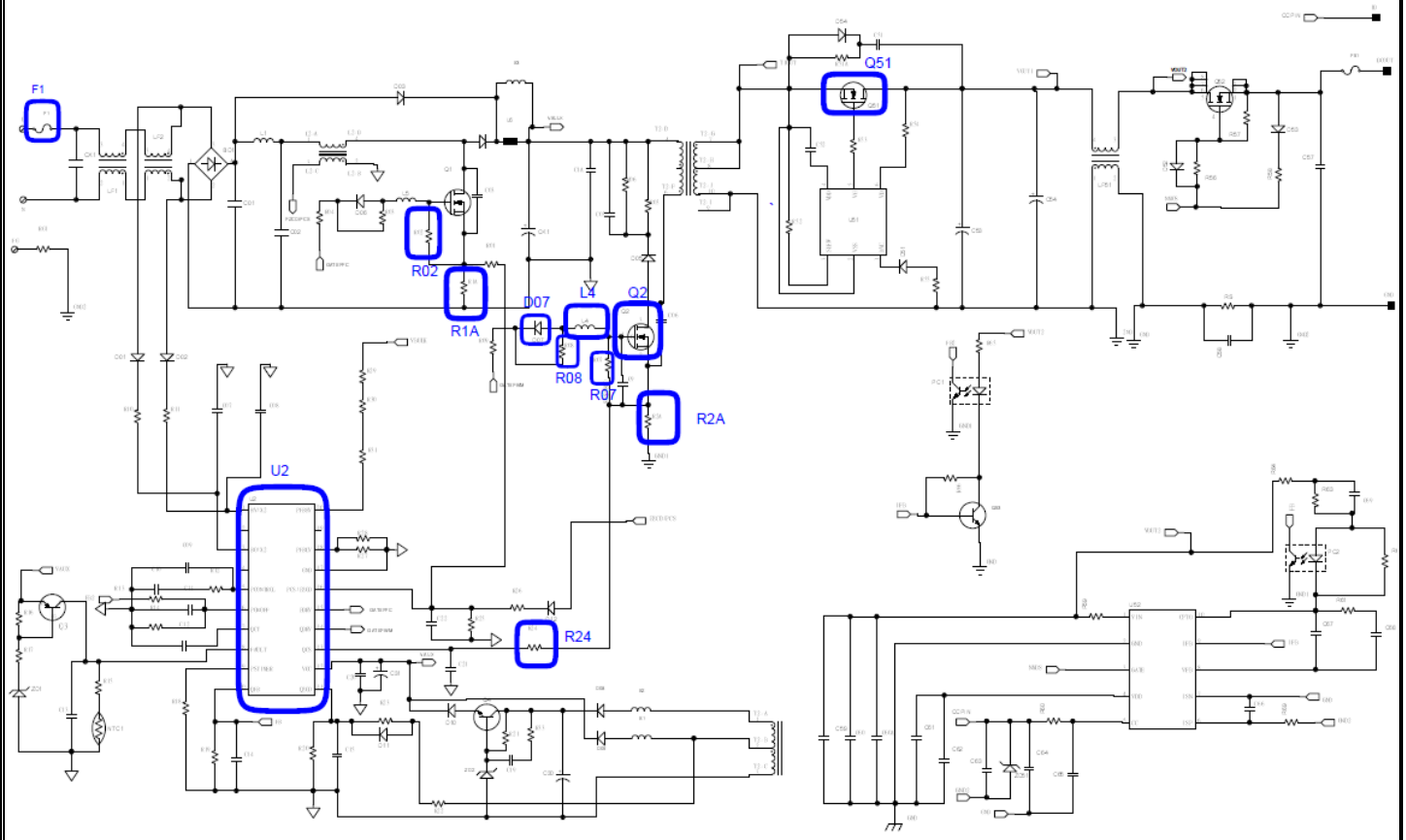
6. Measure the circuit of the key components , the result as below(note: red font =fail , green font=Good

PPID	Component loaction														
	Q2	U2	Q1	Q51	U52	BD1	R1A	R2A	R24	R07	R08	R02	D07	F1	L4
CN-0H2FR2-CH200-1BN-A0IP	short	short	short	short	short	short	open	open	open	open	open	open	open	open	OK
CN-0H2FR2-CH200-1BN-A0IK	short	short	OK	short	OK	OK	open	open	open	open	open	open	open	open	OK
CN-0H2FR2-CH200-1BN-00BL	short	short	OK	OK	OK	short	open	open	open	open	open	open	open	open	open

7. Repair the product by replacing good components then turn on the adapters , they can be power on normally.

Burn in the samples for 24hours, they are still normal.

8. Schematic:



9. Arrange onsite FAE to do more run in test at WCD and hope to find the system loading condition during the failures happened. Finally, we found when the failures occurred, the system power was 60%.

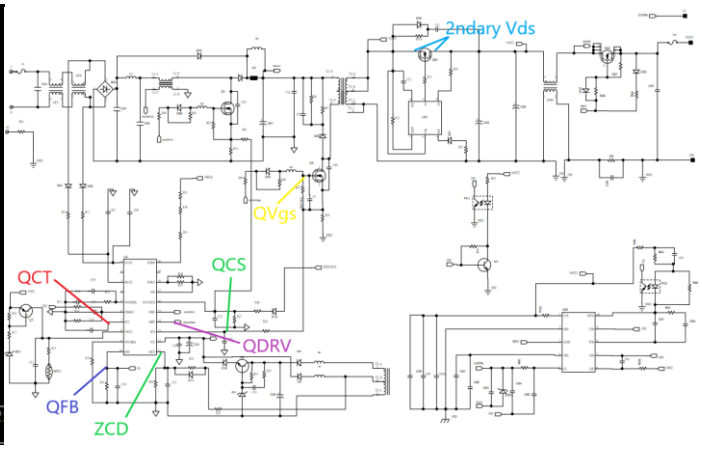
So we infer that the failure condition is product under light load and the system under standby mode.

10. Failure simulation:

Failure can be duplicated at system standby mode(dynamic load) / 220V input.

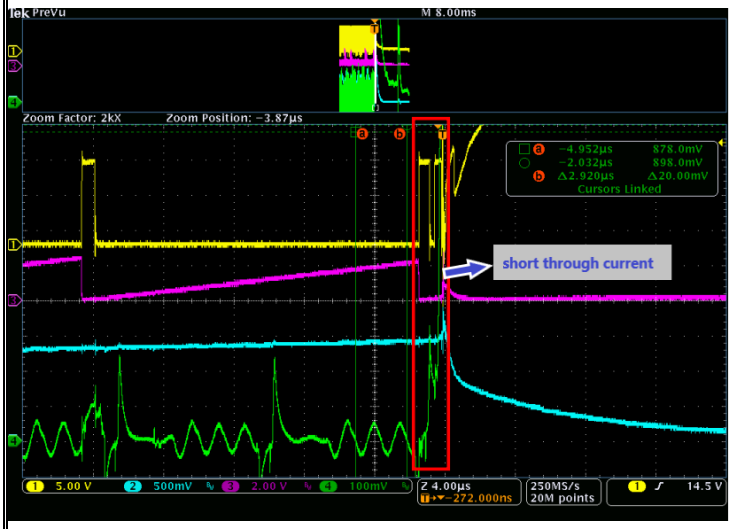
Site	Testing conditon	P/N	Result
Chicony power SZ	Dynamic load: 4A(5ms) -0.5A(150ms) E-Load slew rate: 2.5A/s Input voltage: 220V/50Hz , Tem: 40±5°	E5 PD90W*30pcs E4 90W*20pcs E5 Barrel 90W	NG*6pcs PASS PASS
Chicony power Taipei	Dynamic load:4.5A(10ms) -0.54A(150ms) E-load slew rate: 2.5A/us 220V/50Hz Tem: AMB 25°	E5 PD90W E5 Barrel 90W	Fail PASS

11. Measure the waveform when product damaged, double pulse of QDRV from PWM IC (U2) was observed.



Ch1: QVgs Ch2: 2ndary Vds Ch4: QZCD

12. The double pulse bring a short through current that causes Q2 damaged.



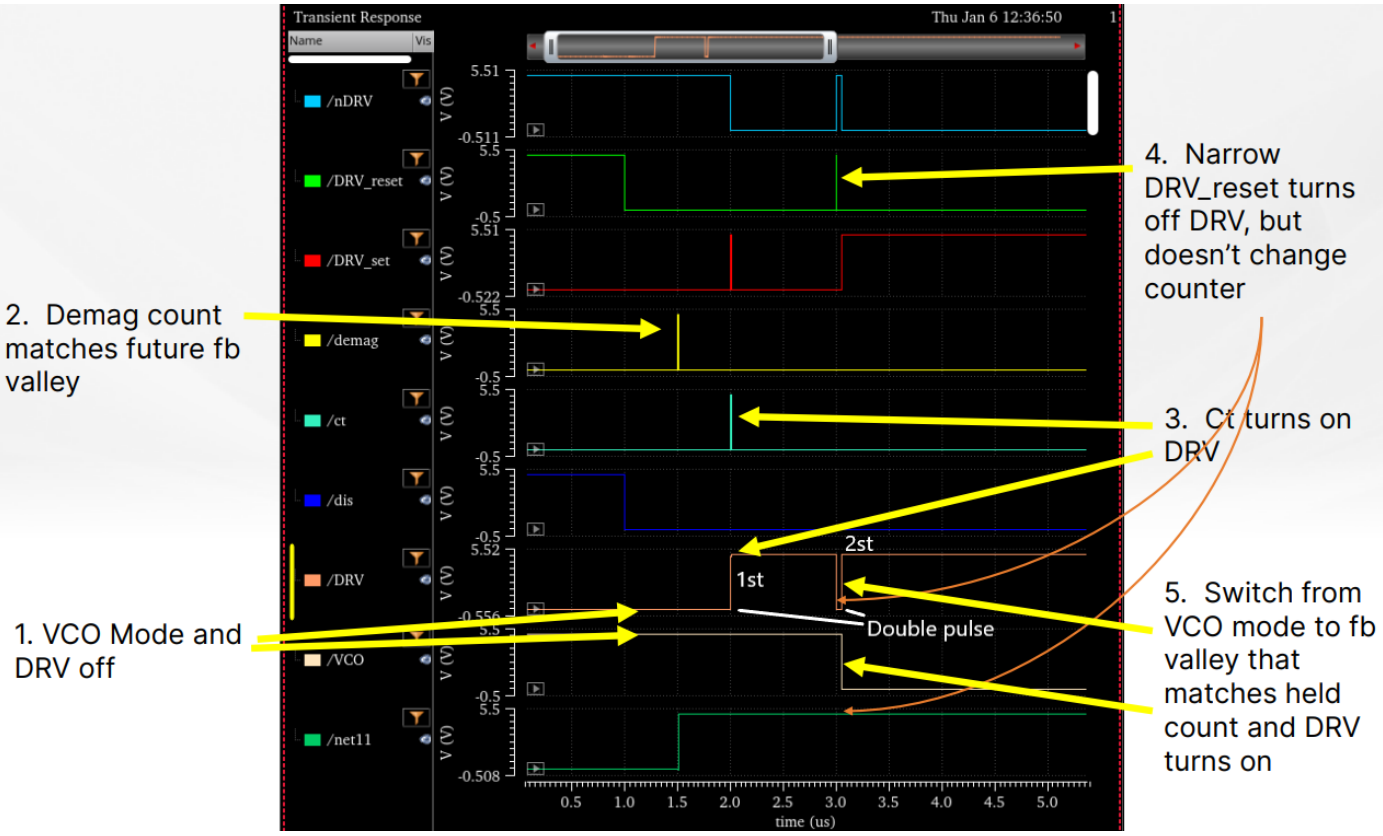
Ch1: QDRV Ch2: QFB Ch3: QCT Ch4: QCS

Root cause analysis from ON-Semi

1.Send the defective IC to On-semi for further analysis and share the double gate waveform also.

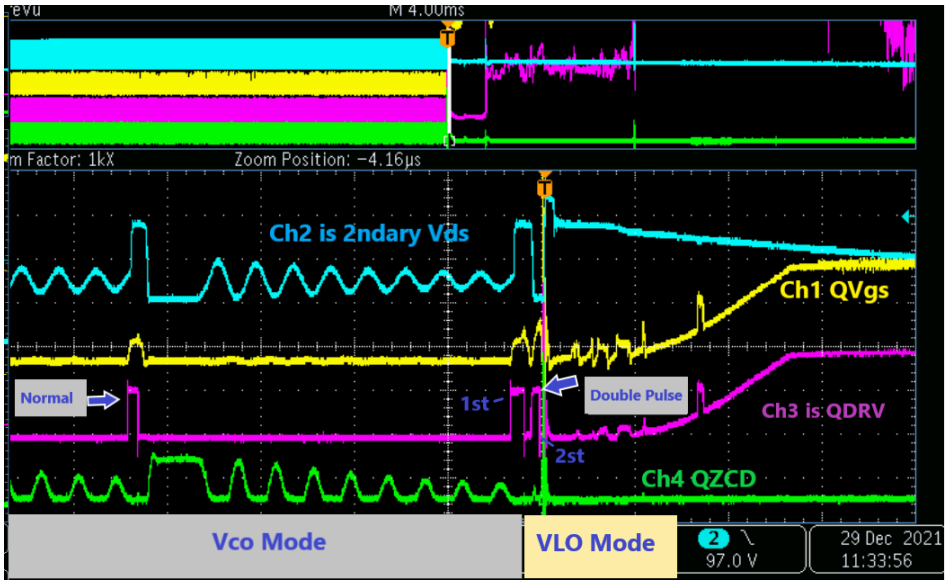
The designer found a blind duration (20ns~30ns) in counter and latch was observer after simulation

.



2. To create the double pulse issue, the condition must be met below at same time.

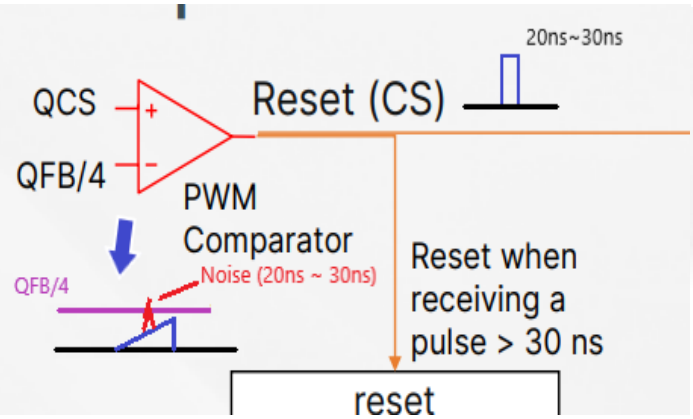
2.1 It is in VCO mode in the 1s DRV of this double QDRV.

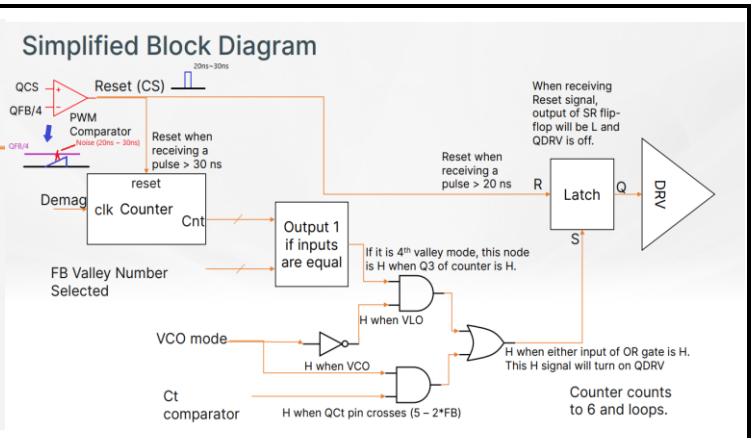


2.2 QCS glitch noise is in range from 20 to 30ns, which sums up with QR flyback's real current signal to be > FB/4 to turn off QDRV, i.e. 350-mV when FB is 1.4 V.

If the noise is shorter than 20 ns, it will NOT turn off the QDRV.

If the noise is longer than 30 ns, it will reset both QDRV and valley counter.



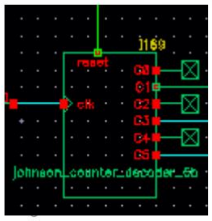


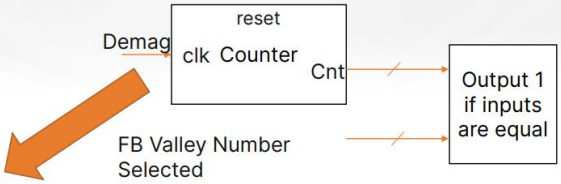
2.3 Previous drive turn on occurred on the 4th or 10th valley. Qct should be designed to transition from above 4th valley and below 10th valley when transitioning from VCO to VLO. (Note: ZCD noise can cause false or miss trips of valley counter and we can see the ZCD have noise coupling from PFC)

2.4 Transition to VLO from VCO after 1st drive turn off.

Explanation for the counter

- Left side block has counter (or called multiplexer) to count how many valleys is detected.
  - In NCP1937, this multiplexer has 6 outputs, Q0 ~ Q5, as shown in below.
- Right side block is like an AND gate, which inputs are output of counter and valley number selected signal.
  - In the 4th valley lockout mode, this right side block is H when Q3 of multiplexer is H.
  - In the 3rd valley lockout mode, this right side block is H when Q2 of multiplexer is H.
  - In the 2nd valley lockout mode, this right side block is H when Q1 of multiplexer is H.
  - In the 1st valley lockout mode, this right side block is H when Q0 of multiplexer is H.





Valley Thresholds		10					V
Transition from 1st to 2nd valley	V_{QFB} decreasing		V_{H2D}	1.316	1.400	1.484	
Transition from 2nd to 3rd valley	V_{QFB} decreasing		V_{H3D}	1.128	1.200	1.272	
Transition from 3rd to 4th valley	V_{QFB} decreasing		V_{H4D}	0.846	0.900	0.954	
Transition from 4th valley to VCO	V_{QFB} decreasing		V_{HVCOD}	0.752	0.800	0.848	
Transition from VCO to 4th valley	V_{QFB} increasing		V_{HVCOI}	1.316	1.400	1.484	
Transition from 4th to 3rd valley	V_{QFB} increasing		V_{H4I}	1.504	1.600	1.696	
Transition from 3rd to 2nd valley	V_{QFB} increasing		V_{H3I}	1.692	1.800	1.908	
Transition from 2nd to 1st valley	V_{QFB} increasing		V_{H2I}	1.880	2.000	2.120	

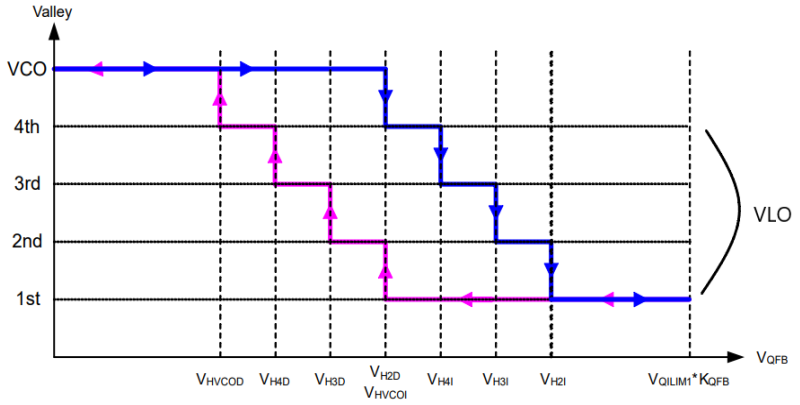
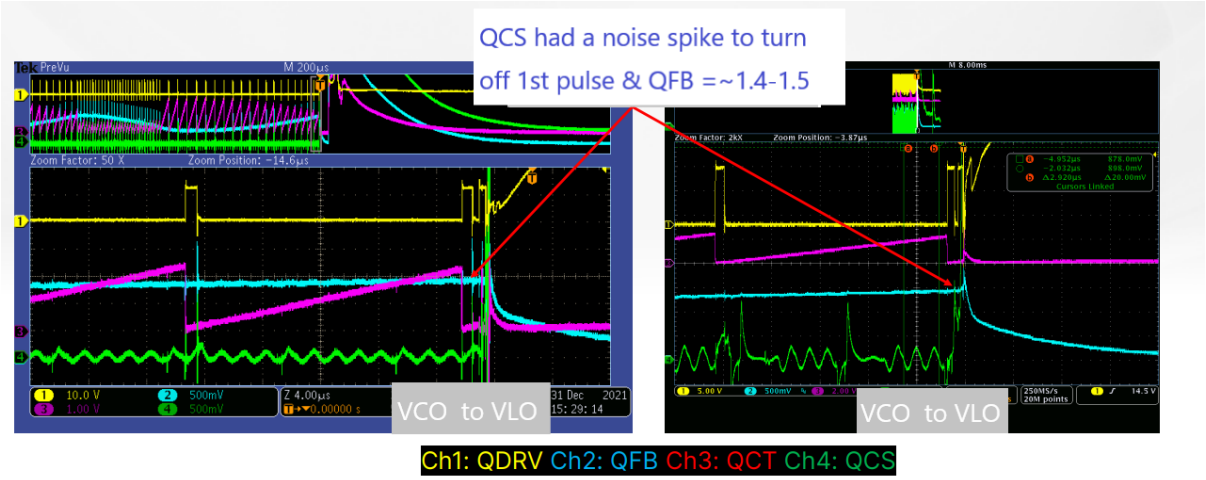
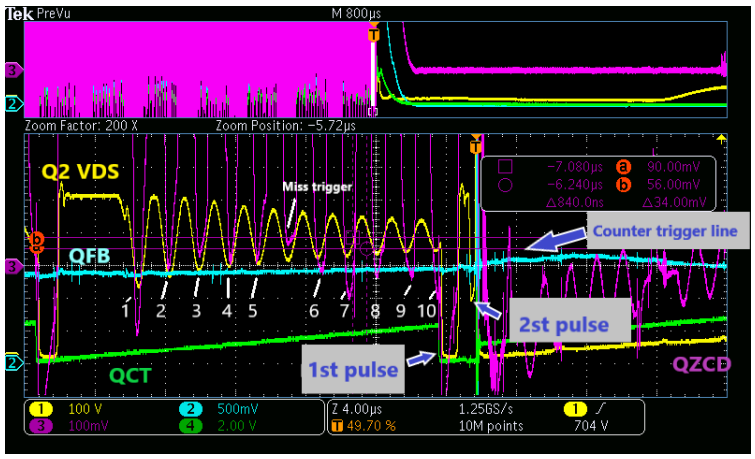


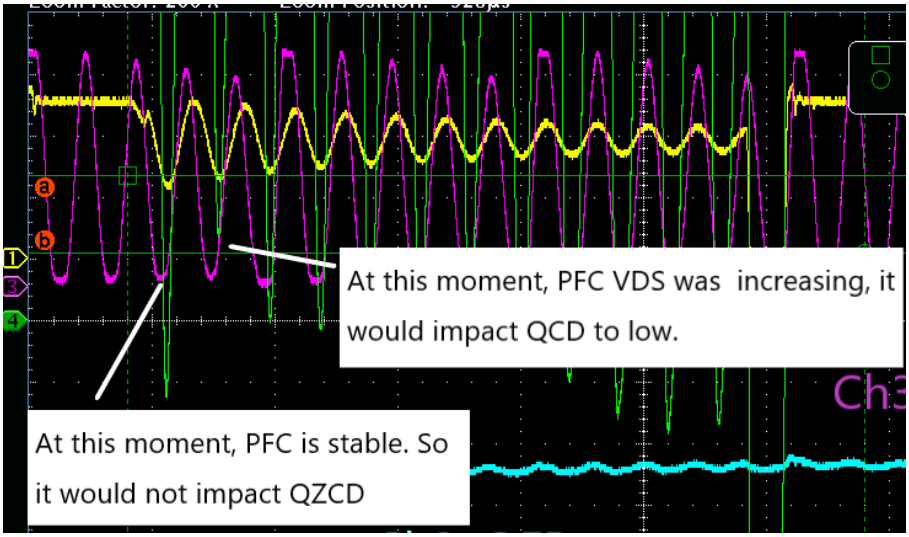
Figure 14. Selected Operating Valley vs. V_{QFB}

3. Compared fail waveform of Chicony, they all met above 4 criteria. (1. In VCO mode at 1st pulse. 2. Qcs had a noise (20ns-30ns) to turn off QDRV. 3. The counted number is 10. 4. The FB is 1.4-1.5V)



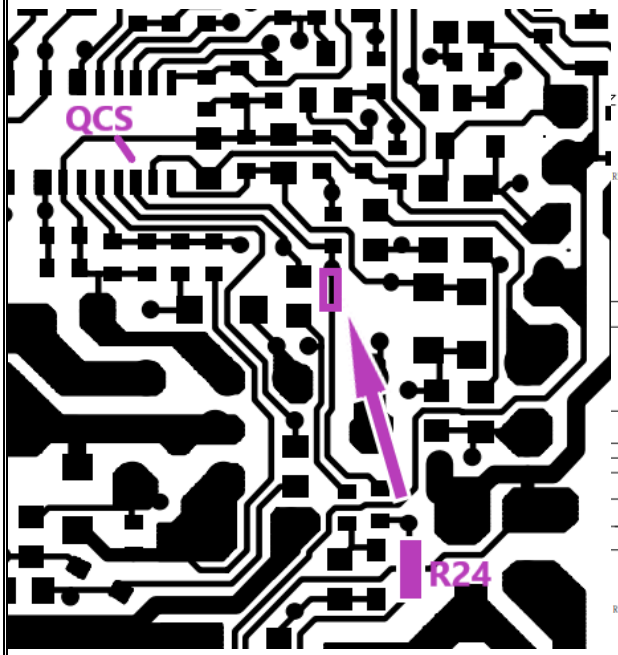


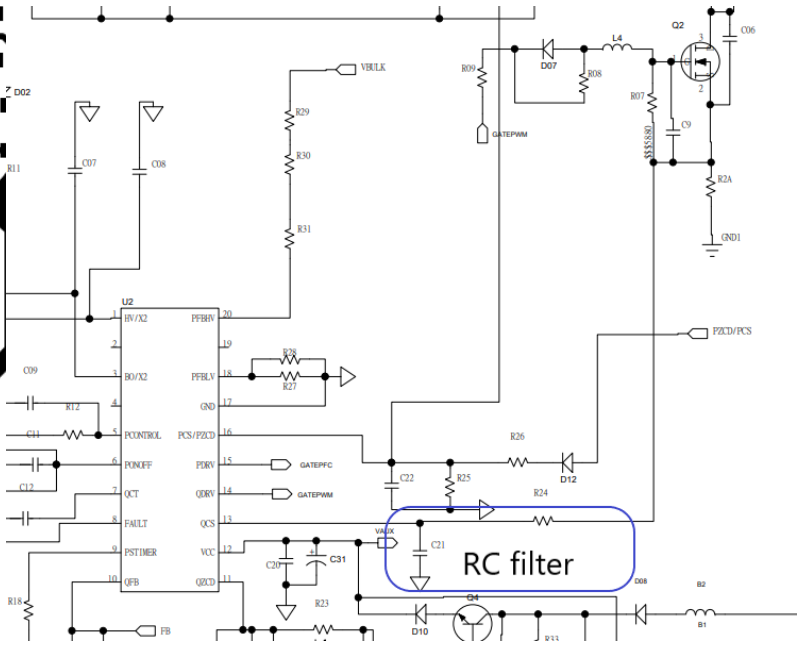
4. The miss trigged analysis: PFC VDS ring would cause ZCD miss trigged.



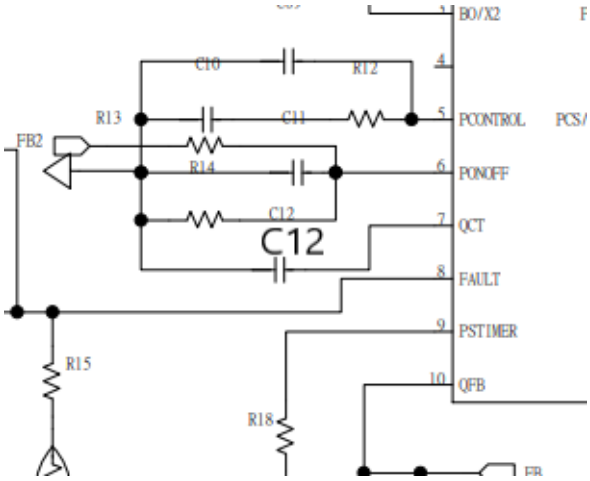
Root cause verification:

- ✓ **Improved RC filter loop to improve noise coupling of QCS**
- **CPT reworked 20pcs finished goods by replacing R24 as below layout drawing and do burn in 48 hours with dynamic load. All sample are pass the burn in test.**





- ✓ **Failure rate deterioration:**
- **CPT reworked 20pcs finished goods by replacing C12 from 150pF to 197pF (150pF + 47pF). To increase chance of counter at 10 and do burn in 48 hours test with dynamic load. All samples are damaged within 24hours.**

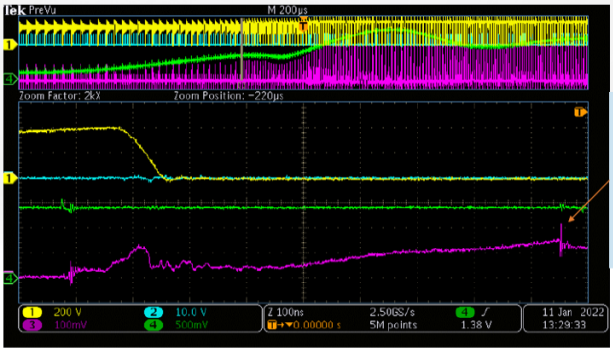


- ✓ **Waveform comparison between E5 PD 90W and E5 Non-PD 90W model, the waveform of non-PD model is cleaner than PD model that's why E4 90W can pass the test.**

Chicony 90W PD – QCS spike

Ch1 Vds Ch2 is PDRV Ch3 is QCS Ch4 is QFB

Chicony 90W non PD – QCS spike



Ch1 Vds Ch2 is PDRV Ch3 is QCS Ch4 is QFB

Conclusion:

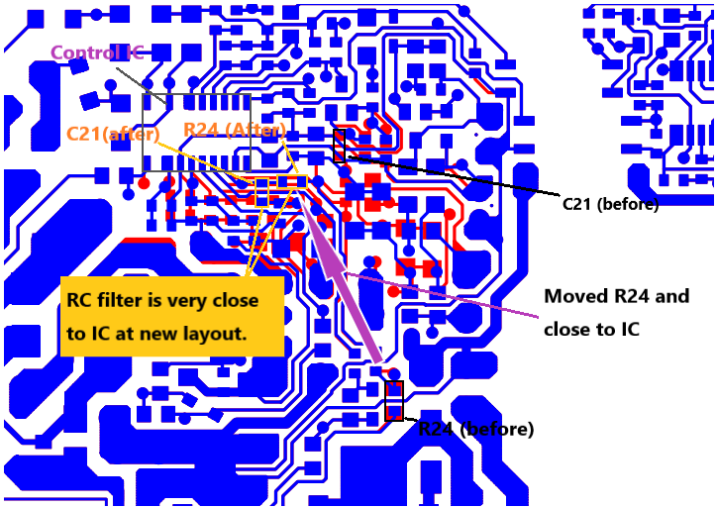
The noise spike(20ns~30ns) on QCS pin and IC blind duration that cause the double pulse issue happened, then bring a short through current that led Q2 damaged, finally cause the adapter damaged.

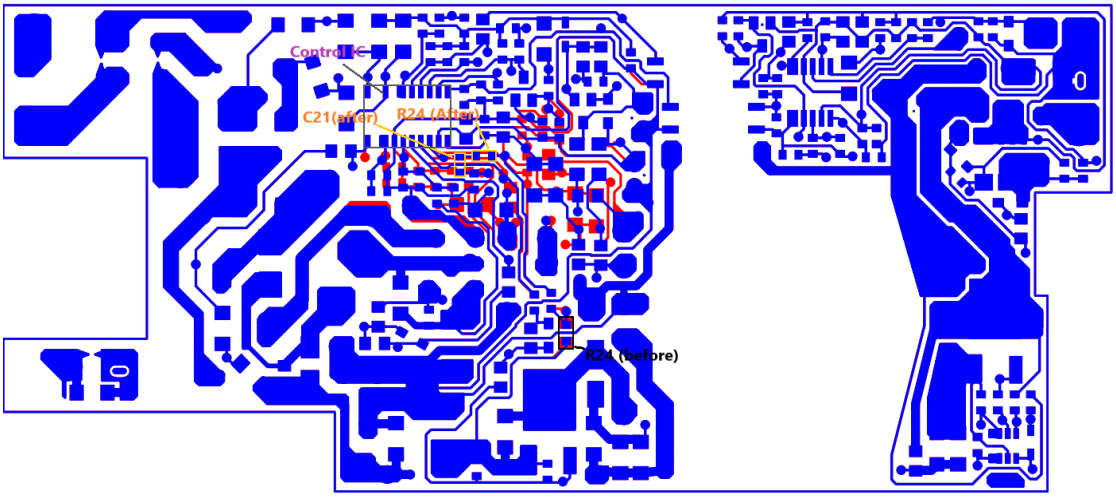
D5.)改善措施:Corrective Action Verification:

(Note: Be make sure the corrective actions is effective in process as well as able to fix the customer complaint problem**)**

Modified the layout to reduce noise coupling issue and new layout is as follow.

Comparison of SMD side (Red =before, Blue=after)





D6.)改善措施實施日期:Implement Permanent Corrective Actions:

(Note: Be provide the phase-in date or lot# of corrective actions **implementation** in process**)**

Cut in schedule please refer to below, adapter cut in revision:X04

Pre-build in Taipei			
Layout	2022/1/12	2022/1/13	
Gerber out	2022/1/13	2022/1/14	
PCB ready	2022/1/17	2022/1/18	
SMD-5pcs for RD pre-test	2022/1/19	2022/1/19	
IC Waveform Measurement	2022/1/20	2022/1/20	
Waveform data review	2022/1/21	2022/1/21	
Material Preparation	2022/1/17	2022/1/24	
Pre-Build	2022/1/25	2022/1/26	
RD debug and verification	2022/1/27	2022/2/9	1/29-2/6 CNY
DVT			
Safety Application - BIS update & other	2022/2/10	2022/4/18	Using Pre-Build samples
BOM update, PCB/Material/Jigs preparation	2022/2/10	2022/2/28	
DVT build	2022/3/1	2022/3/7	
Sample ETA	2022/3/8	2022/3/14	
DQA/Halt test	2022/3/22	2022/4/13	
DVT Phase gate	2022/4/20	2022/4/20	
PVT			
A rev. BOM update, PCB/Material/Jigs preparation	2022/4/20	2022/5/9	
PVT build	2022/5/10	2022/5/17	Audit
PVT Sample ETA	2022/5/18	2022/5/24	
MP			
MP build	2022/5/31		

D7.)預防再發生措施:Prevent Recurrence:

(Note: Modified the management, operating systems, practices, and procedures to prevent recurrence for the problems as well as lessons learned cases**.)**

From this event, we can find two issue in layout and IC waveform review.

- **The layout Process didn't ask RD or IC vendor to provide layout guidance to layout engineer for reference.**
- **At IC waveform review, the engineer hasn't enough experience to find coupling noise may cause potential risk.**

Form059 - Lesson Learned applicatic

Layout engineer must ask RD or IC vender to provide layout guidance, and follow IC layout guidance to do PCB layout. Sometimes layout engineer can't meet layout guidance by single layer PCB or other reasons. We can use IC waveform check to confirm the layout is ok or not.
If adapter has using two convertors (ex: PFC + Flyback), RD must consider coupling noise and confirm each Pin's waveform with IC vender and review it.

D8.)確認並感謝問題解決成員:Check and Congratulate the Team:
(Note: Recognize the collective efforts of the team.**)**

Thanks to you all！

RD:Hunter/Benson
PE: Guoqian
IPQC/QE:Chase Cai
MFG: Xiaohui
IE: Yansong
Sales: Steve

Signature **Team Leader**:	**Cf_Liu**
	Name – Title
Signature by Approver:	
	Name-Title