Eight Discipline Report (8D Report)

To: **Dell**	8D report No.: **XXXXXX**
From:：**Chicony Power Technology**	RMA claim No.: **N/A**
CC： Compal	Chicony Power P/N: **A100AP16P**
	Customer P/N:**GY21C**
Submit date: **2023/12/25**	Product description: **Dell Dark Star 100W**
Receive date: **2023/11/17**	
Subject：ESD Test No Output Power *1pcs	

D1.) 問題解決成員:Use Team Approach

主持者 (Team Leader)：**Benson_Chen**

內部成員 (Internal Team Members):

CQS: Candy_Zhu

QRA: Kitty Zhang

PM: Camp_Ku

Sales: Steve_Kuo

RD: Connie_Chen

外部成員 (External Team Member):

Supplier: OB

D2.)問題說明:Problem Description:

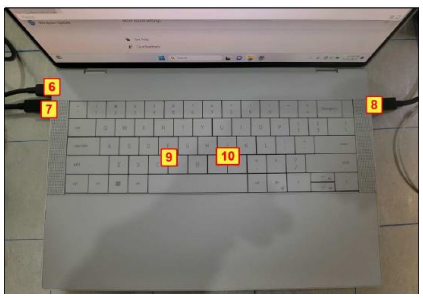
(**Note**: Use **who**, **what**, **when**, **where**, **why**, **how**, **how many** to specify the Customer's problem.)

Time: 2023/11/17

Location: TPE 3rd party lab on 11/17.

PPID: CN0GY21CCH2003AC300KX03)

Compal has feedback that Pista PVT validation with OB PD IC adapter air ESD test is fail at 8KV at point 3 & 6 (230VAC / 50Hz) with 100% failure rate



D3.)內部或客戶的暫時解決辦法及實施日期:Implement and Verify Containment Action:

(Note: Internal / external containment action effectiveness and date.**)**

1. **Compal return this sample for further analysis.**
2. **Check stock and check shopfloor**

Date:2023/11/17

D4.)不良原因確認: Define and Verify Root Causes:

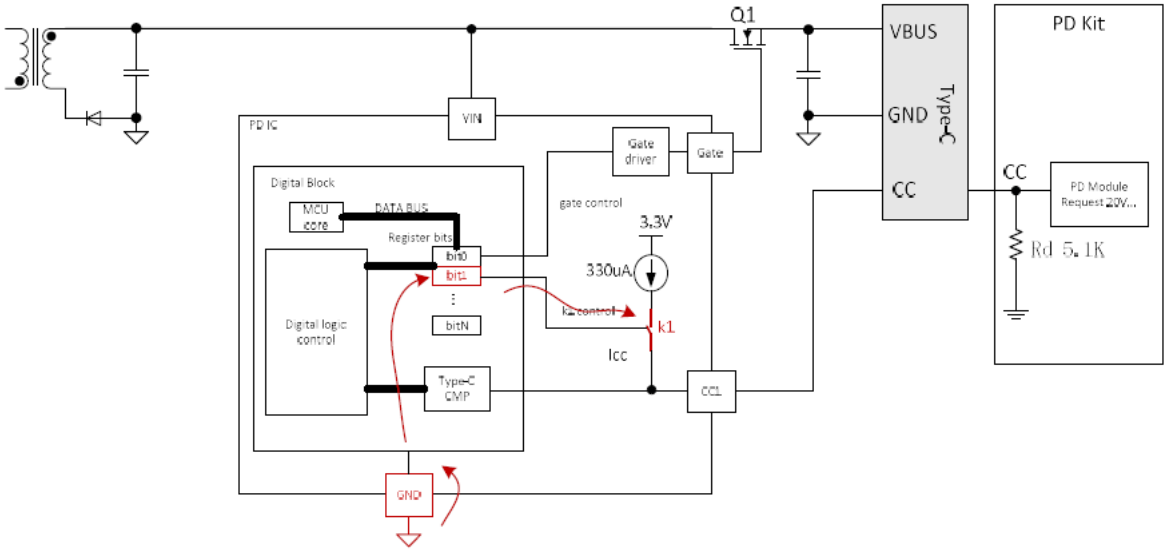
(Note: Identify and verify all suspect causes, which needs explain why the problem occurred.**)**

- **By tracking the PPID in our factory, this adapter passed all the test stations in the production line and no repair record.**
- **Reconfirm this adapter, it's latch of ESD test as same as customer's feedback.**
- **DC latch has been confirmed, but adapter cannot release latch by unplug the DC plug.**

  (If it is primary side latch there is no sound heard and no 5V output voltage on blocking MOSFET, but it has been confirmed that both behavior observed thus it is not AC latch.)
- **Since blocking MOS cannot be turned on, so the PD IC has abnormal**
- **The function related pin, VDD, VCC, CC, has been checked and there is only CC pin voltage is abnormal which is 0V.**
- **Through the IC circuit diagram, the CC pin voltage is controlled by bit1. The bit1 is abnormal checked by data log.**

➢ Conclusion:

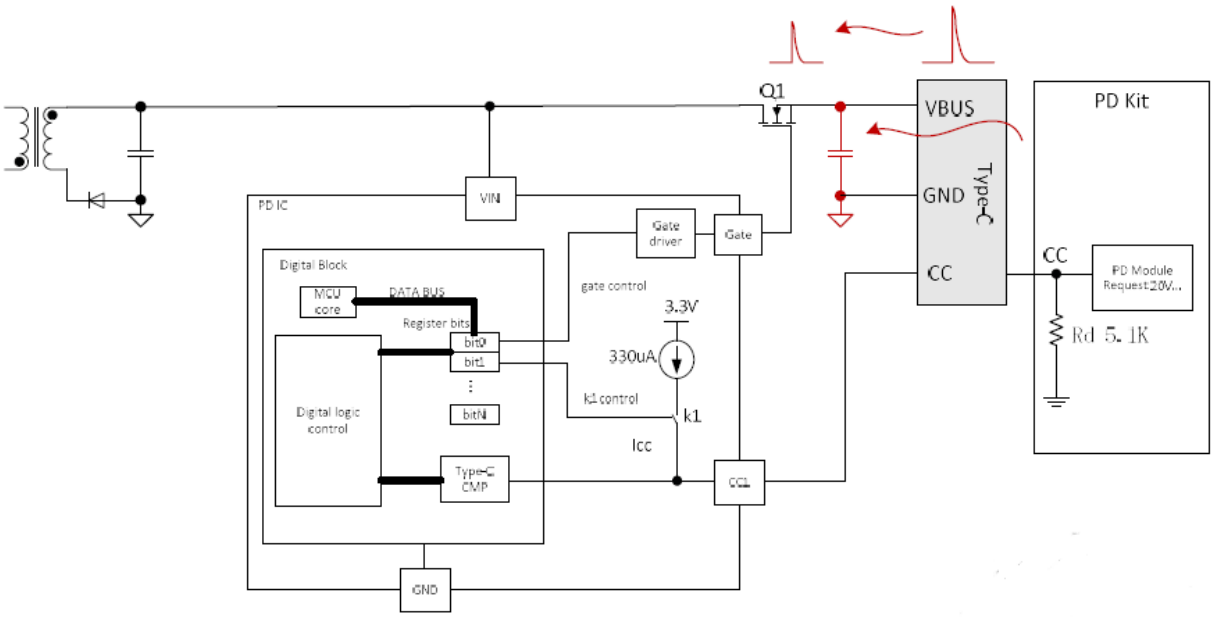
The PD IC has been interfered by ESD energy through the ground loop during the test.



D5.)改善措施:Corrective Action Verification:

(Note: Be make sure the corrective actions is effective in process as well as able to fix the customer complaint problem**)**

Increasing capacitance of C62 to 1uF to improve the capability of anti-interference.



Test ESD 16.5kV Pass

Date:2018/05/02

D6.)改善措施實施日期:Implement Permanent Corrective Actions:

(Note: Be provide the phase-in date or lot# of corrective actions **implementation** in process**)**

immediately
D7.)預防再發生措施:Prevent Recurrence: **(Note:** Modified the management, operating systems, practices, and procedures to prevent recurrence for the problems as well as lessons learned cases**.)**
Same as D5
D8.)確認並感謝問題解決成員:Check and Congratulate the Team: **(Note:** Recognize the collective efforts of the team.**)**
Thanks to you all！！！ **CQS: Candy_Zhu QE: Kitty Zhang Sales: Steve_Kuo RD: Connie_Chen PM: Camp_Ku**

Signature **Team Leader**:	**Benson_Chen**
	Name – Title
Signature by Approver:	**Hunter_Peng**