

July 30, 2025

Page 1 of 4

KPLUG I Kit  
(C) Diana Kamecki 2025  
Multiple uP Frame Board

(280, 6502, 65816, 68K P8)

- 4 I/O Ports

- o 2 x 8 bit <sup>Input</sup> Output Bi-D

- o 1 x 8 bit Output

- o 1 x 4 bit <sup>Output</sup> ~~Bi-D~~ I/O

- o 1 x 4 bit Input

- Supports W29 Rkm

2864 Eram

- Address Code Display

A0-7

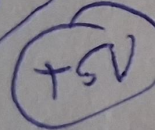
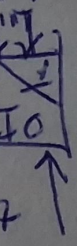
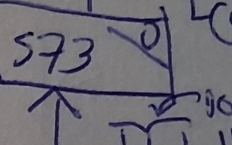
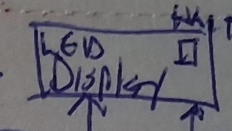
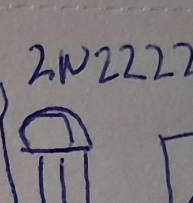
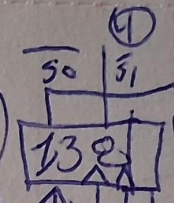
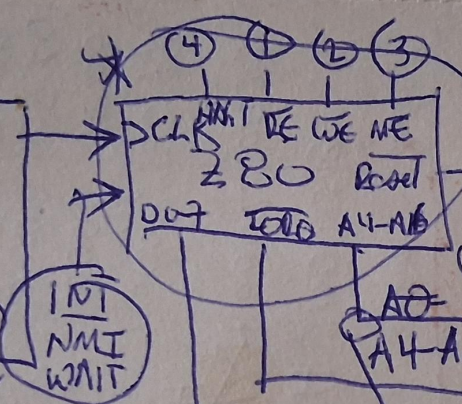


```

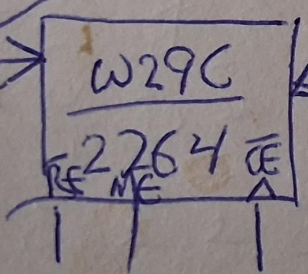
ORG 0000H
LD A, 00H
BD C, 00H
S1:
OUT(C), A
INC A
JMP S1
END

```

Chk  
Sel  
Burl



D0-D7



```

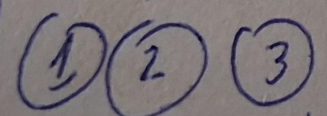
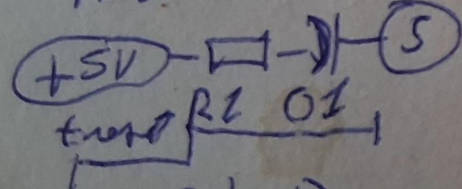
ORG 0000H
LD A, 00H
BD C, 00H
S2: OUT(C), A
INC A
JMP S2
END

```

2N2222

A0-A1

\* Plugable  
Program Mem



```

S2: OUT(C), A
INC A
JMP S2
END

```

S0	P0
0	1
1	0

(C) Diana Kandali 2025  
multimodule up

KPhusT  
Frame Boost

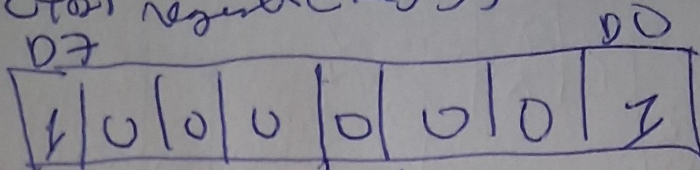
July 30, 2025

Page 24/4

202



Control register (Reg 3)



Port A, B output

Port C, D0-D3, input

Port C, D4-D7, output

A7-A4 A3-A0  
Dev Res

## Test Pgm 2

L1:

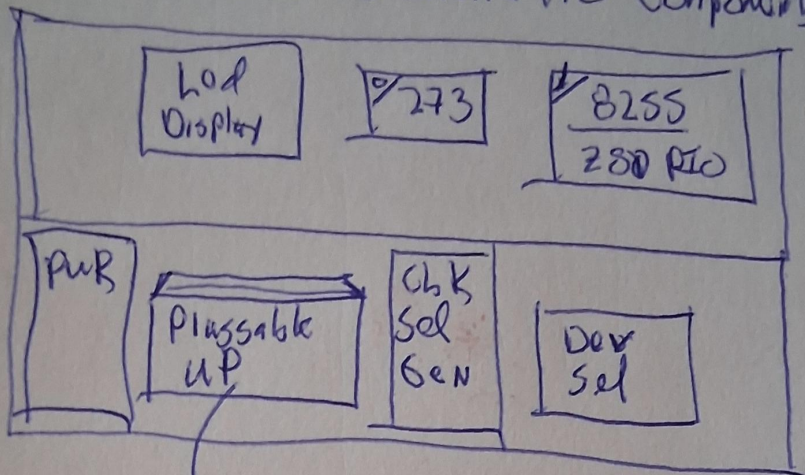
```

ORG 0000
LD A, 081H
LD C, 01110113H
OUT(C), A
LD A, 00H
LD C, 10H
OUT(C), A
INC A
JMP L1
END
    
```

Mem	Date
0000	3E 00
0002	0E 13
0004	ED 79
0006	3E 00
0008	0E 10
000A	ED 79
000C	3C
000D	C3 0000
000F	



July 30, 2025 Page 4 of 4 203  
KPKUG I Schematic Components



\*(250/6502/65816/68K P8)

(C) Diana Karedli 2025  
All Rights Reserved

Test Pgm I	Mem	Date
ORG 0000H		
LD A, 00H	0000	3E 00
LD C, 00H	0002	0E 00
S1: OUT (C), A	0004	ED 77 79
INC A	0006	3C
JMP S1	0007	C3 00 00
GND	000A	

Diana Karedli 2025 All Rights Reserved (C)