Diana Sanchez
1/27/23
53965594

Report – PCB Lab

In this lab, our goal was to learn how to use Altium Designer by creating a schematic and designing a PCB based on the circuit we were assigned to. Through this assignment, we learned how to install libraries that include our primary components, generate the PCB using the footprints of the components, define the board shape on the keep-out layer, place copper on the board using polygon pours, and generate the proper drill files.

Design

The circuit that was assigned to me was the PLL Ultrasonic Generator, shown in Figure 1.

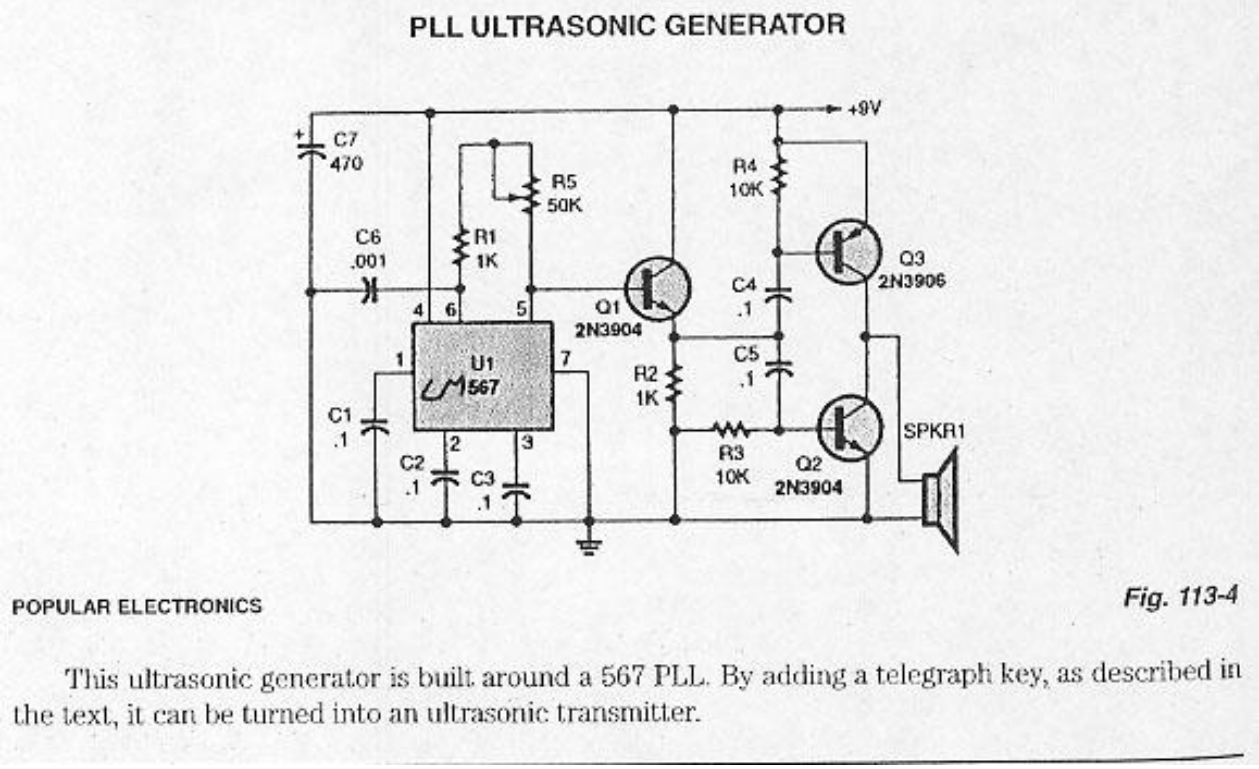

Figure 1 PLL Ultrasonic Generator circuit schematic

To make the Altium schematic, I imported the libraries provided and connected the components accordingly. Since the libraries didn't have the tone decode (LM567), I downloaded a library with the part and its footprints. I included a 2-pin header for the VCC and GND connections. I also included 4 mounting holes for the PCB.

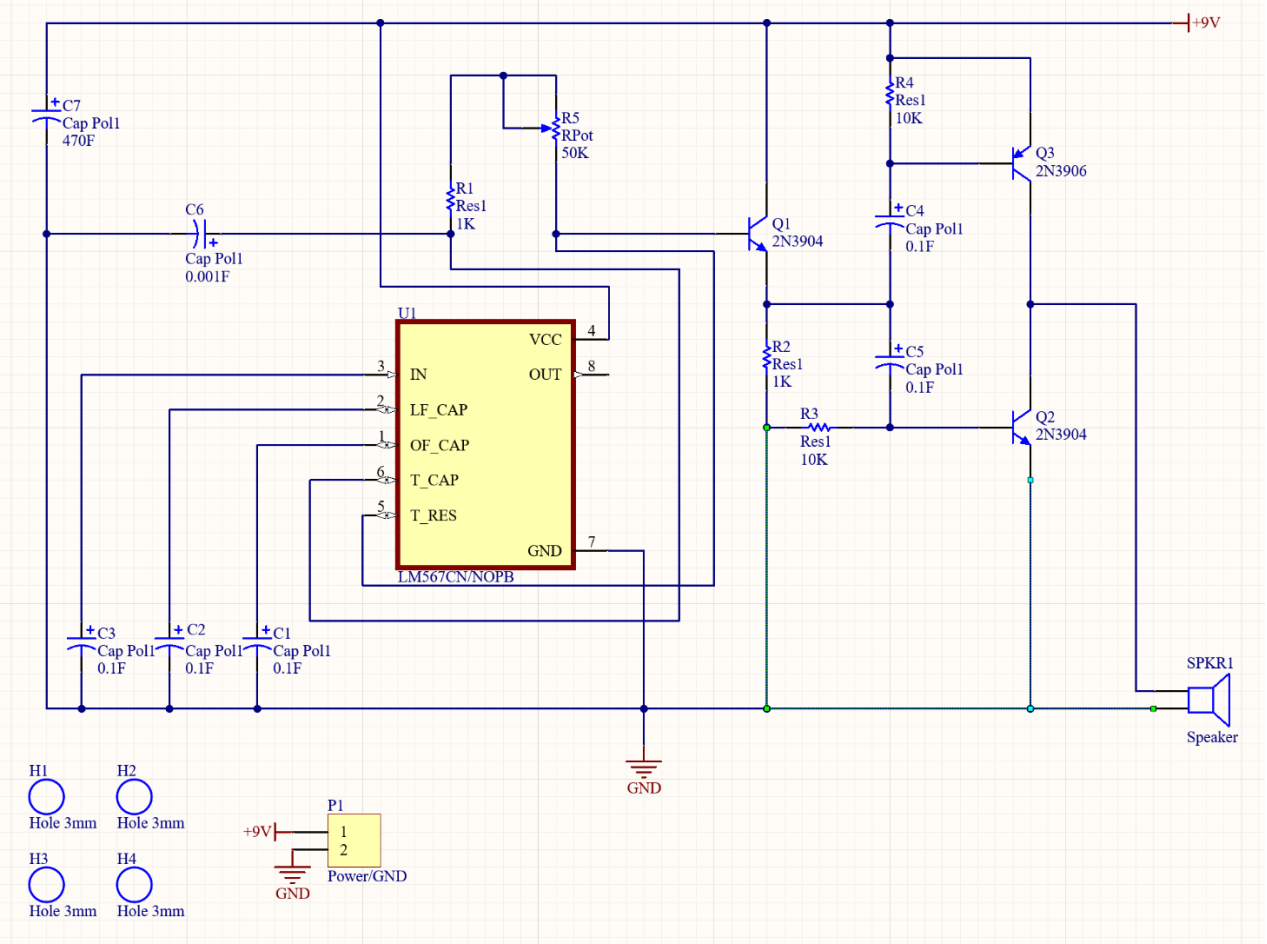

Figure 2. Altium schematic

In order to generate the PCB using the schematic, I validated and executed the changes into the PCB document and organized the parts in one section. Originally, the footprints for the capacitors took up a lot of space on the PCB design since they were large circles, so I changed their footprints to a rad-0.3 for a cleaner layout. I created an outline around the board in the Keep-Out Layer to redefine the board shape. To create the routes between the components, I used auto-route.

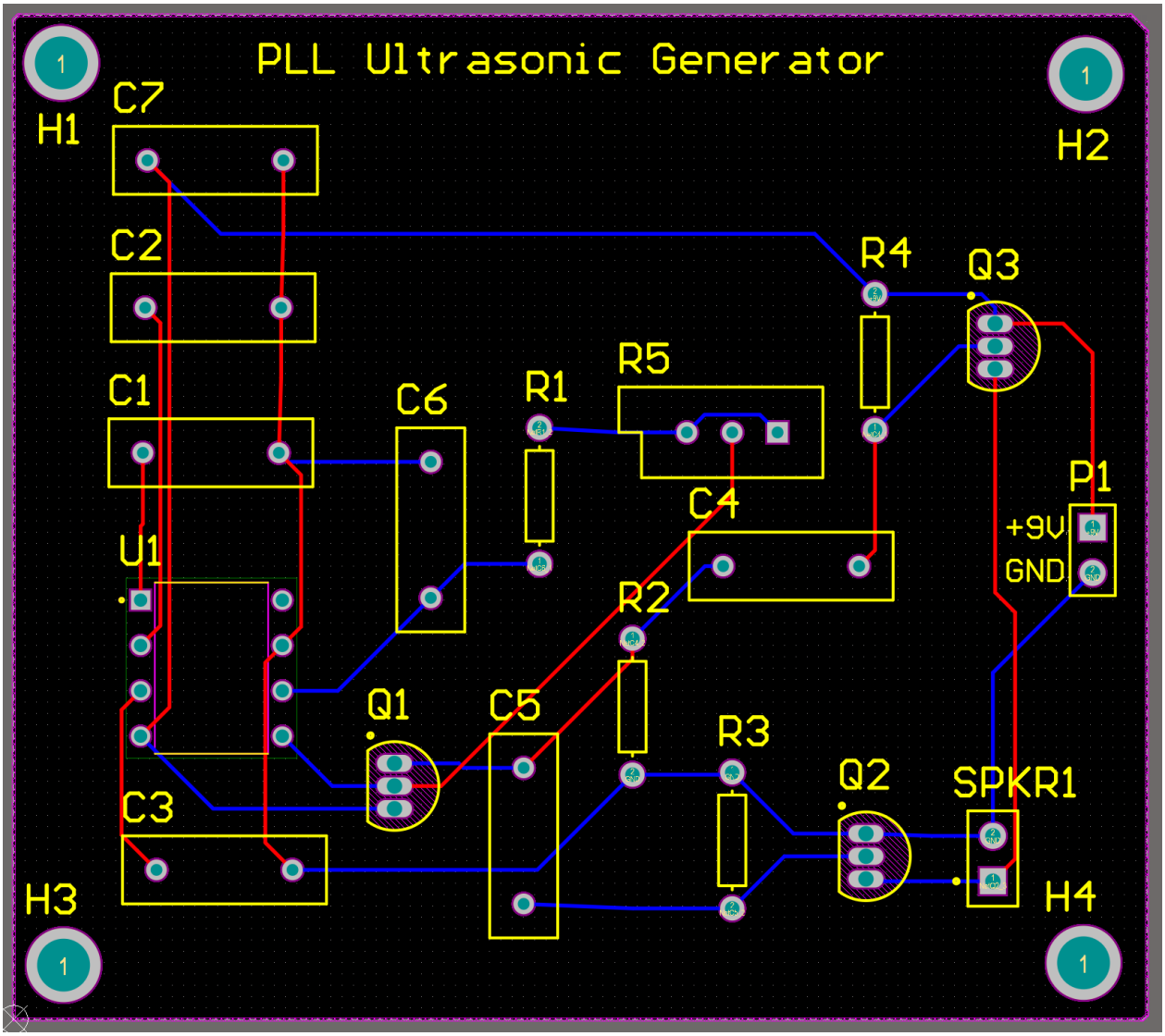

Figure 3. PCB layout

I placed a hatched polygon pour connected to +9V on the top layer (Figure 4) and another one connected to GND in the bottom layer (Figure 5).

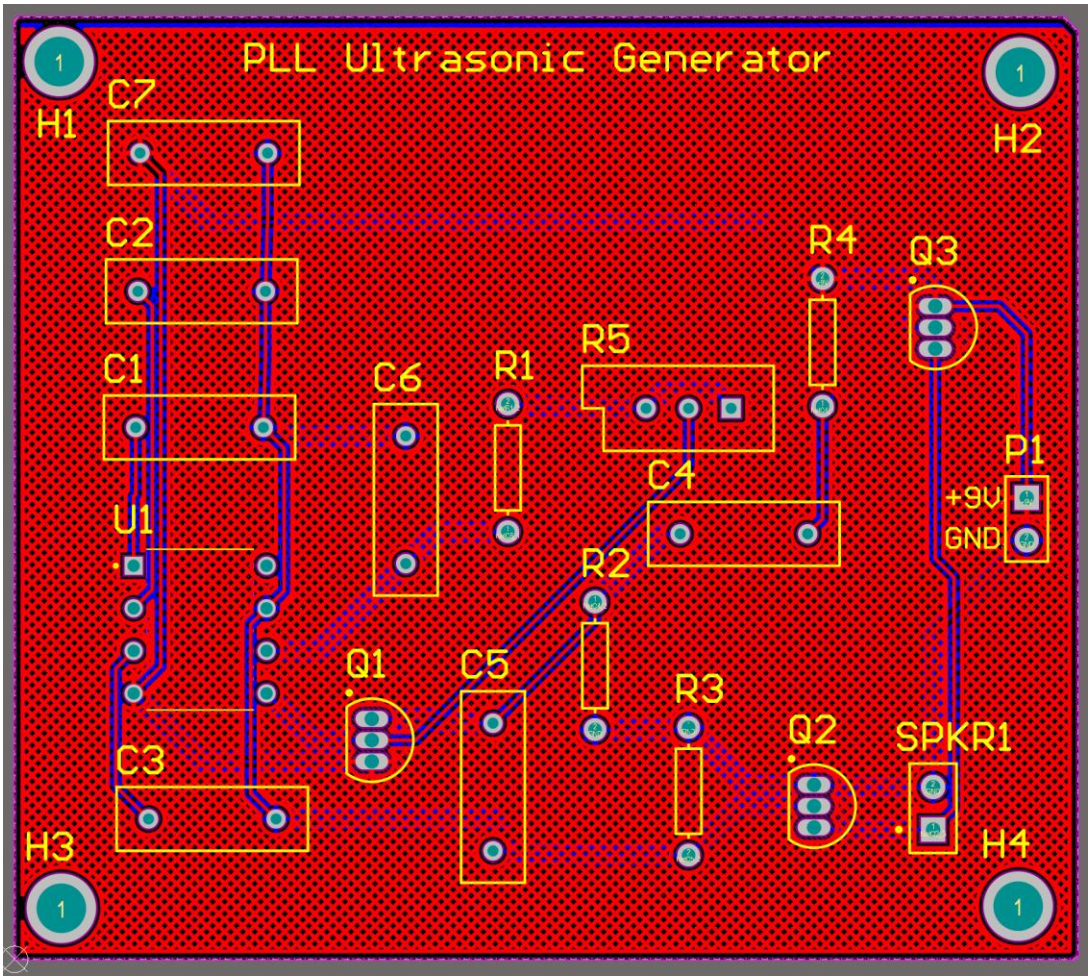

Figure 4. Top-Layer polygon pour connected to +9V

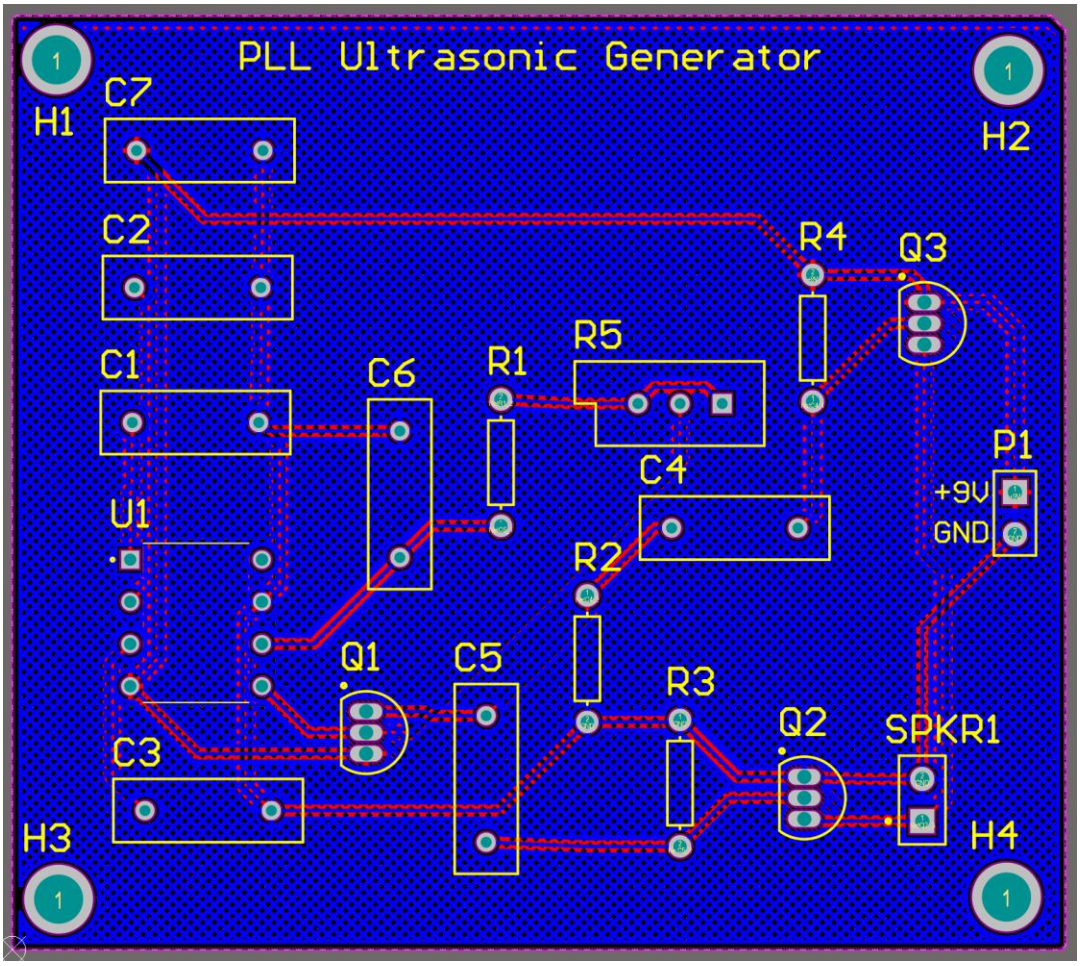

Figure 5. Bottom-Layer polygon pour connected to GND

To create the drill files, I used File-> Fabrication Outputs -> Gerber files and selected the plot layers that were used. I also selected NC Drill files to generate the binary drill file (.DRL).

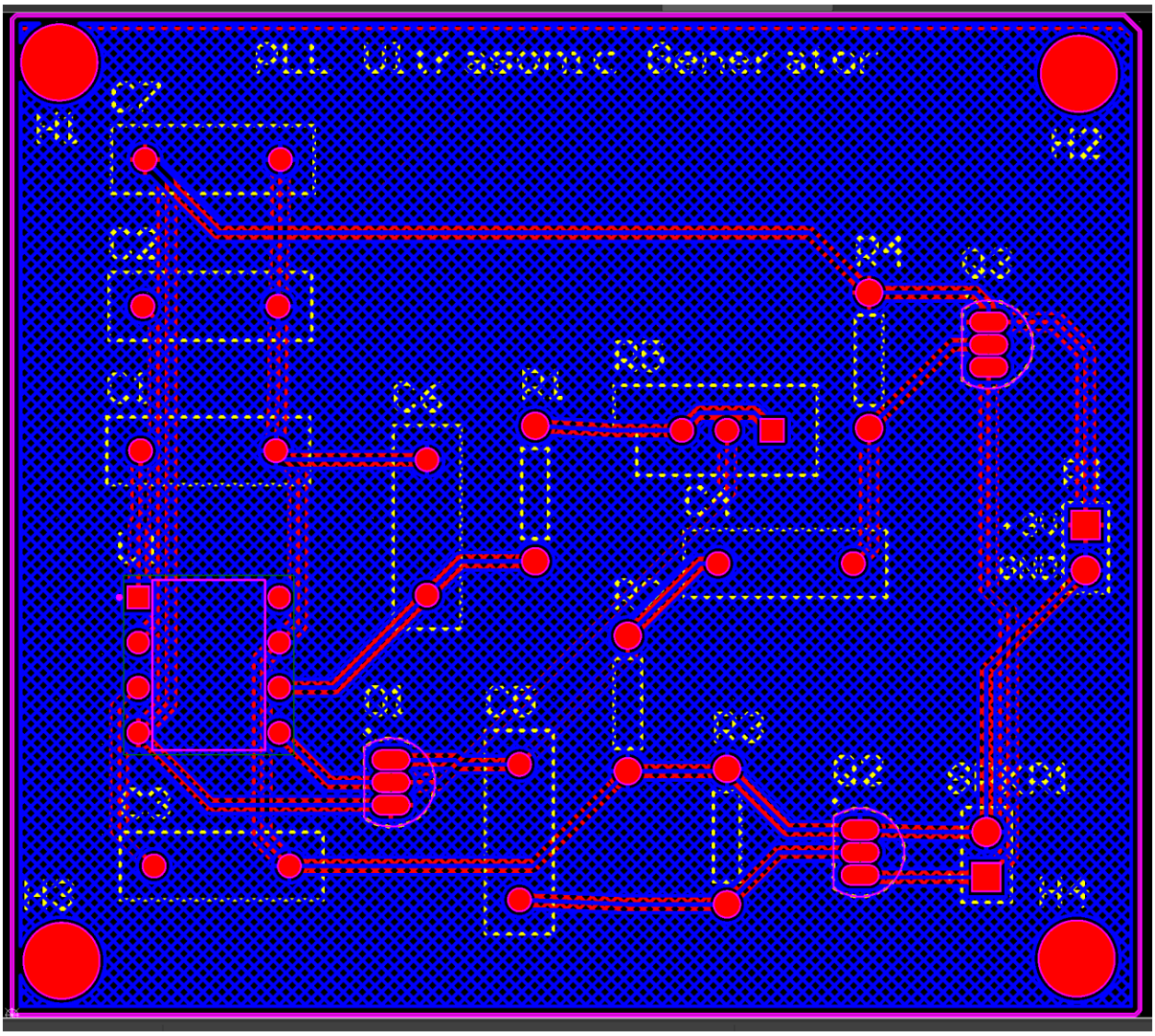

Figure 6. .Cam file generated that contains the copper placement.

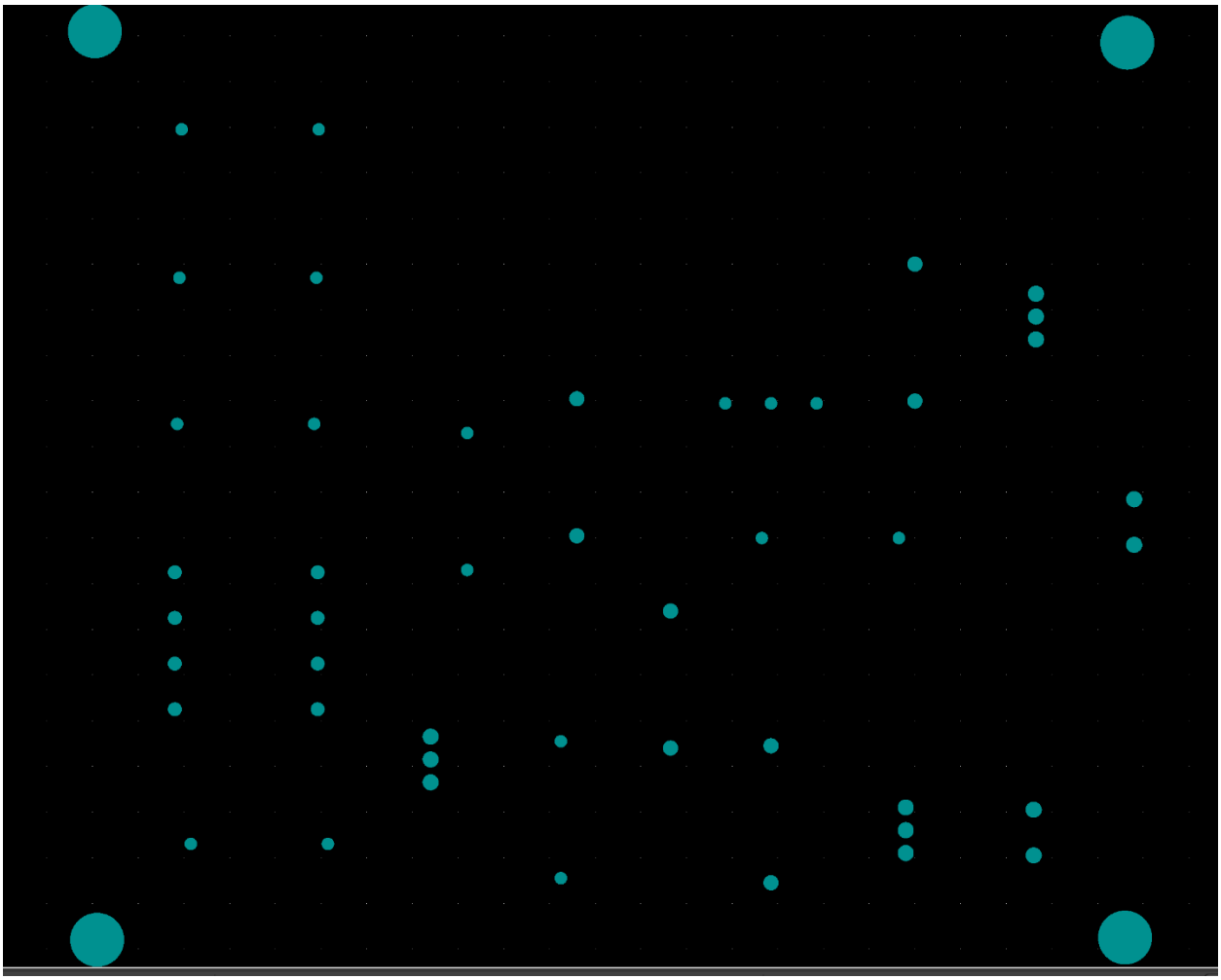

Figure 7. .Cam file generated that contains the all the holes in the board

NCDrill File Report For: PCB1.PcbDoc 1/27/2023 10:37:18 PM

Layer Pair : Top Layer to Bottom Layer
ASCII RoundHoles File : PCB1.TXT
EIA File : PCB1.DRL

Tool	Hole Size	Hole Tolerance	Hole Type	Hole Count	Plated	Tool Travel
T1	28mil (0.7mm)		Round	17	PTH	6.96inch (176.79mm)
T2	31mil (0.78mm)		Round	8	PTH	0.91inch (23.18mm)
T3	33mil (0.85mm)		Round	8	PTH	2.42inch (61.55mm)
T4	35mil (0.9mm)		Round	13	PTH	4.45inch (112.99mm)
T5	118mil (3mm)		Round	4	PTH	6.47inch (164.34mm)
Totals				50		

Total Processing Time (hh:mm:ss) : 00:00:00

Figure 8 .DRR file generated

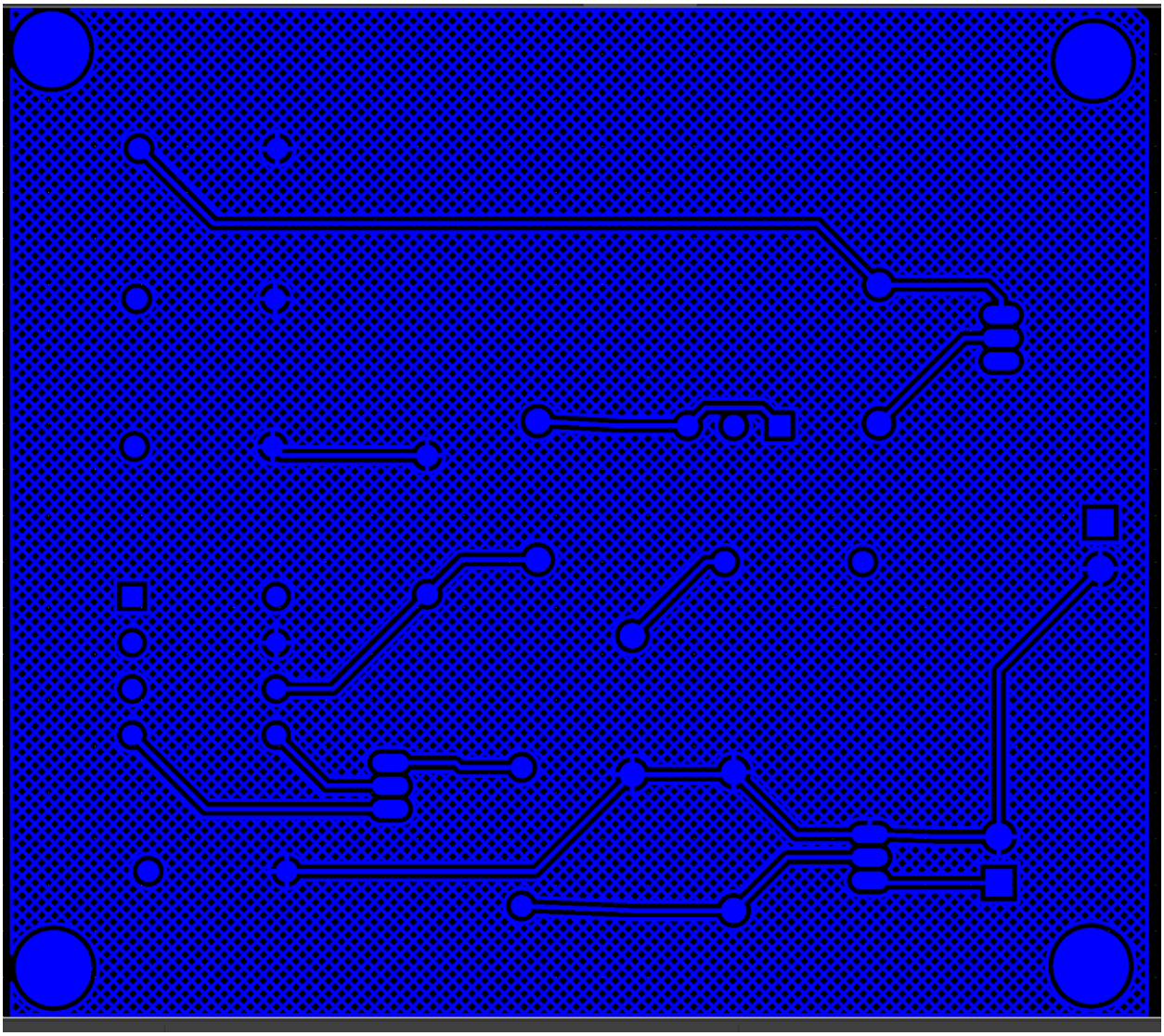

Figure 9 .GBL file generated

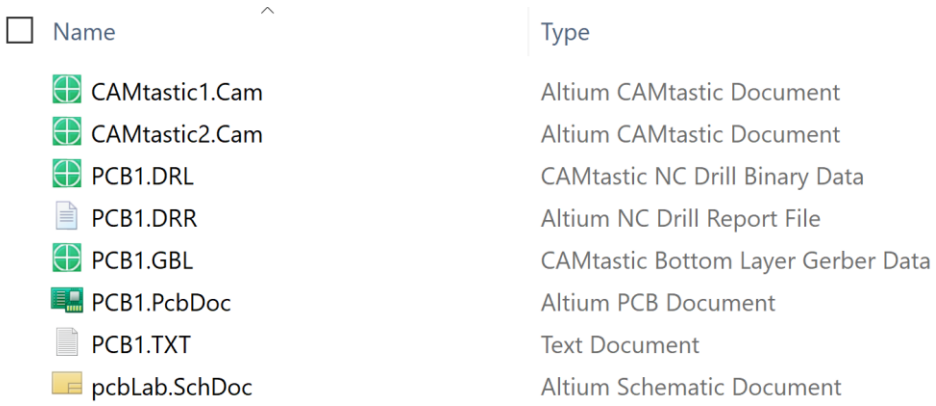

Figure 10. Files included in the zip file

Conclusion

During the design of the schematic and PCB, the only problem I encountered was organizing the components on the board in a clean way, which was resolved by changing the footprints of the capacitors to a rad-0.3 so that it was easier to lay out on the PCB. Overall, the final schematic and PCB outlined all the components based on the given circuit.