Phase 2: Synaptic Processing & Neuron Updates

Goal: Read synapses, accumulate weights, update neurons

- pointer_fifo_controller: Round-robin read from 16 FIFOs
- hbm_processor: Pop pointer → read synapses from Region 3
- hbm_processor: Parse synapses → forward to IEP
- internal_events_processor: Accumulate weights into neurons
- internal_events_processor: Apply neuron model (leak, etc.)
- internal_events_processor: Threshold check → spike?
- internal_events_processor: Write updated state to URAM
- Spikes → spike_fifo_controller → command_interpreter

Output: Updated neuron states in URAM, new spikes generated

If neurons spiked: Loop back to Phase 1b
If no more spikes: Timestep complete

Spike Output

1) spike_fifo_controller round-robbin muxes spikes from individual spk#FIFOs to spk2ci FIFO
2) command_interpreter takes spikes from spk2ci FIFO and batches spikes into 512-bit packets; places them into tx FIFO
   - *Example packet format:*
     - [511:480] = 0xEEEEEEEE (spike output opcode)
     - [479:463] = spike_0 (17-bit neuron ID)
     - [462:446] = spike_1 (17-bit neuron ID)
     - ...
     - [#:0] = padding (unused for < 14 spikes)
3) pcie2fifo takes tx FIFO packets and pushes them thrugh PCIe to Host