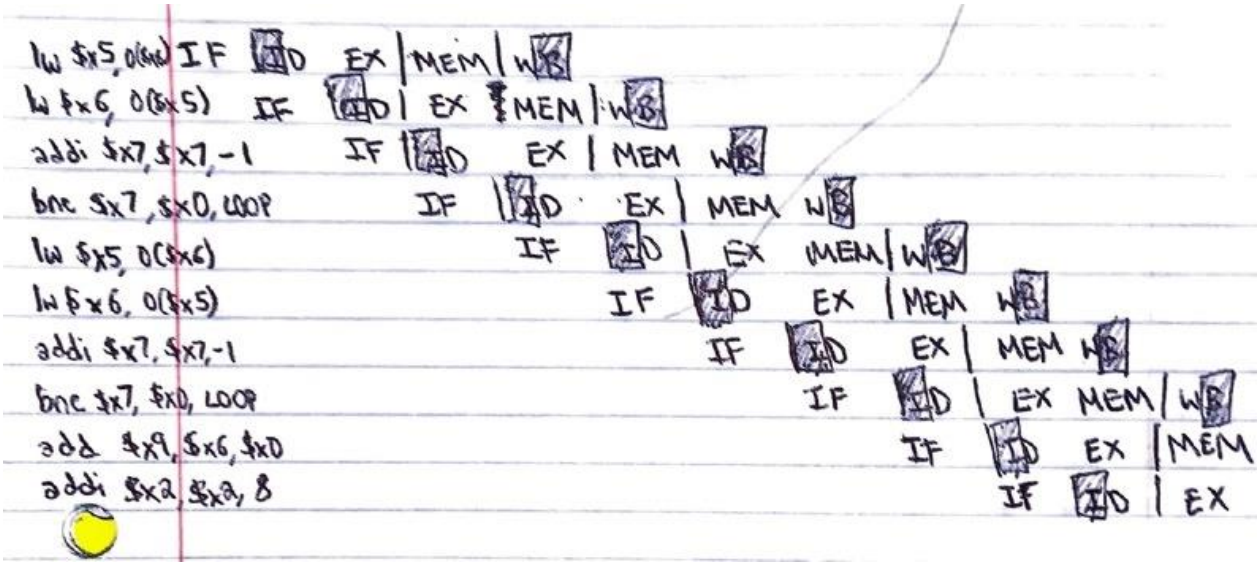
1. A. 350 ps + 300 ps +250 ps + 450 ps + 200 ps = **1550 ps**

   B. 450 ps + 50 ps = **500 ps**

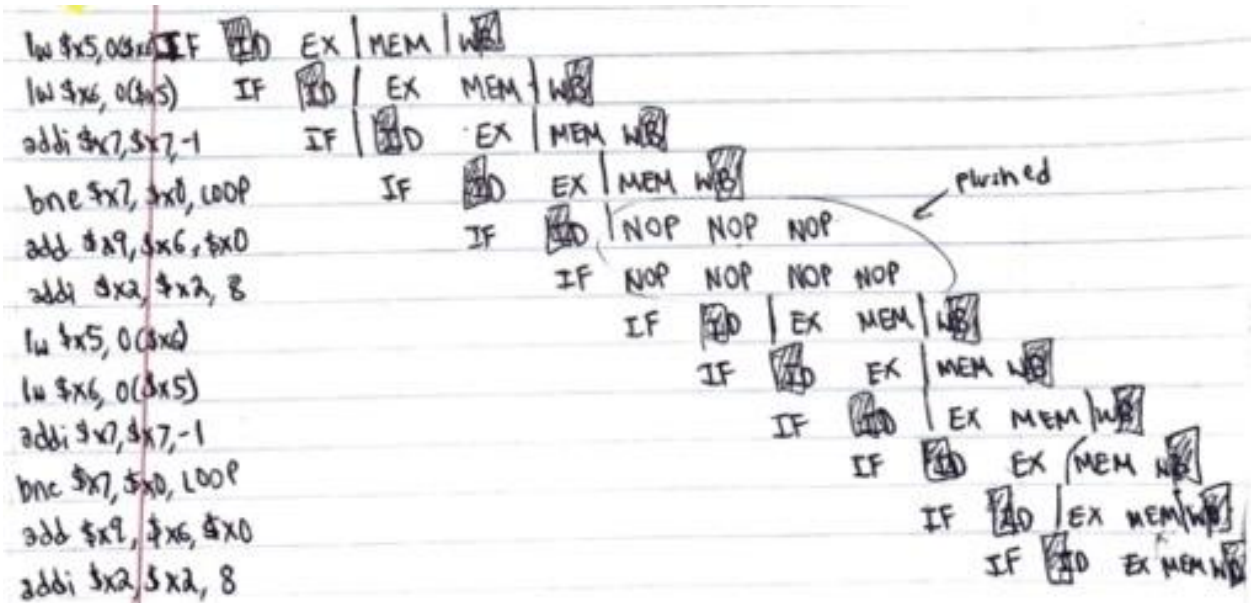
2. A. $x7 = 2

```
LOOP: lw $x5, 0($x6)
      lw $x6, 0($x5)
      addi $x7, $x7, -1
      bne $x7, $x0, LOOP
      lw $x5, 0($x6)
      lw $x6, 0($x5)
      addi $x7, $x7, -1
      bne $x7, $x0, LOOP
      add $x9, $x6, $x0
      addi $x2, $x2, 8
```

   B.



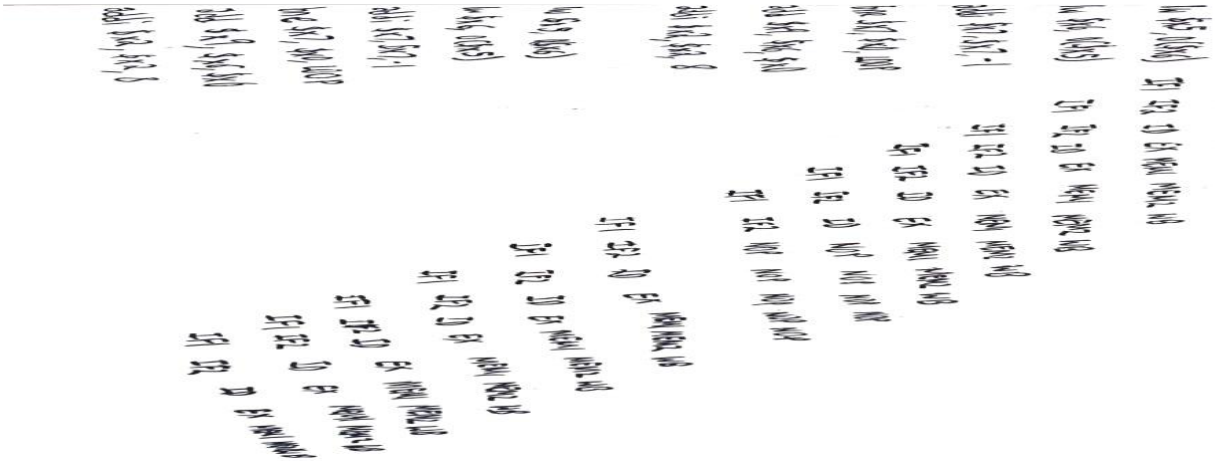
C.



D.

The average CPI is 1 cycle per instruction. It takes 40,004 cycles for the program to reach the last instruction.

E.



F.

The average CPI is 1 cycle per instruction. It takes 60,003 cycles for the program to reach the last instruction.

3. A.

Inst. 2 depends on Inst. 1 for $x5
Inst. 3 depends on Inst. 2 for $x5
Inst. 5 depends on Inst. 4 for $x6
Inst. 7 depends on Inst. 6 for $x5
Inst. 8 depends on Inst. 7 for $x5

Inst. 10 depends on Inst. 9 for $x6

B.
The data dependencies that lead to data hazards in a 5-stage RISC-V pipelined processor supporting full forwarding are:
Inst. 2 depends on Inst. 1 for $x5
Inst. 7 depends on Inst. 6 for $x5

These ones lead to data hazards because it stalls for load-use data hazard even with full forwarding.