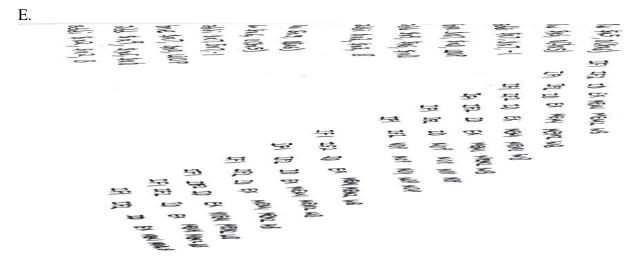
1. A. 
$$350 \text{ ps} + 300 \text{ ps} + 250 \text{ ps} + 450 \text{ ps} + 200 \text{ ps} = 1550 \text{ ps}$$
B.  $450 \text{ ps} + 50 \text{ ps} = 500 \text{ ps}$ 

2. A. \$x7 = 2 LOOP: lw \$x5, 0(\$x6) lw \$x6, 0(\$x5) addi \$x7, \$x7, -1 bne \$x7, \$x0, LOOP lw \$x5, 0(\$x6) lw \$x6, 0(\$x5) addi \$x7, \$x7, -1 bne \$x7, \$x0, LOOP add \$x9, \$x6, \$x0 addi \$x2, \$x2, 8

> В. IN \$x5 oland IF WID W \$x6, 0(8x5) 1-1x2,5x2 ible IF 150 MEM WE MEM WE bne 5x7, 5x0, 4009 EX IF IN \$ x5 0 (\$x6) IF. MEM WE IN \$ x 6, 0(\$x5) IF MEM 1-, TXP , TXP ibbe MEM ME EX bne tx7, \$x0, woo 0x\$, 3x2, Px\$ 660 TF 3 ddi \$x2 \$x3, 8

W \$x5,000 mo F 100	EX	MEM	WED.							
161 \$x6, 0(\$05) IF	Th	EX	MEM .	WB	-					
1-5x2,5x2 ibbe	IF	Bo	. EX	MEM	WE	om				
bne 9x7, 3x0, coop		IF	20	EX	MEM	MIS			Plvs	ined
add \$49,4x6,5x0			IF	西	NOP	NOB		1		
3 , Ext , ext 166				IF	Mob	NOB	NOP	406	1 127	
lu 4x5, ocaxo					IF	Do	EX	MEM		國
14 \$x6, 0(3x5)						IF	西	EK	1	18
addi \$10,\$x7,-1							IF	OTE!	EX	MEN MEN
bnc \$17, 5x0, 2009									(B)	EX MEM WE
0x\$, 3x\$, Px\$ 666										TO EX NEWIND
addi txa sxa, 8									2	LF HO EX HENN

D. The average CPI is 1 cycle per instruction. It takes 40,004 cycles for the program to reach the last instruction.



The average CPI is 1 cycle per instruction. It takes 60,003 cycles for the program to reach the last instruction.

## 3. A.

Inst. 2 depends on Inst. 1 for \$x5

Inst. 3 depends on Inst. 2 for \$x5

Inst. 5 depends on Inst. 4 for \$x6

Inst. 7 depends on Inst. 6 for \$x5

Inst. 8 depends on Inst. 7 for \$x5

Inst. 10 depends on Inst. 9 for \$x6

B.

The data dependencies that lead to data hazards in a 5-stage RISC-V pipelined processor supporting full forwarding are:

Inst. 2 depends on Inst. 1 for \$x5

Inst. 7 depends on Inst. 6 for \$x5

These ones lead to data hazards because it stalls for load-use data hazard even with full forwarding.