# EECE 116L
# Digital Logic Laboratory

## Laboratory Assignment #1

*Pre-lab:*

1) Using Ohm's Law, fill in the blanks:

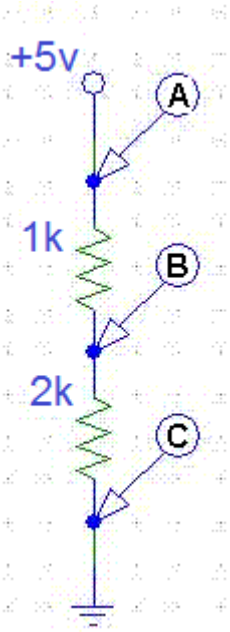
| Voltage | Resistance | Current |
|---|---|---|
| 10 V | 22.4 kΩ | |
| | 1.15 kΩ | 3 mA |
| 4 V | | 2 mA |
| 12 V | | 3.3 mA |

2) Create a schematic (use AND, OR, Inverter gates) for the following functions:
   a. g = XY'Z + X'YZ + XYZ + XYZ'
   b. Given D = W(X' + Y'), F = Y(W + X) and E = X'(Y' + W), compute
      f = EF + DF + ED

3) Using the TTL gates, how would you implement the circuit in 2(a)? (Use the 7404, 7408, and 7432 model gates). You will draw your schematic design using TLL gate ICs indicating connections between IC pins. (http://eecs.vanderbilt.edu/courses/eece116/Standard_TTL_Datasheet.htm),

*In-Lab:*

1) Using your breadboards and your multi-meter, construct the following circuit and measure the voltage at points A, B, and C.




2) Build the circuit you designed in your pre-lab 2(a) using the TTL gates.
3) Demonstrate the working circuit to the TA.

*Post-Lab-Questions*

1.) What were you expecting from the voltage between the two resistors?
2.) Did the result deviate from what you expected? Why?
3.) How did you check to make sure that your circuit worked correctly?