EECE 2116L
Digital Logic Laboratory

Laboratory Assignment #5: Combinational Blocks

Pre-Lab:

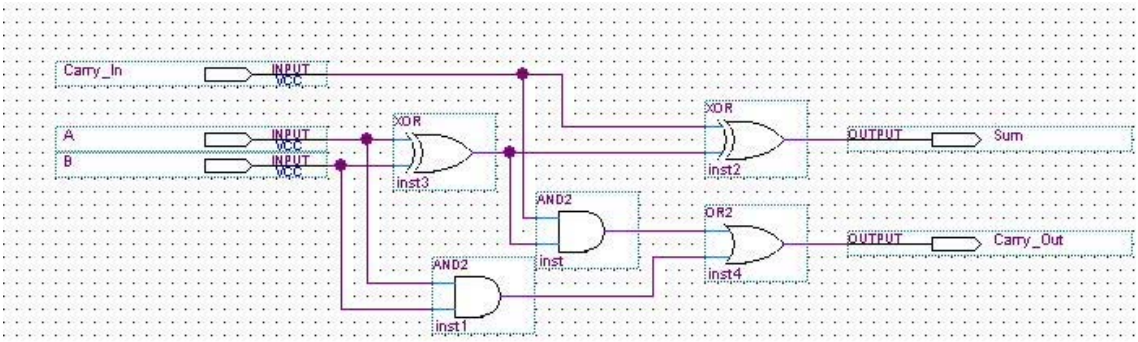
In Quartus II, it is possible to save an existing schematic and use it in an object in another schematic. This can greatly decrease the complexity of a circuit, as well as reduce work necessary. When you save an existing schematic this way, you are creating a "symbol file", similar to the "AND" gate symbols that you insert into the schematics.

1.) Design and Build an 8-to-1 Multiplexer, complete with input pins and output pins. *(Label the input pins In0-In7, where 0 is the least significant bit, and 7 is the most significant bit.)*

Go to *File->Create/Update->Create Symbol Files for Current File*, and save the multiplexer symbol.

2.) Repeat this with 8-pin encoders and decoders, as well as a 1-to-8 demux *(Use a similar naming scheme for the pins on these schematics)*

3.) Using the full adder circuit (shown below), make a 4-bit adder.
9 inputs (4-bit number + 4-bit number + carry_in)
5 outputs: (4-bit number, and carry_out)



(Hint, you can create the full adder circuit, save it as a symbol file, and then import it into another schematic)
(Make sure to name the pins so that '0' is the least significant bit, and '3' is the most significant bit)

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* Please print out each of your circuits, and turn them in for prelab credit.
(To save paper, you can use *file->export*, and then copy the jpegs into a word document)

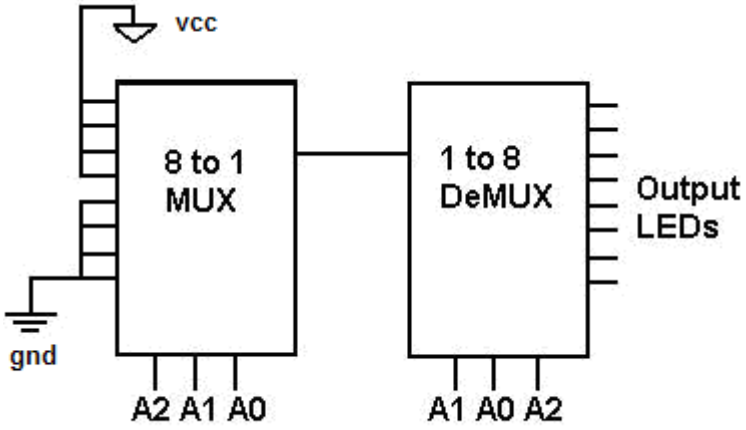
In-Lab:

Part 1

Demonstrate all of your circuits on the LEDs of the FPGA.

Part 2

Build the following circuit using your multiplexer and demux.



Post-Lab

Give an example of a situation in which exporting a circuit to a symbol would be useful. When is it not useful?