Lab 4 Notes Monday, March 5, 2018 - Set TRIS Setting for Pin E2 for external POT (Look at Schematic Diagram in M Drive for Inputor Output) - In order to do ADL, you need to configure the A/D module and the function of the Port Pins ADCOND & ADCONT Registers ADCOND Register (Slile 49) - Configures the A/D module - 8-bit Register A/D conversion clock (use fosc/4) Analog Channel Scluction (use awiktlash schematic PDF) Start A/D, DO NOT Start it until you are ready to Jo the actual ADC Leave ps zero ON/OFF Setting to- A/D Module - Bits 7-6: - Bits 5-3: - Bits 2: - Bits 1: - Bits 0: ADLON 1 Register (slile 50) - contiguous the function of the port pins - 8 bit Register Result Format (Left/Right Justiti, cation) A/D (Dnversion about (Same as AD(ONO) Leave as O Port Configuration (orthor) bits Need Analog Input for Chi vith refunce to Voo & Vss - Bits 7: - Bits 6: - 13its 5-4: - Bits 3-0: - Sompling rate needs to be set before and after ADIONObits. 60 - Delay of X- amount of ms ADC SFRS (SILLE 48) - ADRESH & ADRESL - Register Pair is 16-bits wite - Result is 10-bit vide and can be right/lest justitied - Textra bits are loaded with 2003 - Right Justitied ca) 000000 0101010101 ADRESH ADRESL - Need to combine ADRESH & ADRESL - Bit-Shift ADRESH left by the size of ADRESL - Then Combine 1.1.1 Note: Do not work on SFR, directly, store them to a Variable Displaying Voltage (Slites 36-40) - Display Voltage from 20 to 5.0 V - Display: ADC gives 10 bit result - Solution: ADC gives 10 bit result, so recult ranges invalue upto 10 bit 10 bit = 21°= - Rosult ranges from 2.0 to ? - Simply scale this range to go 1 som 2.0 to 5.0 (Use equation) tenths place may be difficult to display instead you can scale o-50 and split that D. + his for both potentiometers

Comparing Voltages

- Make a comparison of the current Values for each Voltage and light up respective LED

- Use Schematic Diagram to find LFD Port - TRIS Settings - Write to port a 1 or o to turn ON/OFF

Look at Slide 66 for programming example