1. Area percentage: (50/4888)x(100)= 1.023 %
   Delay: 14.708 ns
   Levels of Logic:10
2. On the sheet
3. Delay of the RCA: 42.654
   Levels of Logic: 34
   Considering the time delay of the CLA, 14 ns, the CLA would work faster than the RCA because it passes through less gates.

4. You need 4 16-bit CLA to make a 64-bit CLA. Therefore, with outpu t and input buffers, the number of levels of lgic would be (34*4) +2=138.
5. To create a 64-bit CLA, you must have a pg cell, 16 clls, 1 16-bit cll, and another cll. Connect those in that order and output your sum with a XOR gate. The number of levels of logic for the critical path is 12. First it must pass through a XOR gate which is 1 gate delay, then 4clls which are 2 gate delays, and the pg which is 1 gate delay. This is without i/o buffers.