IEEE Hyderabad Mentorship Programme -2024: Digital IC Design

- **Course Overview:**
  - **Duration:** 6 weeks [Monday to Friday]
  - **Timings:** 7 PM – 8 PM
  - **Mode:** Online [Google meet]
  - **FPGA EDA tools:** AMD's Xilinx's Vivado, Intel's Altera's Quartus,
  - **ASIC EDA tools:** OpenLane
- **Course Content:**
  - **Introduction to Verilog HDL - 4 weeks**
    - Verilog language details
    - Differences between simulation and synthesis
    - Various modelling styles
    - Modelling of combinational logic
    - Modelling of sequential logic
    - FSM design
  - **FPGA Design Approach - 4 weeks**
    - Introduction to FPGA design flow
    - Intel's Altera's Quartus design tool
    - AMD's Xilinx's Vivado design tool
  - **ASIC Design Approach – 4 weeks**
    - Introduction to RTL-to-GDSII design flow
    - ASIC design using open-source PDK
    - ASIC design using open-source EDA tool OpenLane
- **Installation of the required EDA tools:**
  - In order to ensure a smooth learning experience, it is imperative that all participants have the required EDA (Electronic Design Automation) tools installed on their laptops/desktops prior to the commencement of the course. To facilitate this process, we kindly request one week's notice before the scheduled start date of the course.
  - We will handle the installation of these tools directly onto your system. This will be conducted remotely, connecting to your device via AnyDesk to perform the installation seamlessly.
  - We understand the importance of having the necessary tools in place to fully engage with the course material, and we are committed to assisting you every step of the way.
- **Course Instructor:**
  - **Mohammed Zakir Hussain**
  - **SMIEEE 91261181**
- **Google Meet joining info**
  - **link:** https://meet.google.com/kbj-cbxk-qmc

Upon completion of Digital IC Design, you will be undertaking the following mini projects and major projects:

- **Mini Projects:**
  - Design and Simulation of a 8-Bit ALU.
  - Finite State Machine (FSM) for Traffic Light Controller.
- **Major Projects:**
  - Design and Implementation of a Simple RISC Processor.
  - Development of a Digital Signal Processing (DSP) System.

Mini Projects:

- **Design and Simulation of a 8-Bit ALU (Arithmetic Logic Unit)**
  - **Objective:** Design and simulate a 4-bit ALU using Verilog HDL.
  - **Tools:** Xilinx Vivado or Intel Quartus for simulation and synthesis.
  - **Details:**
    - Implement basic arithmetic operations (addition, subtraction).
    - Implement logical operations (AND, OR, XOR, NOT).
    - Test the design using a testbench.
    - Simulate the design to verify functionality and timing.
  - **Learning Outcomes:**
    - Understanding of combinational and sequential logic design.
    - Experience with Verilog HDL for modeling hardware components.
    - Hands-on practice with FPGA tools for simulation and synthesis.

- **Finite State Machine (FSM) for Traffic Light Controller**
  - **Objective:** Design and simulate an FSM-based traffic light controller using Verilog HDL.
  - **Tools:** Xilinx Vivado or Intel Quartus for simulation and synthesis.
  - **Details:**
    - Create an FSM with states for different traffic light phases.
    - Implement timing control for each phase.
    - Test the FSM with a testbench.
    - Simulate the FSM to verify correct state transitions and timing.
  - **Learning Outcomes:**
    - Understanding of FSM design and state transition logic.
    - Practical experience with sequential logic design.
    - Familiarity with FPGA simulation and synthesis tools.

Major Projects:

- **Design and Implementation of a Simple RISC Processor**
  - **Objective:** Design, simulate, and synthesize a simple 8-bit RISC processor using Verilog HDL.
  - **Tools:** Xilinx Vivado or Intel Quartus for FPGA implementation, OpenLane for ASIC flow.
  - **Details:**
    - Implement key components: ALU, registers, control unit, and memory interface.
    - Develop a simple instruction set architecture (ISA).
    - Create test programs to validate processor functionality.
    - Perform synthesis and implement the design on an FPGA.
    - Optionally, use OpenLane to explore the ASIC design flow for the processor.
  - **Learning Outcomes:**
    - Comprehensive understanding of processor architecture and design.
    - Experience with both FPGA and ASIC design tools.
    - Insight into the full digital design flow from HDL modeling to hardware implementation.

- **Development of a Digital Signal Processing (DSP) System**
  - **Objective:** Design, simulate, and synthesize a DSP system capable of performing basic signal processing tasks (e.g., filtering, FFT) using Verilog HDL.
  - **Tools:** Xilinx Vivado or Intel Quartus for FPGA implementation, OpenLane for ASIC flow.
  - **Details:**
    - Implement key DSP modules (e.g., FIR filter, FFT module).
    - Integrate modules into a cohesive DSP system.
    - Develop testbenches to verify the functionality of each module and the entire system.
    - Perform synthesis and implement the design on an FPGA.
    - Optionally, use OpenLane to explore the ASIC design flow for the DSP system.
  - **Learning Outcomes:**
    - Deep understanding of DSP algorithms and their hardware implementation.
    - Practical experience with designing complex digital systems.
    - Exposure to both FPGA and ASIC design methodologies.

These projects will help solidify your understanding of digital IC design, provide hands-on experience with industry-standard tools and open-source EDA tools as well, and prepare you for more advanced design challenges.