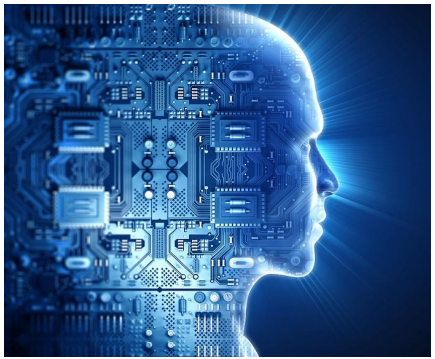

PHYSICAL DESIGN

ETB Samuel Jigme Harrison
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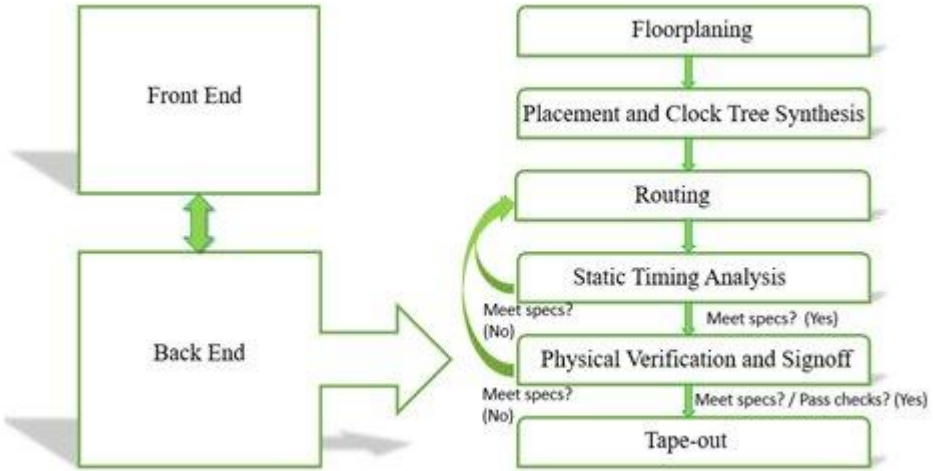
Fellow - IETE, ISVE & CET(I), Life member - ISTE, Senior member - IEEE & IEDRC
Member - IEI, IES, IET, SSIA, EngNZ, IAENG, IEICE, ASR, USERN, IRED, AICTSD, NIITSD, ACM

Backend Implementation / Physical Design

The circuit representations are converted to geometric description of shapes with various metal layers and when manufactured, the metal layers will ensure the functioning of the circuit.



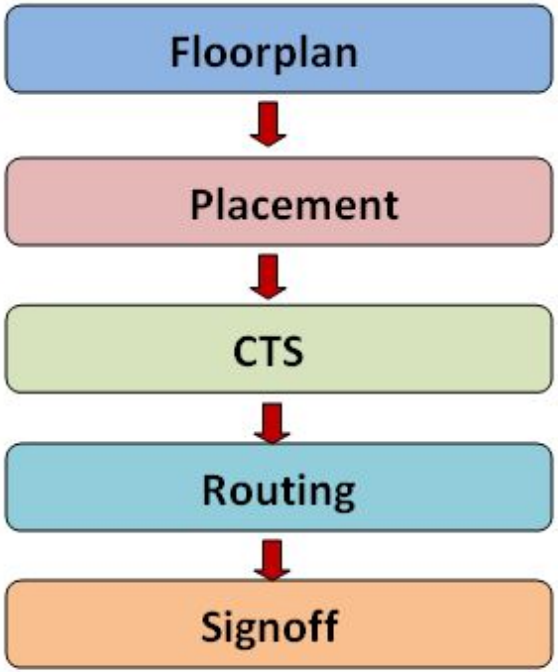
Inputs and Challenges in Physical Design

- ➔ The inputs to Physical Design are a netlist, library information of the cells in the design, a technology file with the manufacturing constraints and timing constraints.

- ➔ Timing, power and design constraints are to be met during Physical Design.

Steps in Physical Design

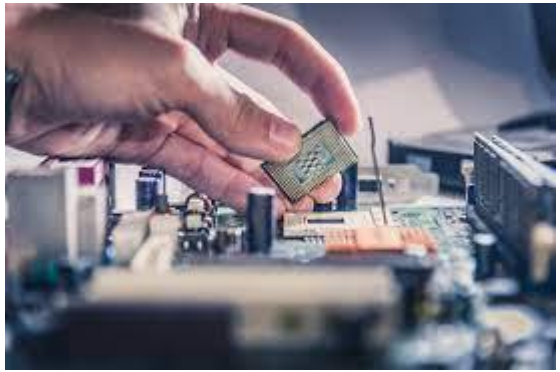
- ➔ Floorplanning & Powerplanning
- ➔ Placement
- ➔ Clock Tree Synthesis
- ➔ Routing
- ➔ Static Timing Analysis
- ➔ Physical Verification
- ➔ Power analysis



Terminologies in Physical Design

- ➔ **Component -** functional element of a circuit - transistors, resistors and capacitors
- ➔ **Module** - collections of components
- ➔ **Block** - A module with dimensions
- ➔ **Standard cell** - cell which represents the functionality - INV, NAND, NOR
- ➔ **Macro** - cell with large physical layout which will contain millions of transistors - CPU, ROM, RAM etc
- ➔ **Flip - flops** - digital electronic circuits used to store information in bits
- ➔ **Registers** - combination of flip flops
- ➔ **Contact** - connection between silicon and metal layer. This connection is inside a cell
- ➔ **Instance count** - number of standard cells

FLOORPLANNING



Floorplanning

➔ **Goals of a Good Floorplan**

- Minimized total chip area
- Routability of the design
- Minimal congestion
- Low power consumption

Floorplanning

➔ **Inputs for Floorplanning**

- **Netlist** - representation of the connectivity of the circuit in the design, in the VHDL or verilog format
- **Timing Constraints** - input and output delay of the cell and clock definitions, exceptions, etc.
- **Physical Libraries** - Layout Exchange Format (LEF) containing physical information of std cells, macros and pad cells

Floorplanning

- **Logic Libraries** - timing and functionality information of cells and hard macros
- **Power Requirements** - Power and GND Nets

Floorplanning

➔ **Steps in Floorplanning**

- Size of the chip
- I/O pin placement
- Macro placement
- Creating standard cell rows
- Adding Routing and Placement Blockages

Floorplanning

➔ **Output of Floorplan Step**

- **DEF (Design Exchange Format)** - It contains die/core area information, macro information, placed IO pin, pad information and blockage details.

Floorplanning

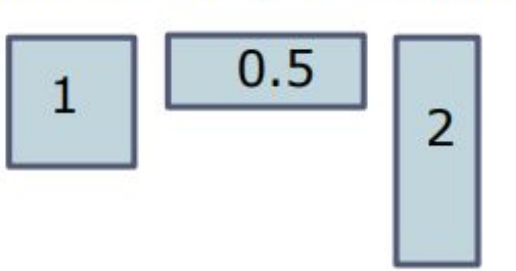
➔ Floorplanning can be controlled by the following two parameters:
- ◆ Aspect Ratio
- ◆ Core Utilization

➔ **Aspect Ratio**
- ◆ Aspect Ratio is the width to height ratio of the chip. Width can be related to horizontal routing resources and height can be related to vertical routing resources.

  - **Aspect Ratio = $\frac{\text{Number of horizontal routing resources}}{\text{Number of vertical routing resources}}$**

Floorplanning

- ➔ If AR=1, then the block shape will be a square.
- ➔ If AR>1, then the block shape will be rectangular with more routing resources in the vertical direction, height > width.
- ➔ If AR<1, then the block shape will be rectangular with more routing resources in the horizontal direction, width > height.



Floorplanning

➔ **Core Utilization**

- The area occupied by the standard cells and macros (i.e) the percentage of area used for cell placement.

- **Core Utilization = $\frac{\text{(Standard cell area + Macro area)}}{\text{Total core area}}$**

- If the core utilization is 0.6, it means that 60% of the area is used for cell placement and the rest 40% is used for routing.

Floorplanning

➔ **Core rows**

- The height of the standard cells determine the spacing between the core rows.
- Alternate rows are flipped to change the row orientation.
- By flipping the row orientation, standard cells are connected to POWER and GND stripes accordingly.

Floorplanning

➔ **Spacing between macros**

- A minimum spacing must exist between macros for pin sides.

Channel spacing = (number of pins X pitch)/(total number of available layers/2)

- The pitch should correspond to the top most metal layer among the two macros.

- We are dividing by 2 - vertical and horizontal metals

Floorplanning

- Spacing is a must between the macros and edge of the chip to allow for power stripes to feed standard cell rows.
- The allocated routing resources should be well utilized.

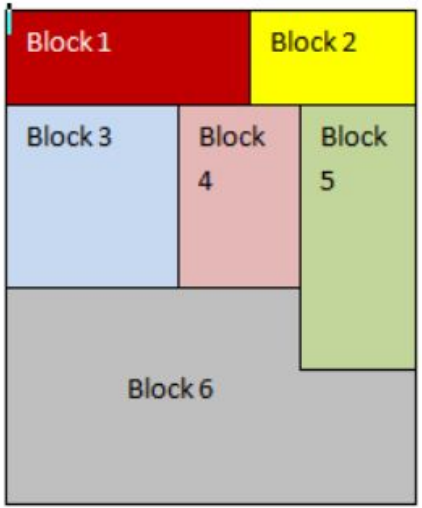
Floorplanning

➔ Macro Placement

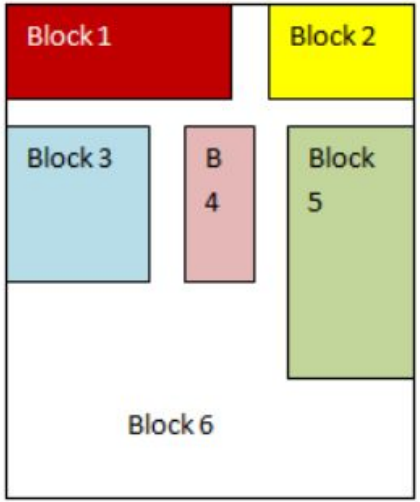
- The designer should understand the pin and orientation requirements of macros.
- The pin of the macros should face towards the logic area.
- Use a data flow diagram as reference to place the macros.
- Make sure that the routing channels between macros is big enough to accomodate the signal routes and power stripes too.

Floorplanning

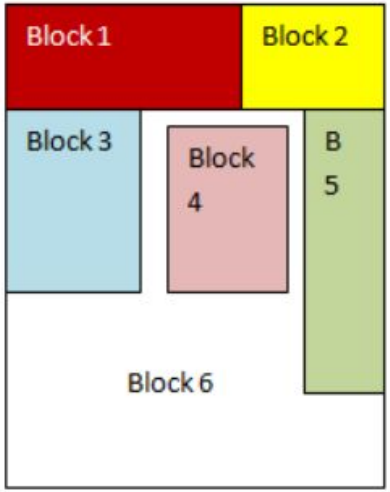
➔ Macro Placement



Abutted



Non - abutted



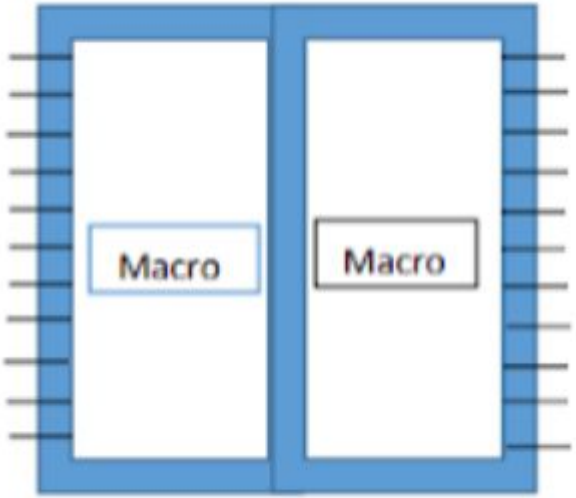
Mixed

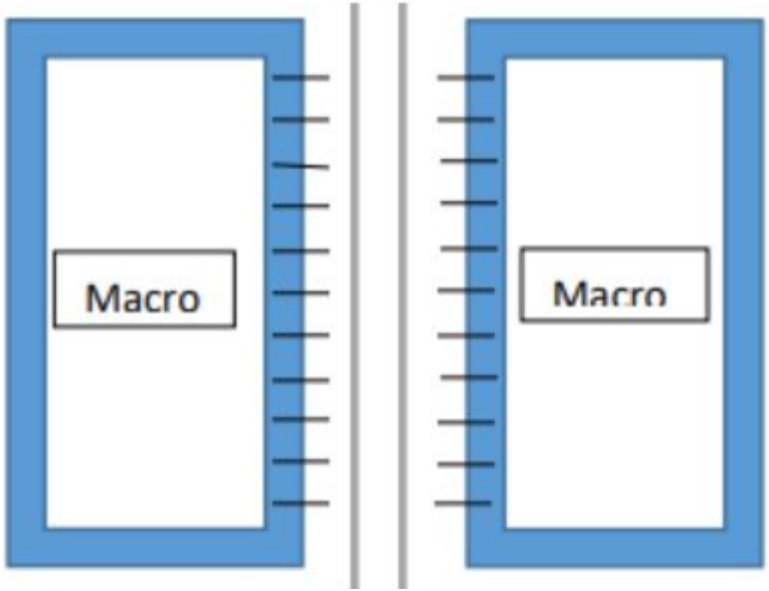
Floorplanning

- Flylines can also be used as a reference in macro placement.
- Macros can also be abutted with the pin sides in the opposite direction.
- Avoid criss cross placement of macros to save routing resources.

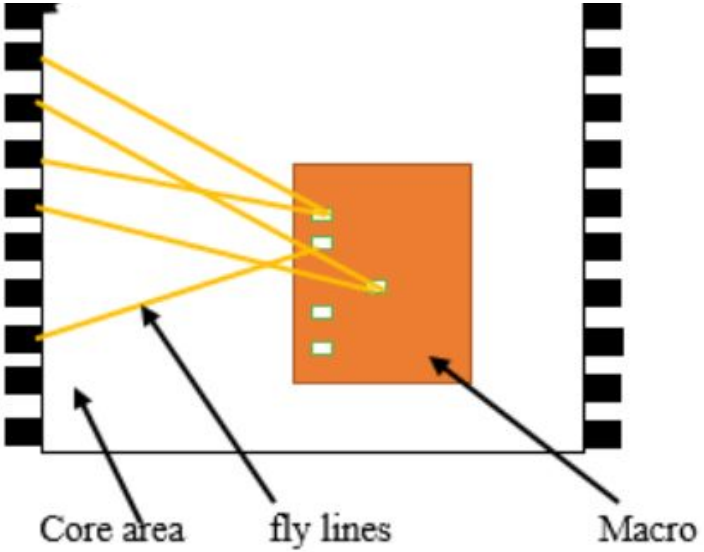
Floorplanning

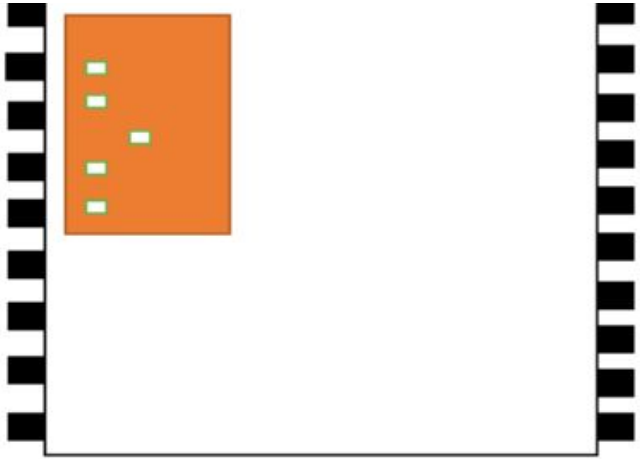
➔ **Macro Placement**



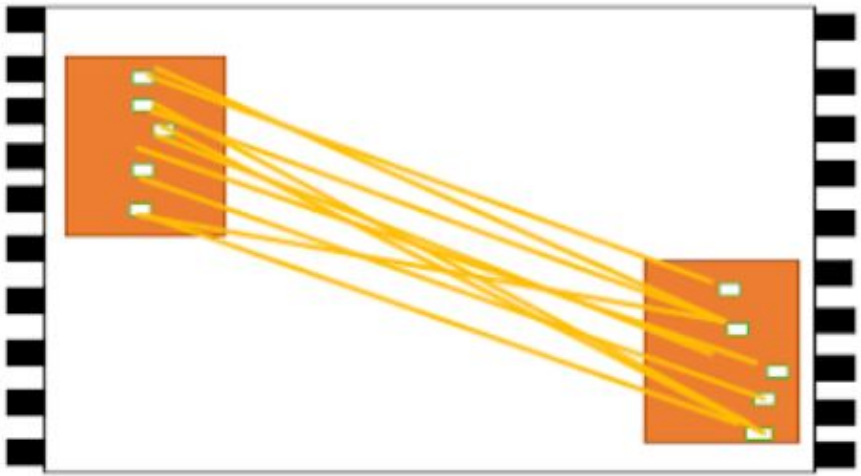


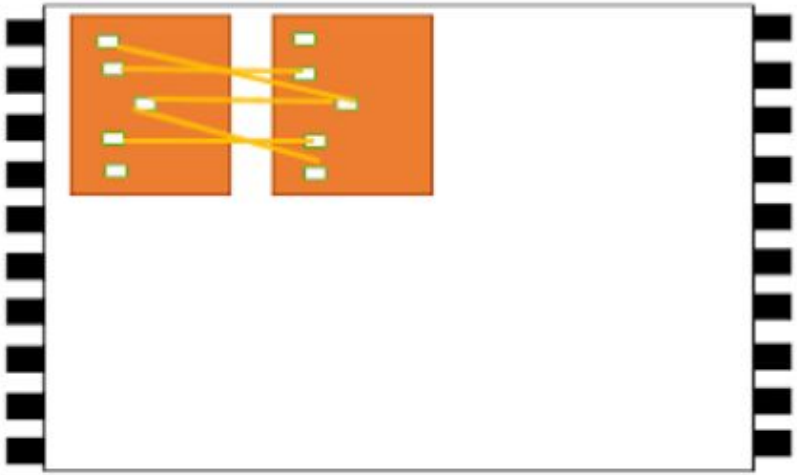
Floorplanning





Floorplanning





Floorplanning

➔ **Blockages**

- **Placement Blockage** - This prevents placement of standard cells, buffers and inverters. Placement blockage must be used in thin spaces between macros.

- **Routing Blockage** - This prevents routing of metal layers in the blocked region

Floorplanning

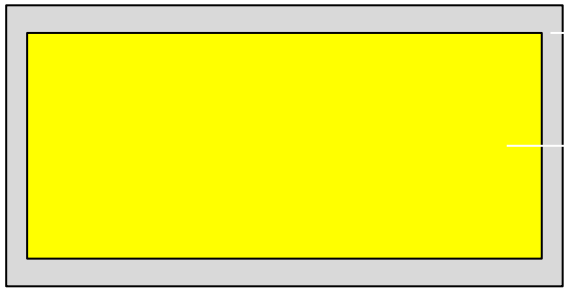
Blockages are differentiated as Hard and Soft blockage.

- Hard - Standard cells and buffers cannot be placed in this area.
- Soft - No standard cells but buffers can be placed in this area.

Floorplanning

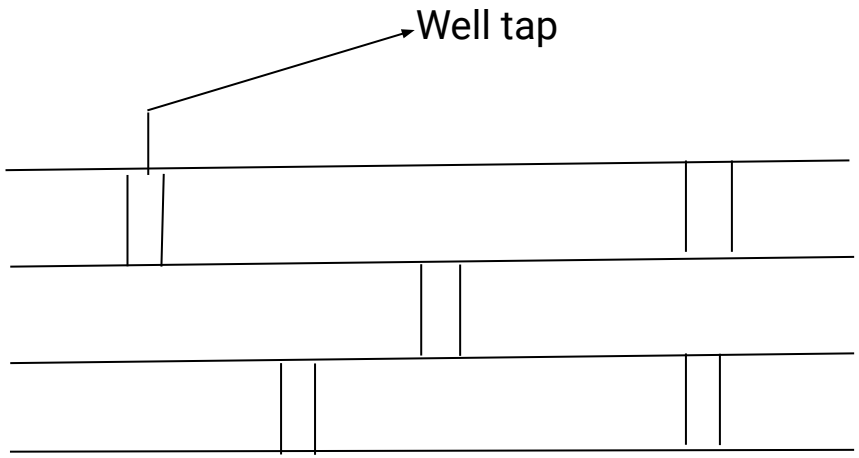
➔ **Halo**

- It is the region around the fixed macro in which no standard cells can be placed.
- Buffers and inverters are allowed to be placed in this region.
- When the macro is moved from one location to another, the halo should also be moved



Floorplanning

- **Physical Cells**
  - **Well taps**
    - Well taps are inserted in the design to prevent latch-ups.
    - They are used so that the VDD and GND are connected to substrate and n-wells.
    - Well taps are used to reduce the resistance between the power and ground connections to wells of the substrate.



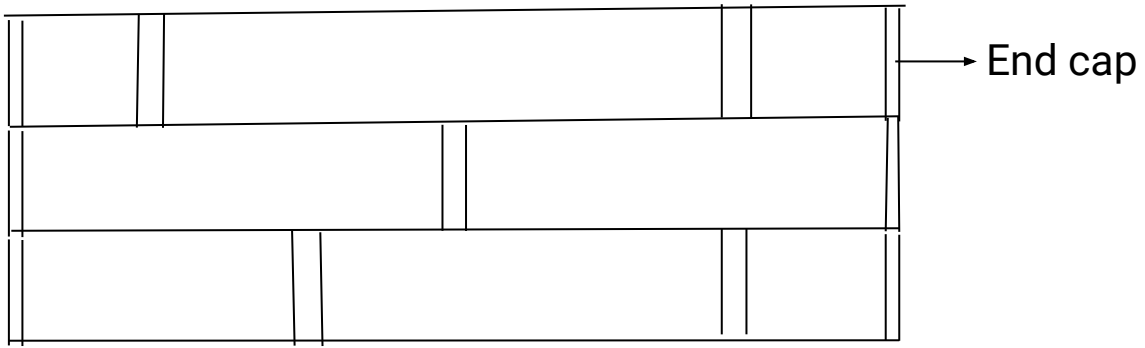
Floorplanning

➔ **End cap cells**

- End caps are placed at every edge of every standard cell row.
- They do not have any functionality and are connected to the power and ground rails.

Floorplanning

- These cells ensure that gaps do not occur between well and implant layers.
- End caps ensure proper termination of rows and no DRC is created.



Floorplanning

➔ **Filler cells**

- Filler cells are used as continuity of the N well and implant layers in the standard cells rows.
- They are used to fill the empty spaces between the cells and thus the continuity of power and ground exists between the cells.

Floorplanning

➔ **Tie cells**

- They are special purpose cells used to connect the gate of the transistor to either Power or Ground.
- The unused inputs in the netlist should be either connected to Vdd or Vss.
- The inputs which are required to connect to Vdd, connect to tie high cells.
- The inputs which are required to connect to Vss, connect to tie low cells.

Floorplanning

➔ **Decap cells**

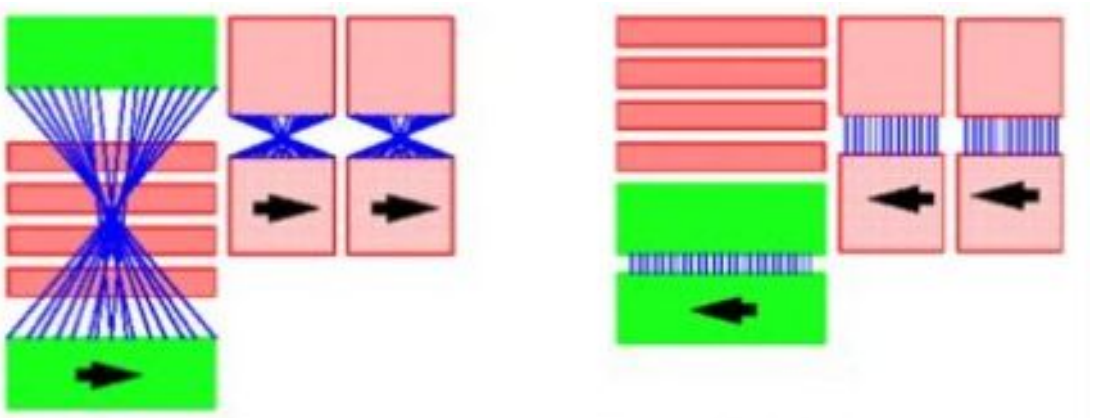
- The Decap cells act as capacitance between ground and power stripes and they behave as a charge reservoir.
- They become active when there is high demand of power from the design.

Floorplanning

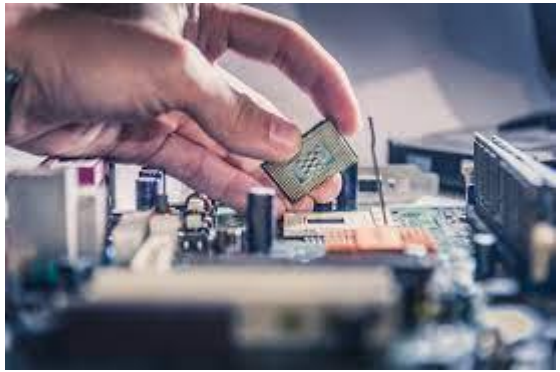
- These cells do not have any logical functionality.
- When current requirement is high, the decap discharges and boosts up the power grid.
- The main use of decap cells is to overcome dynamic voltage drop.

Floorplanning

Macro Placement



POWER PLANNING



Powerplanning

➔ **Goal of Powerplanning**

- To make sure that the power mesh is properly created
- All the standard cells and macros should get the required power supply.
- To meet the IR drop budget

Powerplanning

➔ **Powerplan Components**

- Block ring
- Core ring
- Routing standard cell pins
- Adding VDD and GND stripes in the core area
- Connecting pad pins
- Connecting block pins
- Global Net connections

Powerplanning

- **Power Pads**
  - These pads supply power to the chip.
  - The power is connected to the vertical and horizontal metal stripes.

- **Block Power Rings**
  - These are power stripes around the macros.
  - The width of the power stripe and spacing between the power stripes are calculated by the designer.

Powerplanning

➔ **Horizontal and Vertical Power Stripes**

- The VDD and GND power stripes run over the entire section of the die.
- The block rings, the standard cell power rails are connected to the power pads through the VDD and GND power stripes.
- These power stripes use the widest and highest routing layer.

Powerplanning

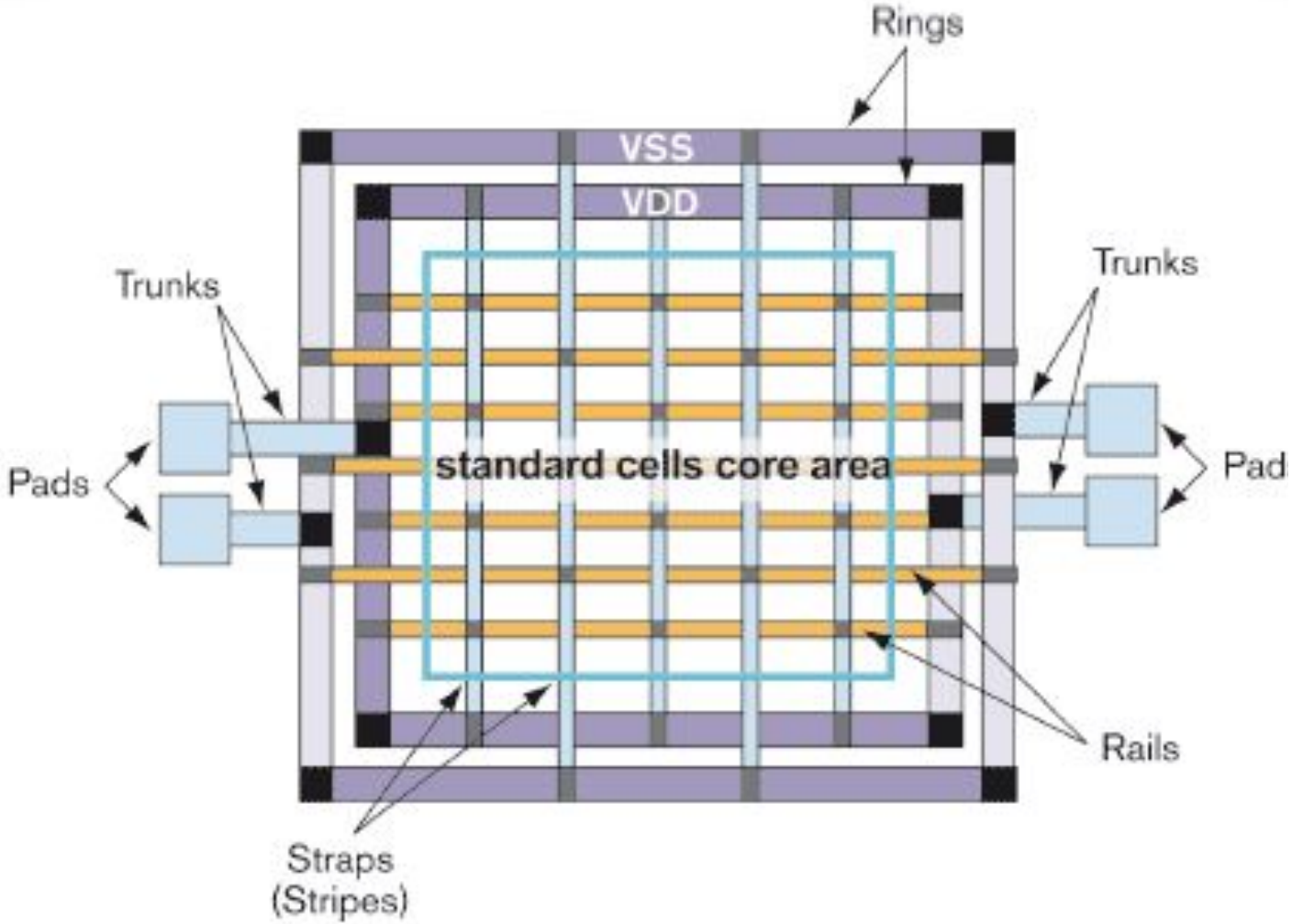
➔ **Power Domain Creation**

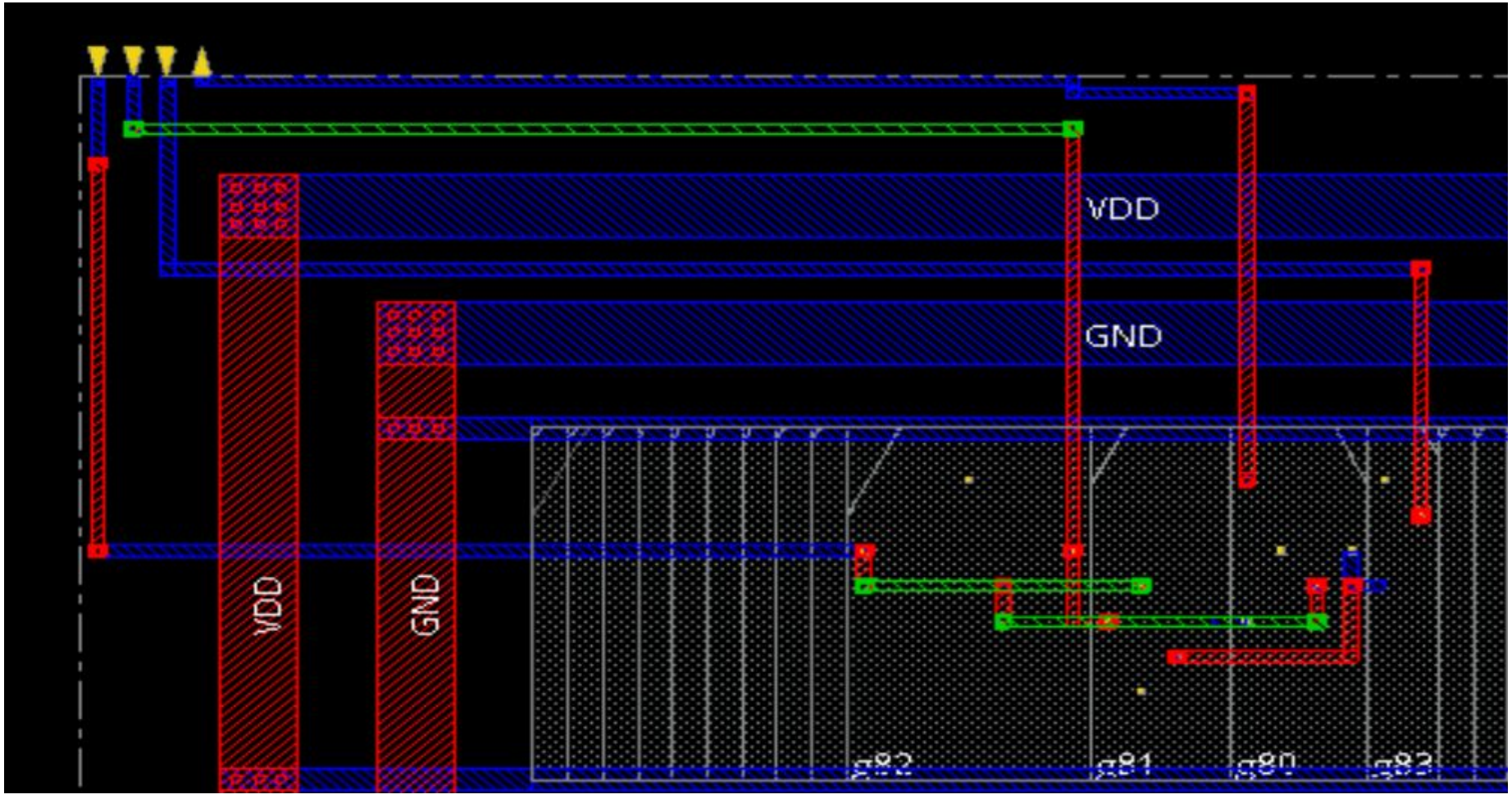
- Power domains should be created if the design operates with multiple power domain.
- When few cells cross signals from one domain to another, power domain has to be created for these kind of cells.

Powerplanning

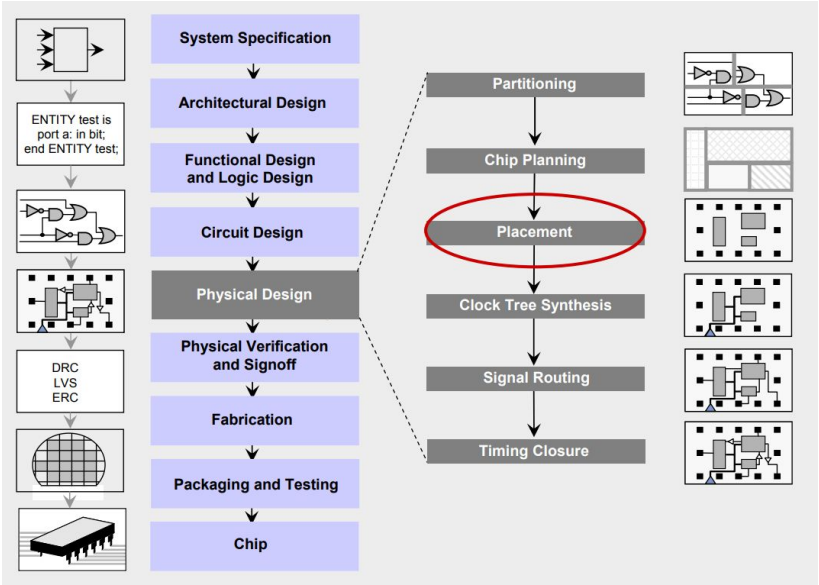
➔ **Standard Cell Rails**

- These rails are used to supply power to the standard cells.
- The cells are connected to the rails through the follow pins.
- The follow pins are usually in either M1 or M2.
- The row orientation of alternate stand cells rows is flipped, so that the standard cells are connected to both VDD and GND accordingly.


Rings
VSS
VDD
Trunks
Trunks
Pads
standard cells core area
Pad
Rails
Straps
(Stripes)


VDD
GND
VDD
GND

PLACEMENT


System Specification
Architectural Design
Functional Design and Logic Design
Circuit Design
Physical Design
Physical Verification and Signoff
Fabrication
Packaging and Testing
Chip
ENTITY test is port a: in bit; end ENTITY test;
DRC
LVS
ERC
Partitioning
Chip Planning
Placement
Clock Tree Synthesis
Signal Routing
Timing Closure

Placement

➔ **Objectives of a Good Placement**

- Timing and power
- Minimum cell density and pin density
- Routable design
- Good control over congestion

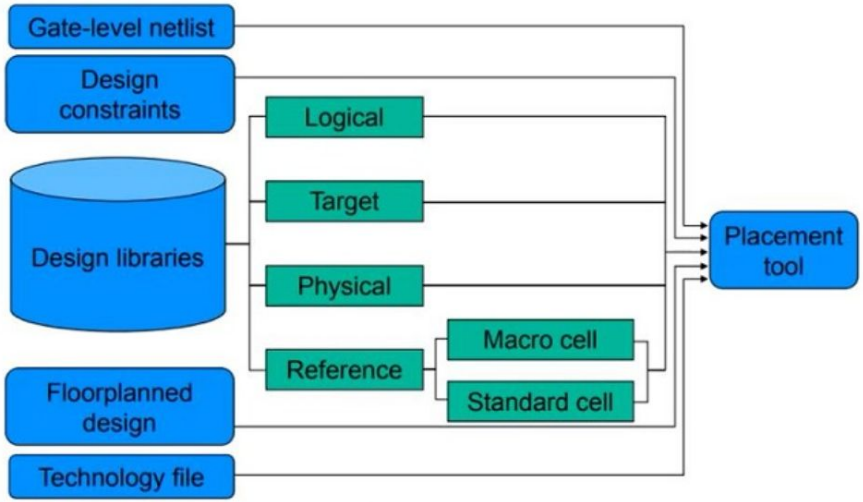
Placement

➔ **Inputs for Placement**

- Floorplan DEF - It contains die/core area information, macro information, placed IO pin, pad information and blockage details.
- Logical Library - timing and functionality information of cells and hard macros.
- Physical Library - Layout Exchange Format (LEF) containing physical information of std cells, macros and pad cells.

Placement

- Netlist - representation of the connectivity of the circuit in the design, in the VHDL or verilog format.
- Technology file - technology - specific information like physical and electrical characteristics of each metal/via layers and the routing design rules.



Placement

➔ Checks before Placement

- Missing placement / routing blockages
- Don`t touch on cells and nets
- Density
- Understanding of optimization and placement switches
- No high WNS timing violation
- Clock should be ideal
- Integration of IPs - log files
- Fixed status - macros and pre - placed cells
- Pins should be accessible

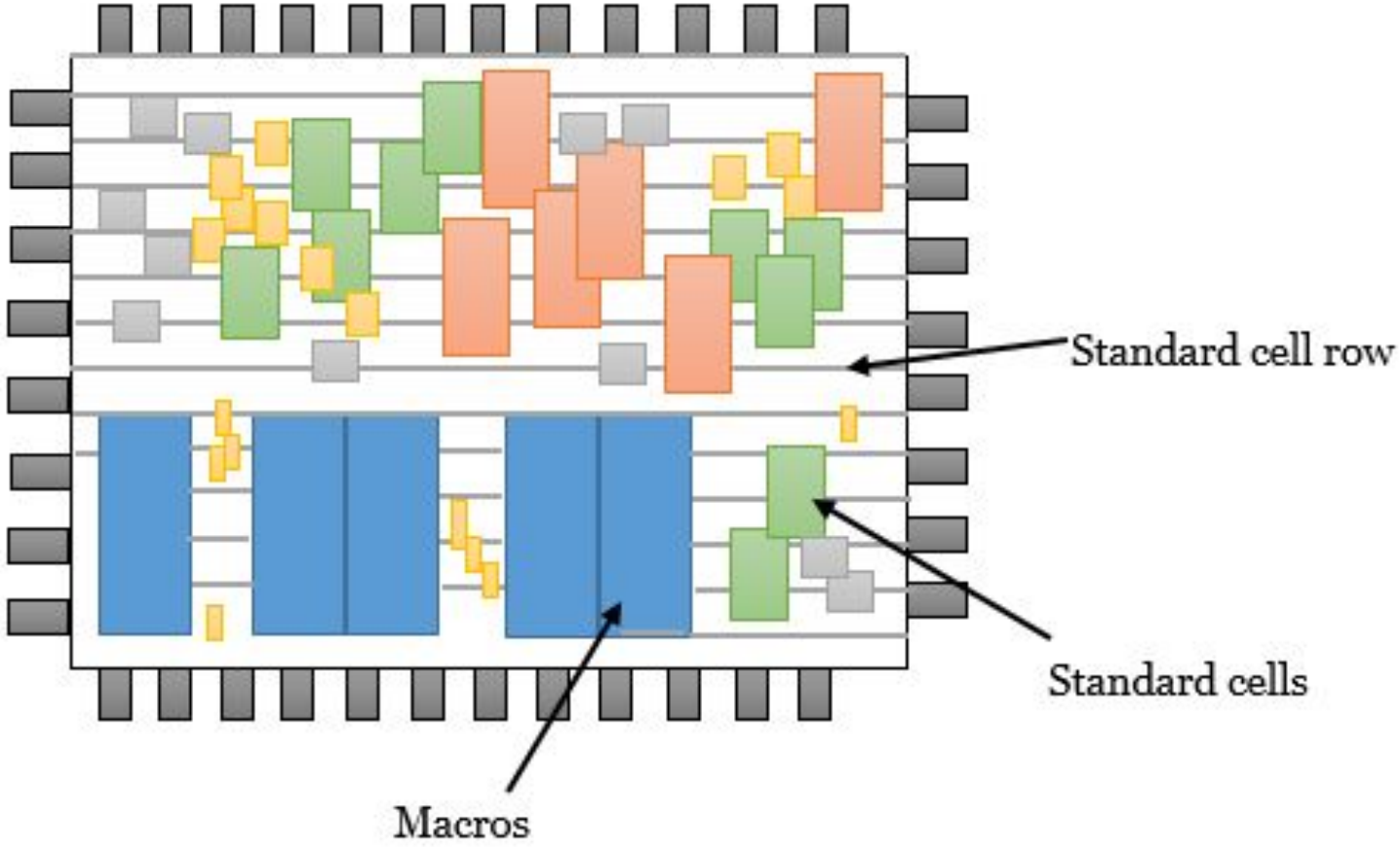
Placement

➔ **Steps of Placement**

◆ **Global Placement** (Takes around 50% of the runtime)

- The tool finds an approximate location for the cell based on timing and congestion.
- The placed cells overlap each other and they do not align with the power rails.
- This placement technique is quite fast and accurate for the initial timing and congestion analysis.
- The main objective is to reduce the wire length of the interconnect nets.

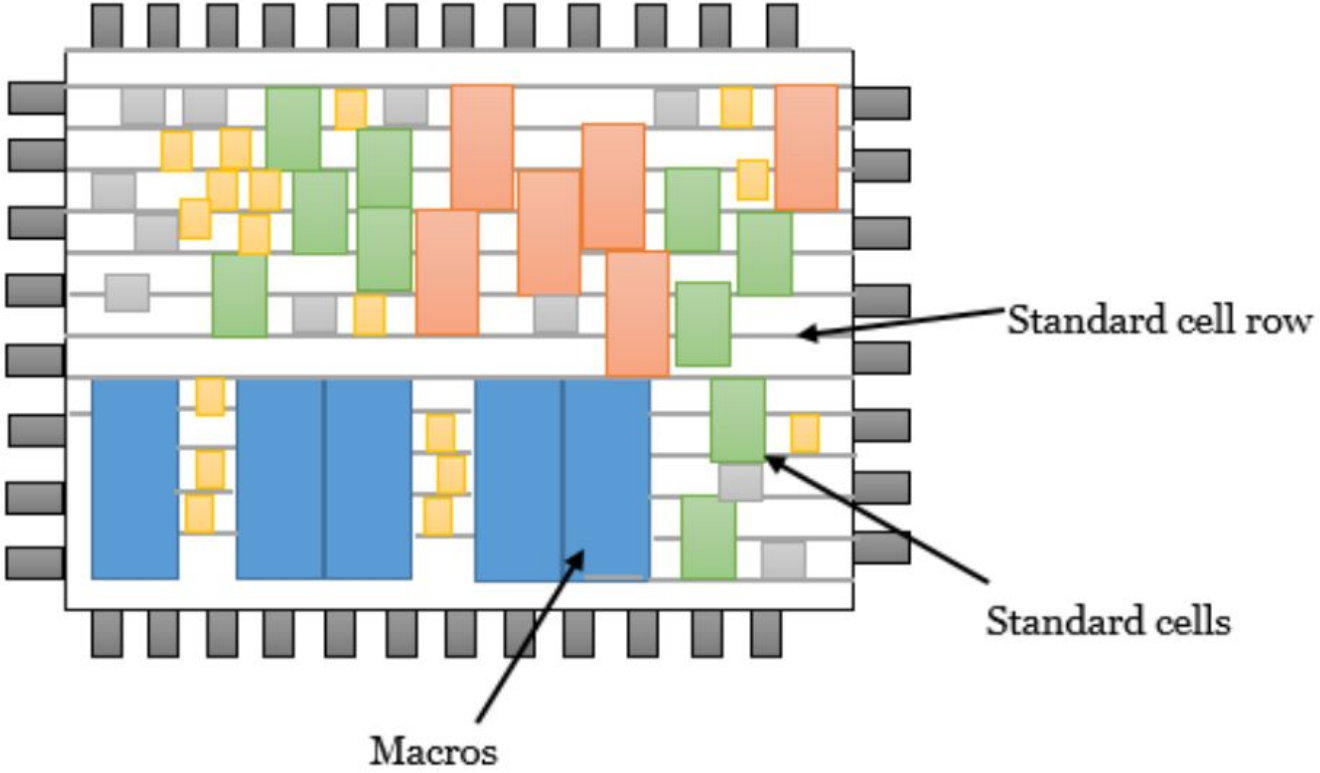
Placement



Placement

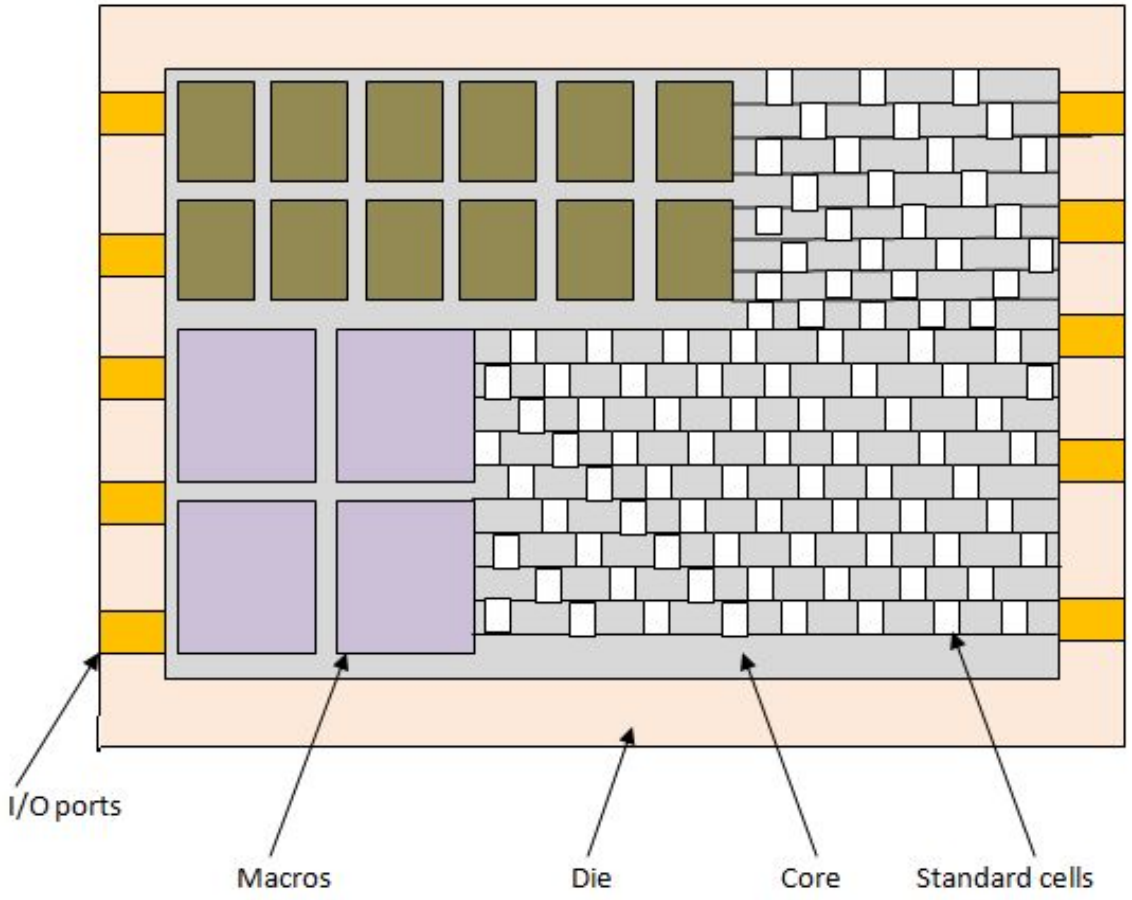
- **Legalization**
  - The tool moves the cells to the legal locations on the placement grid and overlaps are eliminated between cells.
  - During this movement, the length of the wire connections are reduced.
  - Cells are also aligned to the routing tracks.
  - Cells connect to power & ground rails.
  - Cells are also moved to unused space in the layout.

Placement



Placement

- **Detail Placement** (Takes around 50% of the runtime)
  - This is the step where minor modifications in the locations of smaller modules occurs and the standard cell placement is finalized.
  - Minor swapping of neighbour cells


I/O ports
Macros
Die
Core
Standard cells

Placement

➔ **Addition of Spare Cells**

- These cells are also part of the standard cell library and they are dummy cells which are inserted in the netlist.
- These cells are used to accommodate future Functional Engineering Change Order (ECO) after the tape-out of the chip.

Placement

➔ **Via ladder Insertion**

- Stacked via - bottom pin layer to upper pin layer
- Via resistance is reduced and performance is improved

Placement

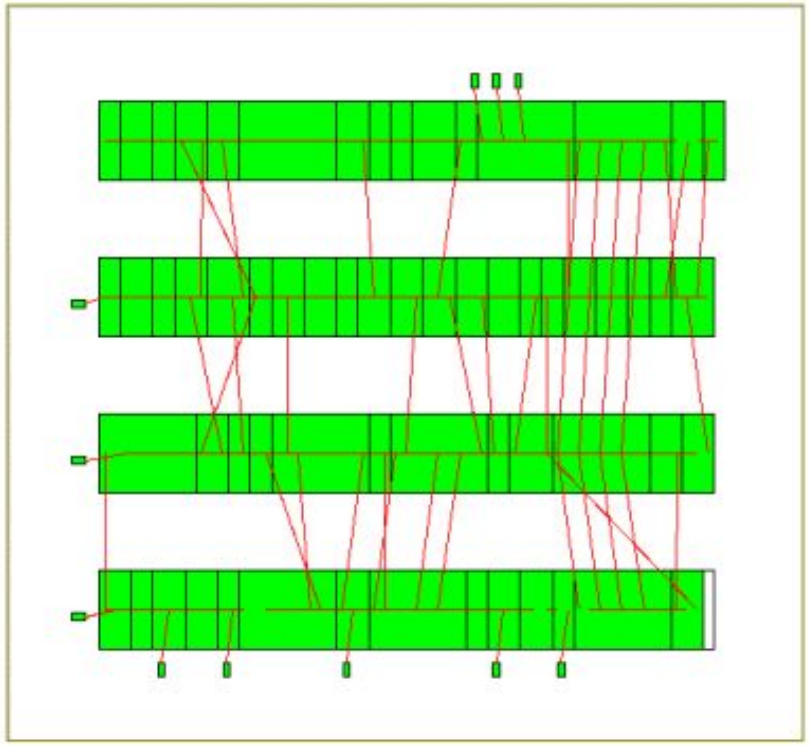
➔ **Tasks in Placement step**

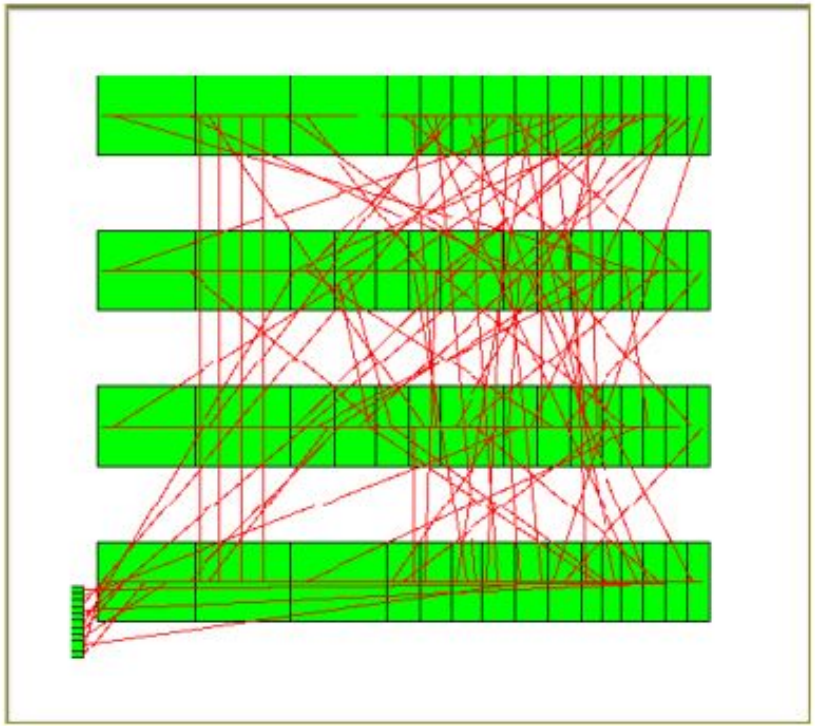
- Placement of standard cells in core rows
- The GND and VDD pins of the standard cells should be in sync with the GND and VDD power rails
- Optimization in terms of congestion, power and timing
- Legalization of cells
- HFNS - High Fanout Net Synthesis

Placement

➔ **HFNS**

- Process of buffering the high fanout nets to balance the load - to reduce delay and transition time (time taken for a signal to rise from 10% to 90% or fall from 90% to 10%)
- Load is directly proportional to delay
- High Fanout nets are reset, preset etc
- set_max_fanout value





Good placement

Bad placement

Good Placement vs Bad Placement

Good Placement	Bad Placement
Decrease in area and length of the wires	Increase in area and length of the wires
Easier routability	Routability is difficult
Shorter wires - Less dynamic power dissipation	Longer wires - High dynamic power dissipation
Less hotspots - maximum performance	More hotspots - performance degradation

Placement

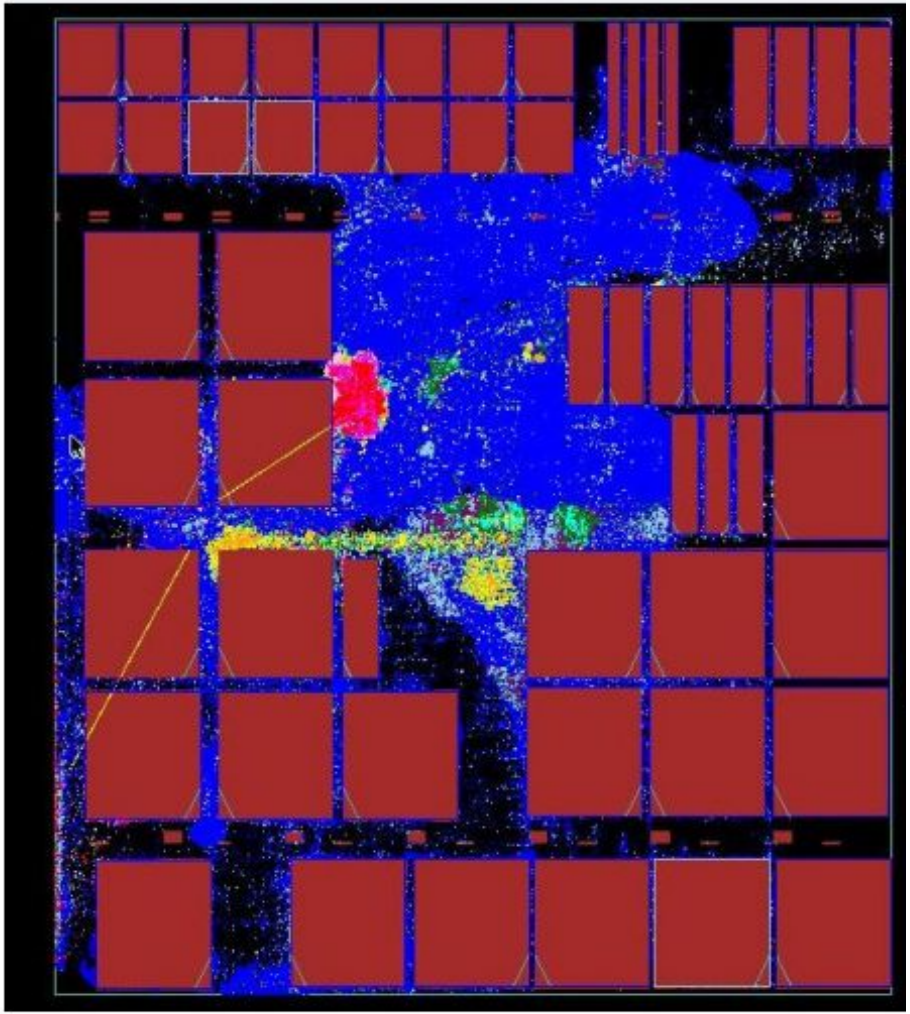
➔ **Congestion**

- Congestion occurs if the number of available routing resources is less than the required routing resources.
- A congestion map can help us to visualize the quality of placement. It shows the different levels of overflow in the selected layers.

Placement

➔ **Reasons for congestion**

- High standard cell density creating hotspots
- No proper placement blockages
- Less routing resources
- Placement of macros in centre of the chip instead of the boundary
- Tool does buffering during I/O placement resulting in lots of cells in logic area



Placement

➔ **Strategies to fix congestion**

- Identify areas with low utilization and modify the floorplan
- Spread out the top level ports or move to other sides
- Increase of spacing between macros
- Add proper blockages and halos
- Block resizing to reduce overall congestion
- Macro pins should face towards the logic region

Placement

➔ **Checks after placement**

- Check legalization
- Check PG connection
- Check congestion and density maps
- Horizontal and vertical congestion should be analyzed
- Timing - WNS and TNS should be under control
- Setup timing violation is understood
- Don’t touch cells and nets should be preserved

Placement

➔ **Checks after placement**

- Routability
  - After placing all the standard cells, based on the density and congestion values, we should be able to estimate the difficulty in the level of routing.
  - Optimization after placement step also helps in minimizing the route length and optimizing the route.

Placement

➔ **Checks after placement**

- Runtime
  - If high effort settings are selected, then the tool takes a longer run time to achieve the target - Good floorplan skills help to reduce placement runtime a lot
  - Tool may not find the right location to place the cell during optimization - longer run time
  - Longer run time during legalization - congestion in the area

Placement

➔ Placement optimization

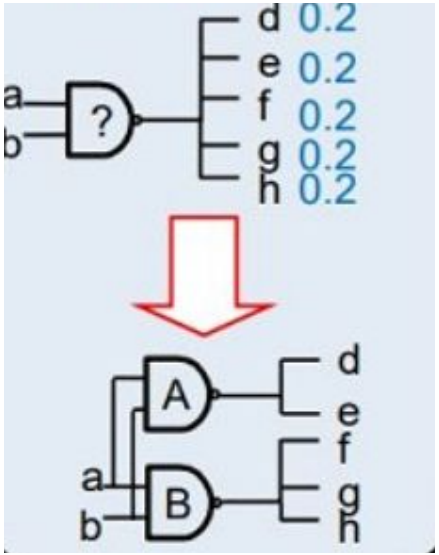
- Cell sizing - upsize - timing - downsize - area
- VT swapping - optimize leakage power - HVT, LVT, SVT
  - HVT - saving power - less leakage - timing is not critical
  - LVT - consumes more power - high leakage - timing is critical
  - SVT - Medium power consumption - medium delay
  - Usage - HVT - SVT - LVT
- Cloning - fanout reduction
- Buffering - Long nets - Reduce delay

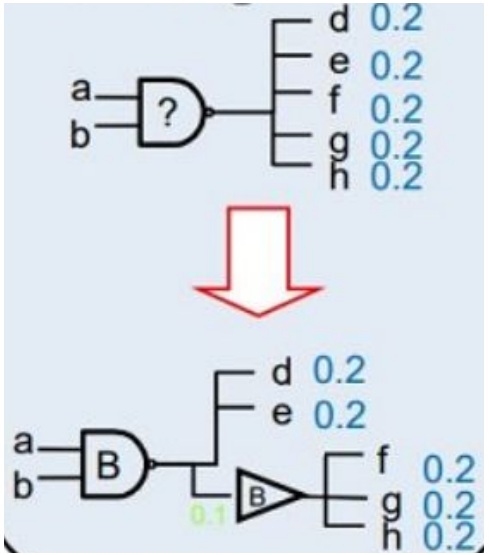
Placement

➔ **Placement optimization**

- Logic restructuring
  - Optimize timing and area - no change in function
  - Break complex cells to smaller cells

Placement


a
b
?
d 0.2
e 0.2
f 0.2
g 0.2
h 0.2
A
B
a
b
d
e
f
g
h


a
b
?
d 0.2
e 0.2
f 0.2
g 0.2
h 0.2
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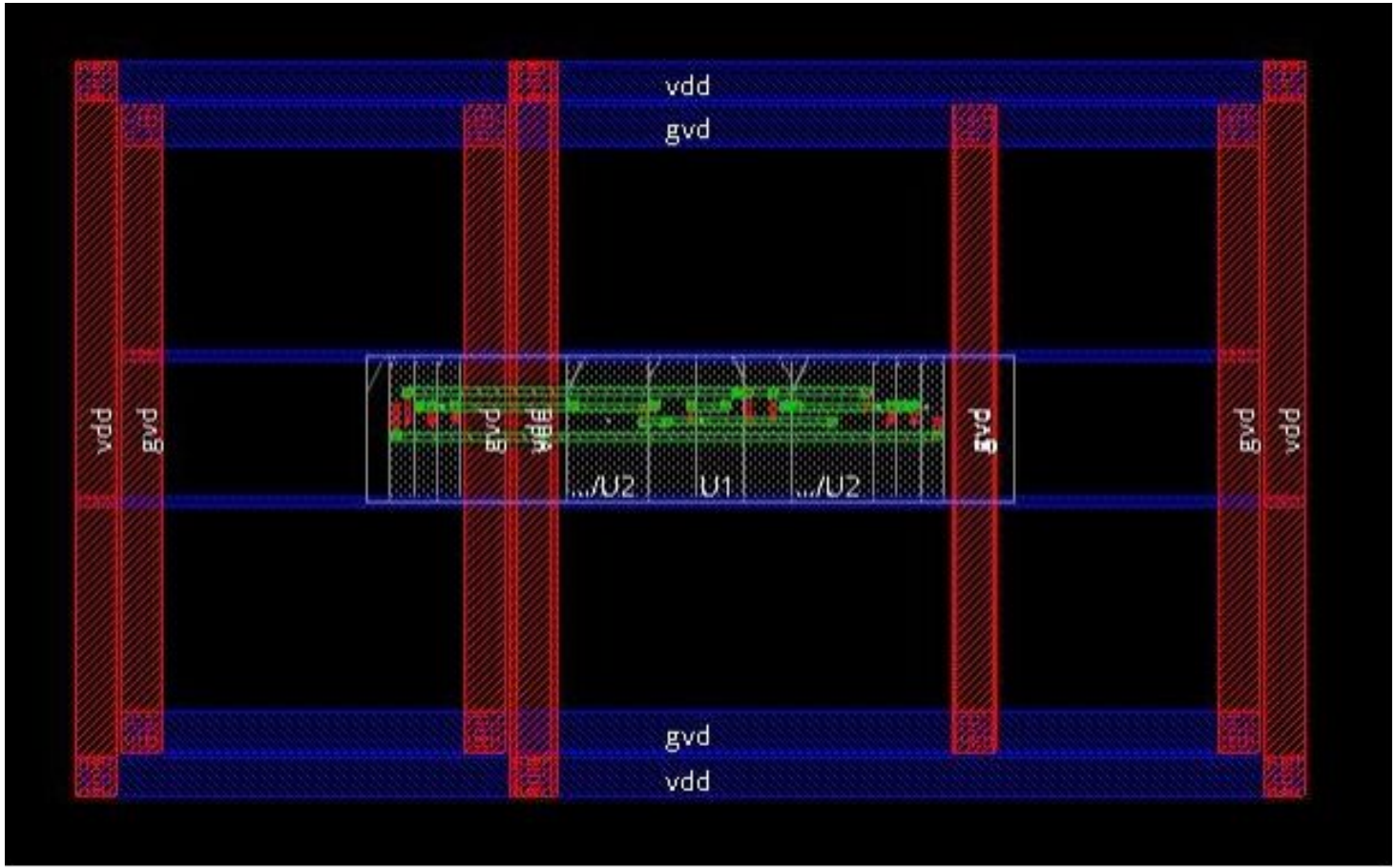
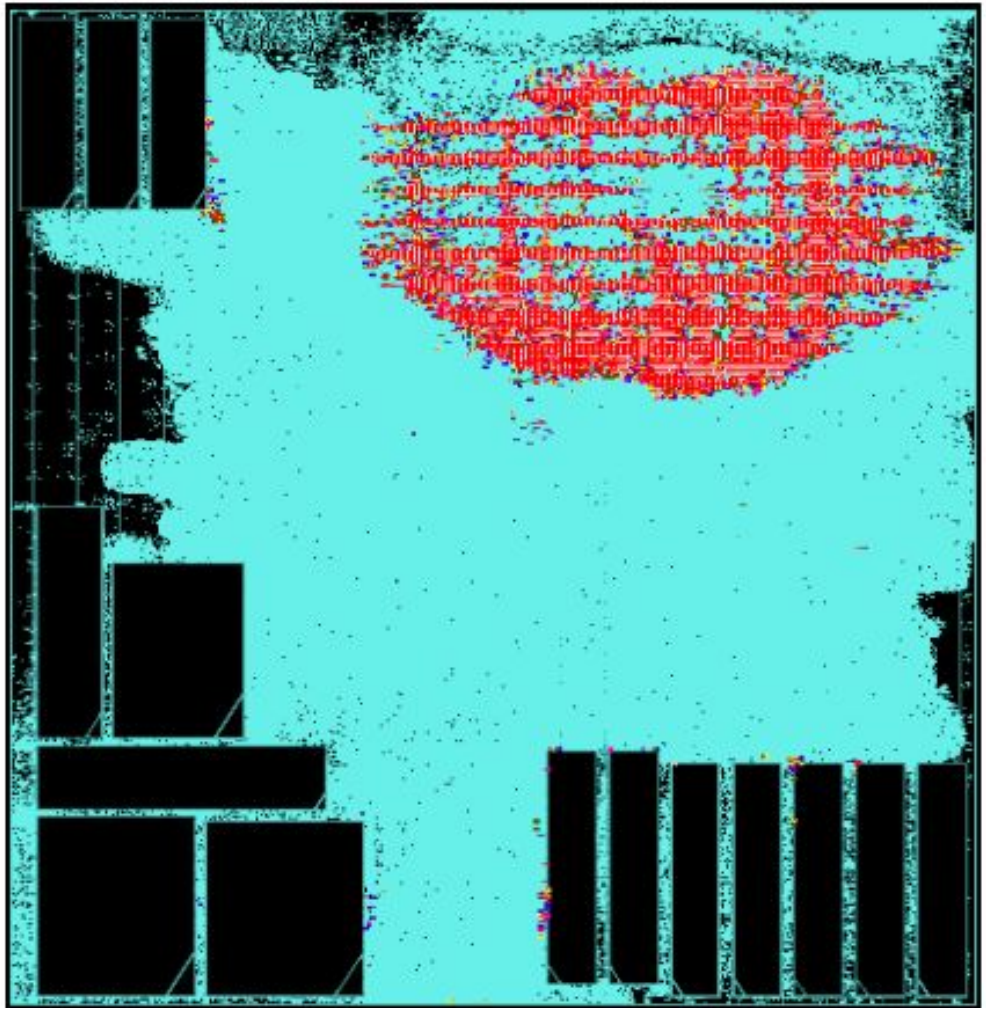
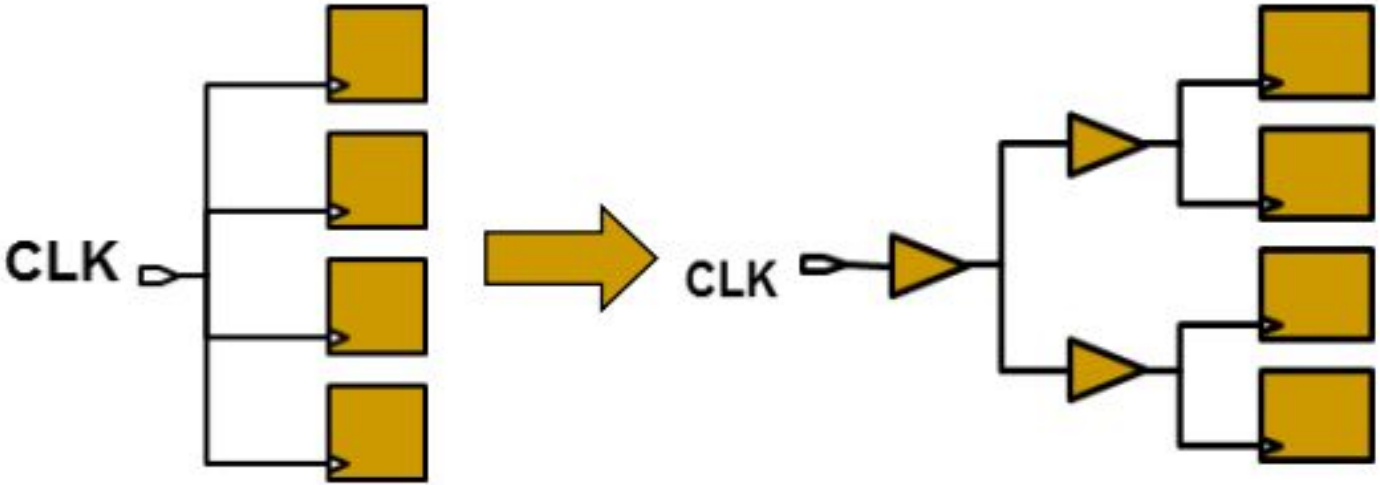
b
d 0.2
e 0.2
B
f 0.2
g 0.2
h 0.2


vdd
gvd
vdd
gvd
gvd
vdd
gvd
vdd
.../U2
U1
.../U2
gvd
vdd



CLOCK TREE SYNTHESIS



Technique to distribute the clock equally among all the flops in the design

Clock Tree Synthesis

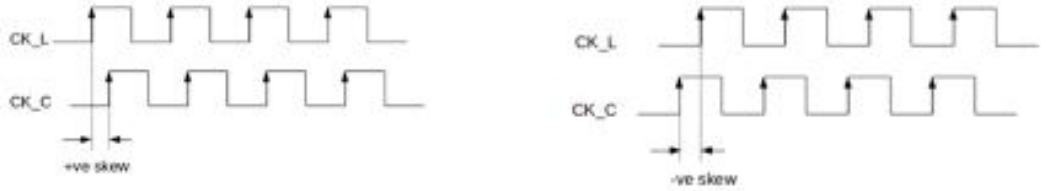
➔ **Terminology in CTS**

- **Clock skew -** Difference in clock arrival time between two different registers
- **Slew** - t(rise)/t(fall) of clock signal
- **Clock uncertainty** - Time difference between arrival of clock signals at registers in one clock domain or between domains

Clock Tree Synthesis

➔ Terminology in CTS

- **Positive skew** - Capture clock comes later than Launch clock
- **Negative skew** - Capture clock comes early than Launch clock
- **Local skew** - Difference in arrival of clock at two consecutive pins
- **Global skew** - Difference between shortest clock path delay and longest clock path delay
- **Useful skew** - skew inserted to resolve violation



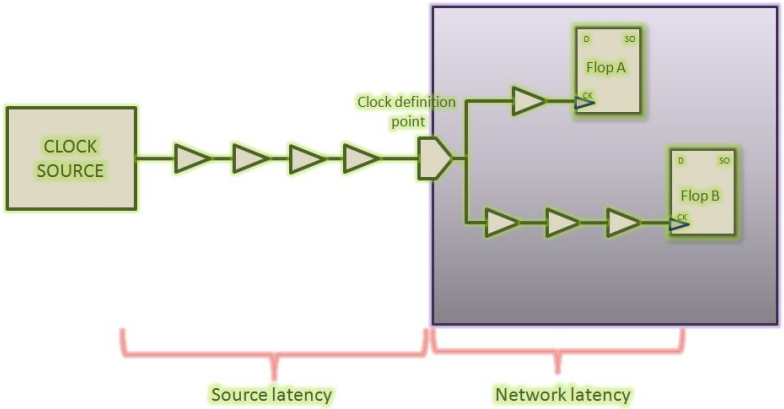
Positive and Negative Skew

Clock Tree Synthesis

➔ Terminology in CTS

◆ Clock Latency - virtual delay

- Source insertion latency + network delay
- Time taken by the clock signal to reach the register
- Target given to the tool through SDC

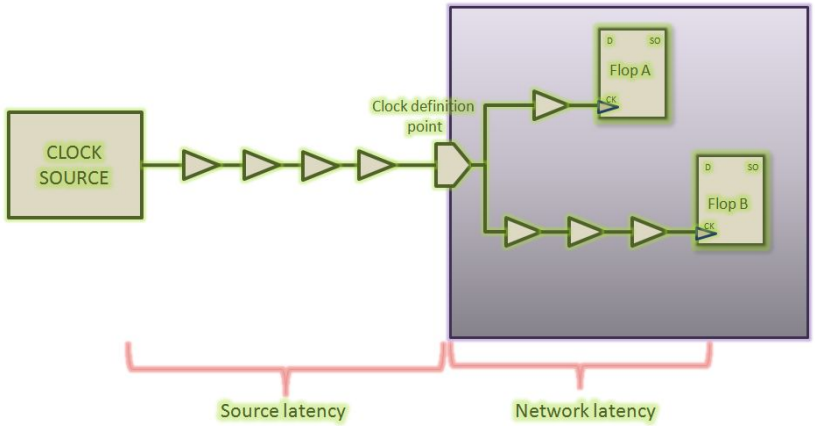


Clock Tree Synthesis

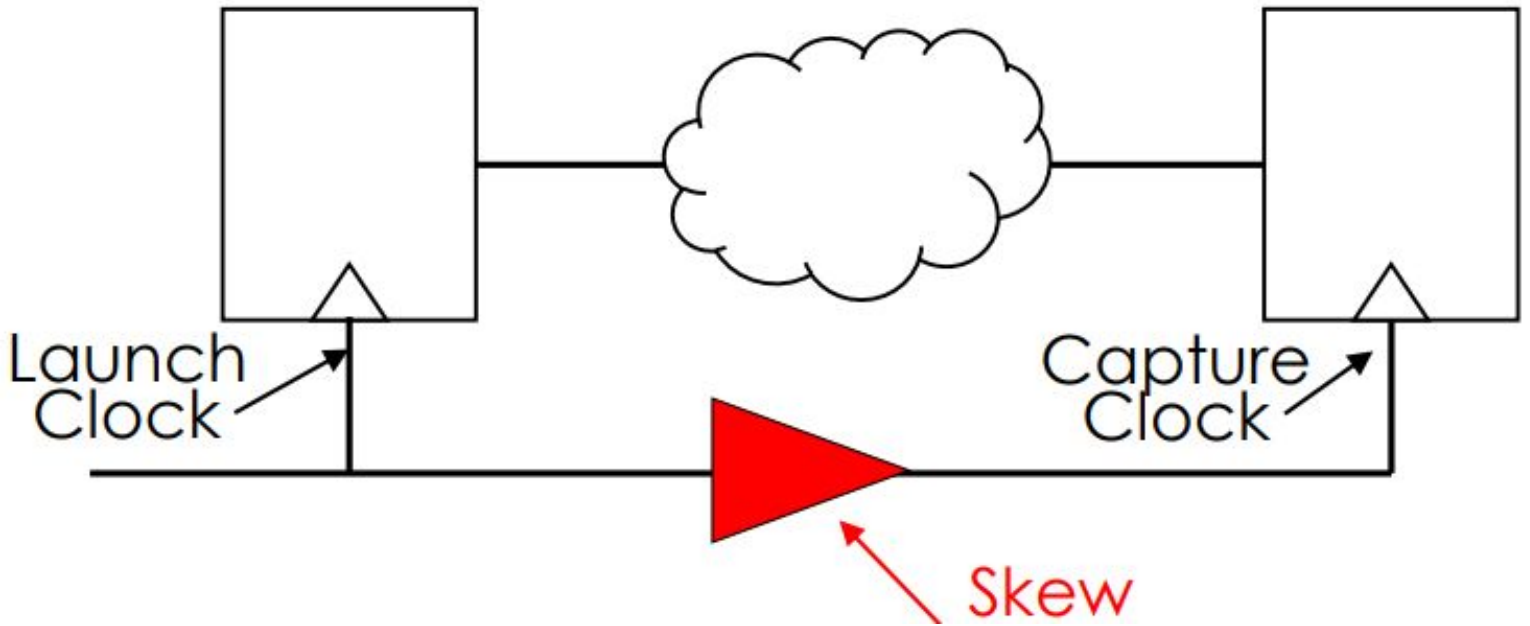
➔ Terminology in CTS

◆ Insertion delay - physical delay

- It is clock latency after synthesis
- Time taken by the clock signal to reach the register
- Delay achieved after CTS



Clock Tree Synthesis



Clock Tree Synthesis

➔ **Objectives of Clock Tree Synthesis**

- Minimum skew
- Minimum insertion delay
- Maximum transition
- Maximum capacitance

Clock Tree Synthesis

➔ **Checks before CTS**

- Legality
- Check power stripes and standard cell rail connections
- Setup time should be under control
- Congestion - CTS on a highly congested database will create further issues with respect to routability
- don’t_use attribute on clock buffers & inverters should be removed
- Density of the design

Clock Tree Synthesis

➔ **Inputs for CTS step**

- Placement DEF file
- Clock buffers and clock inverters in the library
- Clock tree constraints - latency, skew, max transition, max capacitance, max fan-out etc
- Clock spec file - insertion delay, skew, clock cells, NDR type, CTS exceptions, list of clock buffers and clock inverters etc.

Clock Tree Synthesis

➔ **Outputs from CTS step**

- Timing report
- Congestion report
- Skew report
- Insertion delay report
- CTS DEF file

Clock Tree Synthesis

➔ **Effects of CTS**

- Addition of clock buffers and clock inverters
- Increase in Congestion
- Crosstalk noise

Clock Tree Synthesis

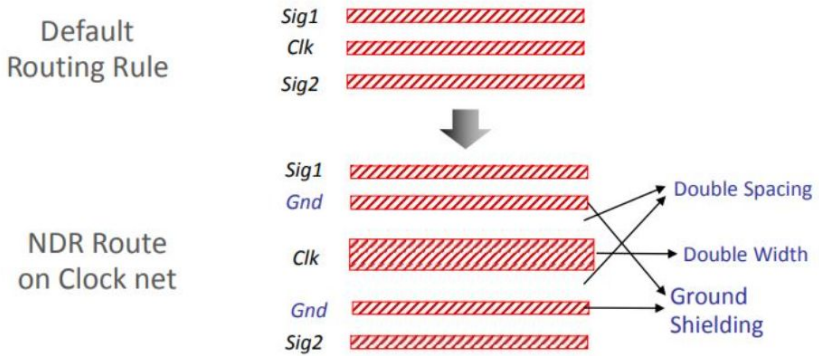
➔ **How is CTS achieved ?**

- Addition of clock buffers and clock inverters
  - To balance the clocks and minimize skew
  - To meet the max tran and max cap violations
- Non Default Rules (NDR) is applied to clock nets.

Clock Tree Synthesis

➔ **Non Default Routing Rules and shielding**

- Improve insertion delay
- Double / Triple width - EM
- Double / Triple spacing - Cross talk



Clock Tree Synthesis

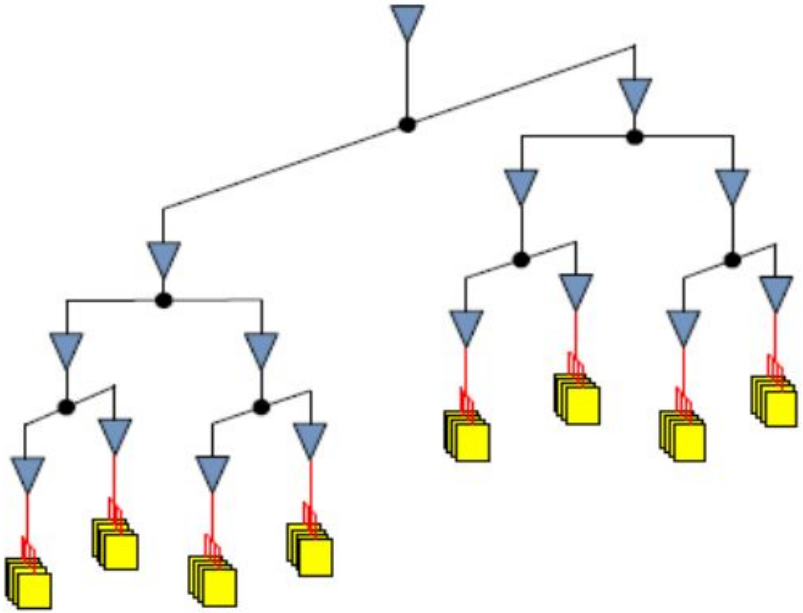
➔ **Clock buffers and clock inverters**

- Clock inverters are used for clock tree building and clock buffers for clock tree balancing.
- Clock buffers have equal rise and fall time maintaining 50% duty cycle.
- Clock buffers are increased in size than normal buffers.

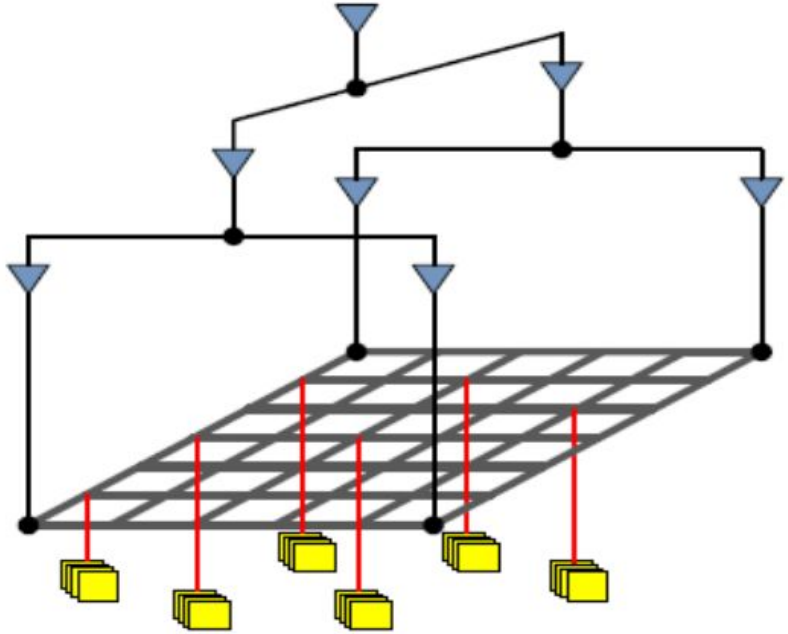
Clock Tree Synthesis

➔ **HFNS vs CTS**

- Clock inverters and clock buffers - CTS
- Normal buffers and inverters - HFNS
- HFNS - reset, scan enable and static signals
- CTS - clocks as it`s constantly switching and active



Clock Tree (Conventional CTS)



Clock Mesh

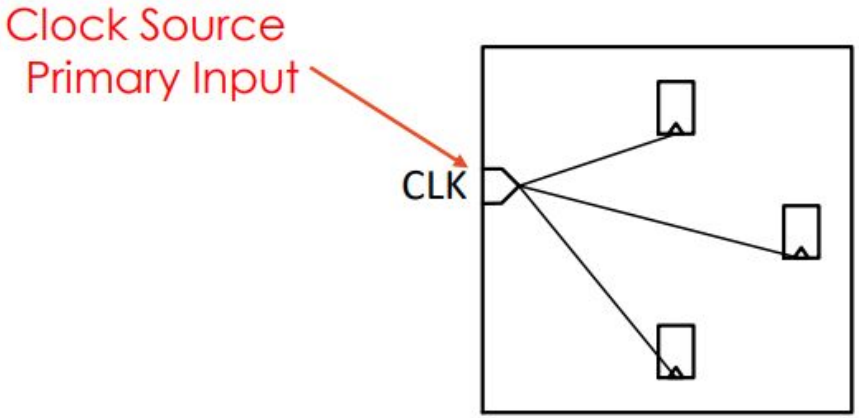
Clock Tree Synthesis

- **Clock Concurrent Optimization (CCOpt)**
  - CCOpt Methodology - CTS flow
    - Build a clock tree - fix DRVs
    - Fix timing (setup & hold) violations, if any.
    - The timing paths should come from the same clock branch and great efforts in skew balancing is reduced.

Clock Tree Synthesis

➔ Clock Source

- It is a primary input to the design.
- It is also the pin from which a clock usually fans out.
- This can occur at a gate output and macro output.



Clock Tree Synthesis

➔ **Clock Sink**

- The pin which receive the clock signal is known as clock sink (primary output).

➔ **Skew group**

- All the sinks of a clock tree are in the same skew group. Skew within the same group can be easily balanced.

Clock Tree Synthesis

➔ Clock Tree Analysis

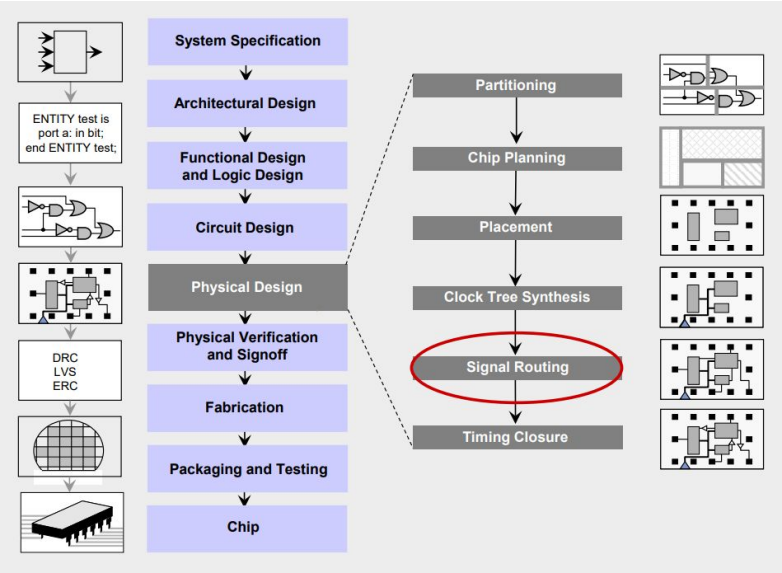
- Report timing path - Setup & Hold
- Report insertion delay and skew
- Report fanouts, Capacitance and Transition
- Check if the clock sink is reached
- Clock tree exceptions applied
- Check log files
- Check Design Rule constraints
- Check Routing constraints
- Report power and area

Clock Tree Synthesis

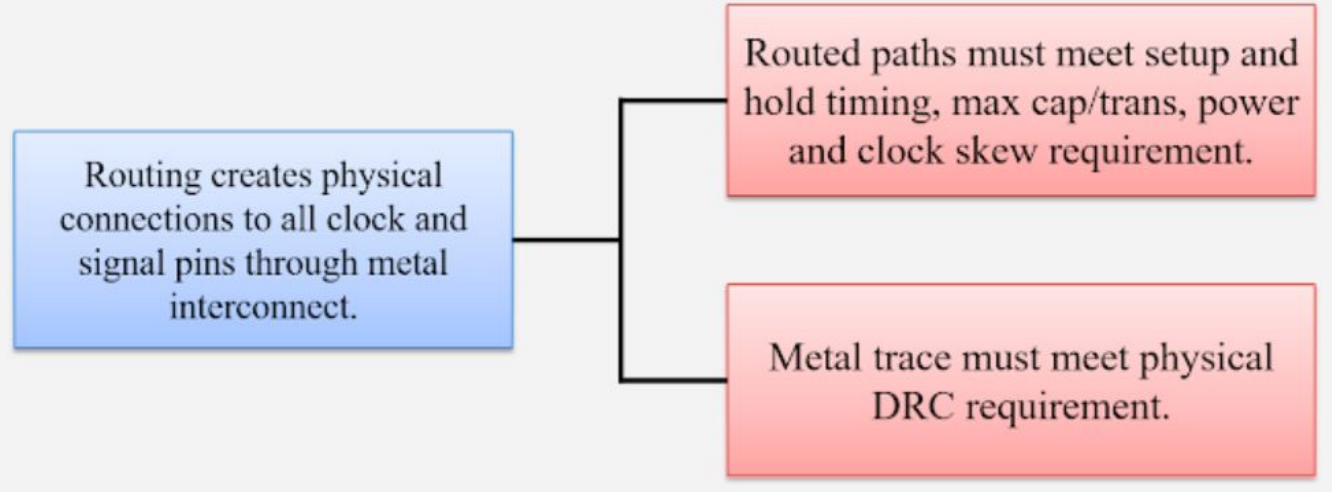
➔ **Post CTS Optimization**

- Optimization with useful skew
- Shielding
- Buffer resizing
- Buffer relocation
- Fix hold time first - Best and Worst corner
- Area optimization

ROUTING


ENTITY test is
port a: in bit;
end ENTITY test;
DRC
LVS
ERC
System Specification
Architectural Design
Functional Design
and Logic Design
Circuit Design
Physical Design
Physical Verification
and Signoff
Fabrication
Packaging and Testing
Chip
Partitioning
Chip Planning
Placement
Clock Tree Synthesis
Signal Routing
Timing Closure

Routing


Routing creates physical connections to all clock and signal pins through metal interconnect.
Routed paths must meet setup and hold timing, max cap/trans, power and clock skew requirement.
Metal trace must meet physical DRC requirement.

Goals of Routing

- ➔ Minimize the total wire length in the design
- ➔ Minimize the critical path delay
- ➔ Minimize congestion hotspots
- ➔ Minimize the number of metal layer changes
- ➔ Open/shorts clean
- ➔ Routed nets must meet setup and hold time
- ➔ Minimal DRC and LVS violations
- ➔ Design is 100% routed
- ➔ Timing DRCs is met
- ➔ Power, Performance and Area is good
- ➔ Crosstalk noise reduction

Pre - route checks

- ➔ All standard cells and macros should be placed in the core area.
- ➔ CTS should be properly done and clock nets routed.
- ➔ Setup and Hold time should be acceptable, congestion should be under control.
- ➔ Physical pins accessibility in the standard cells
- ➔ No overlapping cells in the design as they cause pins to short and cause metal DRC violations
- ➔ Check if the ports of macro cell are blocked or accessible
- ➔ Check if all pins in the design are on the routing tracks

Routing

➔ **Inputs for Route step**

- Netlist and DEF from CTS step
- Cells and ports must be legally placed
- Technology file
- SDC

➔ **Outputs from Route step**

- Routed DEF with no shorts and opens
- Timing and congestion report
- Skew and insertion delay report

Routing Order

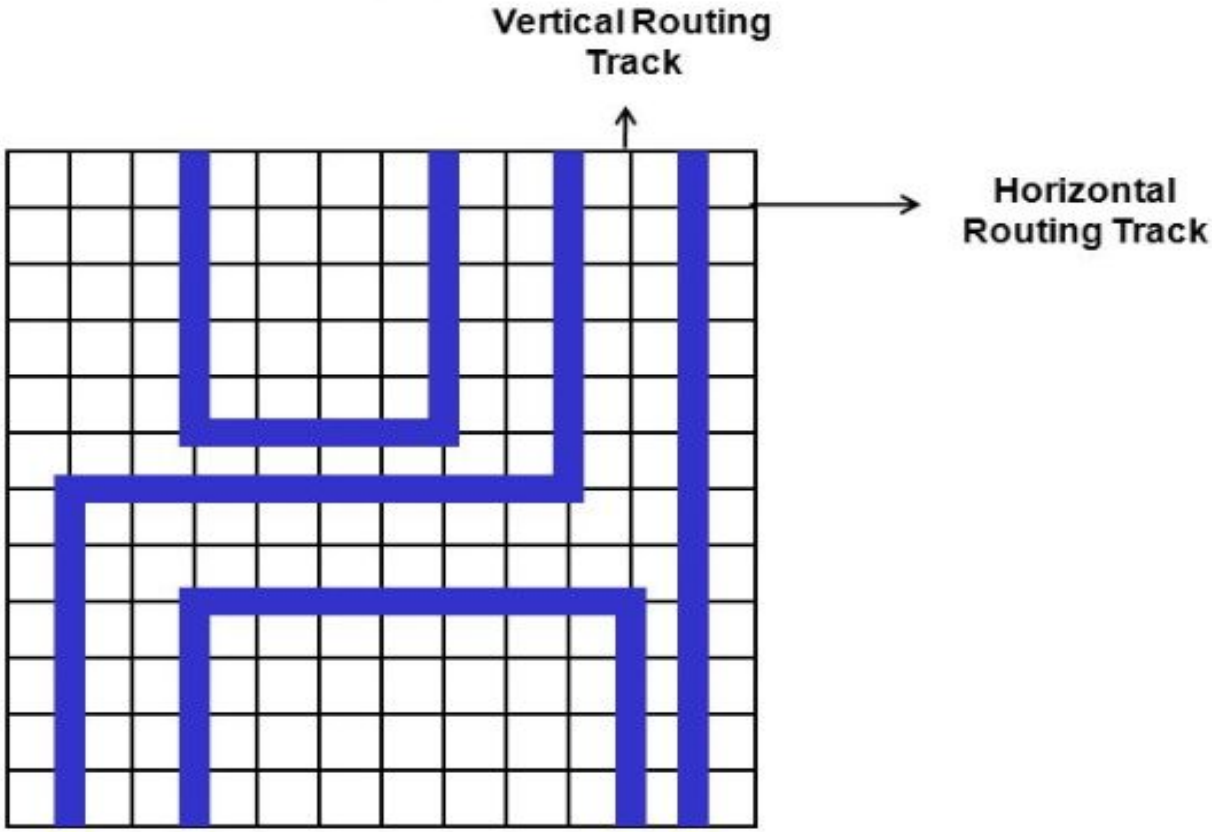
- **Power Routing**
  - Connecting the macro and standard cell power pins to the VDD and GND power stripes of the design
- **Clock Routing**
  - The clocks are given higher priority in using the routing resources.
  - Clock routing is limited to higher metal layers.

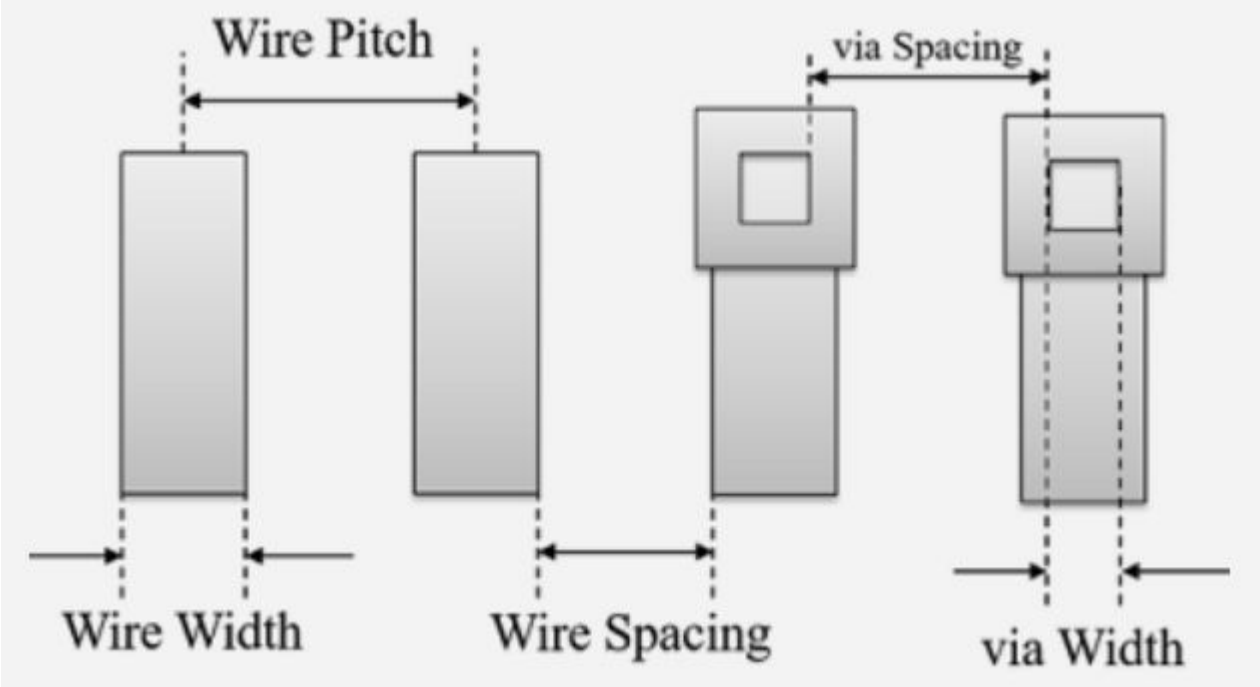
Routing Order

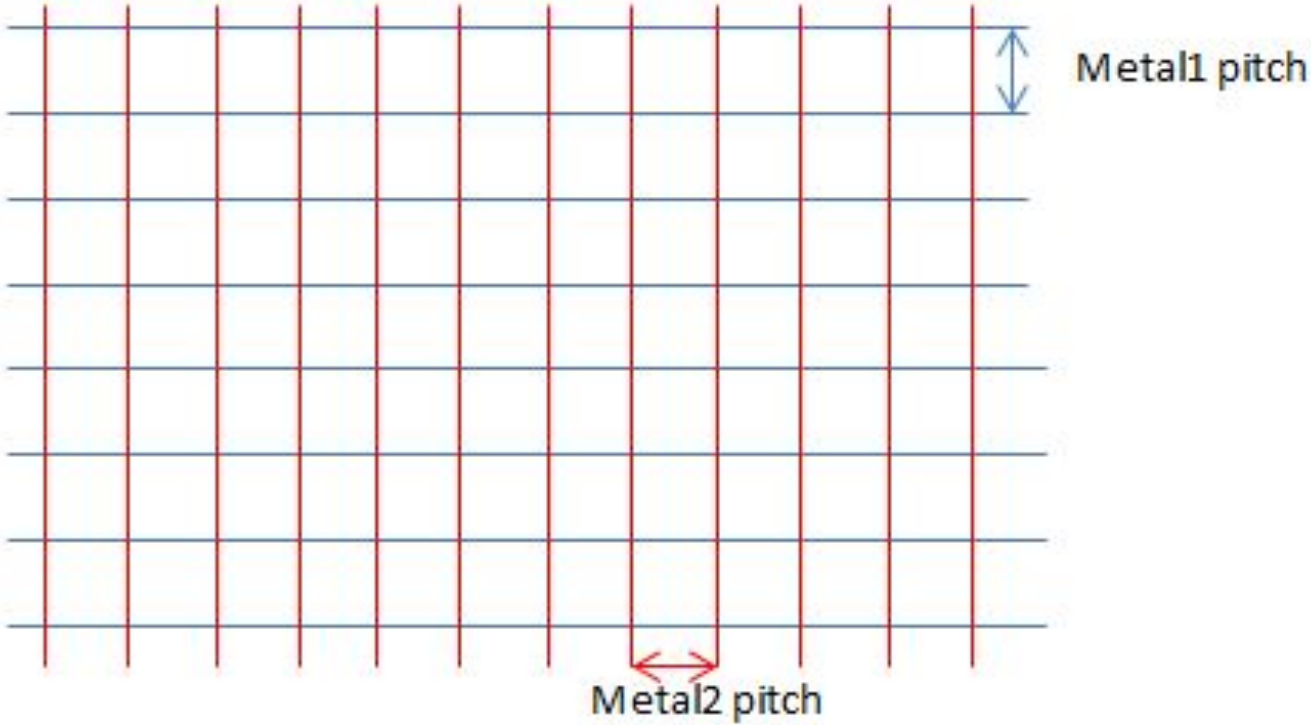
- **Signal Routing**
  - The rest of the nets in the design is routed.
  - The entire routing resources can be used at this stage as power and clock nets are already routed.

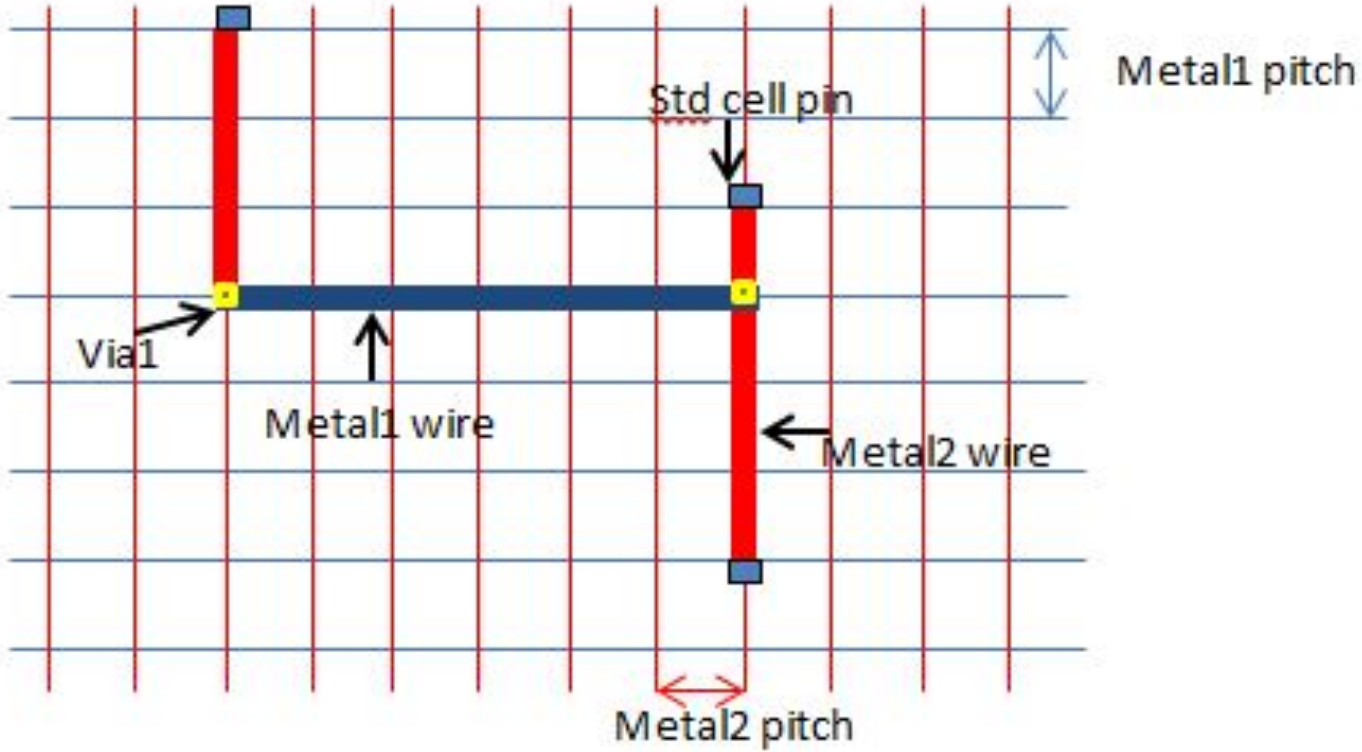
Routing Grids

- ➔ Routing grids are defined for the entire layout.
- ➔ Routing direction is defined for each metal layer.
- ➔ M1 will be assigned horizontal routing tracks with seperate pitch value and M2 will be assigned vertical routing tracks with seperate pitch value. M3’s horizontal routing track will be superimposed on M1’s routing track and so on.


Vertical Routing Track
Horizontal Routing Track


Wire Pitch
via Spacing
Wire Width
Wire Spacing
via Width

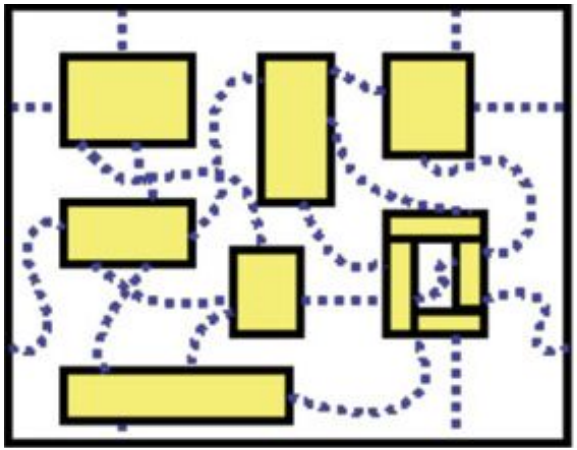

Metal1 pitch
Metal2 pitch


Metal1 pitch
Std cell pin
Via1
Metal1 wire
Metal2 wire
Metal2 pitch

Stages of Routing

Global Routing

- ➔ Identify routable path for nets - shortest distance
- ➔ Avoids congested areas and long detours
- ➔ Avoids routing over blockages
- ➔ Avoids routing over pre-routed nets



Objectives of Global Routing

- ➔ Minimize overflow of congestion
- ➔ Reduce total wire length
- ➔ Run time reduction

Types of Global Routing

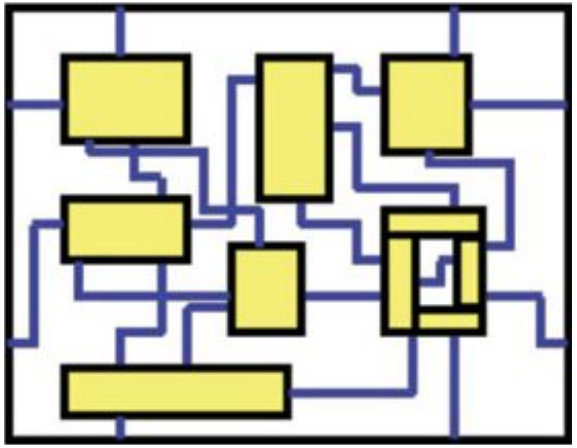
- ➔ Time-Driven - The wire delays are calculated before global routing.
- ➔ Cross-Talk Driven - Avoids the creation of long paths that run parallel on adjacent tracks.

Tracking Assignment

- ➔ Takes the Global routed layout and assigns each net to the track.
- ➔ Helps to fix all the overlaps in routes
- ➔ Via minimization in routed nets happens
- ➔ Timing is taking into consideration
- ➔ DRC is not taking into account

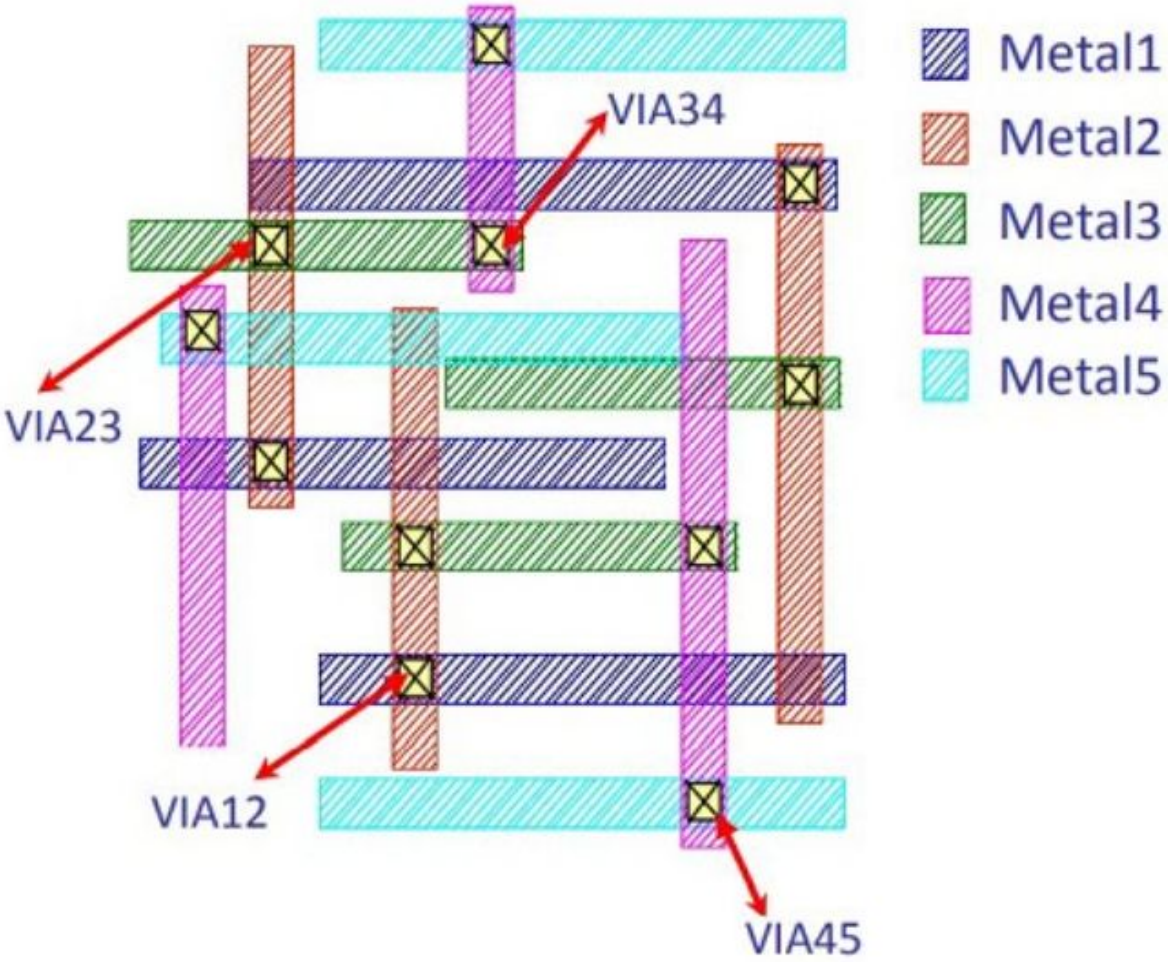
Detailed Routing

- The detailed router uses the routing plan created during Global Routing and Track assignment and lays actual metal layers
- DRC and timing aware routing takes place
- Final stage of routing
- Violations created during Track assignment stage are fixed



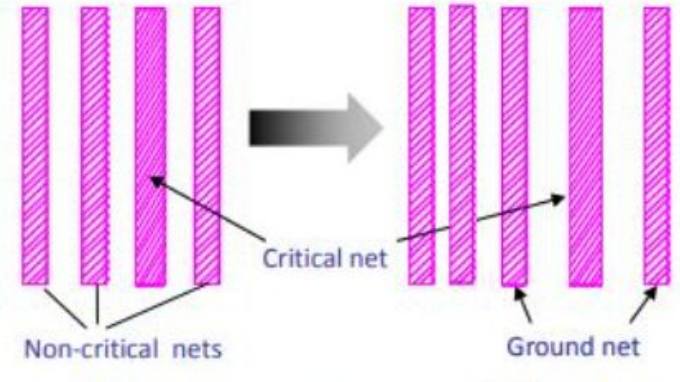
Search and Repair

- ➔ This step is performed along after the first iteration of detailed routing.
- ➔ The spacing violations and shorts are completely fixed in this process.


VIA34
VIA23
VIA12
VIA45
Metal1
Metal2
Metal3
Metal4
Metal5

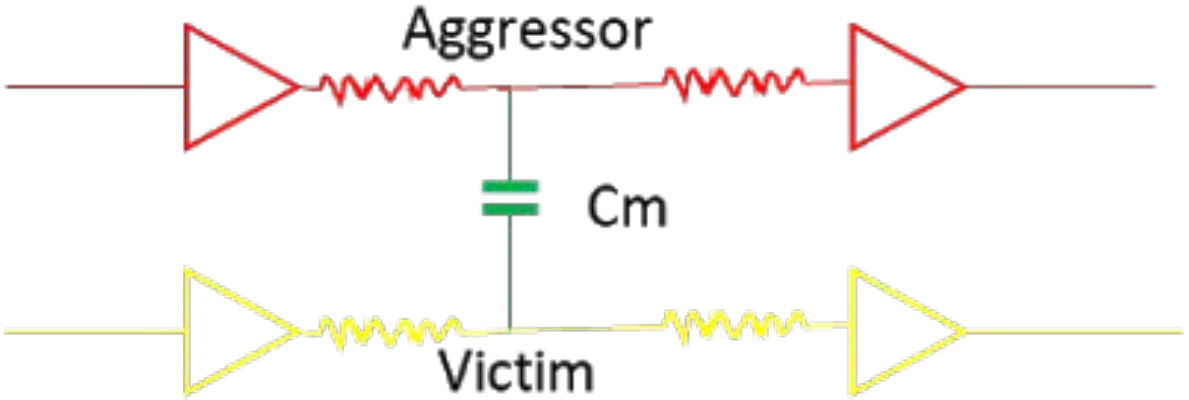
Post route optimization

- ➔ Signal integrity optimization and shielding sensitive nets
- ➔ Timing is also optimized - buffering, cloning etc
- ➔ DRC violations are also fixed



Signal Integrity

- ➔ Signal integrity during routing is closely associated with crosstalk.
- ➔ A switching signal will affect the neighbouring net.
- ➔ The affected net is called the victim.
- ➔ The switching net is called the aggressor.



Signal Integrity

➔ The signal will slow down when the aggressor and victim switch in the opposite direction.

➔ The signal will speed up when the aggressor and victim switch in the same direction.

Signal Integrity

➔ **Crosstalk prevention**

- Limit length of parallel nets
- Shield special nets
- Upsize driver or buffer

Routing Congestion

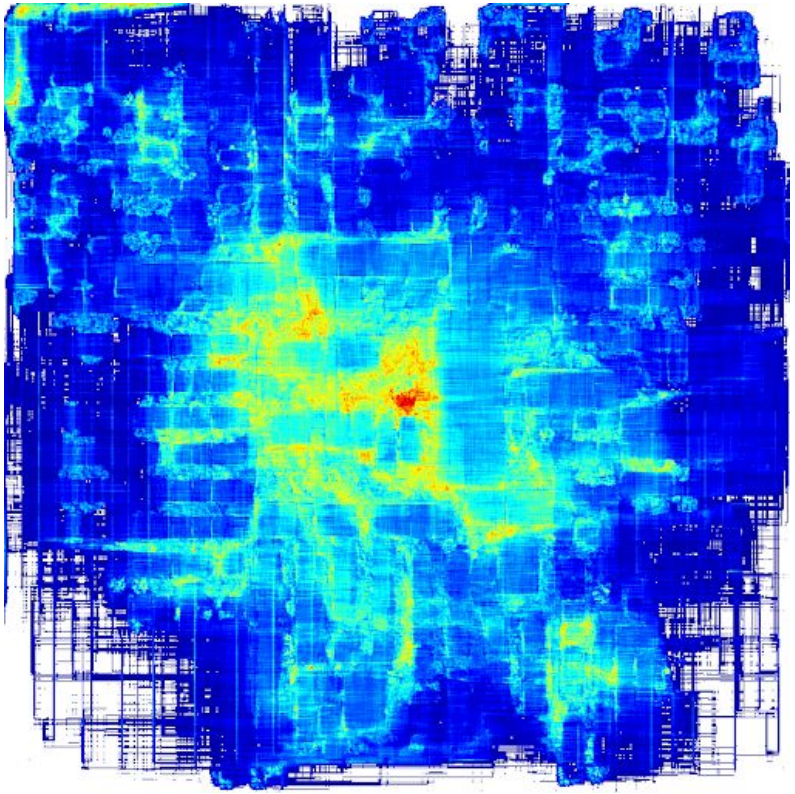
➔ Routing congestion occurs when routes need to go through a specific area that does not have enough routing resources.

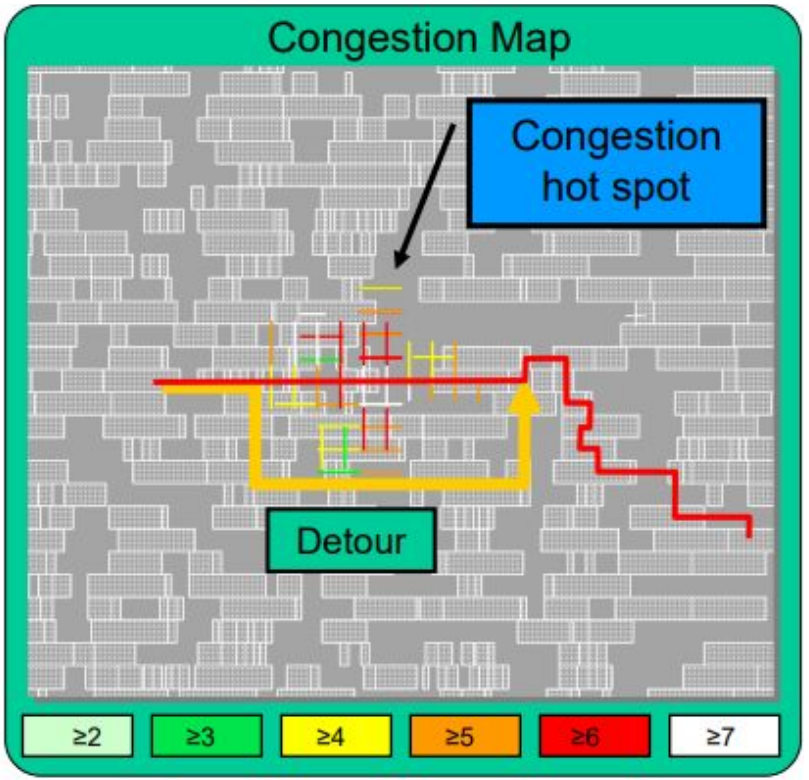
➔ **Causes of Congestion**

- Floorplan congestion - between memories / area around macros
- High placement density - clustering of standard cells in one area
- Logic induced congestion - number of connections in one area

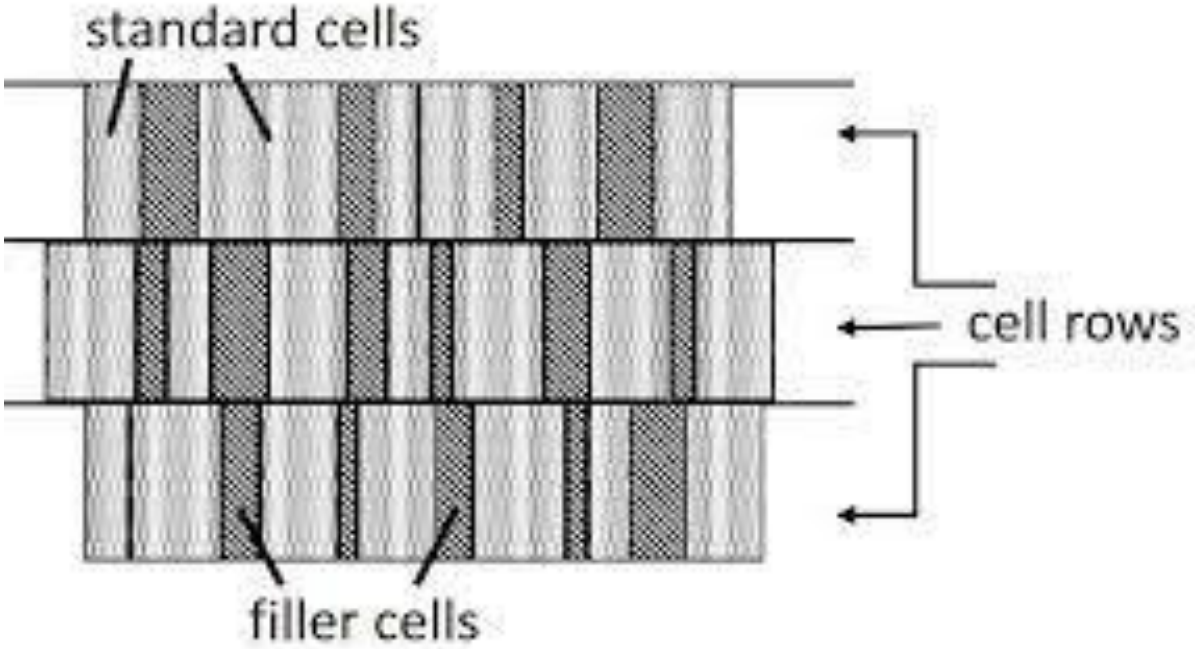
Routing Congestion

- **Strategies to fix congestion**
  - **Floorplan congestion**
    - Change in macro orientation
    - Placement blockages
    - Creating more space around macros
  - **High placement density**
    - Spread the standard cells




Congestion Map
Congestion hot spot
Detour
≥2
≥3
≥4
≥5
≥6
≥7

Filler Cells



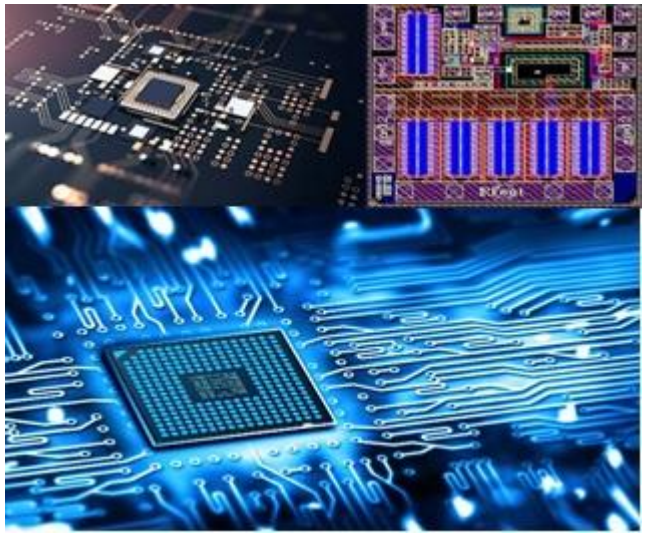
Metal Fills

- ➔ Filling up empty metal tracks with metal shapes
- ➔ They are floating metal nets which are considered as dummy metal layers and they are placed in empty spaces of the design in order to maintain the uniformity in metal layer density
- ➔ They are added to meet the metal density DRC rules in order to avoid density violations

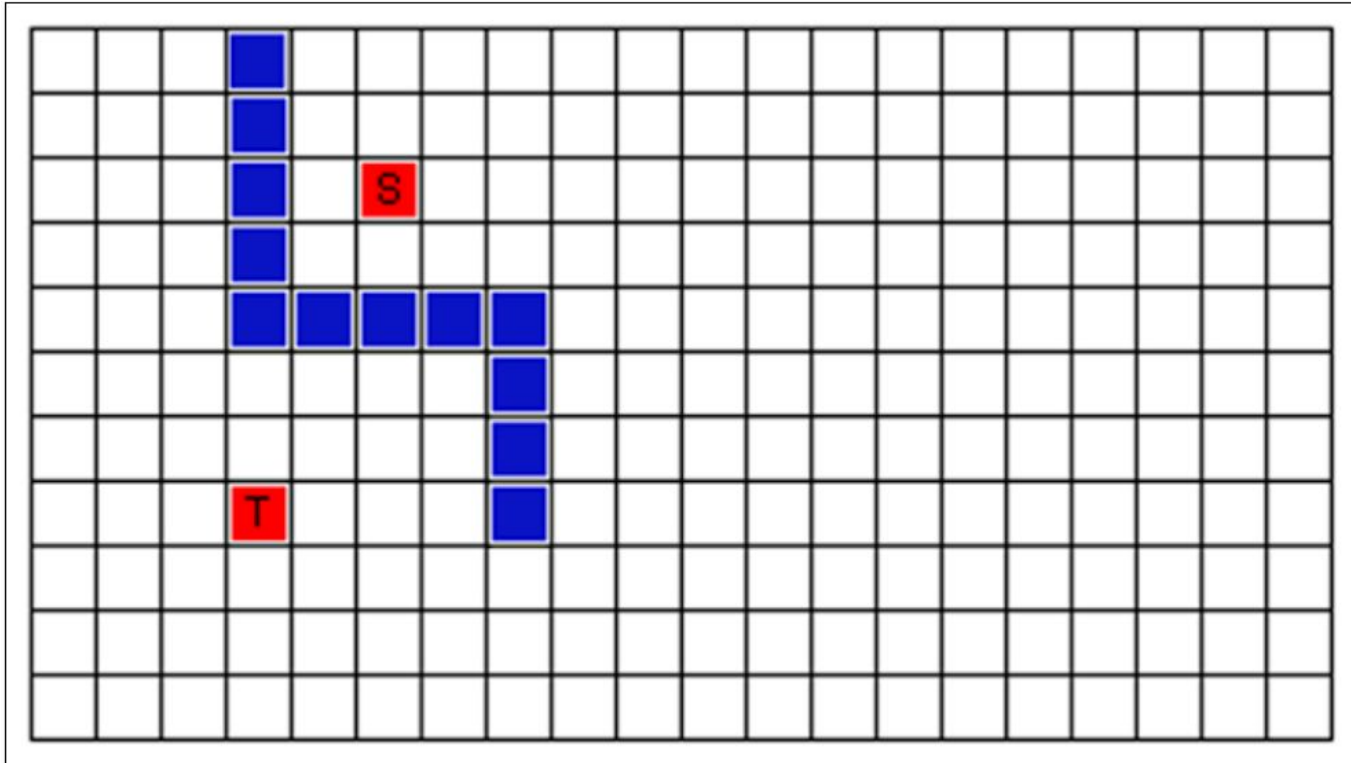
Checklist after Routing

- ➔ Filler cell insertion
- ➔ Final utilization
- ➔ Congestion
- ➔ Power consumption
- ➔ Setup and hold time
- ➔ DRC violations
- ➔ Routing in which layers

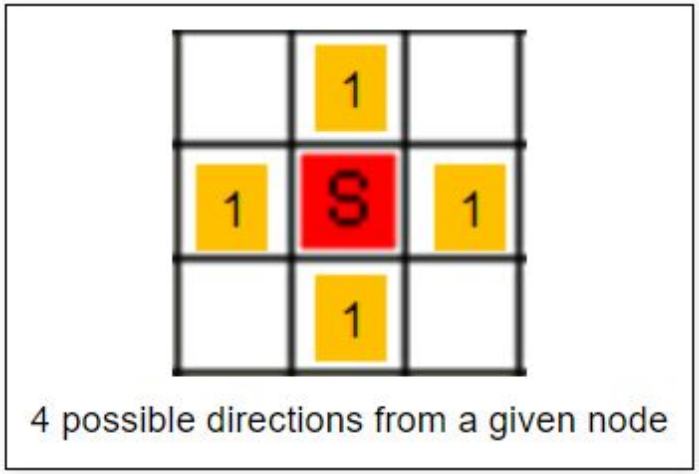
ROUTING ALGORITHM



MAZE ROUTER - Lee`s Algorithm

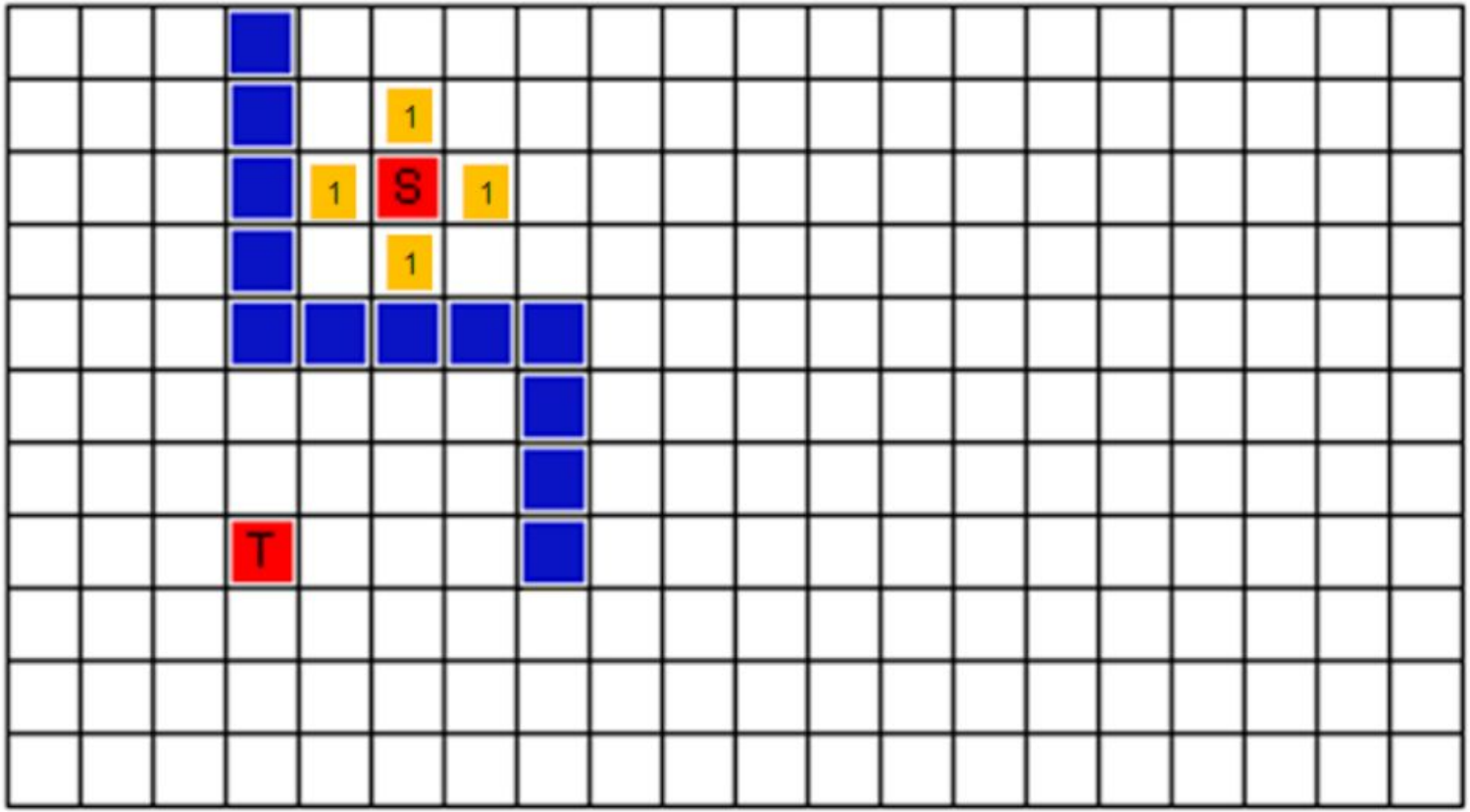


MAZE ROUTER - Lee`s Algorithm

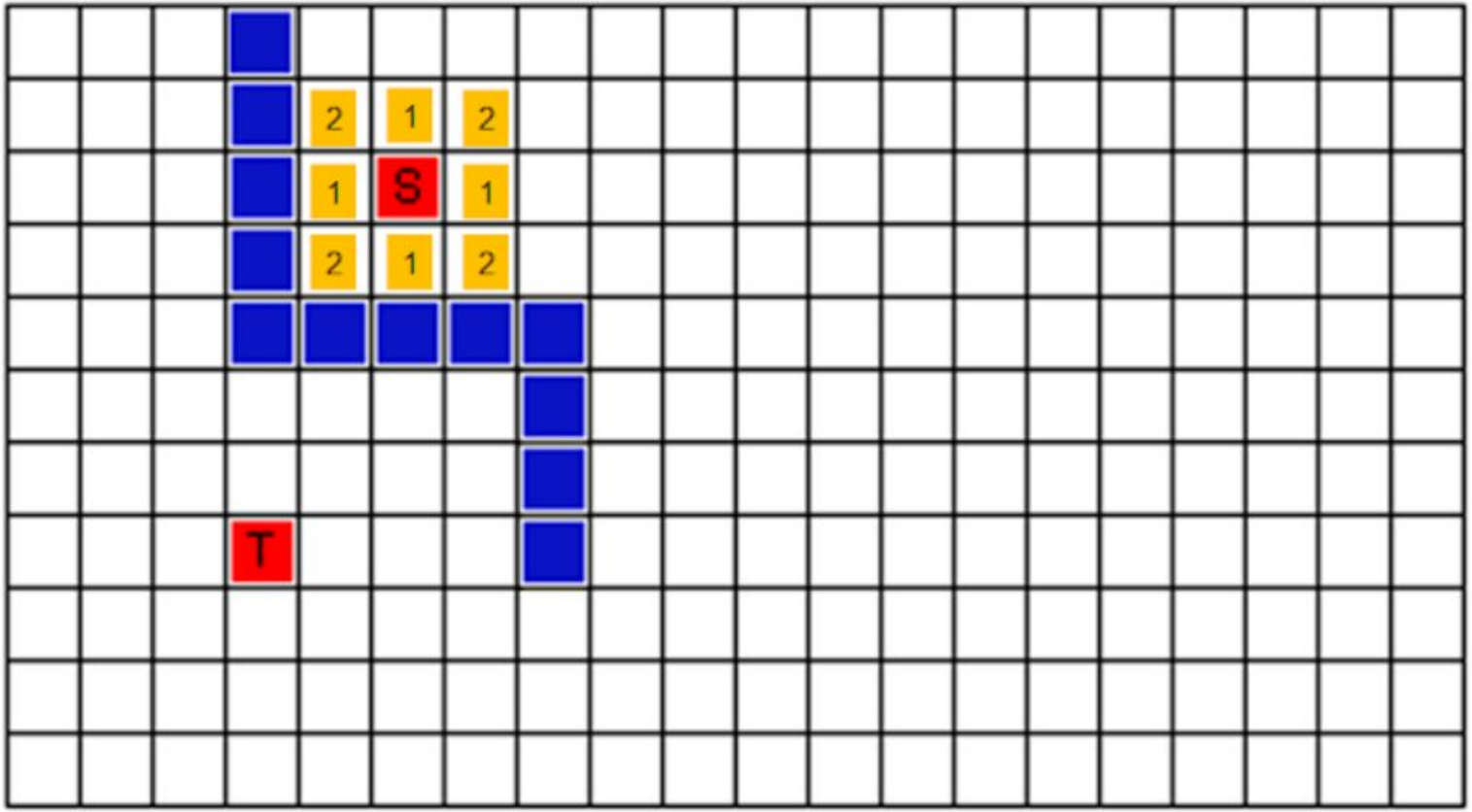


4 possible directions from a given node

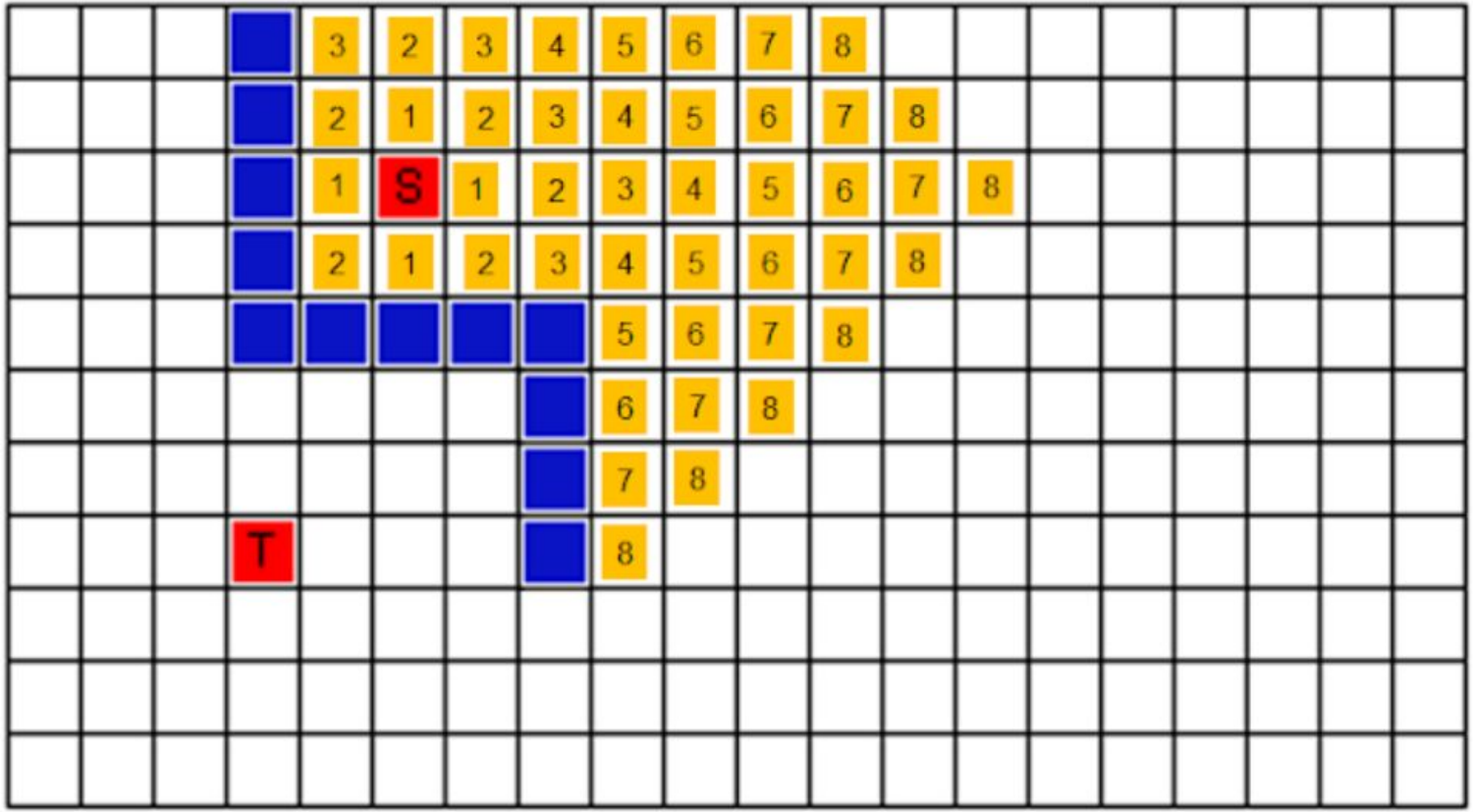
MAZE ROUTER - Lee`s Algorithm



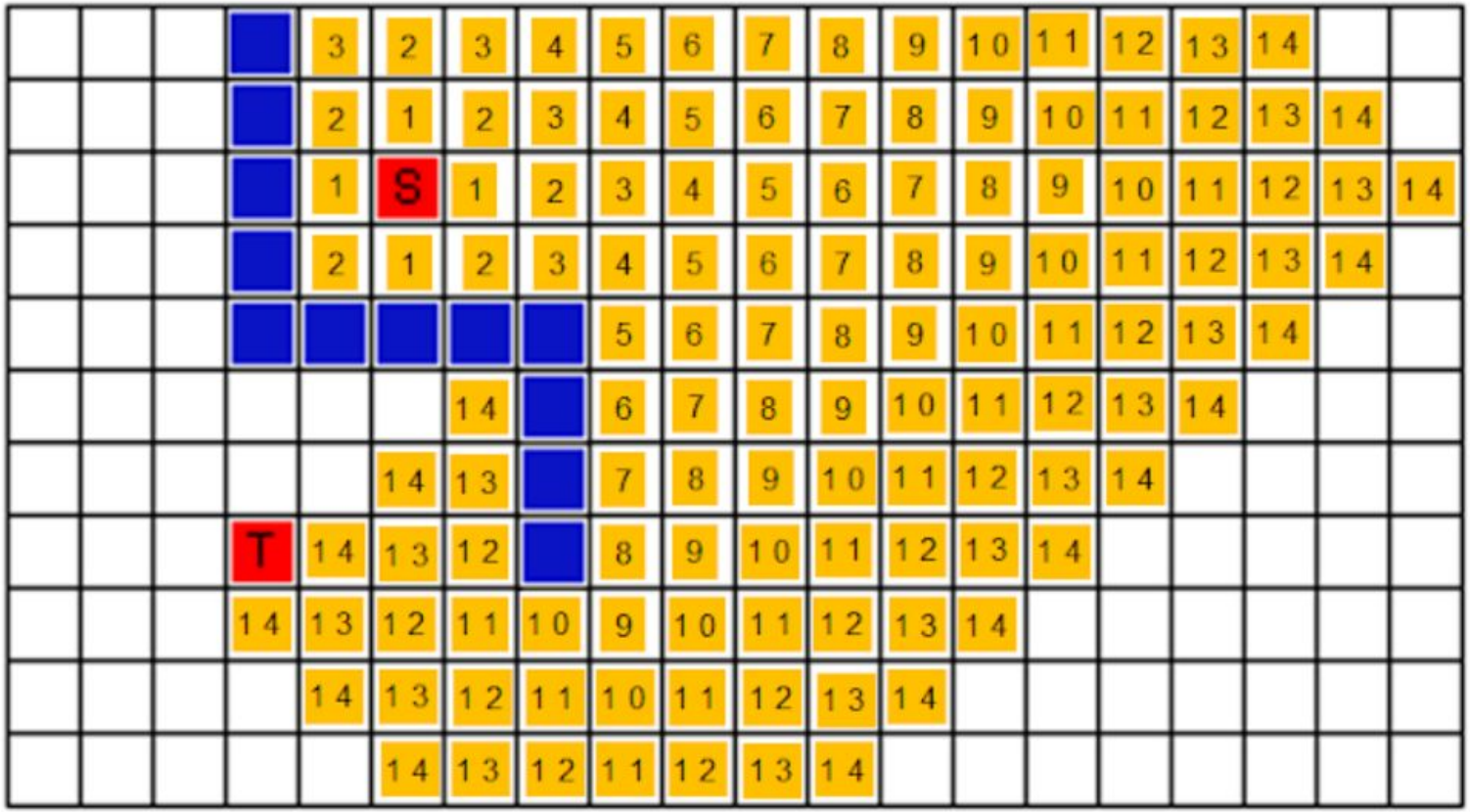
MAZE ROUTER - Lee`s Algorithm



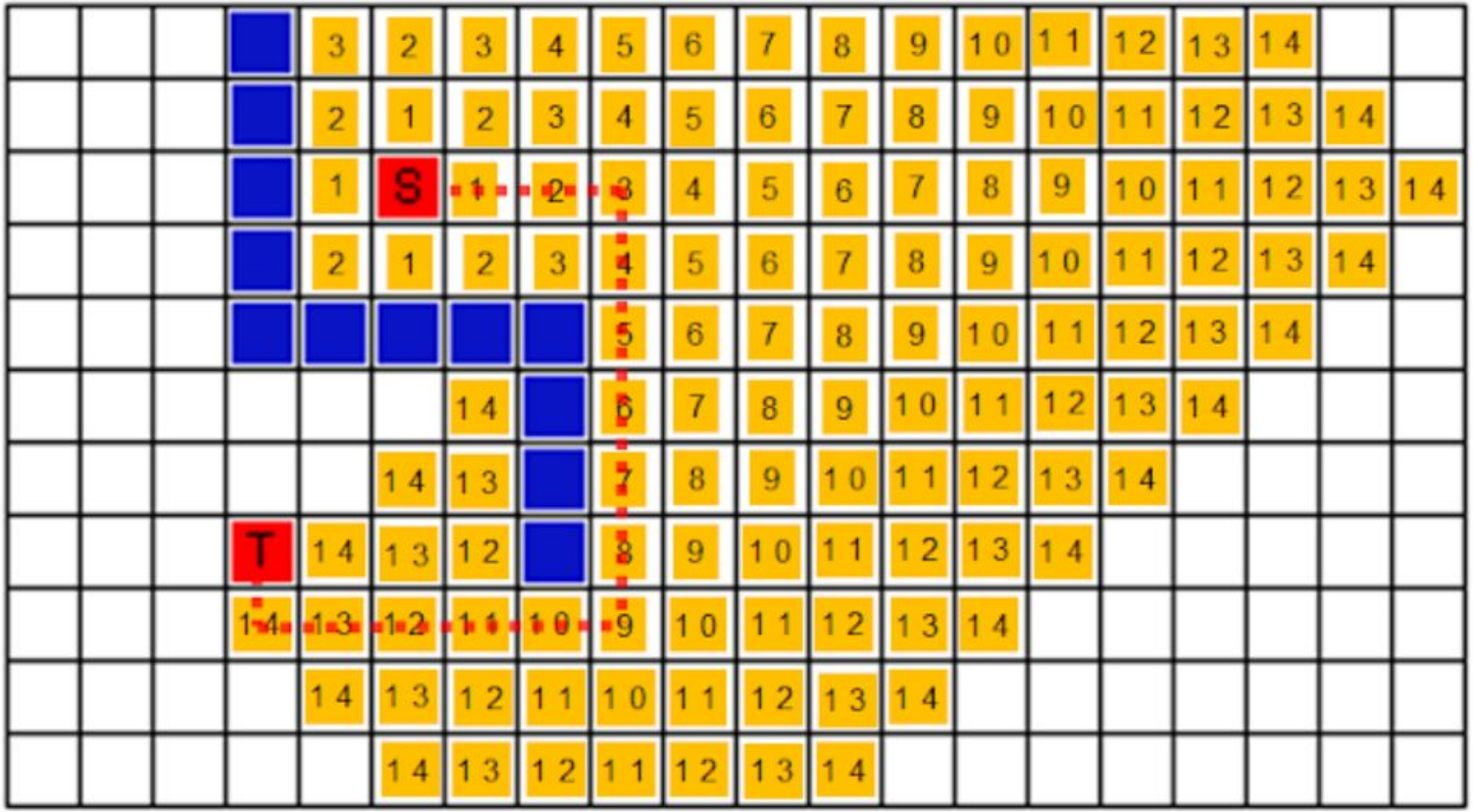
MAZE ROUTER - Lee`s Algorithm



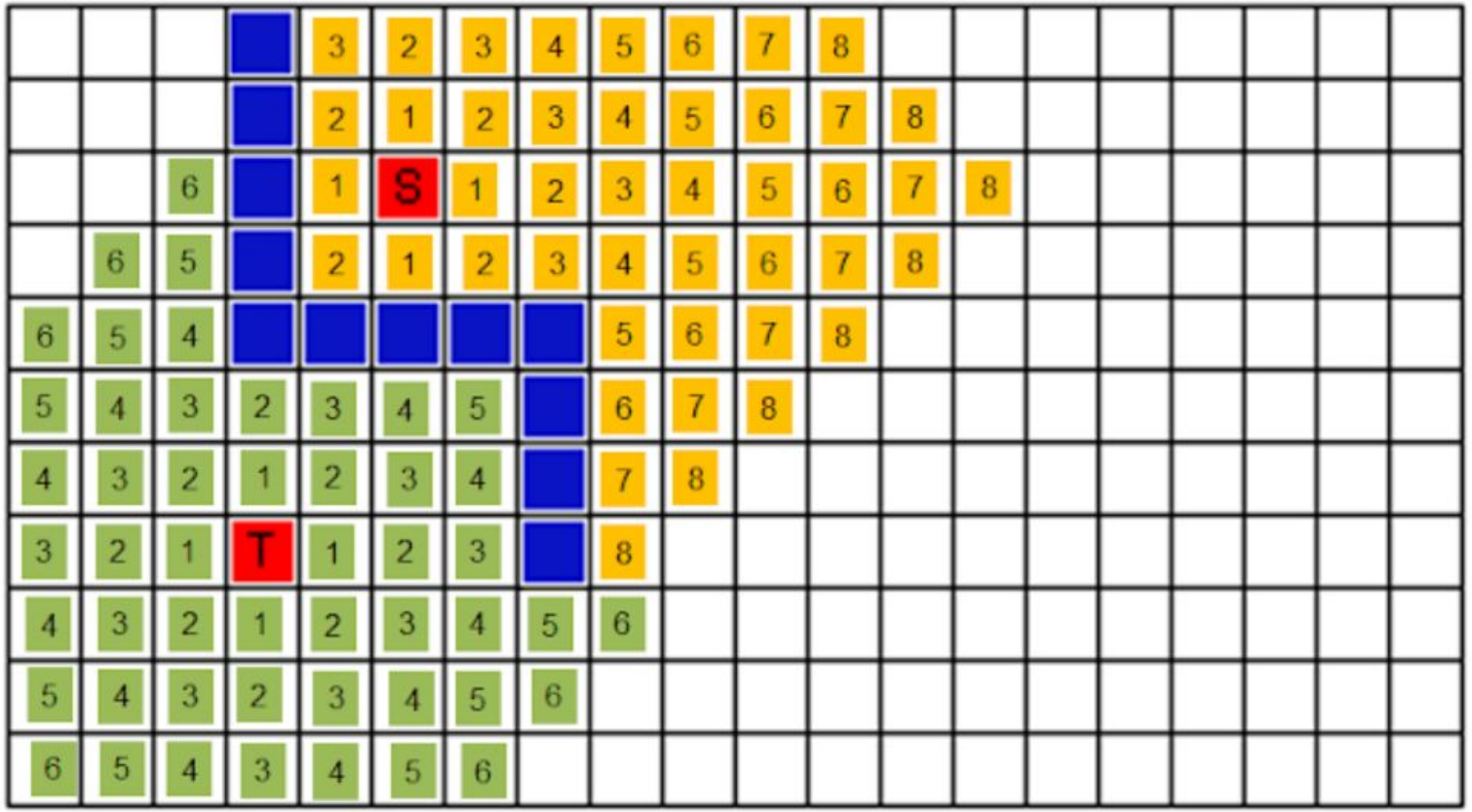
MAZE ROUTER - Lee`s Algorithm



MAZE ROUTER - Lee`s Algorithm



MAZE ROUTER - Lee`s Algorithm

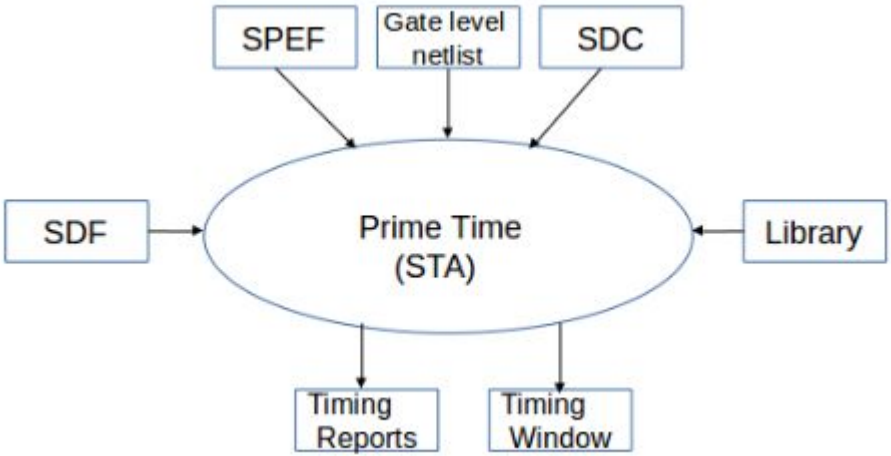


STATIC TIMING ANALYSIS

What is STA?

- ➔ Static timing analysis is one of the techniques used to verify the timing of a digital design.
- ➔ It makes sure that our design meets the timing constraints.
- ➔ STA can only check the timing and not the functionality of the circuit.

Inputs and Outputs of STA



STA Definitions

- Clock
  - It oscillates between a high and slow state.
  - Clock controls timing in the design.
  - Multiple clocks are present in a design.

STA Definitions

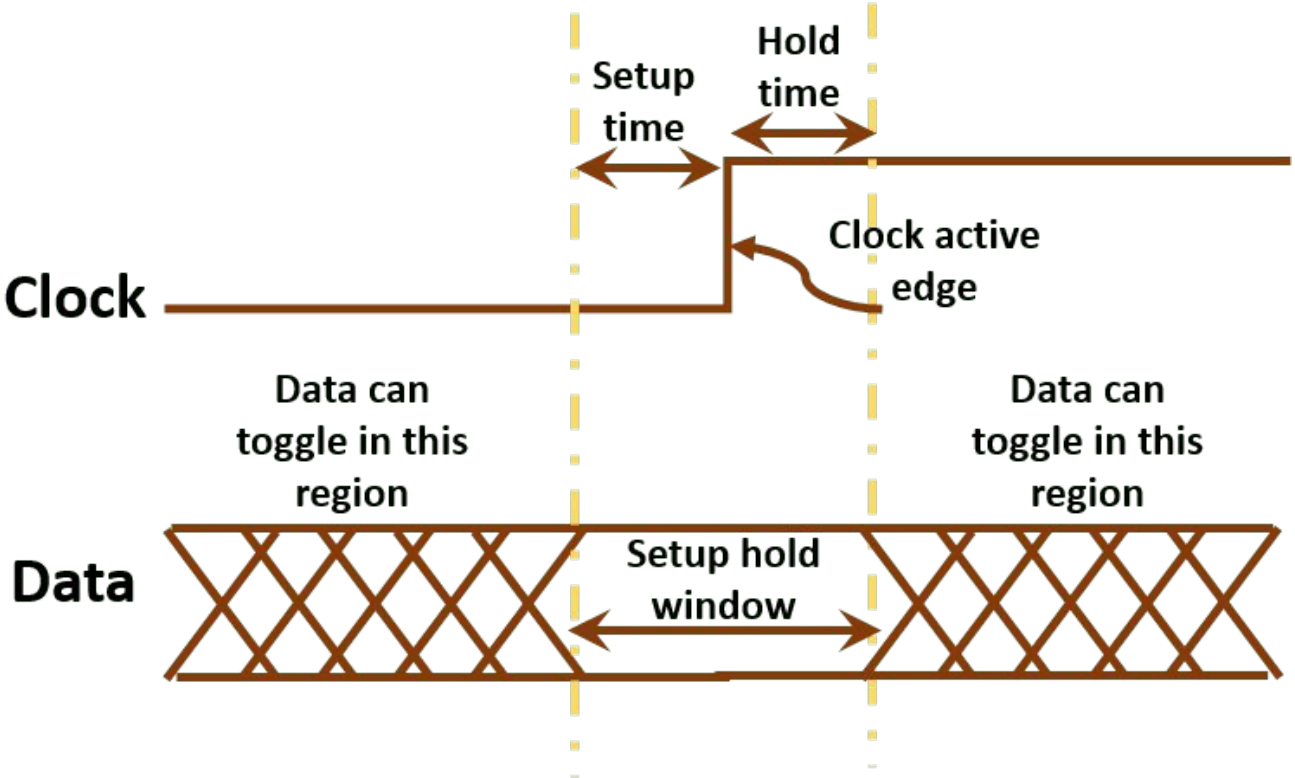
➔ **Setup Time**

- Setup time is the minimum amount of time the data signal should be held steady before the clock`s active edge so that the data are reliably sampled by the clock.

➔ **Hold Time**

- Hold time is the minimum amount of time the data signal should be held steady after the clock`s active edge so that the data is reliably sampled

Setup and Hold time



STA Definitions

➔ Transition Time

- Longest time required by the driving pin to change logic values
- It is decided on the basis of rise and fall time
- Time to rise from 10% to 90% of VDD - rise time
- Time to fall from 90% to 10% of VDD - fall time
- It will increase Dynamic power dissipation as both nmos and pmos will be on for an extended period of time
- Crosstalk violations are possible on the nets

STA Definitions

➔ **Required Time**

- ◆ It is the time required for data to arrive at a certain point.

➔ **Arrival Time**

- ◆ It is the time at which data arrives at a certain point.

STA Definitions

- **Slack**
  - It is the difference between the required time and arrival time of a signal.
  - Positive slack indicates that the design is meeting timing.
  - Negative slack indicates that the design is not meeting timing.
- **Setup Slack**
  - Required time - Arrival time
- **Hold Slack**
  - Arrival time - Required time

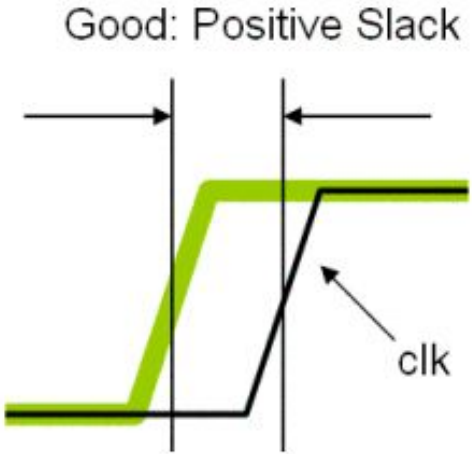
STA Definitions

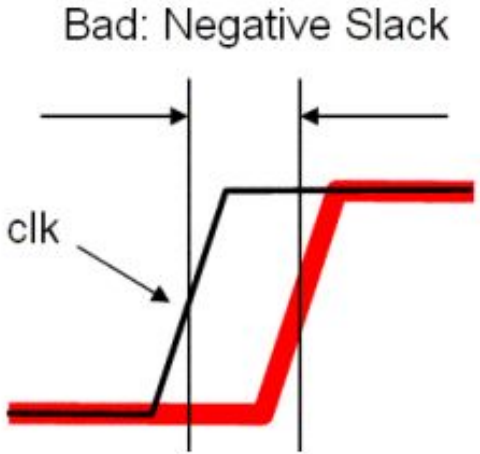
➔ **Positive Slack**

- Required time > Arrival time

➔ **Negative Slack**

- Arrival time > Required time



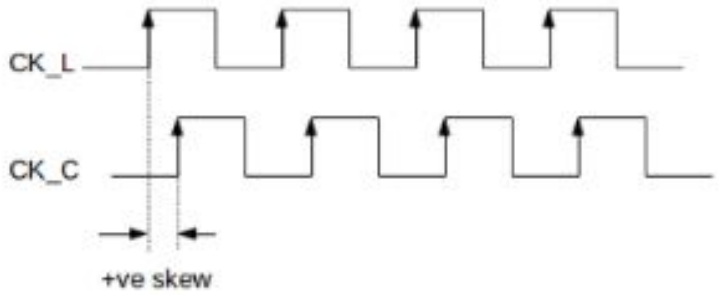


STA Definitions

➔ Clock Skew

- It is the difference in the arrival time of the capture edge of two adjacent registers.

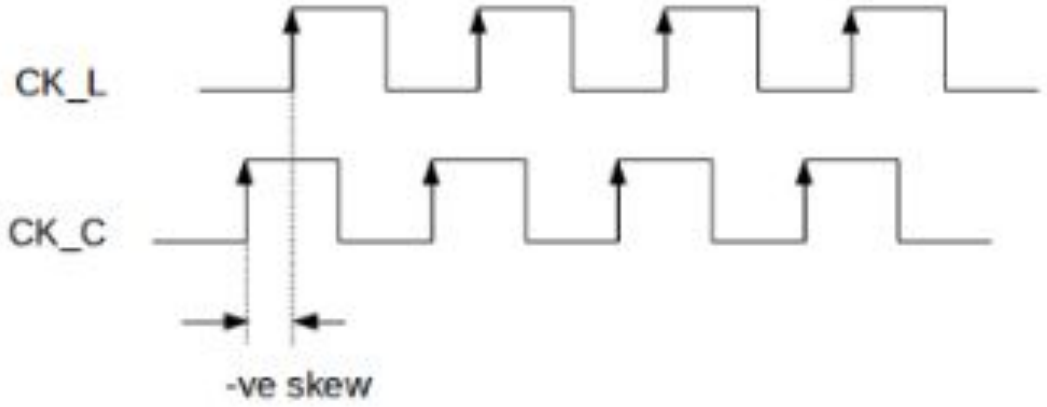
- Positive skew - capture clock comes late than the launch clock



STA Definitions

➔ Clock Skew

- ◆ Negative skew - Launch clock comes late than the Capture clock



Timing Exceptions

- False Path
  - This path does not affect the output and does not contribute to the delay of the circuit.
  - Paths between asynchronous clocks
  - Set_false_path command is used for this purpose.
  - Once false path is set, it removes the timing constraints from the path.

Timing Exceptions

- ➔ Multicycle Path
  - These paths require more than one clock cycle for the data to travel from launch flop and propagate to the capture flop.
  - Set_multicycle_path is the command used to specify the number of clock cycles.

Timing Path

- The timing path consists of three elements:
  - Start Point
  - Combinational Logic
  - End Point

Timing Path

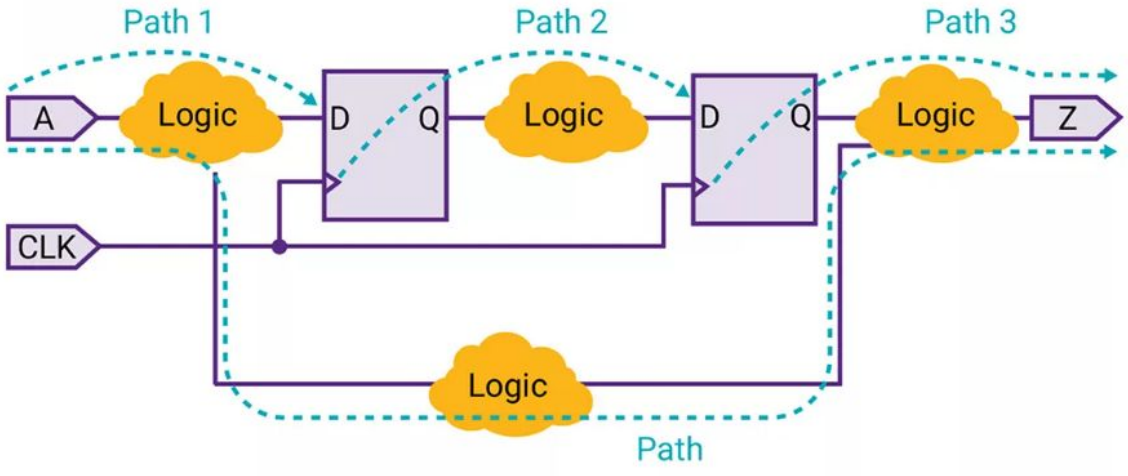
- ➔ Start Point
  - ◆ The start of a timing path where the data is launched by the clock edge.
  - ◆ Start point consists of a clock, a primary input port, sequential, pin with input delay.

Timing Path

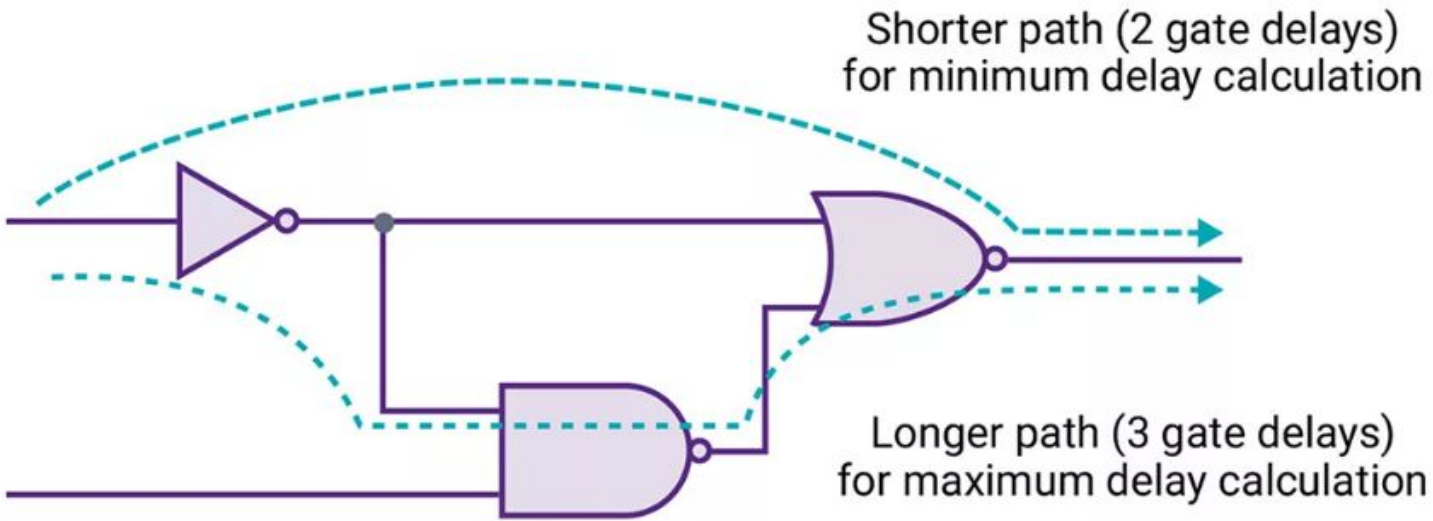
- ➔ Combinational Logic
  - ◆ They contain AND, OR, XOR elements. Flip-flops, registers and latches are not included in combinational logic.
- ➔ End Point
  - ◆ The end of the timing path where data is captured by the clock edge. Every endpoint must be an output port.
  - ◆ End point consists of a clock, a primary output port, pin with output delay.

Types of Timing Paths

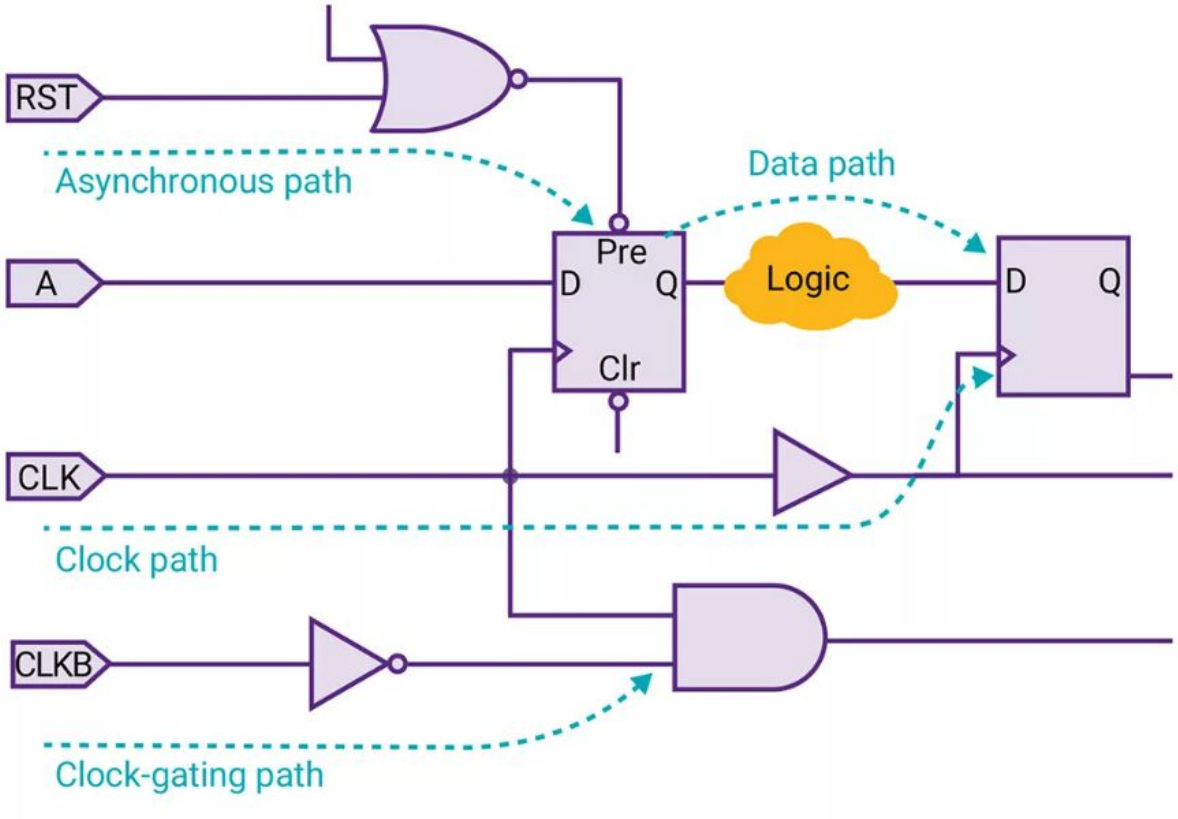
- ➔ Input Port to Register
- ➔ Register to Register
- ➔ Register to Output Port
- ➔ Input Port to Output Port



Shortest and Longest path

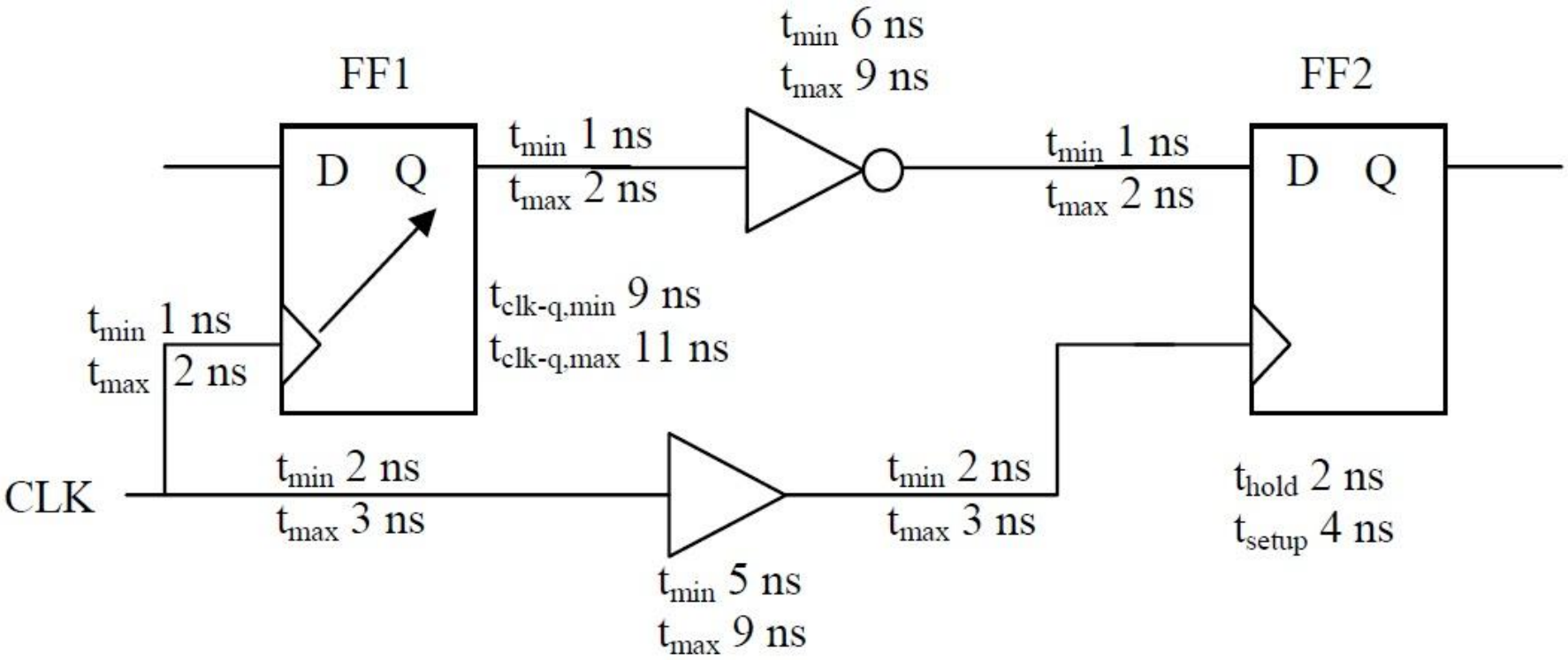


Types of paths - Timing analysis



SETUP AND HOLD TIME CALCULATION

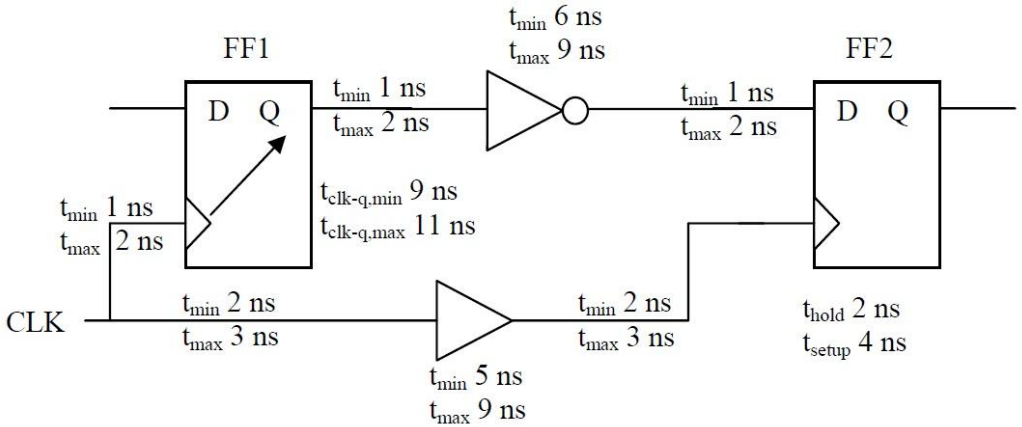
Setup and Hold violations



Setup and Hold violations

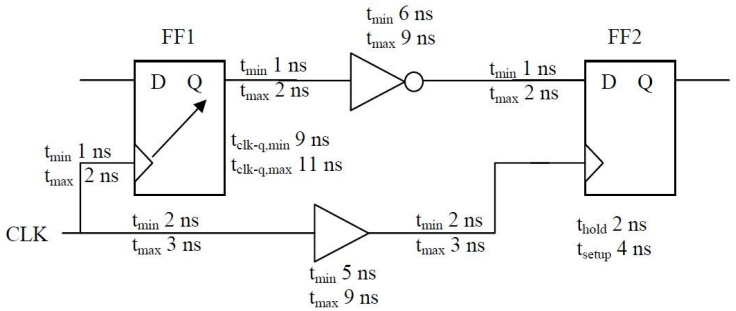
➔ Hold violation (Min delay - data path and Maximum delay - clk path)

- Data path (min) - CLK -> FF1/CLK -> FF1/Q -> INV -> FF2/D
- Delay (Td) - 1 + 9 + 6 + (1+1) = 18ns



Setup and Hold violations

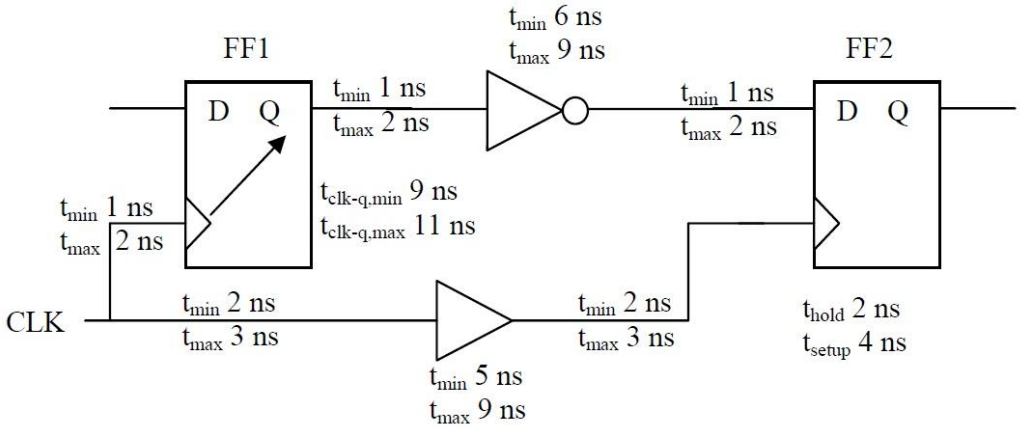
- ➔ Hold violation - Hold is checked at same clock edge
  - Clock path - CLK -> buffer -> FF2/clk
  - Clock delay (Tclk) - 3 + 9 + 3 + 2 (thold) = 17ns
  - Hold slack = Td - Tclk = 18ns - 17ns = 1ns (positive)
  - If thold = 4ns then hold slack will be -1ns (violation)



Setup and Hold violations

➔ Setup violation (Max delay - data path and Min delay - clk path)

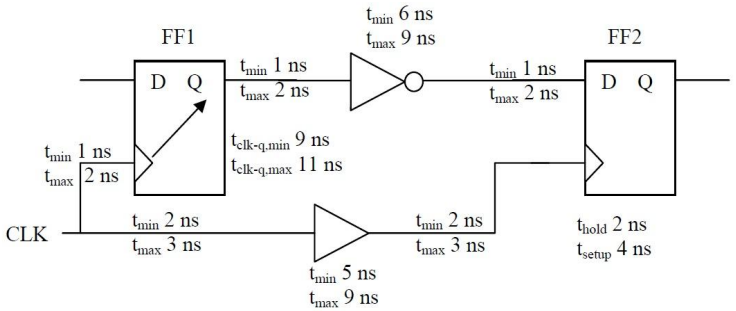
- Data path (min) - CLK -> FF1/CLK -> FF1/Q -> INV -> FF2/D
- Delay (Td) - 2 + 11 + 9 + (2+ 2) = 26ns



Setup and Hold violations

➔ Setup violation - Setup is checked at next clock edge

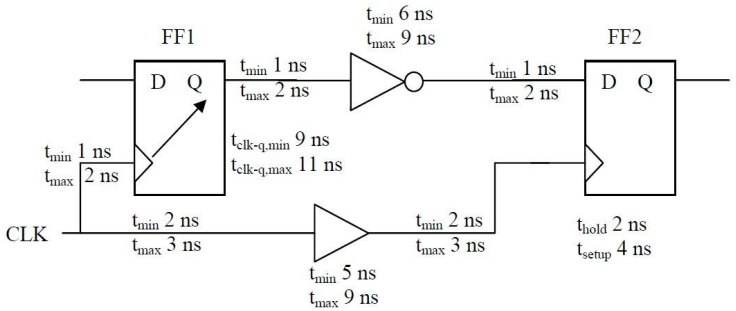
- Clock path - CLK -> buffer -> FF2/clk
- Clock path delay - add clock period (15ns)
- Clock delay (Tclk) - 15 + 2 + 5 + 2 - 4 = 20ns
- Setup slack = Tclk - Td = 20ns - 26ns = -6ns (negative)



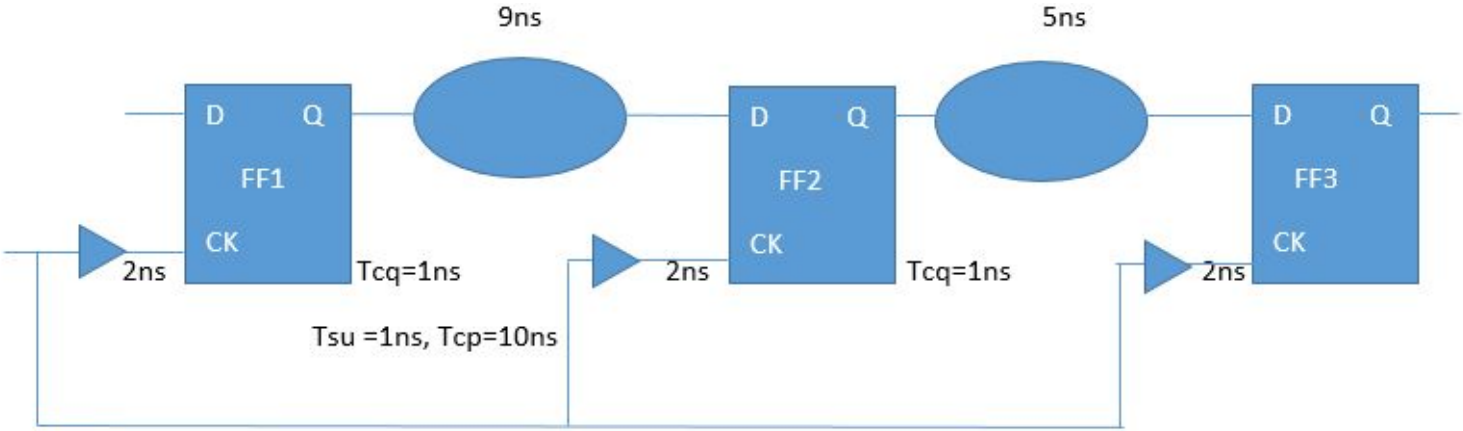
Setup and Hold violations

➔ Setup violation - increase clock period / less max delay of inverter

- Bigger clock period - 22ns
- Tclk = 22 + 2 +5 + 2 - 4 = 31 - 4 = 27ns
- Td = 26ns
- Setup = Tclk - Td = 27ns - 26ns = 1ns (positive)

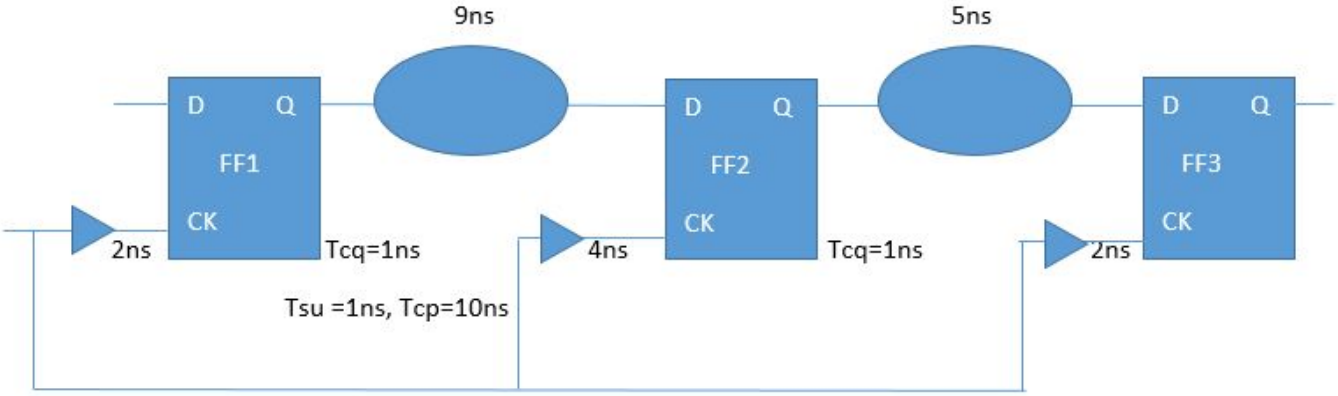


USEFUL SKEW

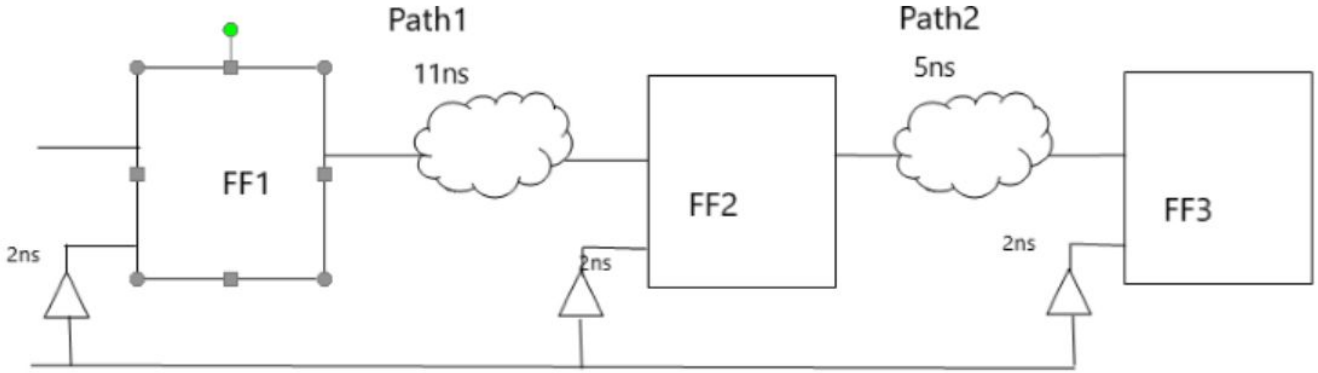


- Path - FF1 to FF2
  - Arrival time = 2 + 1 + 9 = 12ns
  - Required time = 10ns + 2ns - 1ns = 11ns
  - Setup = Required time - Arrival time = 11ns - 12ns = -1ns (setup violation)

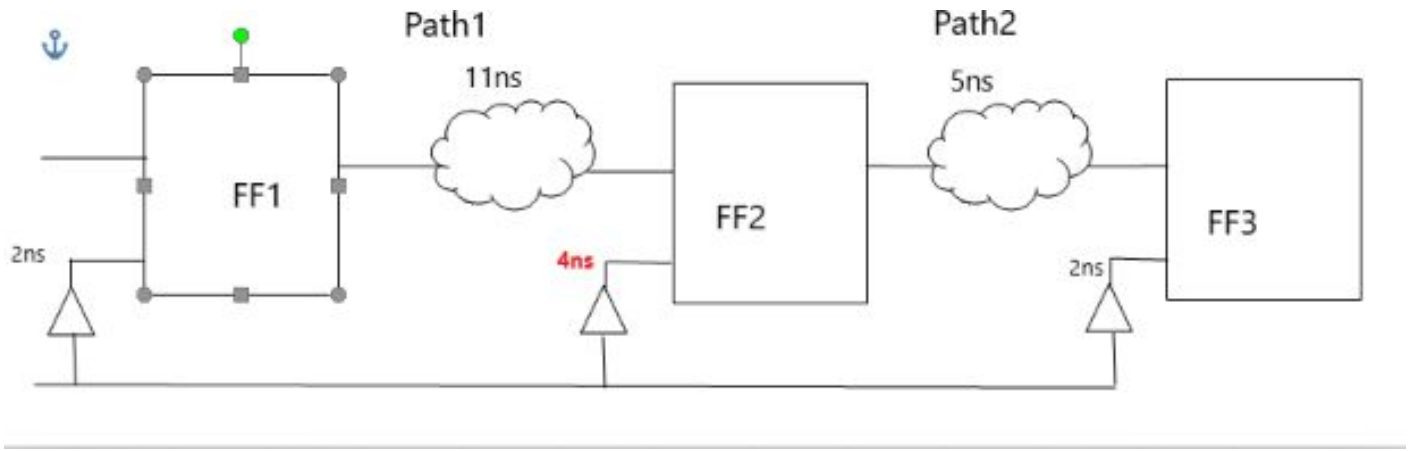
- Path - FF2 to FF3
  - Arrival time = 2 + 1 + 5 = 8ns
  - Required time = 10ns + 2ns - 1ns = 11ns
  - Setup = Required time - Arrival time = 11ns - 8ns = 3ns (no setup violation)



- Path - FF1 to FF2
  - Arrival time = 2 + 1 + 9 = 12ns
  - Required time = 10ns + 4ns - 1ns = 13ns
  - Required time - Arrival time = 13ns - 12ns = 1ns (no setup violation)
- Path - FF2 to FF3
  - Arrival time = 4 + 1 + 5 = 10ns
  - Required time = 10ns + 2ns - 1ns = 11ns
  - Required time - Arrival time = 11ns - 10ns = 1ns (no setup violation)



- Clk period - 10ns, insertion delay - 2ns to clk pin of each register
- Path 1 combinational delay - 11ns and Path -2 combinational delay - 5ns
- Setup - 2ns (clk path FF1/CP + 11ns < 2ns (clk path FF2/CP + 10ns (clk period) [13ns < 12ns] - Timing violation



- Useful skew - 2ns
- Setup in path 1 - 2ns (clk path FF1/CP + 11ns < 4ns (clk path FF2/CP + 10ns (clk period) [13ns < 14ns] - No Timing violation
- Setup in path 2 - 4ns (clk path FF2/CP + 5ns < 2ns (clk path FF3/CP + 10ns (clk period) [9ns < 12ns] - No Timing violation

Fix Setup Violations

- ➔ Upsize the cell
- ➔ Insert buffers
- ➔ Reduce clock uncertainty
- ➔ Increase delay in the clock

Fix Hold Violations

- ➔ Add delays
- ➔ Detoured routing
- ➔ Downsizing the cells
- ➔ Use data path cells with high threshold voltage

Fix max capacitance Violations

- ➔ Increasing drive strength of the cell

Fix Transition Violations

- ➔ Upsize driver cells
- ➔ Decrease the net length - macros, routing blockages, fixed cells
- ➔ Adding buffers at output of driving gate.
- ➔ Splitting the load through buffers - Reduction in fanouts
- ➔ Changing VT - hvt to svt or lvt
- ➔ Reduce the load by downsizing the cells

Timing Report

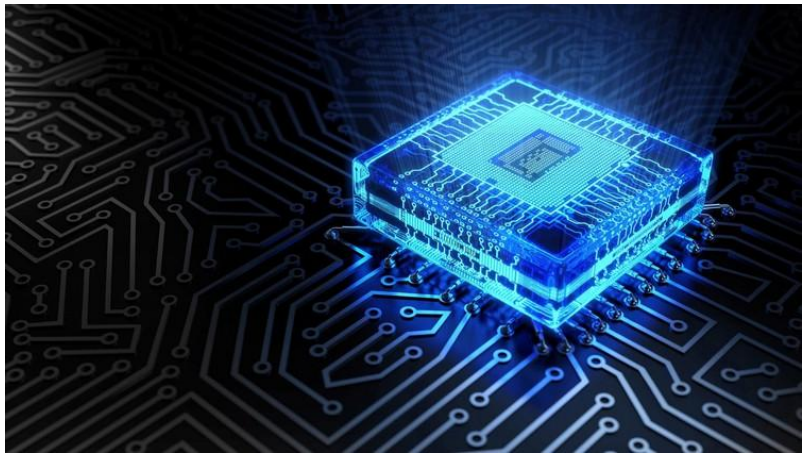
```
Startpoint: UF11 (rising edge-triggered flip-flop clocked by Iclk)
Endpoint: UF21 (rising edge-triggered flip-flop clocked by Iclk)
Path Group: Iclk
Path Type: max

Point                                    Incr       Path
-----------------------------------------------------------
clock Iclk (rise edge)                   0.00       0.00
clock network delay (propagated)       256.97     256.97
UF11/CK (SCJFD21S10)                     0.00     256.97 r
UF11/Q (SCJFD21S10)                    390.18     647.15 f
UD11/A (SCJBF10010)                      0.00     647.15 f
UD11/X (SCJBF10010)                     91.96     739.12 f
UF21/D (SCJFD21S10)                      0.00     739.12 f
data arrival time                                 739.12

clock Iclk (rise edge)                10000.00   10000.00
clock network delay (propagated)        256.97   10256.97
UF21/CK (SCJFD21S10)                             10256.97 r
library setup time                     -197.26   10059.72
data required time                               10059.72
-----------------------------------------------------------
data required time                               10059.72
data arrival time                                 -739.12
-----------------------------------------------------------
slack (MET)                                      9320.60
```

Arrival time

Required time

Slack

PHYSICAL VERIFICATION



Physical Verification Checks

- ➔ Design Rule Check (DRC)
- ➔ Layout vs Schematic (LVS)
- ➔ Electrical Rule Check (ERC)
- ➔ Antenna
- ➔ XOR
- ➔ Logical Equivalence Check (LEC)

DESIGN RULE CHECK (DRC)

- ➔ DRC is a process where the physical design database is checked against design rules.
- ➔ These design rules are provided by the manufacturers to the design engineers.
- ➔ Some of the rules are spacing between metal layers, minimum width rules, etc.

DESIGN RULE CHECK (DRC)

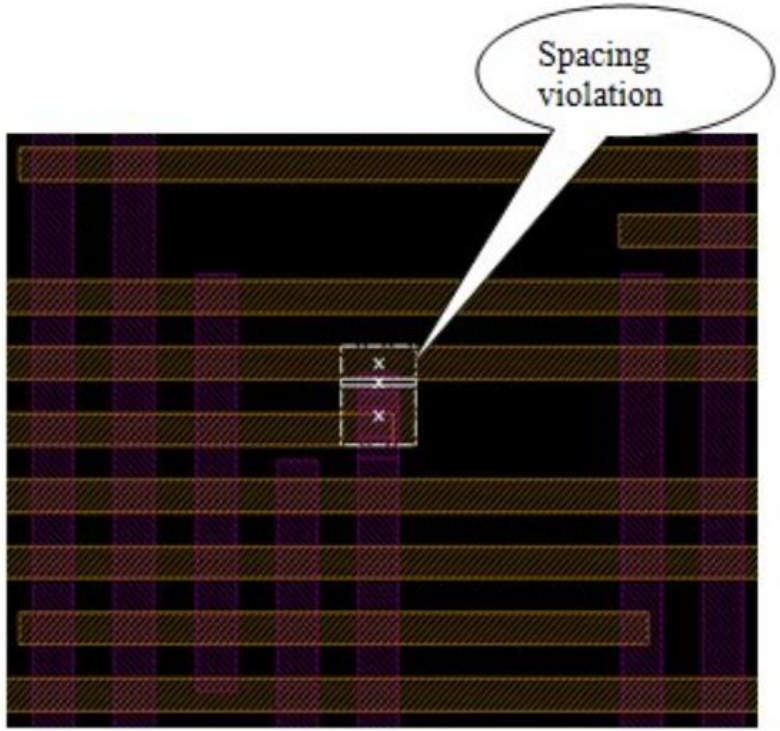
- ➔ DRC should be clean before the chip is passed to the foundry.
- ➔ Spacing rules may change depending on the width of one or both of the layers as well.
- ➔ The complexity of design rules has been increasing with rapid advancement in technology nodes.

DESIGN RULE CHECK (DRC)

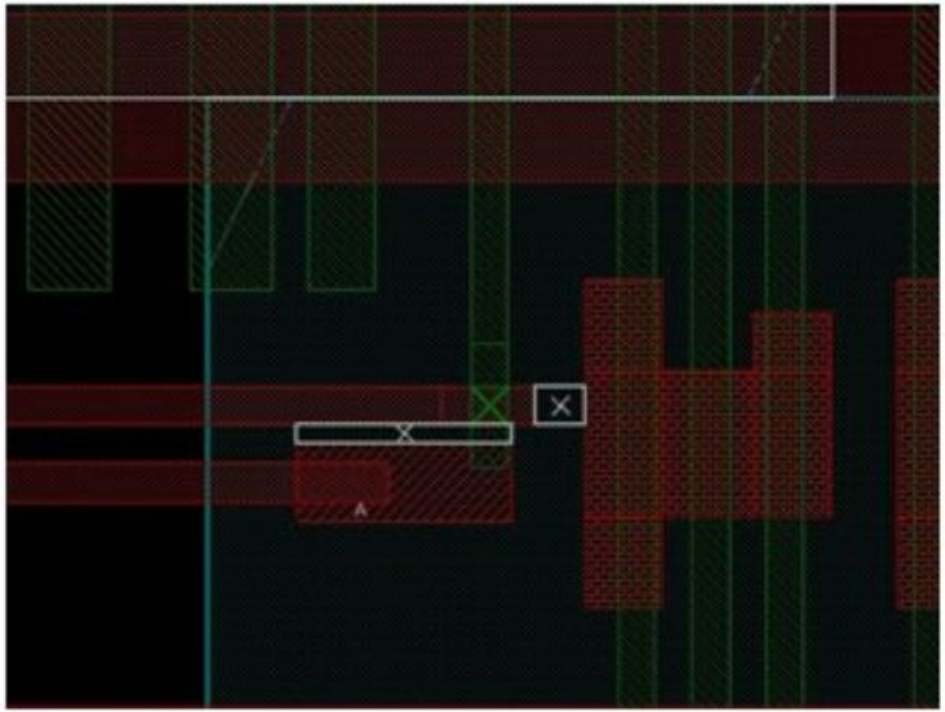
- ➔ Types of DRCs
  - ◆ Minimum width of a metal layer
  - ◆ Shorts
  - ◆ Minimum spacing of a metal layer
  - ◆ Minimum width and spacing for VIA
  - ◆ Minimum area
  - ◆ Wide metal jog
  - ◆ Different net spacing

DESIGN RULE CHECK (DRC)

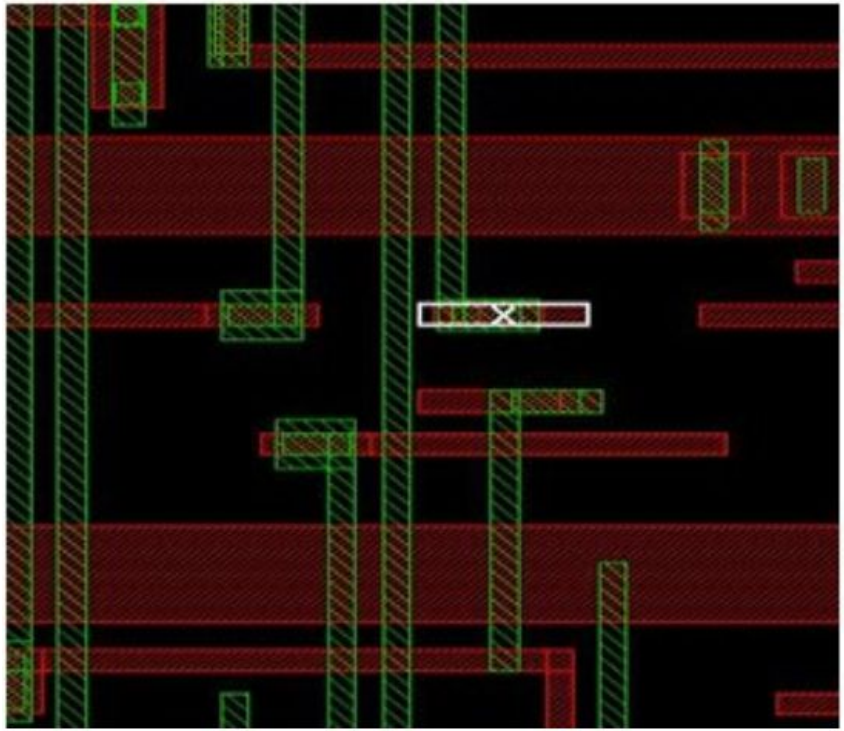
DESIGN RULE CHECK (DRC)



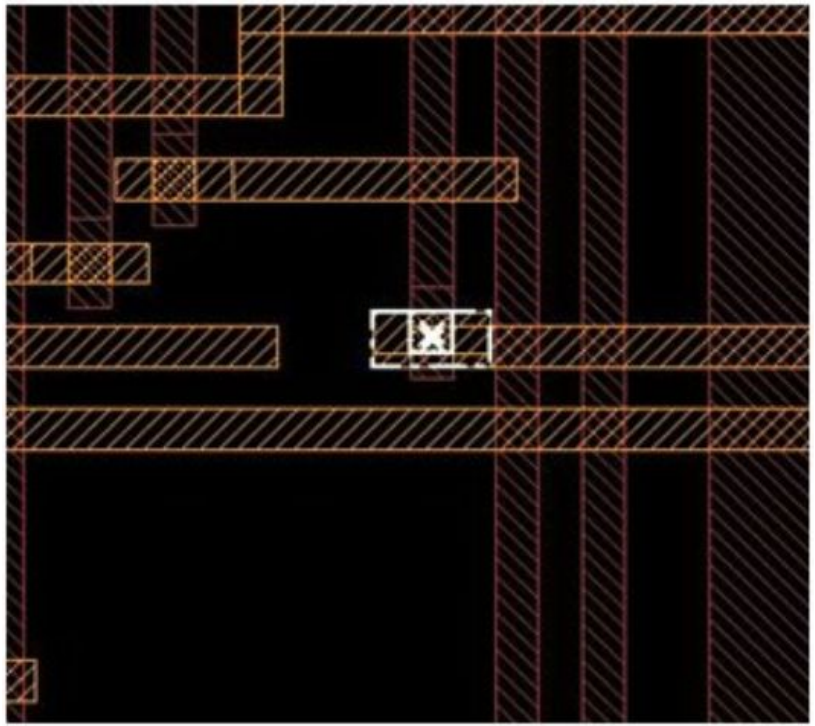
DESIGN RULE CHECK (DRC)



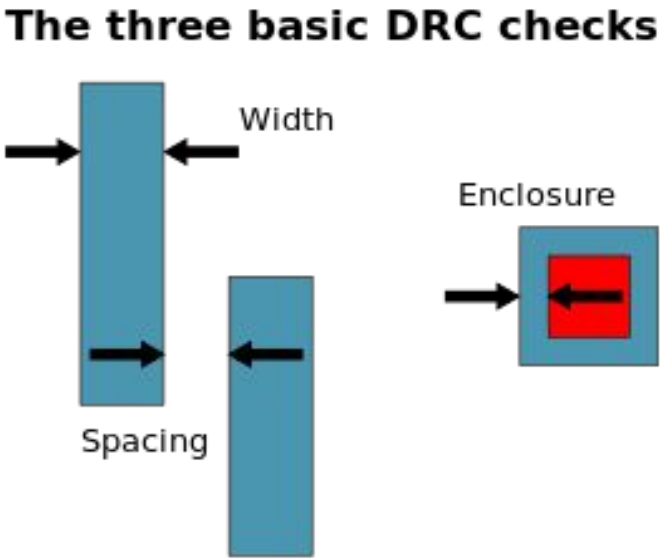
DESIGN RULE CHECK (DRC)



DESIGN RULE CHECK (DRC)



DESIGN RULE CHECK (DRC)



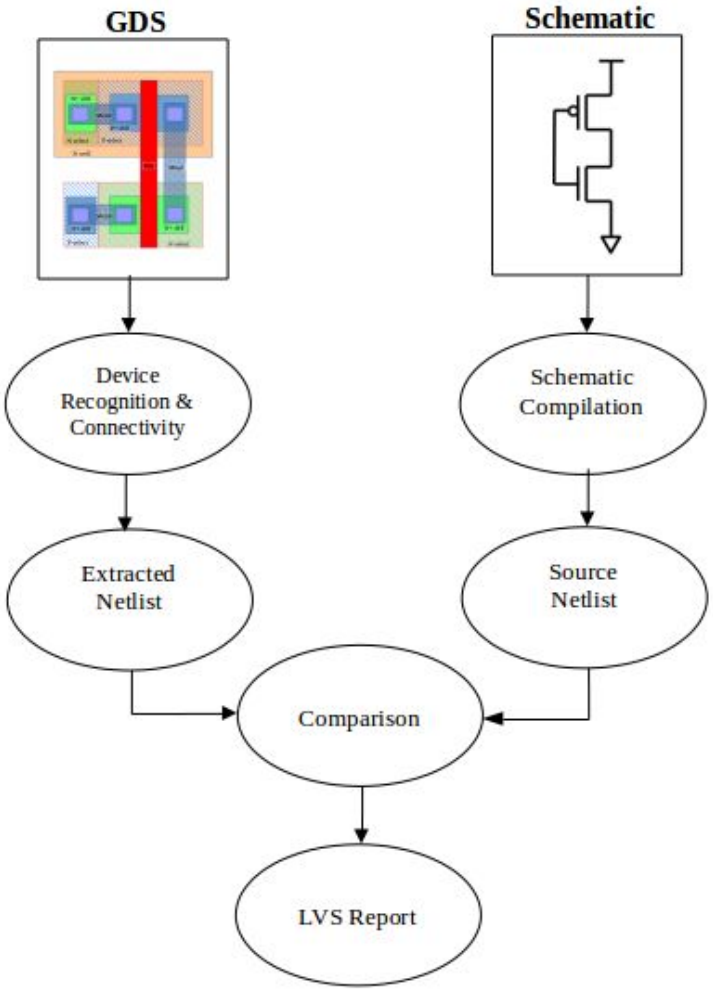
LAYOUT versus SCHEMATIC CHECK (LVS)

- ➔ This is a very important check in Physical Verification.
- ➔ Check to verify if the layout created is functionally the same as the schematic of the design.
- ➔ The LVS tool will create a layout netlist and it is compared with the schematic netlist.

LAYOUT versus SCHEMATIC CHECK (LVS)

- Inputs for LVS
  - .v – incoming netlist
  - LVS rule deck
  - GDS – Routed layout database
- .v and GDS should be from the same routed database.

LVS FlOW

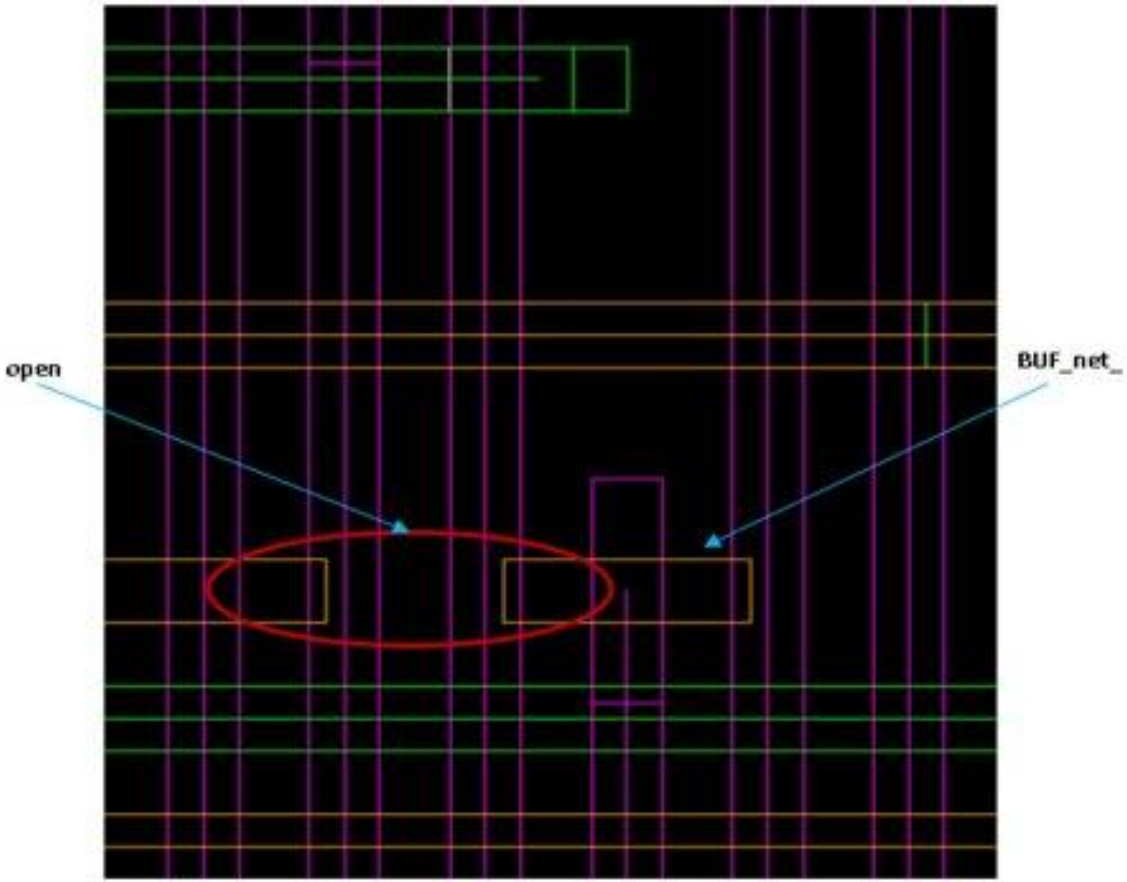

GDS
Schematic
Device Recognition & Connectivity
Schematic Compilation
Extracted Netlist
Source Netlist
Comparison
LVS Report

LAYOUT versus SCHEMATIC CHECK (LVS)

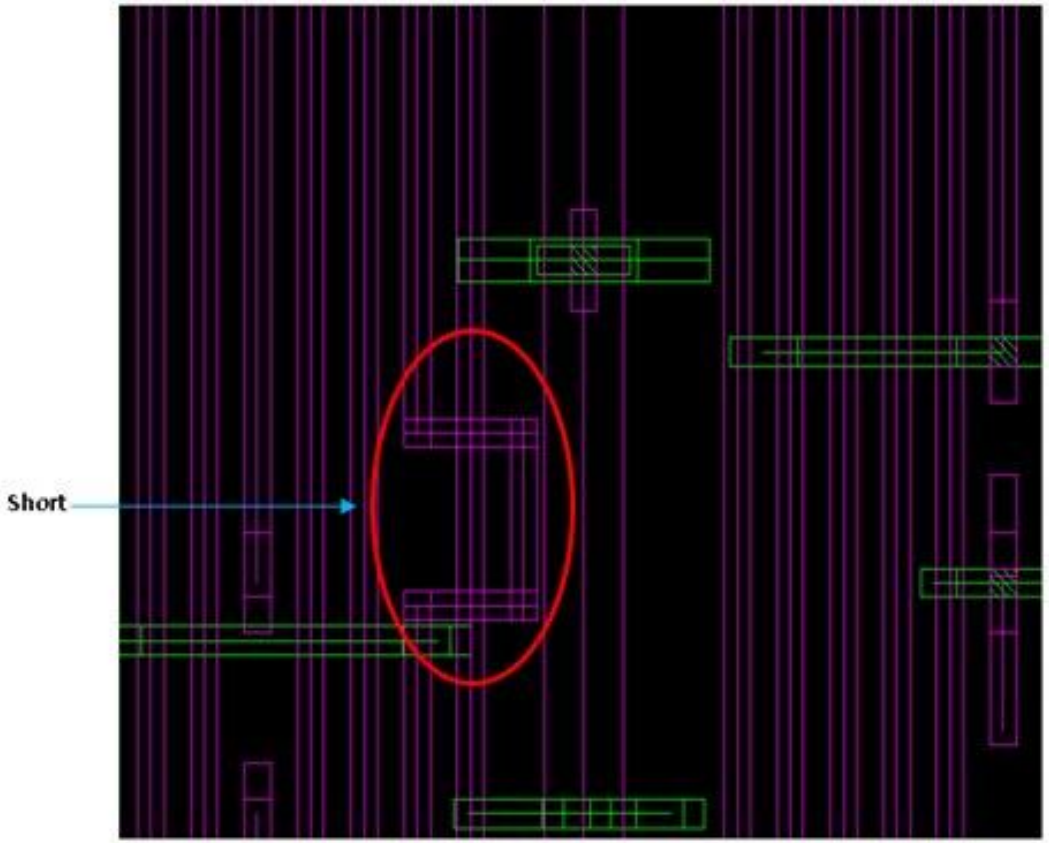
➔ Types of LVS errors

- Shorts
- Opens
- Parameter mismatch – matching a resistor in both layout and schematic, but the resistor values may be different.
- Unbound pins – If the pins don’t have a geometry, but all the connections to the net are made, and unbound pin is reported.

LVS - OPEN



LVS - SHORT



ELECTRICAL RULE CHECK (ERC)

➔ Electrical rule checking (ERC) is a methodology used to check the robustness of a design, both at schematic and layout levels against various “electronic design rules”.

➔ ERC helps to check

- Floating gates
- Floating interconnect, Metal, Poly
- Shorted Drain & Source of a MOS
- No substrate- or well contact

ANTENNA

- ➔ At the time of plasma etching in chip fabrication, there will be change to collect more charges at the gate and cause damage to the gate oxide layer as it is very thin.

- ➔ The antenna effect can potentially cause yield and reliability problems during the manufacture of MOS integrated circuits.

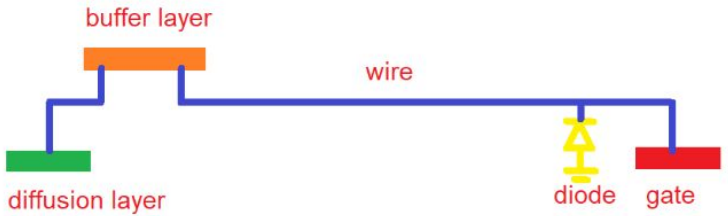
ANTENNA

- ➔ Solutions for Antenna Violations
  - ◆ Metal Jumpers
    - Break signal wires and route to high metal layers using Jumpers.

    - Jumper breaks the long wire, thereby connecting it to high metal layers, making it short and less capable of collecting charge.

ANTENNA

- Solutions for Antenna Violations
  - Diode insertion
    - Connecting diodes near gate inputs provides a discharge path to the substrate, which saves the gate of the transistor.
    - Adding diode rises the area and capacitance and eventually makes the circuit slower and consumes more power.



XOR

- ➔ This check is run where the original and modified database are compared.
- ➔ This is done to confirm that only the required modifications have been made and no other modifications have been made by accident.
- ➔ This step involves comparing the two layout databases/GDS by XOR operation of the layout geometries.
- ➔ This check will generate a report which has all the mismatching geometries in both the layouts.

Logical Equivalence Check (LEC)

- ➔ LEC is one of the most important checks in the entire chip design process.

- ➔ Design passes through steps like place and route, sign-offs, ECOs, and numerous optimizations before it reaches production.

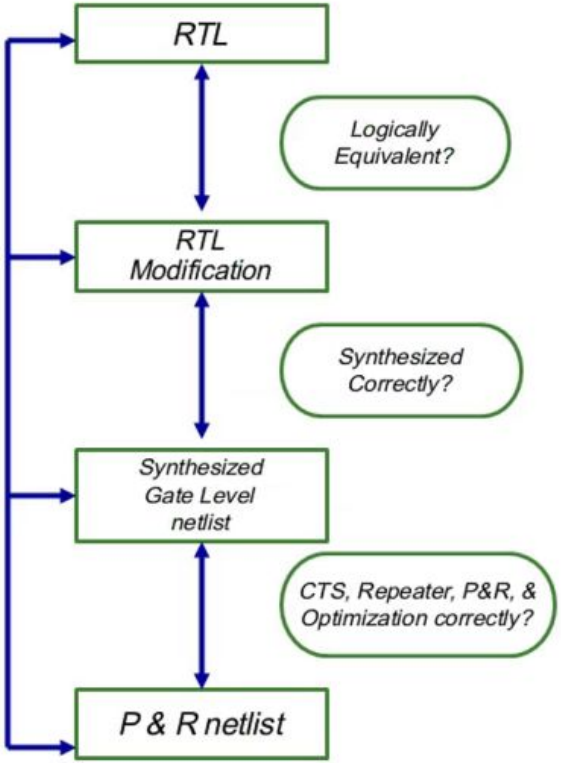
- ➔ At every stage, we need to make sure that the logical functionality is intact and does not break because of any of the automated or manual changes.

Logical Equivalence Check (LEC)

- ➔ The entire chip becomes useless if the functionality of the product changes during the chip design cycle.

- ➔ With shrinking technology nodes and increasing complexity, LEC check plays a major role in ensuring the correctness of the functionality.

Logical Equivalence Check (LEC)



POWER ANALYSIS

Power Consumption

- **Components**
  - Dynamic or switching power
  - Static or leakage power
- **Total Power**
  - Total power = Switching power + Short circuit power + Leakage power
  - Dynamic power is the sum of switching power and short circuit power.

Power Consumption

➔ **Switching Power**

- Switching power is dissipated when the internal and net capacitances are charged or discharged.

➔ **Short circuit Power**

- Short-circuit power is the power dissipated by a short-circuit connection between the supply voltage VDD and the ground, when the gate switches state.

Power Consumption

➔ Leakage Power

- Static or Leakage power is the power consumed while the circuit is inactive.
- Leakage power is a function of the supply voltage Vdd, the switching threshold voltage Vth, and the transistor size.
- Transistor size = W/L

Power Consumption

➔ **How to reduce dynamic power ?**

- Reducing switching activity
- Selecting cells which consume less dynamic power
- Architectural improvements
- Reducing supply voltage

Power Analysis

➔ IR Drop

- The power supply in the chip is distributed uniformly through VDD and VSS metal layers.

- When voltage is applied to the metal wires in the design, current starts to flow through these layers and some voltage is dropped because of the resistance of metal wires causing IR drop.

- It causes delaying of the cells resulting in setup and hold violations.

Power Analysis

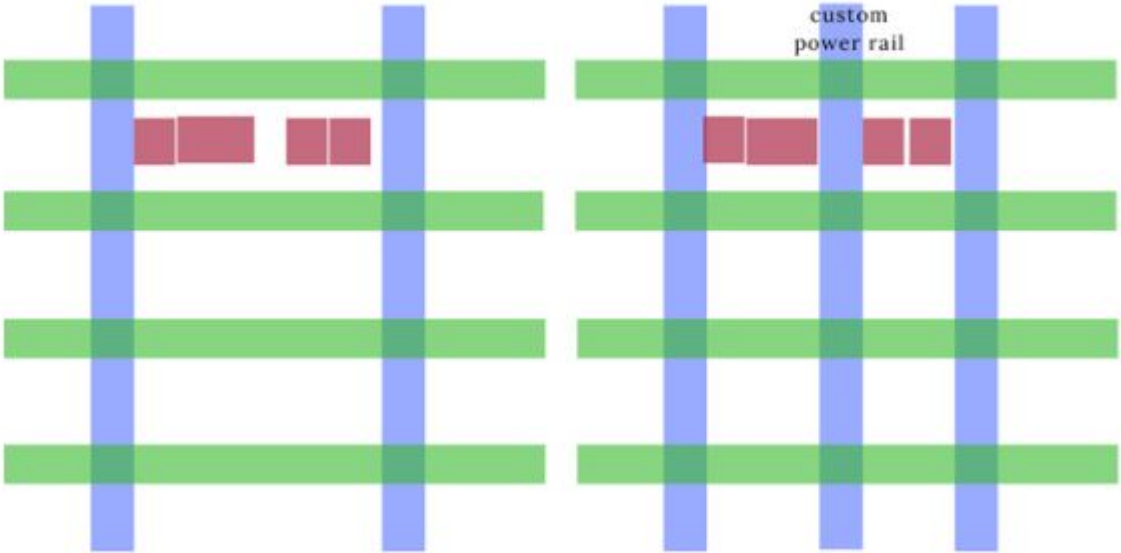
- **Types of IR Drop analysis**
  - **Static IR Drop analysis**
    - Calculates voltage drop of entire chip with no activity
    - This is a vectorless power analysis.
  - **Dynamic IR Drop analysis**
    - This is a vector based analysis with worst switching currents.
    - The voltage drop is calculated in the chip with switching activity.

Power Analysis

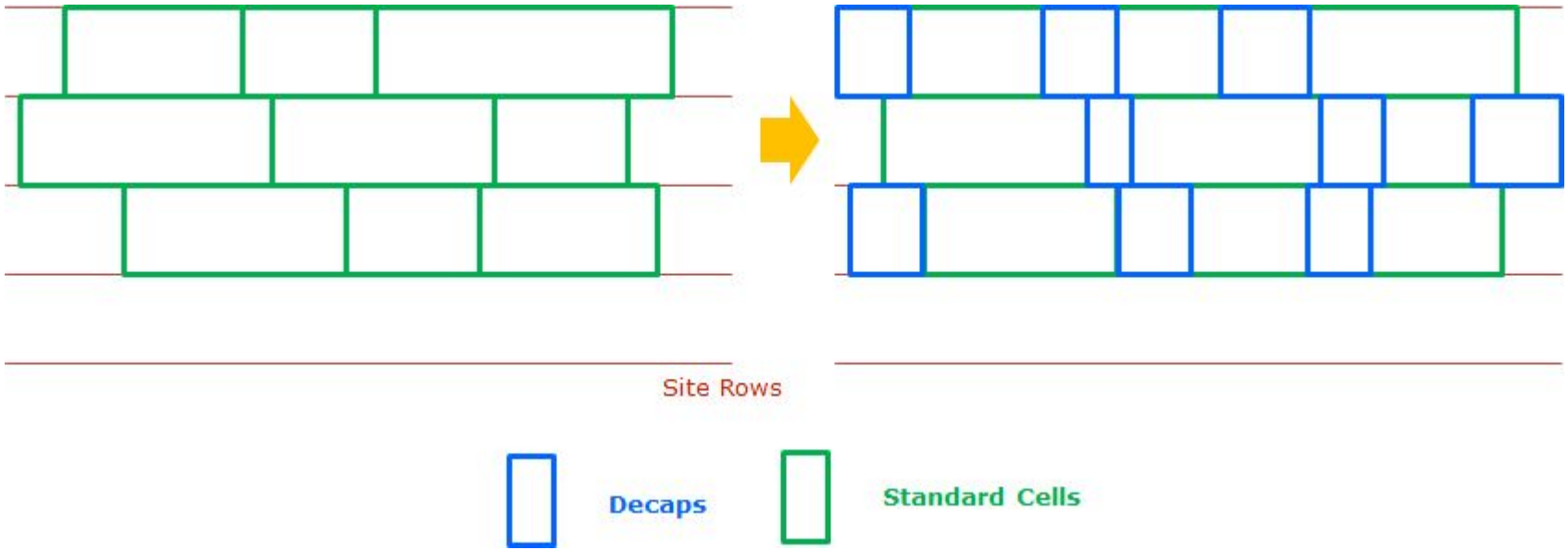
➔ **Methods to reduce IR drop**

- **Robust power mesh**
  - Adding extra power stripes in certain regions will make the power mesh robust.
- **Decap cells**
  - These are decoupling capacitors which are spread across the region with high switching activity to maintain the voltage.

Robust Power Mesh



Decap cells



Power Analysis

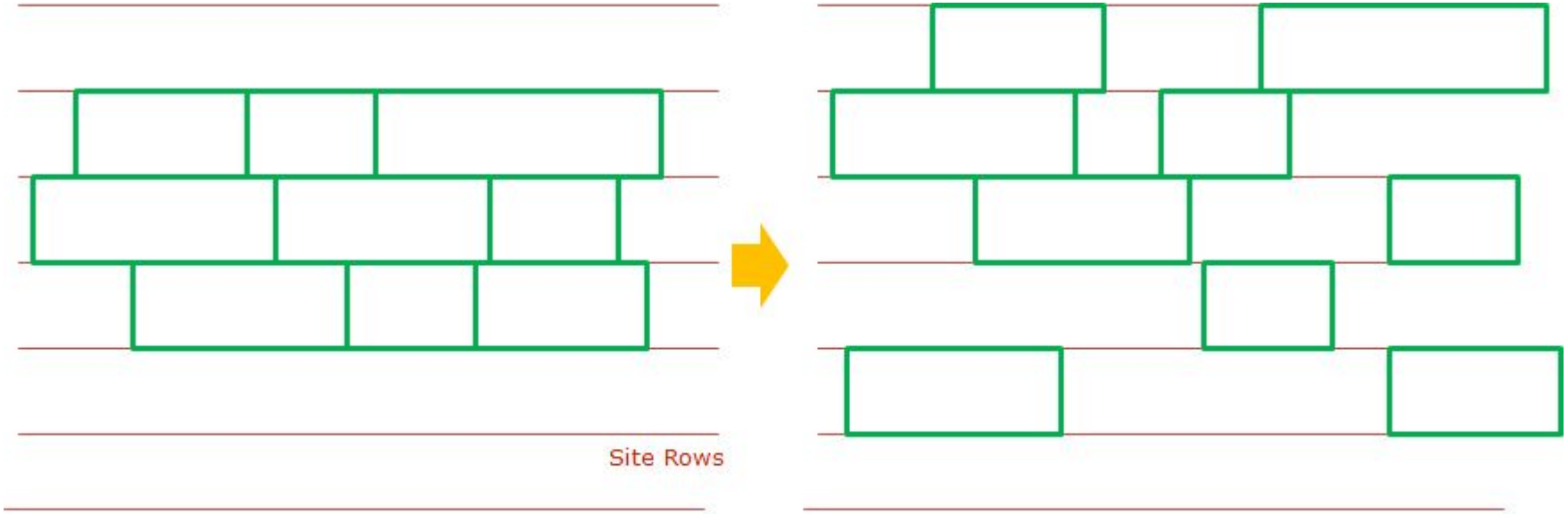
➔ Methods to reduce IR drop

- PG connection
  - Power pins of macros should be properly connected to the power rails. Increase strap width if required.
- Power switches
  - The number of power switches can be increased to reduce IR drop.

Power Analysis

- ➔ Methods to reduce IR drop
  - ◆ Cell padding
    - This is a method to space out cells which switch simultaneously.
    - This will help to reduce the peak current demand at one particular region in the power grid.

Cell Padding



Power Analysis

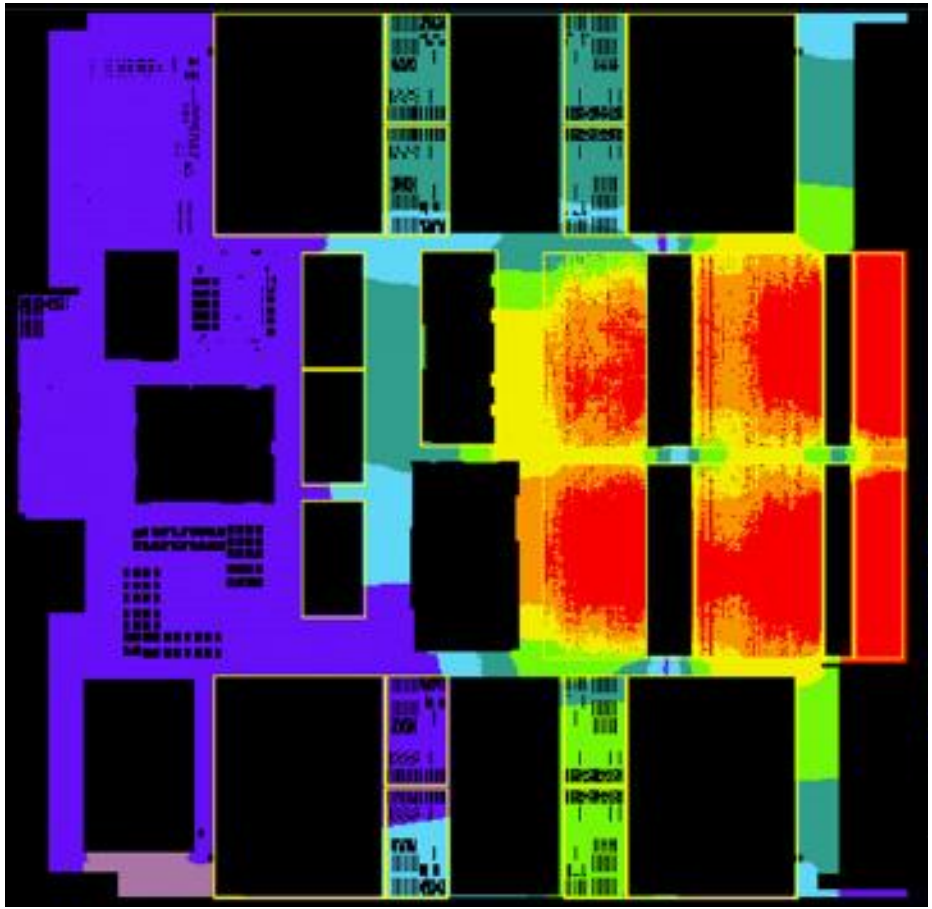
- ➔ Reasons for Poor Power Grid
  - ◆ Disconnected Instances
  - ◆ Disconnected Wires
  - ◆ Shorts
  - ◆ Missing vias

Power Analysis

➔ Tips to strengthen the power grid

- Incremental addition of vias to drop from higher metal layers to lower metal layers.
- Add wider PG stripes to improve current conductivity.

IR Drop Map



Impact of Physical Design

- Performance - long routes - wire delays
- Area - wrong placement of modules
- Reliability - large number of vias
- Power - large transistors/cells and long wires
- Yield - routing of wires too close - electrical shorts - fabrication

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