**BASIC LEVEL COURSE**
**RTL CODING AND TESTBENCH DEVELOPMENT**
**USING VERILOG HDL**
**(EDA Tool:**Xilinx ISE Design Suite**)**

**1. Logic Synthesis and Verification**
– What is logic synthesis?
– Impact of logic synthesis
– Verilog HDL synthesis
– Synthesis Design Flow
– Verification of Gate-level netlist
– Modeling tips for logic synthesis
– Design Partitioning
– Sequential Circuit Synthesis

**2. Switch Level Modeling**
– Switch modeling Elements
– MOS switches
– CMOS switches
– Design: CMOS NOR gate, 2:1 MUX, Simple CMOS Latch

**3. Gate-Level Modeling**
– Gate Types
– Gate Delays

**4. Dataflow Modeling**
– Continuous Assignments
– Delays
– Expressions, operators and operands
– Operator type
– Design: 4:1 MUX, 4-bit full adder
– Ripple Counter

**5. Behavioral Modeling**
– Structured Procedures
– Procedural Assignment
– Timing Control
– Conditional statements
– Multiway branching
– Loops
– Sequential and parallel blocks
– Generate Blocks
– Design: 4:1 MUX, 4-bit counter
– Traffic signal controller

**6. Tasks and Functions**
– Difference Between task and function
– Tasks
– Automatic(Re-entrant) task
– Functions
– Automatic(Recursive ) function

**7. Hierarchical Modeling concept**
– Design of 4-bit ripple carry adderModules
– Instances
– Components of a simulation
– Example: Design Block, Stimulus Block

**8. Useful Modeling Techniques**
– Procedural Continuous Assignments
– Use of force and release
– Overriding Parameters
– Conditional Compilation and execution
– Time Scale
– Useful system tasks