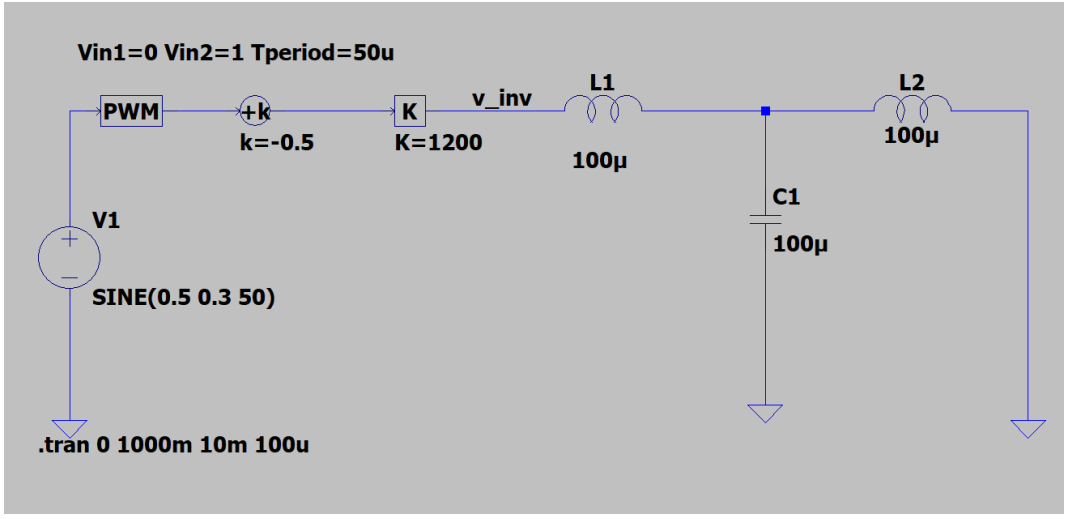
Single Phase inverter

Objective: To design a 2.2 KW single phase inverter with following specs:

Grid Voltage: 325 Vpeak 50Hz
Grid Current: 10A rms, with steady state error < 10mA (without grid influence) (-40dB)
Current Error in steady state: 10A without grid voltage (~-54dB)
Reactive Power: 156W (5 percent of peak power (2.2Kw*sqrt(2)))
Switching frequency: 20KHz
Input voltage 1200V (+-600V wrt grid reference)
THD: < 2 %

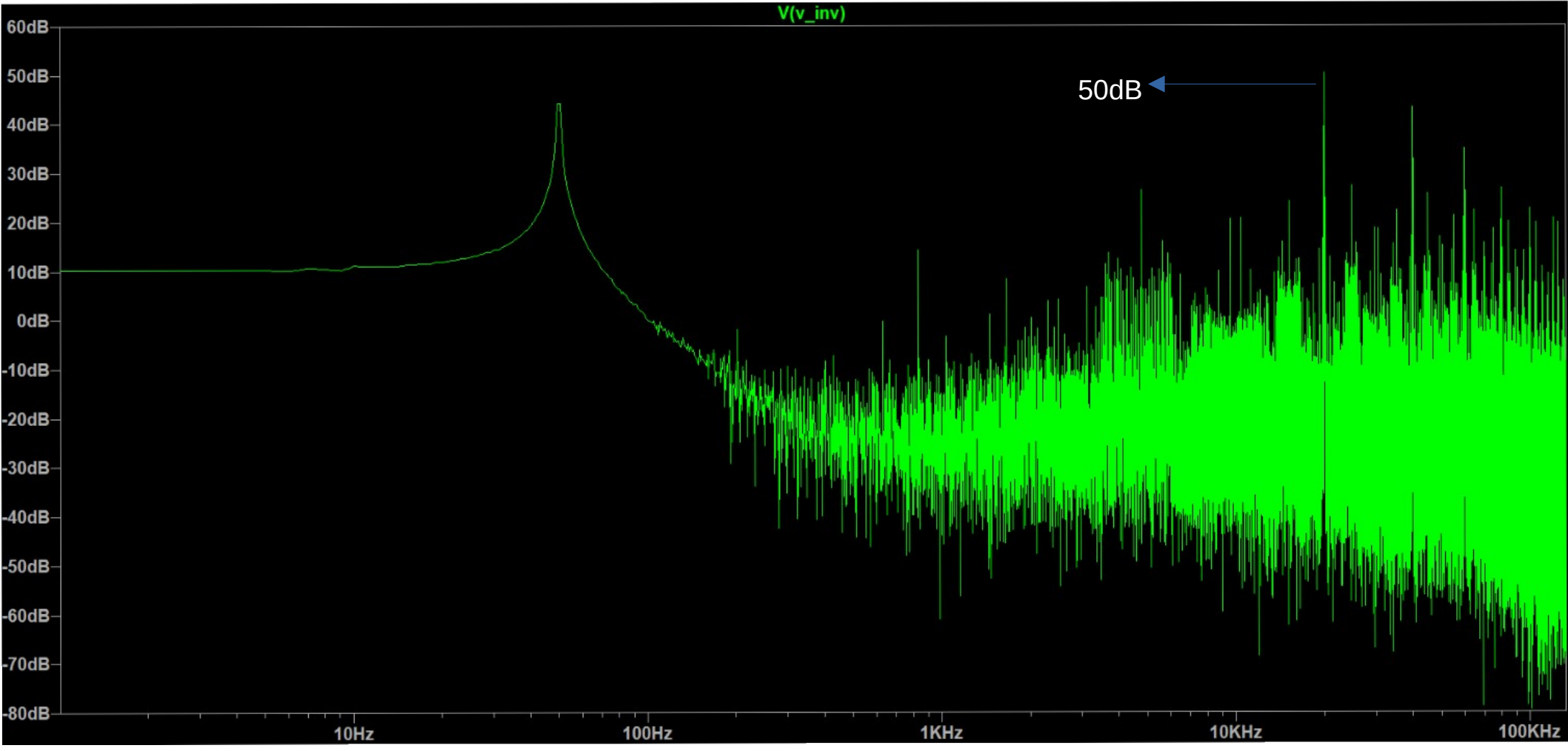
Design of LCL filter with capacitive feedback



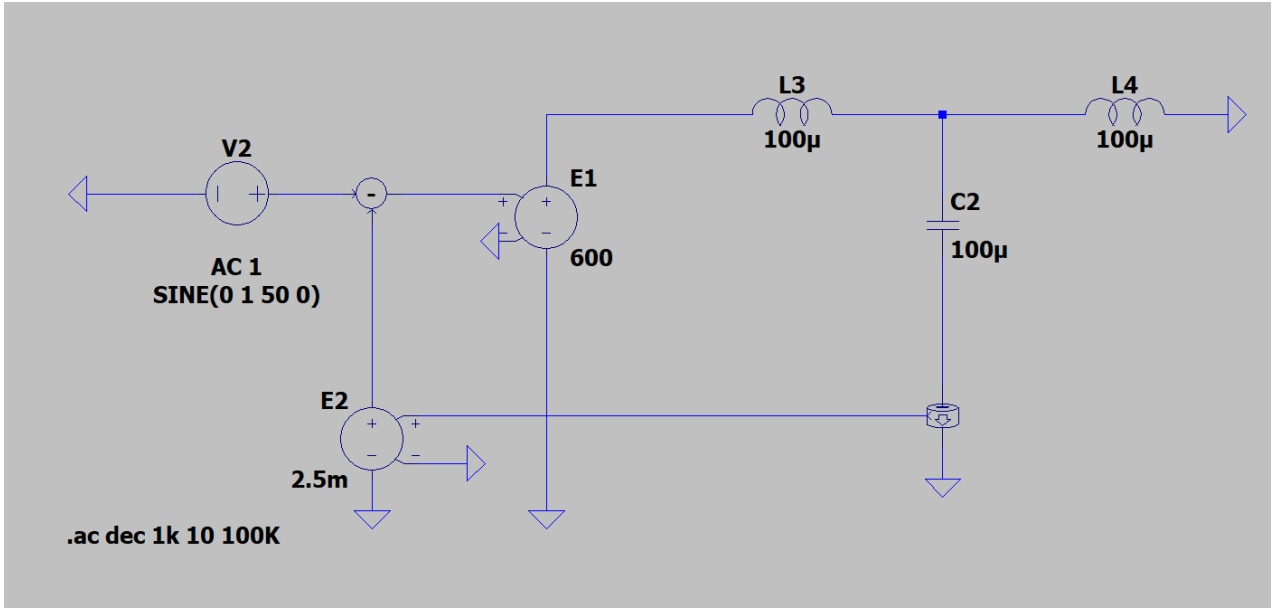
The above consists a simplified model of inverter with LCL filter.

The max current is 10*sqrt(2)=14.14A, so 1 percent max current at 20KHz would be ~0.1414A (~-17dB)

On the next slide an fft of the inverter voltage is shown



The inverter voltage ripple at 20KHz is ~50dB

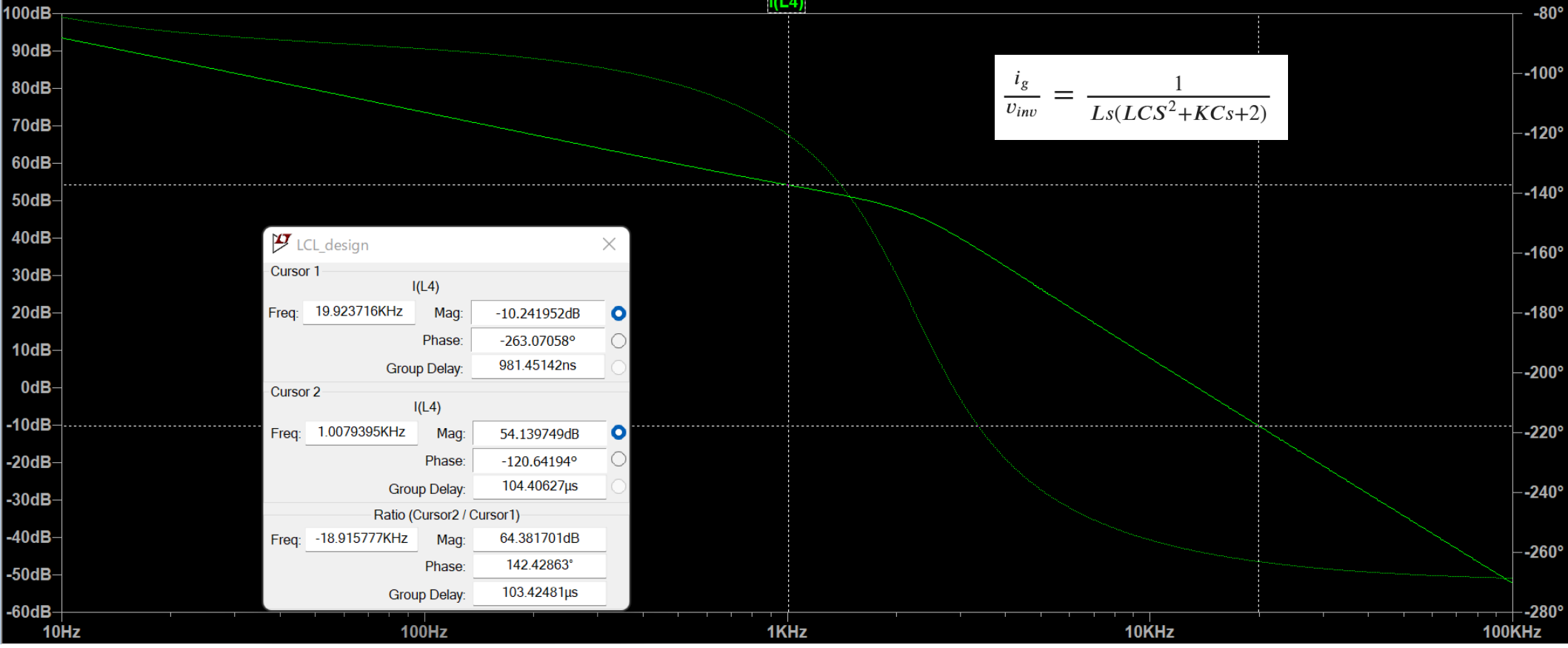


The proposed LCL filter with capacitive feedback, its designed to make the phase margin 120 degree at 1KHz which is the controller Bandwidth

L=100uH, C=100uF (also meets the reactive power requirement), K=2.5m*600

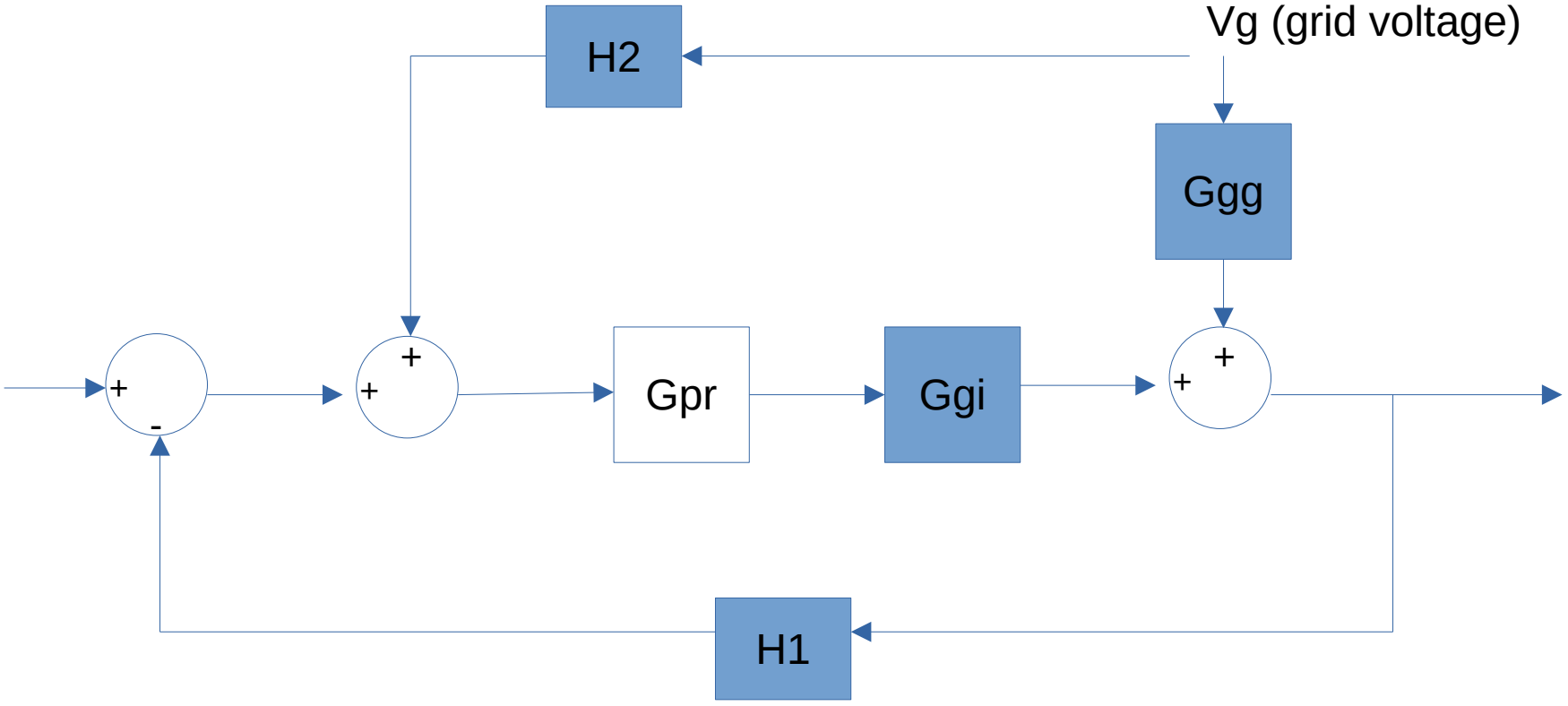
$$\frac{i_g}{v_{inv}} = \frac{1}{Ls(LCS^2+KCs+2)}$$

Vg is 50dB, and ig required is ~-17dB



The above plot is ig/vi, at 20KHz, vg is supposed to be 50dB at 20KHz, here since the way simulation is performed vg is 55.56dB at 20KHz, which results in -10.24dB Ig, this means from the filter we have ~67dB attentuation at 20KHz, so if vg is 50dB at 20KHz, we would have ig as -17dB which is the required value

The system block diagram



$$G_{gi} = \frac{i_g}{v_{inv}} = \frac{1}{Ls(LCS^2+KCs+2)}, G_{gg} = -G_{gi}(1 + LCs^2)$$

$$i_g = \frac{i_{ref} G_{PR} G_{gi}}{1+H_1 G_{PR} G_{gi}} + \frac{v_g(G_{gg}+H_2 G_{PR} G_{gi})}{1+H_1 G_{PR} G_{gi}}$$

$H_2 = \frac{-G_{gg}}{G_{PR} H_2}$ at 50Hz (phase is 0 degree at 50Hz for PR controller its designed as such)

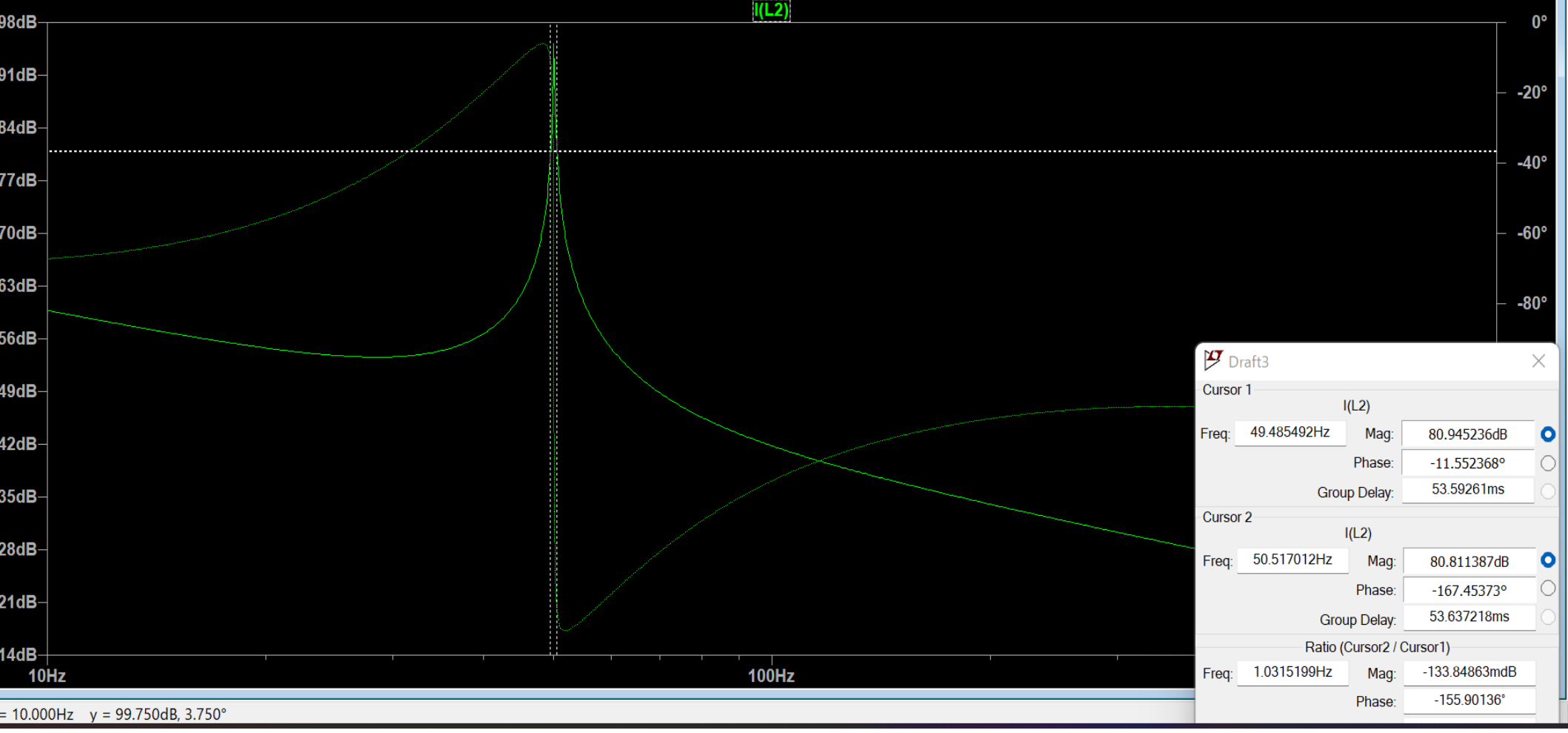
The steady state error in grid current is

$$i_g = \frac{i_{ref} G_{PR} G_{gi}}{1+H_1 G_{PR} G_{gi}}$$

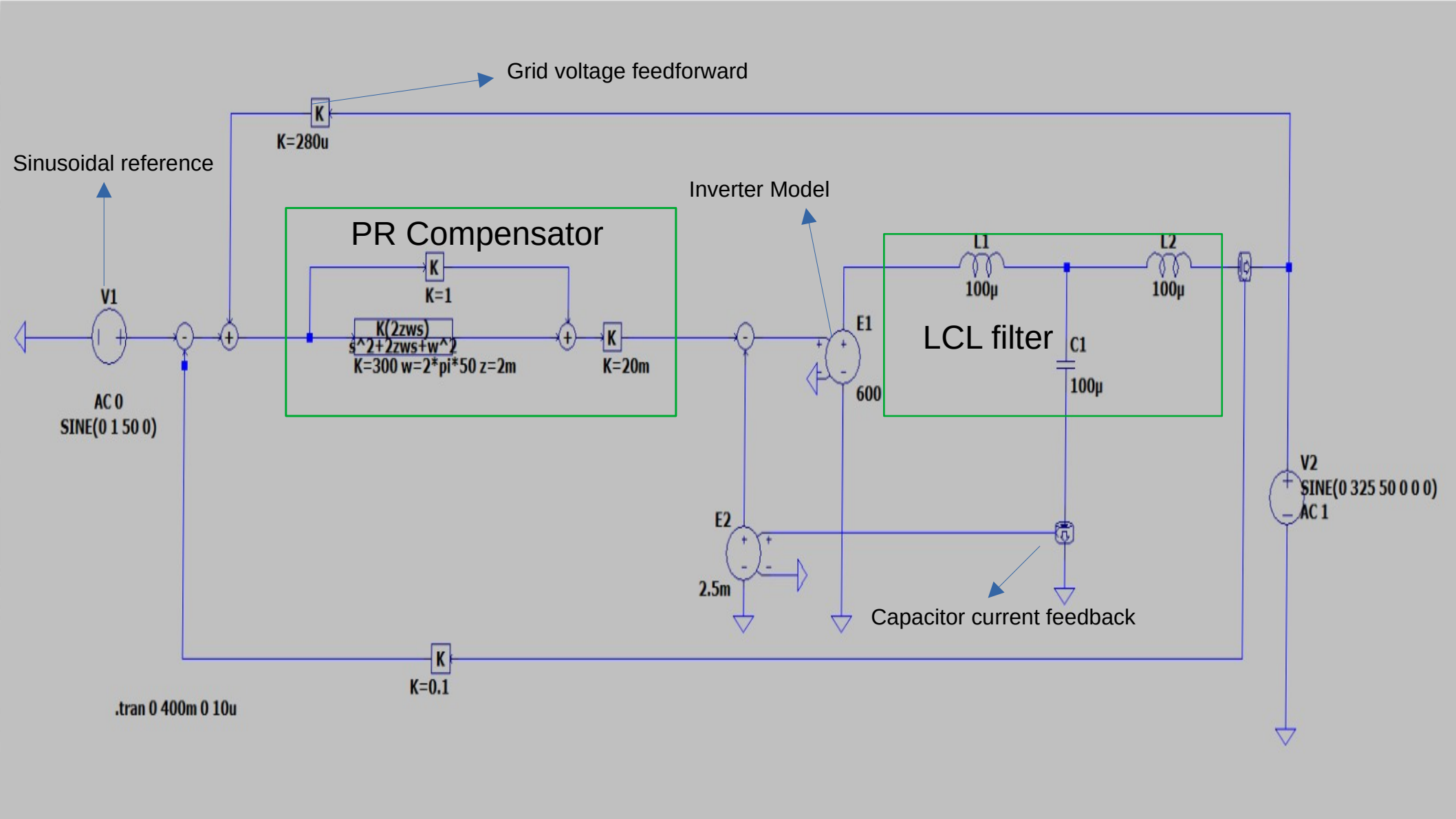
$$i_{ref}/H_1 - i_g = \frac{i_{ref}}{H_1(1+H_1 G_{PR} G_{gi})} < -40dB, H_1 = -20dB$$

$G_{PR} G_{gi} > 80dB$ at 50Hz

The phase deterioration by PR controller is limited to at max 5 degree from -180 and since, the grid frequency can vary the bandwidth of PR controller is chosen to be 1Hz around 50Hz



Bode Plot of Gpr*Ggi, the phase margin requirement is met and the magnitude is above 60dB for the required bandwidth


Grid voltage feedforward
K
K=280u
Sinusoidal reference
Inverter Model
PR Compensator
K
K=1
V1
K(2zws)
s^2+2zws+w^2
K=300 w=2*pi*50 z=2m
K
K=20m
AC 0
SINE(0 1 50 0)
E1
600
L1
100µ
L2
100µ
LCL filter
C1
100µ
V2
SINE(0 325 50 0 0 0)
AC 1
E2
2.5m
Capacitor current feedback
K
K=0.1
.tran 0 400m 0 10u

Time domain simulation