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COMP256 – Computing Abstractions
Dickinson College
LAB #4
Volatile Memory: Dynamic and Static RAM

Introduction:

Computer memory comes in two main varieties:

- **Persistent Memory**: This is storage that persists when the machine's power is turned off. It is used to save data and programs between power cycles. Common persistent memory includes disk drives (HDD, SDD), flash (USB/thumb) drives and tapes, CDs or DVDs.
- **Volatile Memory**: This is storage that holds instructions of programs that are currently executing and the data on which they are operating. Volatile memory in modern computers includes the main memory (RAM), the CPU registers and the cache memory.

This lab will examine two types of volatile memory:

- **Dynamic RAM (DRAM)**: Dynamic RAM is very small and relatively inexpensive to build. Thus, it is possible to create lots of it on a single chip. This is the type of RAM that makes up the computer's main memory. Typical computers today have between 8 and 32 GB (gigabytes = 2^{30} = 1073741824 bytes) of main memory. While small and cheap, DRAM also has properties that we will see makes it operate more slowly than SRAM.
- **Static RAM (SRAM)**: Static RAM requires more transistors to build than DRAM and thus costs more and takes up more space on a chip. However, it is significantly faster than DRAM. The registers and cache memory in computers are built using SRAM to make them as fast as possible, despite the higher cost.

A DRAM Cell:

A DRAM cell can store one bit; a single 0 or 1. It is constructed from a single N-Type transistor (Figure 1), a resistor (Figure 2) and a capacitor (Figure 3). A capacitor is an electronic component that is like a very small rechargeable battery. When the capacitor is charged it stores a 1, when it is discharged (think dead battery) it stores a 0.

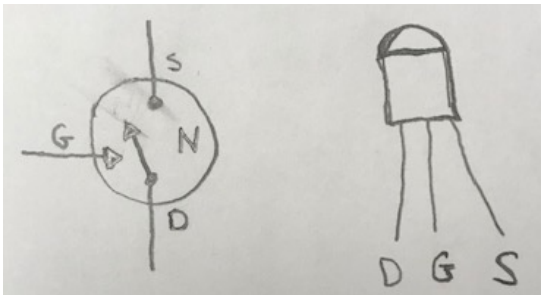

Figure 1: An N-Type Transistor

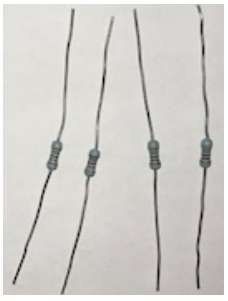
Figure 2: Four Resistors

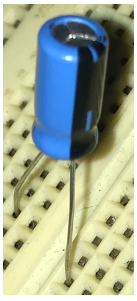
Figure 3: A Capacitor

1. Use an N-Type transistor, a resistor and a capacitor to build the circuit for a DRAM cell as shown in Figure 4. Note that the shorter lead of the capacitor (also indicated by the black line and a '-' sign) should be connected to ground. The *Sel (select)* and *b (bit value)* inputs should be connected to Logic Switches and the *Q* output should be connected to a Logic Indicator. **Show your circuit to the instructor before continuing.**

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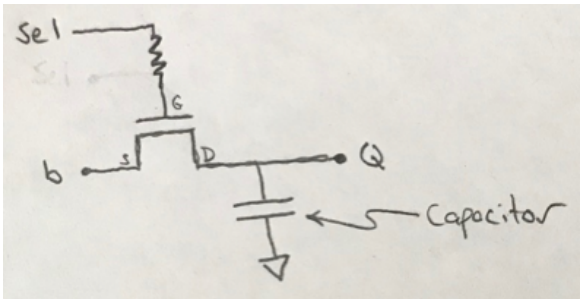

Figure 4: A DRAM Cell and the capacitor schematic symbol.

2. In the DRAM cell the Sel and b inputs control writing to the cell and the Q output indicates the value stored in the cell. To help understand these inputs, experiment with the circuit and answer the following questions.

a. If Sel = 1 what happens to Q when b is changed from 0 to 1 or 1 to 0?

b. What values of Sel and b will always make Q = 1?

Sel ____ b ____

c. What values of Sel and b will always make Q = 0?

Sel ____ b ____

d. With Q = 1 and Sel = 0, what happens to Q when b is changed from 0 to 1 or 1 to 0?

e. With Q = 0 and Sel = 0, what happens to Q when b is changed from 0 to 1 or 1 to 0?

3. Based on your experiments in the previous question describe the process by which a bit value (0 or 1) can be stored into the DRAM cell. Note: A value is stored when the Q output reflects that value even while the b input is changing.

4. Using the DMM measure the voltage at Q with Sel = 1 and as the value in the cell is changed from 0 to 1.

a. Does the voltage at Q go immediately to its maximum value?

b. What is the maximum voltage after a 1 is stored in the cell? About how long does it take to reach this voltage?

c. Set Sel = 0 to store the value 1. What happens to the voltage over time after Sel is set to 0?

d. About how long does it take before the voltage drops to where the cell no longer stores a 1 (i.e. the high Logic Indicator goes out)?

What you have just observed are two of the aspects of DRAM that give it the *dynamic* part of its name.

- To store a 1 or a 0 requires that the capacitor be charged (1) or discharged (0). While this happens much faster than it does for your cell phone battery, it still takes some time. The capacitors used in actual DRAM chips are much much smaller so the charge and discharge significantly faster than we observed. However, it still takes some time. This makes DRAM slower than SRAM which, as we will see does not use a capacitor.

- The charge on the capacitor "leaks". Thus, a 1 stored in a DRAM cell will slowly degrade over time until it is no longer a 1. To compensate for this DRAM also contain refresh circuits that periodically (typically every 64 milliseconds or about 16 times/second) read and rewrite all of the 0's and 1's in the memory to keep them "fresh." (Note: We will not build this part of a DRAM – ours will stay leaky.)

A (very) Small DRAM Module:

The DRAM cell above stored 1 bit. Computer main memories obviously store more than that, typically 8 to 32 GB today. In this section, we'll build a (very) small DRAM module to understand how complete bytes or words can be stored into memory.

5. Construct the 2x2 DRAM module shown in Figure 5. This circuit will be able to store two words of 2-bits each (thus 2x2). Connect the Sel and b inputs to Logic Switches and the Q outputs to Logic Indicators. **Show your circuit to the instructor before continuing.**

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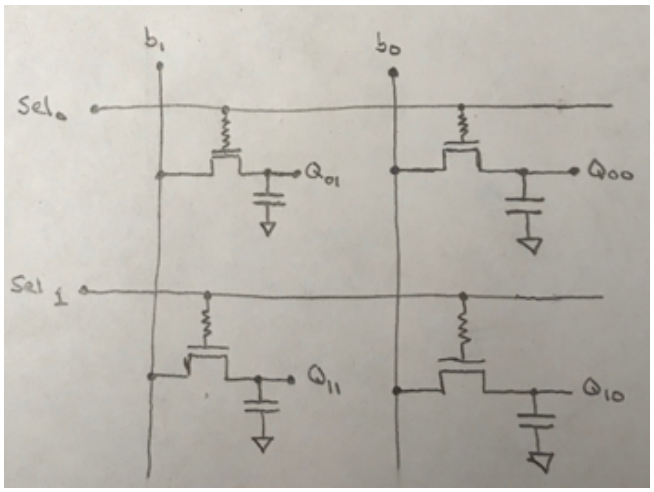

Figure 5: A 2x2 DRAM Module

6. The subscripts on Sel and b indicate the word and bit within the word. For example, Sel_0 is the select for word 0 and b_1 is the value to write to bit 1 of the 2-bit word. Fill in the values below to indicate how to perform each of the actions.

a. Store the word 01 into word 0 of the DRAM module. Word 1 should be unchanged.

Sel_0 ____ Sel_1 ____ b_1 ____ b_0 ____

b. Store the word 11 into word 1 of the DRAM module. Word 0 should be unchanged.

Sel_0 ____ Sel_1 ____ b_1 ____ b_0 ____

c. Briefly explain the general process for storing a value into a word in the DRAM.

An SRAM Cell:

As we saw DRAMs do not require many components to build. Thus, they are small and inexpensive. However, because they rely on charging and discharging a capacitor they are also slow and "leaky." This turns out to be a good cost / performance tradeoff for the very large main memory of the computer. However, modern CPUs can process data much faster than a DRAM can provide it. Thus, other parts of the computer's memory hierarchy (e.g. registers and cache) are built using much faster SRAM cells.

7. Construct the SRAM cell circuit shown in Figure 6. This particular type of SRAM cell is often called a Clocked or Gated D-Latch. The part numbers and the pinout diagrams for the chips can be found on the back page of this lab. **Show your circuit to the instructor before continuing.**

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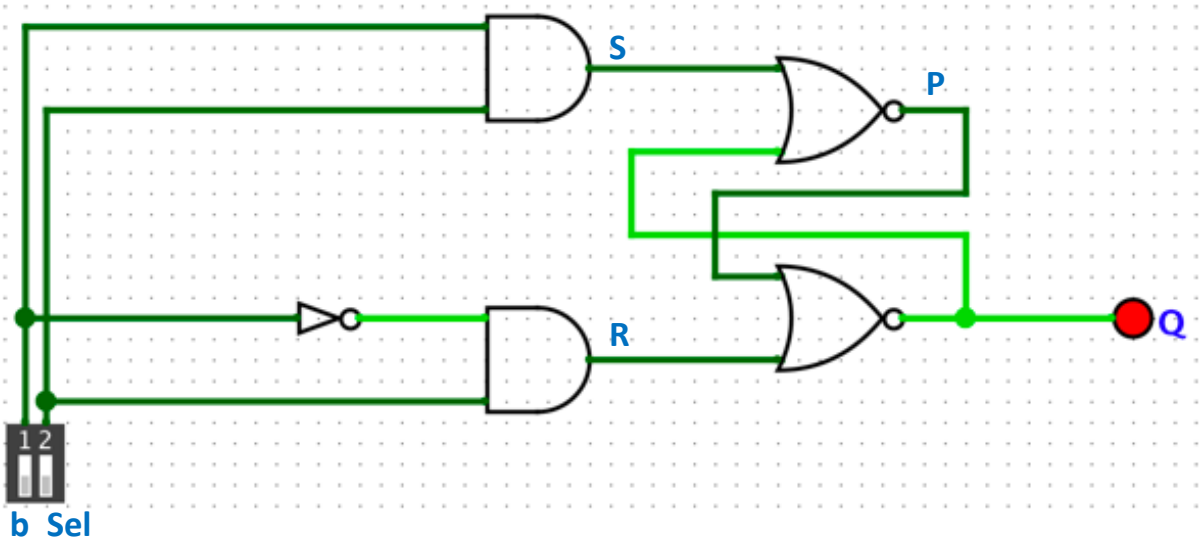

Figure 6: A Clocked D-Latch based SRAM cell.

8. Like in the DRAM cell, the Sel and b inputs control writing to the SRAM cell and the Q output indicates the value stored in the cell. Experiment with the circuit and answer the following questions.

a. If Sel = 1 what happens to Q when b is changed from 0 to 1 or 1 to 0?

b. What values of Sel and b will always make Q = 1?

Sel ____ b ____

c. What values of Sel and b will always make Q = 0?

Sel ____ b ____

d. With Q = 1 and Sel = 0, what happens to Q when b is changed from 0 to 1 or 1 to 0?

e. With Q = 0 and Sel = 0, what happens to Q when b is changed from 0 to 1 or 1 to 0?

f. How does the behavior of the SRAM cell you just observed compare to that of the DRAM cell you experimented with in question 2?

9. Is the SRAM cell “leaky” like the DRAM cell is? Describe how you determined this.

10. How many transistors are in the SRAM cell in Figure 6?

11. It should be fairly clear at this point that to produce larger memories using SRAM cells, we could simply replace the DRAM cells in Figure 5 with SRAM cells. How many transistors would be in the 2x2 RAM module if it were built with SRAM cells?

12. Fill in the table below indicating the advantages and disadvantages of DRAM and SRAM memories.

	Advantages	Disadvantages
DRAM memory		
SRAM memory		

Combinational vs Sequential Circuits

Notice that the SRAM circuit in Figure 6 is different from other circuits that we have built because it contains a feedback loop. The output of each NOR gate is connected back to an input of the other. Circuits with this type of feedback are called *sequential circuits*. The feedback loop in this sequential circuit makes it so that a change in the output of one of the NOR gates will change the input to the other NOR gate. That in turn, might change its output, which changes the input to the other, and so on and so on... While we will see that this type of cycle does occur, the circuit is designed so that the values will settle down rather quickly to a stable state where no further changes occur.

By comparison, in all of the other circuits we have built the inputs flowed through the circuit directly from the input to the output without any feedback. Circuits of that type are called *combinational logic circuits* (or just logic circuits for short).

13. Let's dig in a little to understand how a sequential circuit, and our SRAM cell in particular, works. We will do this by separating the behavior of the circuit base on the value of Sel.

a. If Sel = 0 what are the values of S and R?

S ____ R ____

b. Given those values of S and R we can build the following truth table that shows what will happen to the value of Q when Sel = 0. Fill in the value of P (by using the values of S and Q) and then fill in the *next value* of Q (by using the values of P and R).

Sel = 0

S	R	Q	P	Next Q
0	0	0		
0	0	1		

c. Based on the truth table in part b, write a sentence summarizing abstractly how the next value of Q relates to its current value when Sel = 0?

d. If Sel = 1 give an expression for S and R in terms of the input b?

S = _____ R = _____

e. Given the above relationships between b and S and R when Sel = 1 we can build the following truth table that shows what will happen to the value of Q when Sel = 1. Fill in the values of S, R, P and the *next stable value* of Q. To find the next stable value of Q you will need to change the values P and Q going around the feedback loop until there are no further changes.

Sel = 1

b	Q	S	R	P	Next Stable Q
0	0				
0	1				
1	0				
1	1				

f. Given the table in part e, write a sentence summarizing abstractly how the next stable value of Q relates to b when Sel = 1?

g. Write a few sentences explaining abstractly how this SRAM behaves as a function of b, Sel and Q and why that makes it a 1-bit memory.

14. Clean up your workspace by removing all wires and chips from the Proto-Board, returning the chips to the parts bin, powering off the Proto-Board and DMM and neatly storing the DMM with its leads wrapped around it.

Logic Chips and Pin-Out Diagrams: