

NAMES: _____

COMP256 – Computing Abstractions
Dickinson College
LAB #2
CMOS Logic Gates and Integrated Circuits

Introduction:

In the first lab you were introduced to the Proto-Board (Figure 1) and the Digital Multimeter (DMM) (Figure 2). You explored the properties of switching using a “knife” switch, an electromagnetic relay and both N-Type and P-Type transistors. In this lab you will build upon that experience by creating several logic gates from transistors and then experimenting with integrated circuit chips that package those gates into easier to use abstractions.

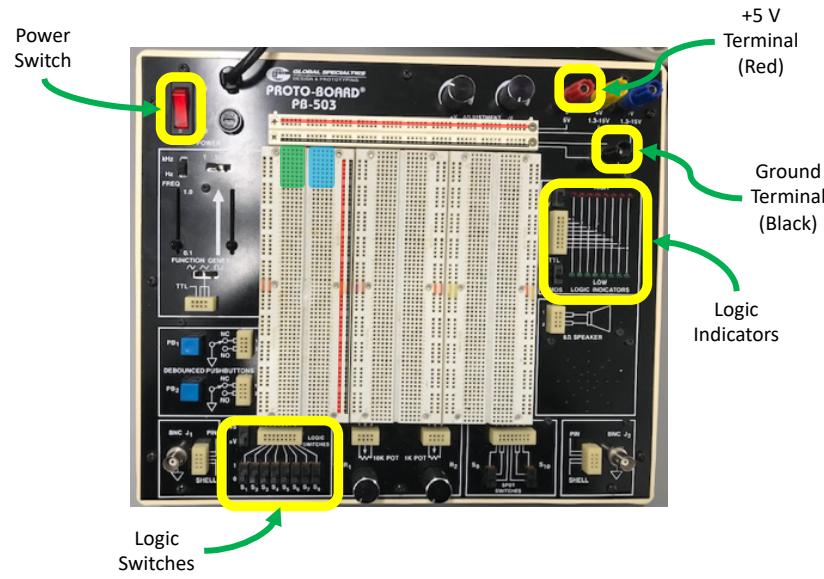


Figure 1: The Proto-Board with the essential elements labeled.

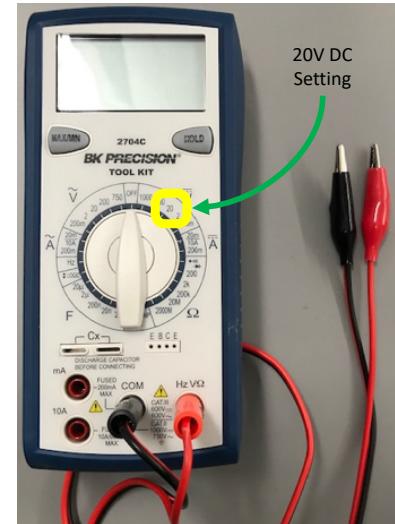


Figure 2: Digital Multimeter

A CMOS NOT gate:

We've seen the circuit for a Complementary Metal Oxide Semiconductor (CMOS) NOT gate in class and you have simulated it using Logisim-Evolution for homework. In this part of the lab you will build it using resistors and N-Type and P-Type transistors. Figures 3-5 identify and illustrate the resistors and transistors that are in the small parts bin at your lab station.

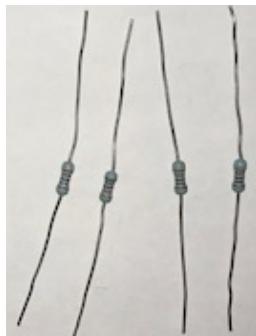


Figure 3: Resistors



Figure 4: Transistor



Figure 5: Transistor pin map

1. Ensure that the switches beside the Logic Switches and Logic Indicators are set to CMOS. And then use the resistors and transistors, one N-Type and one P-Type, from your parts bin to build a CMOS NOT gate as shown in Figure 6. Connect a Logic Switch as the input and a Logic Indicator as the output. **Have the instructor inspect your circuit when it is complete and before turning on the Proto-Board power.**

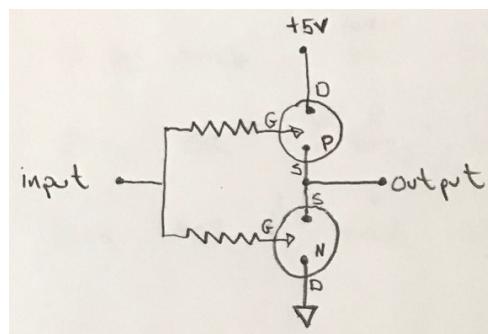


Figure 6: A CMOS NOT gate.

2. Using your CMOS NOT gate and the DMM complete the following table.

Input Logic Level	Input Voltage(V)	Output Logic Level	Output Voltage (V)
0 (low/false)			
1 (high/true)			

Another CMOS Logic Gate:

3. Construct the circuit shown in Figure 7. **Have the instructor inspect your circuit when it is complete and before turning on the Proto-Board power.**
-

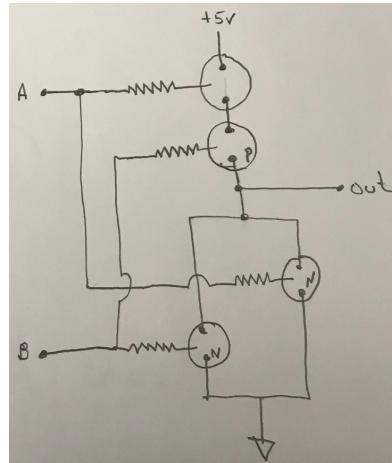


Figure 7: A CMOS logic gate circuit to be identified.

4. Design an experiment and collect data to determine what logic gate is implemented by the circuit in Figure 7. Describe your experiment in a few complete sentences. Provide the data you collected in a well-organized table in the space below. Use the data you have collected to identify the logic gate and then give its schematic symbol.

The 4049 Hex Inverter Integrated Circuit:

Rather than building complex logic circuits directly from transistors it is more common to use integrated circuits that package up multiple logic gates into a single *chip*. Figure 8 shows a typical dual in-line package (DIP) integrated circuit chip. You will find several of these in the parts bin at your station.

Each chip has lettering and numbering on it that indicates its functionality. The *pins* on the sides of the chip provide connections to the circuitry (i.e. transistors) that is built into the chip. Figure 9 shows how the pins of the 4049 chip are connected to the inverters (NOT gates) that are built into this chip.

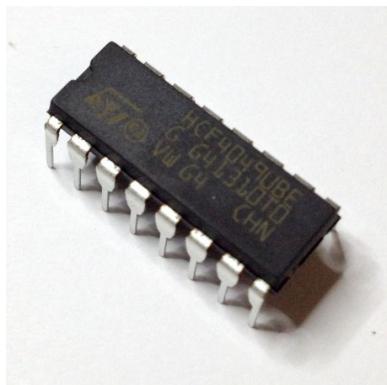


Figure 8: A DIP integrated circuit chip.

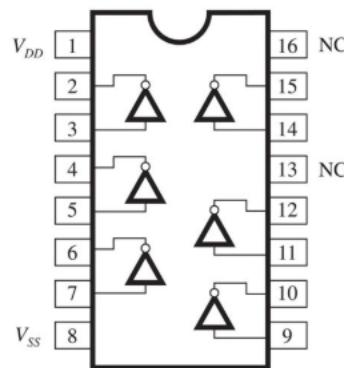


Figure 9: Schematic of the 4049 Hex Inverter.

5. Notice the semi-circular notch in one edge of the chip and also shown in Figure 9. What is the purpose of this notch? NOTE: Some chips may have a full circle cut into the plastic of the chip rather than just a notch in the edge.

6. V_{DD} and V_{SS} are common notations for ground and the positive voltage supply (e.g. +5 V) respectively. So, for the 4049, which pin should be connected to ground? Which should be connected to 5V?

The Proto-Board is designed to make wiring of DIP integrated circuits convenient. Figure 10 shows a 4049 chip wired on the protoboard. Notice how the chip goes across the vertical channel between the wide vertical columns. Recall that the holes in these wide vertical columns are connected horizontally. Thus, this configuration provides a convenient way to connect to the input and output pins of the chips.

7. Being careful that that pins fit precisely in the holes, place a 4049 chip on your Proto-Board and wire it as shown in Figure 10. Use a Logic Switch as the input (blue wire coming in from left) and a Logic Indicator as the output (green wire going out to right). **Have the instructor inspect your circuit when it is complete and before turning on the Proto-Board power.**

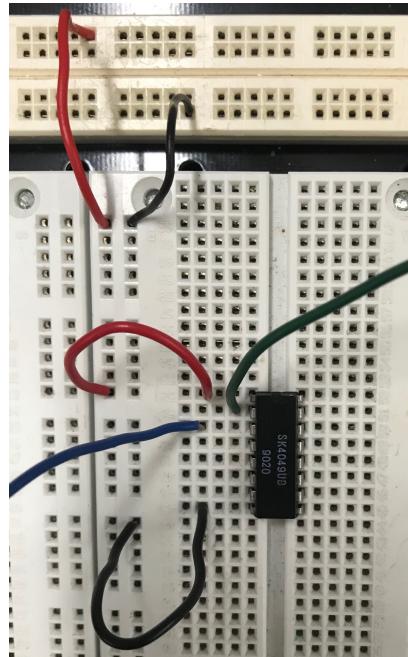


Figure 10: Wiring for the 4049 Hex Inverter chip

8. Using the circuit from #7 with the 4049 chip and the DMM complete the following table.

Input <u>Logic Level</u>	Input <u>Voltage(V)</u>	Output <u>Logic Level</u>	Output <u>Voltage (V)</u>
0 (low/false)			
1 (high/true)			

Other CMOS Integrated Circuits:

In your parts bins you will find several other chips that contain logic gates as well. There should be two 4071 chips and two 4081 chips. Note that there may be additional letters around or even between the number 4071 and 4081 that indicate other characteristics of the chips that are not of particular interest to us.

Figure 11 shows an obscured schematic diagram for these chips. This diagram is the same for both the 4071 and 4081. Typically, however, the schematic diagram for the chip will show the schematic symbol of the gates. In Figure 11, I have obscured those symbols with a '?' because you will be asked to figure them out.

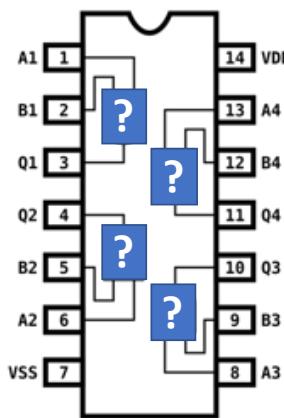


Figure 11: Obscured schematic of the 4071 and 4081 chips.

9. Answer the following questions about these chips based on the schematic in Figure 11.

a. Which pin should be connected to ground?

b. Which pin should be connected to +5V?

c. For each gate on the chip add a row under the headings below that indicates which pins are its inputs and which pin is its output.

<u>Input Pins</u>	<u>Output Pin</u>
-------------------	-------------------

10. Wire up one of the gates (they are all the same) on a 4071 chip using two Logic Switches as inputs and a Logic Indicator as the output. Fill in the table below by measuring the outputs for all possible combinations of Logic Level (0, 1) for Inputs A and B. Then identify the type of logic gate contained on the 4071 and give its schematic symbol.

Input A <u>Logic Level</u>	Input B <u>Logic Level</u>	Output <u>Logic Level</u>	Output <u>Voltage (V)</u>
-------------------------------	-------------------------------	------------------------------	------------------------------

11. Repeat question #10 for the 4081 chip.

Input A <u>Logic Level</u>	Input B <u>Logic Level</u>	Output <u>Logic Level</u>	Output <u>Voltage (V)</u>
-------------------------------	-------------------------------	------------------------------	------------------------------

Challenge: Designing & Building a Logic Circuit:

Now that we know we have chips containing NOT, AND and OR logic gates you can use those to implement computations.

A particular manufacturing process has three sensors (A,B,C). Each of these three sensors outputs either a 0 or a 1. The production of an acceptable product requires that:

- Sensor A must be a 1
- Sensor B may be a 1 but only if C is a 0.
- Sensor C may be a 1 but only if sensor B is also a 1.

12. Create a truth table for a logic function Z that has the value 1 if the product is acceptable and 0 if it is not.

13. Write a Sum-Of-Products (SOP) expression for Z in terms of the sensor readings A, B, and C.

14. Simplify the SOP expression from #13 using the Boolean Identities.

15. Draw a schematic diagram for a circuit that implements the expression from #14.

16. Build the circuit from #15 using the 4049, 4071 and 4081 chips. Test that your circuit works correctly by completing the table below for all combinations of the inputs A, B, C.

Input A <u>Logic Level</u>	Input B <u>Logic Level</u>	Input C <u>Logic Level</u>	Output <u>Logic Level</u>	Output <u>Voltage (V)</u>
-------------------------------	-------------------------------	-------------------------------	------------------------------	------------------------------

17. Demonstrate your circuit for the instructor when it is functioning correctly.

18. Clean up your workspace by removing all wires and chips from the Proto-Board, returning the chips to the parts bin, powering off the Proto-Board and DMM and neatly storing the DMM with its leads wrapped around it. See Figure 12 for the suggested technique for removing chips from the Proto-Board using the tweezers. This technique prevents the pins from being bent during removal.



Figure 12: Removing a chip from the protoboard.