VIETNAM NATIONLA UNIVERSITY, HO CHI MINH CITY
UNIVERSITY OF INFORMATION TECHNOLOGY
FACULTY OF COMPUTER ENGINEERING
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DIGITAL CIRCUIT DESIGN- CE222.O23.MTCL

REPORT LAB 02

DESIGN AND SIMULATION OF A FULL ADDER USING ONLY NAND GATES (2 INPUT)

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STUDENT ID: 21521970
Lecturer: Tạ Trí Đức

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CHAPTER 1. DESIGN AND SIMULATION OF A 2-INPUT NAND GATE

1. Theory of the 2-Input NAND Gate

1.1. Introduction

The NAND gate (NOT-AND) is one of the basic logic gates in digital electronics. A NAND gate has two inputs and one output. The output of the NAND gate will be high (1) if at least one of the inputs is low (0). Conversely, the output will be low (0) only when all inputs are high (1).

1.2. Truth Table

Here is the truth table for a 2-input NAND gate:

Input A	Input B	Output (A NAND B)
0	0	1
0	1	1
1	0	1
1	1	0

Table 1. True table of NAND

In this table:

- A and B are the input bits.
- Output (A NAND B) is the result of the NAND operation on inputs A and B.

2. Design schematic,symbol and find W/L of PMOS and NMOS

2.1. Design schematic and symbol

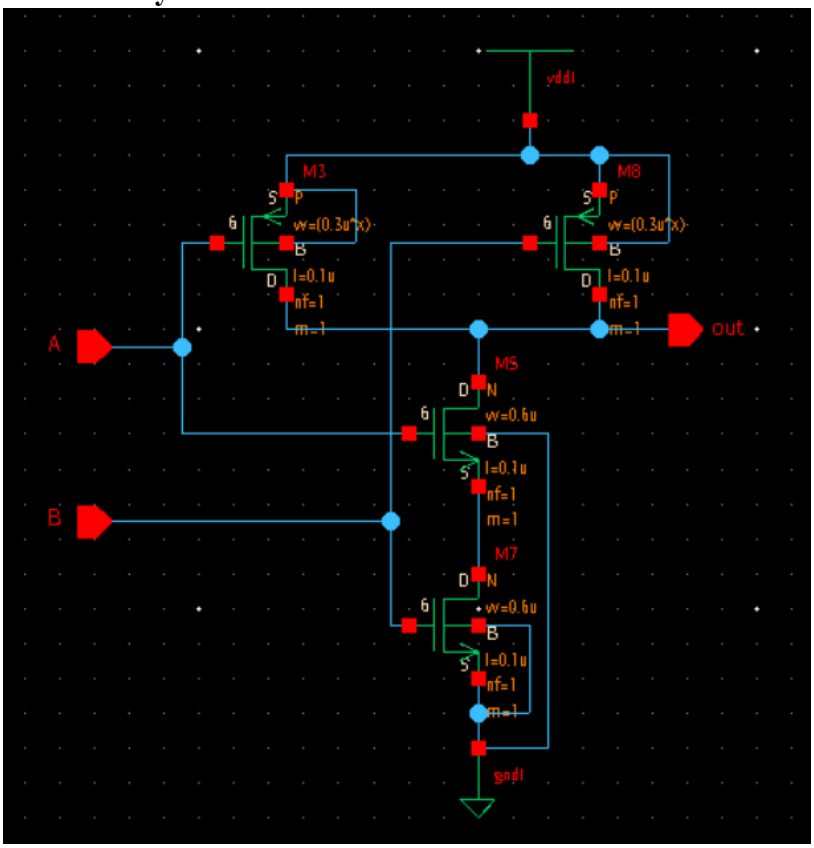

Figure 1. Schematic of NAND

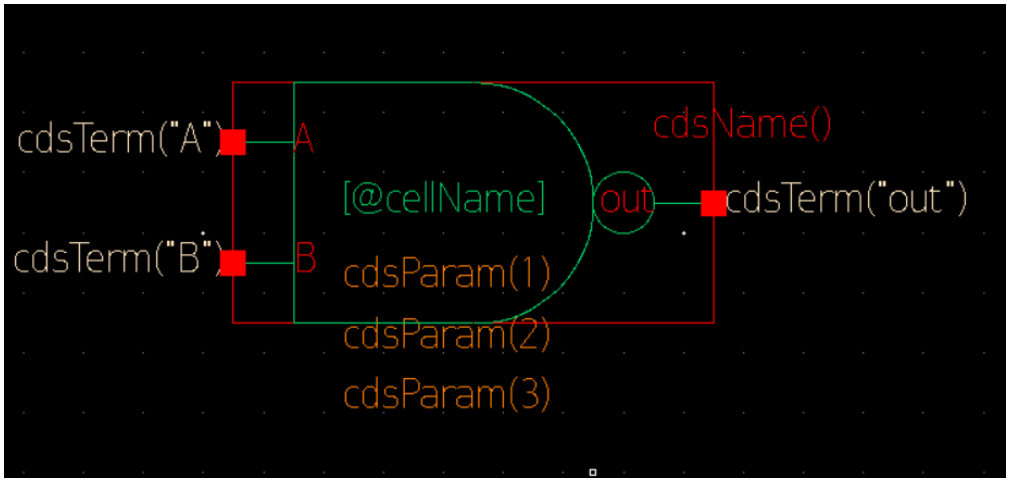

Figure 2. Symbol of NAND

2.2. Find W/L of PMOS and NMOS

We have:

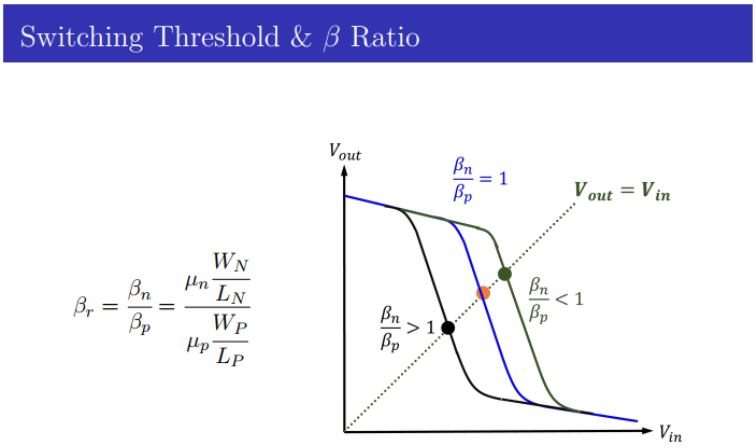

Figure 3. Switching Threshold & B ratio

The following parameters are provided by the library: nmos u0=4.031486^{-2},pmos u0=8.391744^{-3}

⇨ Wp/Wn = 4.8 ≈ 5 (I already show my equation in lab01)

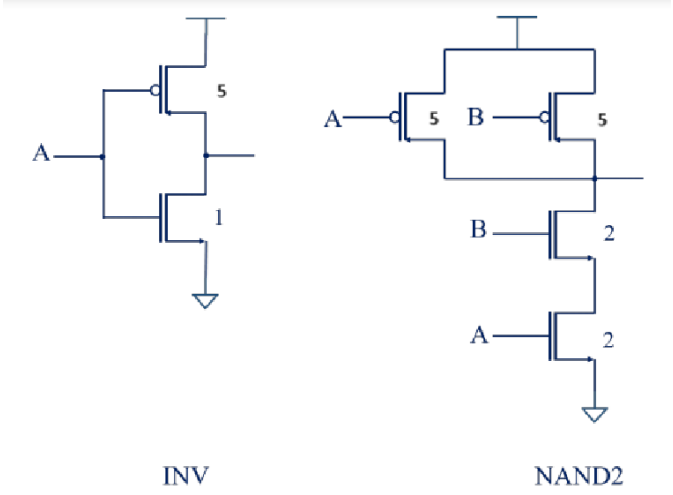

Figure 4. Transistor sizing.

Note:1 unit = 0.3um

	WIDTH	**LENGTH**
PMOS	1.5um	0.1u
NMOS	0.6um	0.1u

Table 2. W/L of NAND by theoretical calculation

2.3. Using tool to assist in finding the W/L ratio

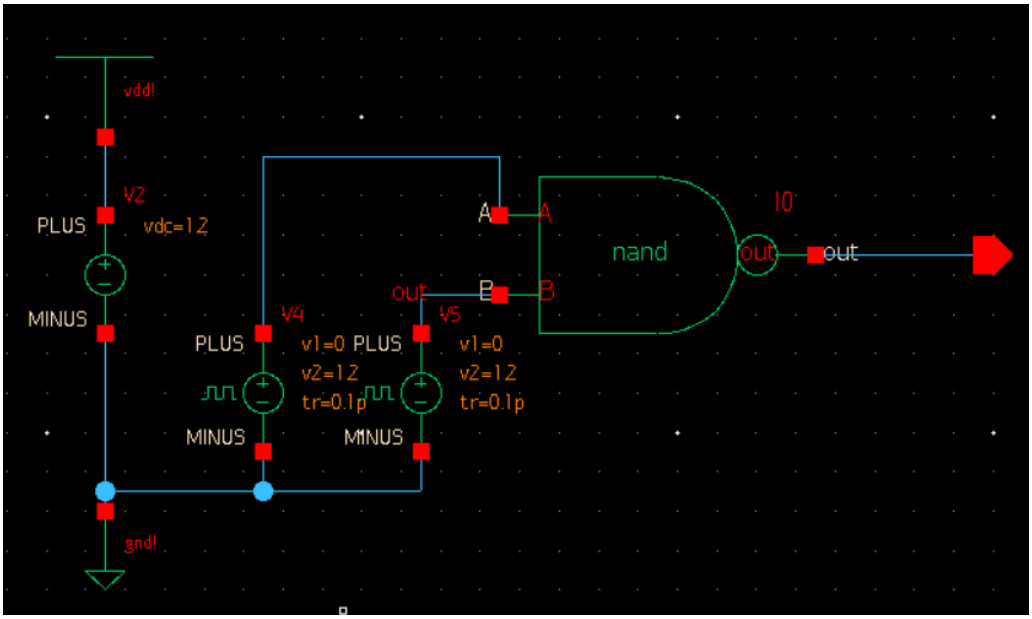

Figure 5. Testbench of NAND

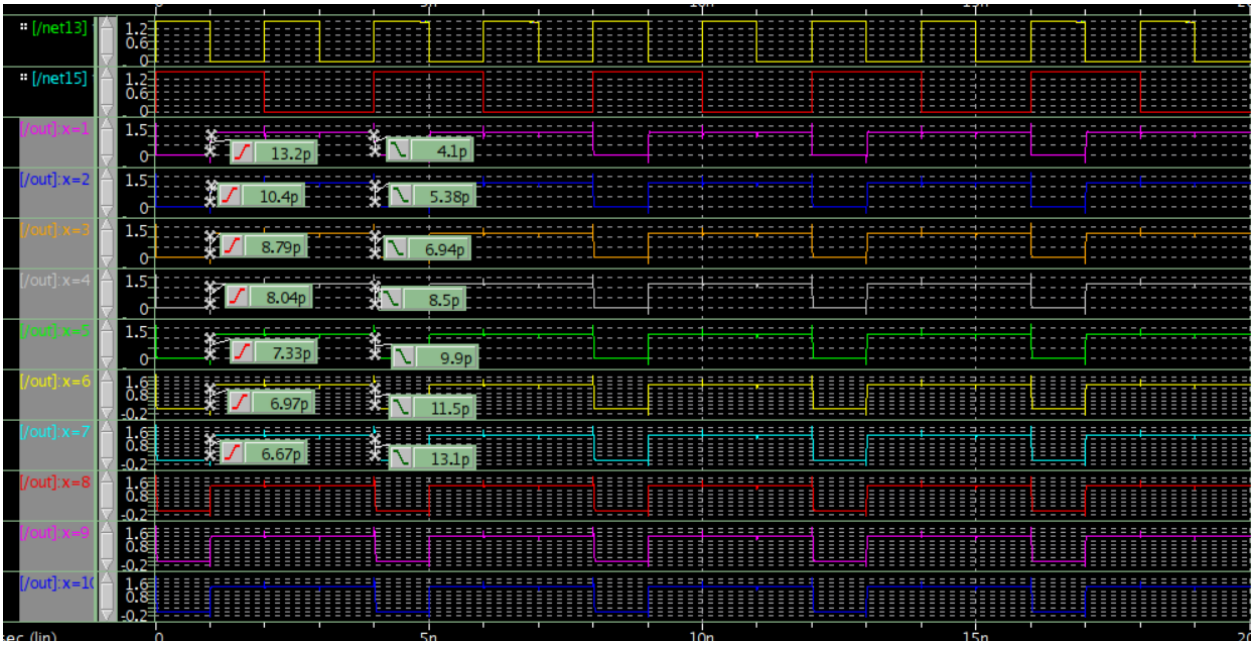

Figure 6. Waveform of testbench

Based on the difference between the rise time and fall time, we can see that at x=4, the discrepancy is the smallest. Therefore, we will choose the width (W) of the PMOS to be 0.3*4=1.2.

Finally, We will have the specifications for the transistors in the NAND gate as follows:

	WIDTH	**LENGTH**
PMOS	1.2um	0.1u
NMOS	0.6um	0.1u

Table 3. W/L of NAND by simulation

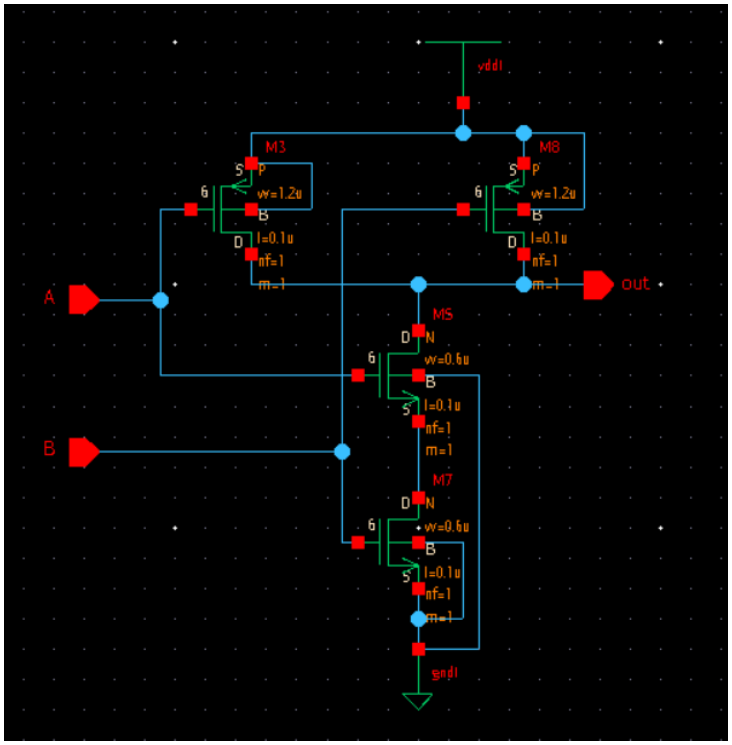

Table 4. Final Schematic of NAND

2.4. Control rise time and fall time

As we can see in the waveform, when we increase the size of the PMOS, the rise time decreases while the fall time increases. The size of the NMOS is kept constant, so it will not be considered. However, the fall time and rise time of the circuit are still not balanced (8.04≠8.5), so we will increase x within the range from 4 to 5 to find a more precise value.

The signal delay for fall time and rise time in the subsequent FA circuits will depend on the NAND gates, as the FA is composed of a collection of NAND gates. Therefore, we need to balance these here to minimize errors downstream.

Rise time	**Fall time**
8.04p	8.5p

Table 5. Rise time and Fall time of out signal

3. Layout NAND

3.1. Layout

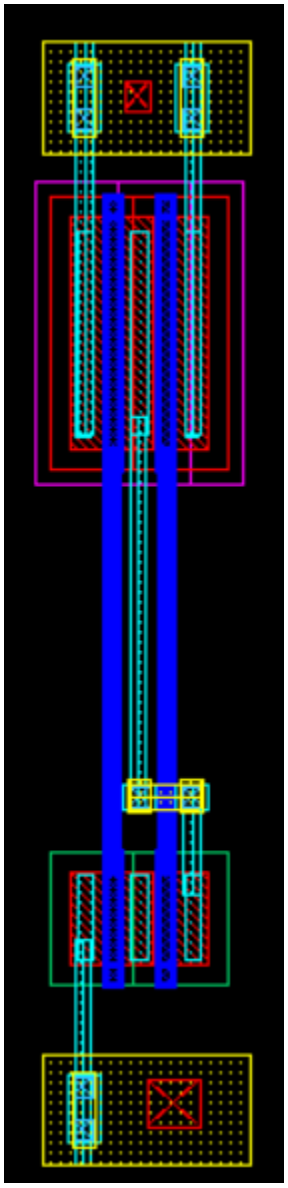

Figure 7. Layout of NAND

3.2. DRC

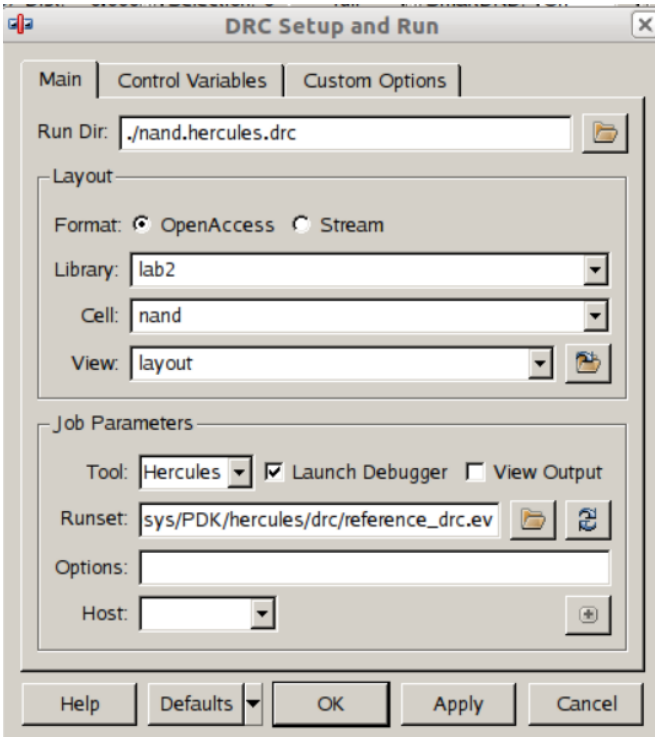

Figure 8. DRC main of NAND

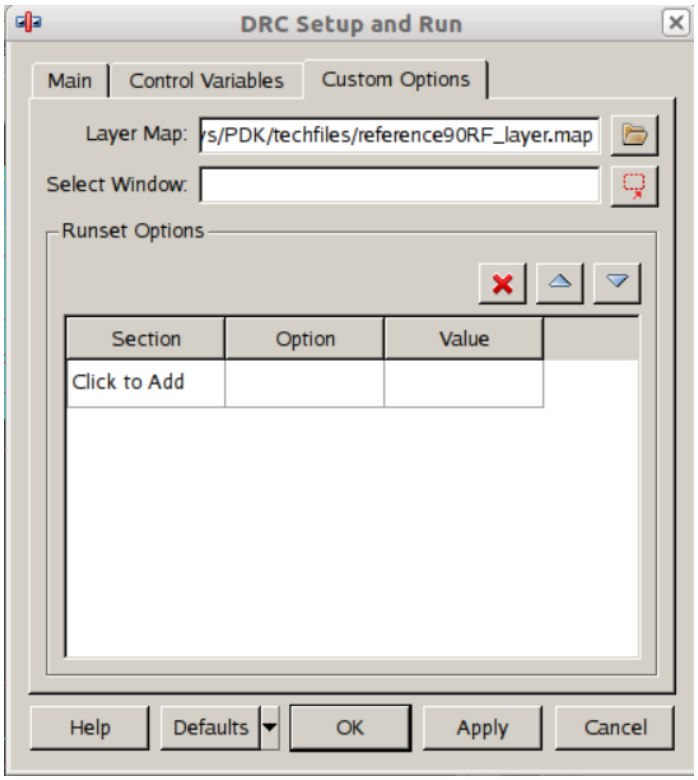

Figure 9: DRC Custom options of NAND

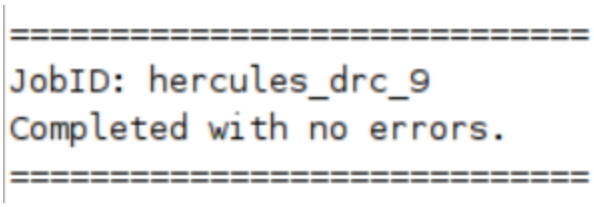

Figure 10. DRC result of NAND

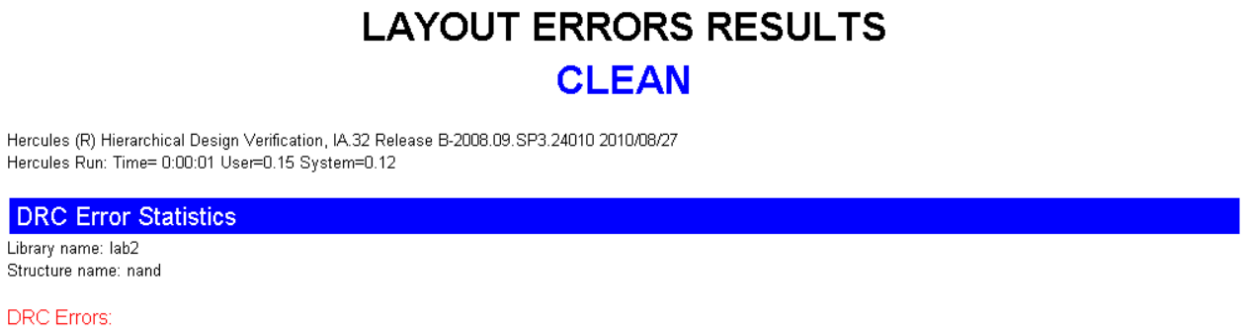

Figure 11. Debug DRC of NAND

3.3. LVS

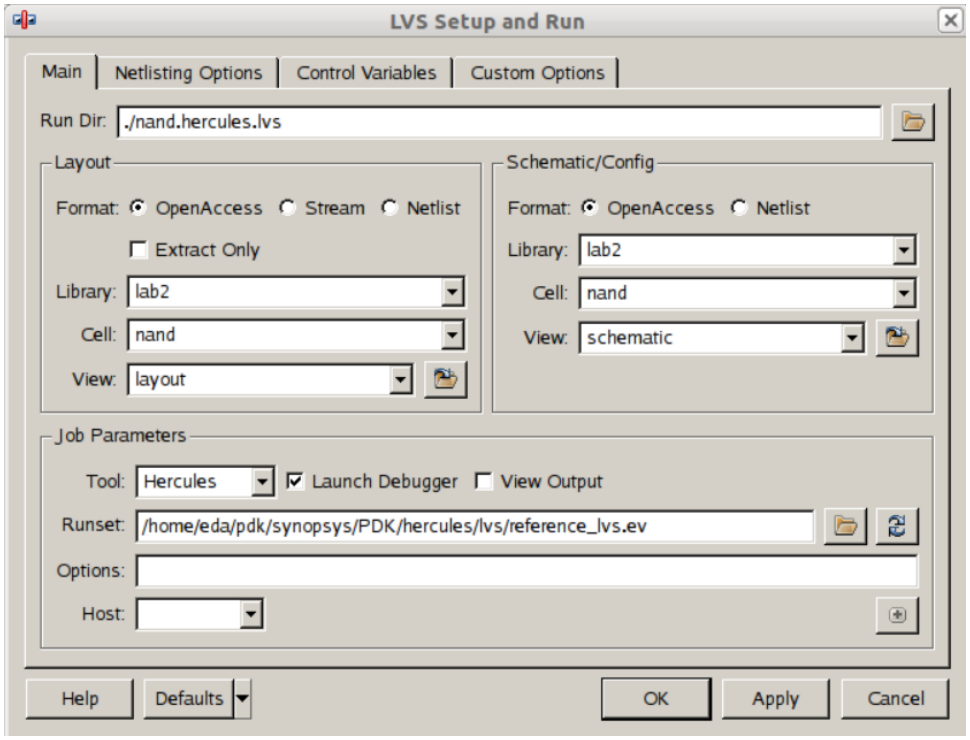

Figure 12. LVS MAIN of NAND

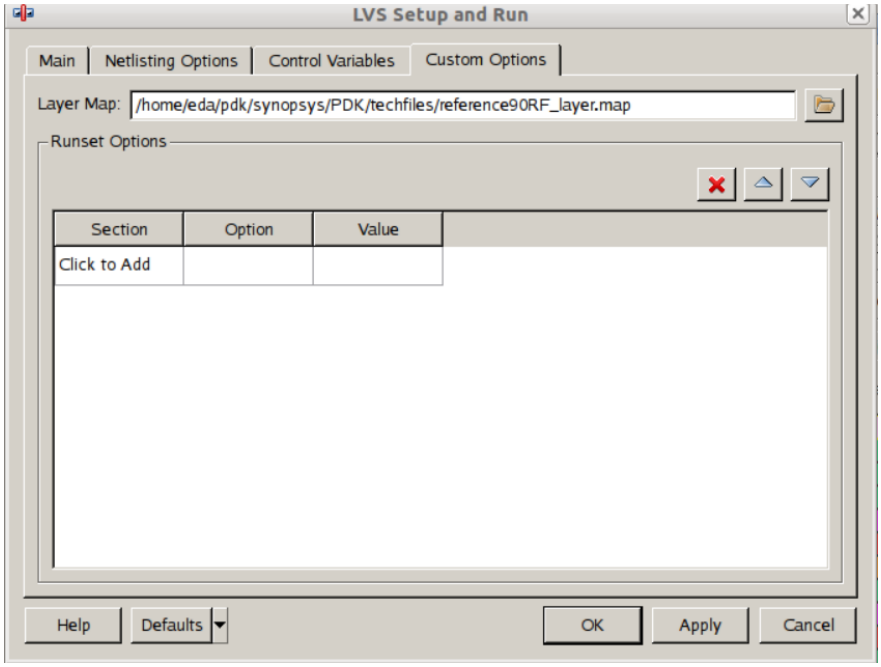

Figure 13. LVS Custom options of NAND

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JobID: hercules_lvs_8
Completed with no errors.
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Figure 14.LVS result of NAND

TOP BLOCK COMPARE RESULTS

CLEAN

[nand == nand]

Hercules (R) Hierarchical Design Verification, IA.32 Release B-2008.09.SP3.24010 2010/08/27
Hercules Run: Time= 0:00:04 User=0.30 System=0.72

Netlist Extraction Statistics

Library name: lab2
Structure name: nand

Extraction Errors:

Layout vs. Schematic Statistics

Schematic: /home/ltk/nand.hercules.lvs/nand.sch_out
Comparison completed with 1 successful equivalencies
Comparison completed with 0 failed equivalencies

Figure 15. Debug LVS of NAND

3.4. LPE

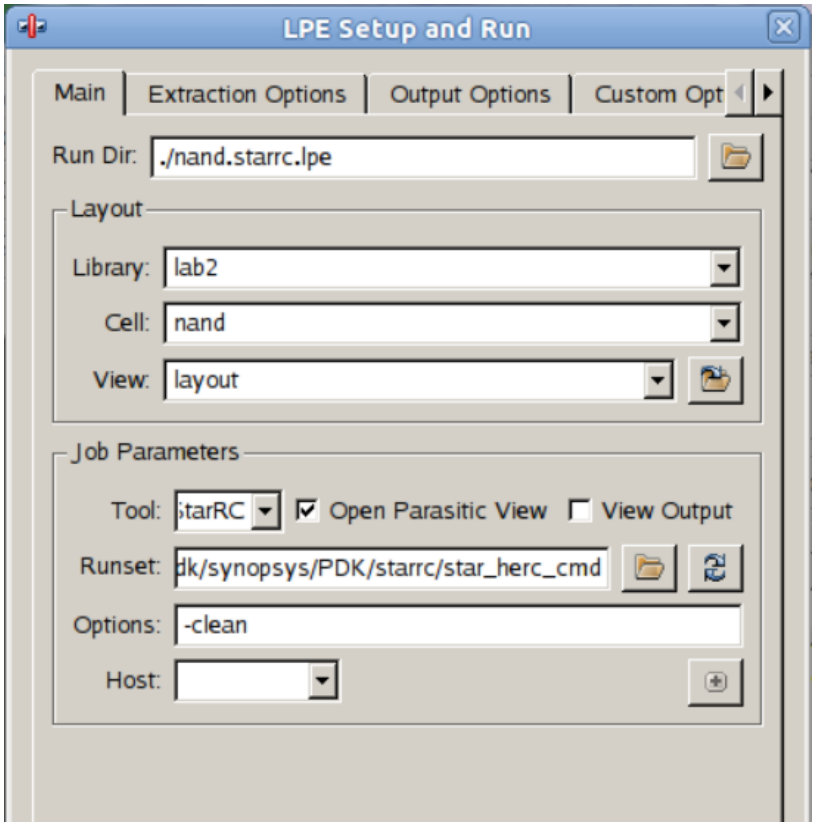

Figure 16.LPE main of NAND

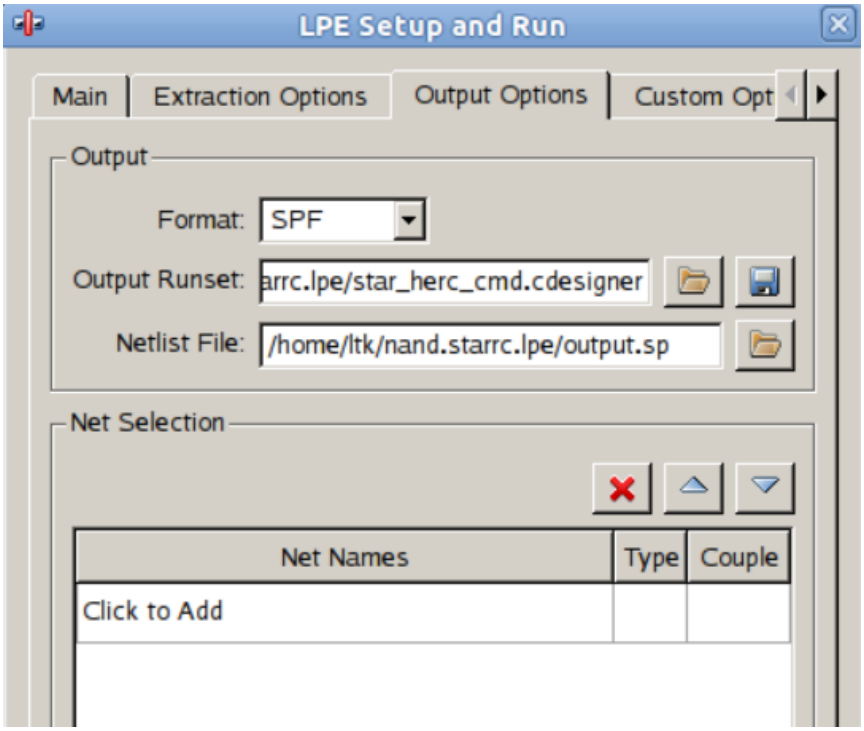

Figure 17.LPE Output option of NAND

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JobID: starrc_lpe_9
Completed with no errors.
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Figure 18. LPE result of NAND

3.2. Post Layout

Top Cellview

Library: lab2 Cell: nand_test View: schematic

View Search List: schematic hspice symbol

View Stop List: symbol

Library Search List:

Instance	Bound	Selected	View Search List
lab2/nand_test	schematic		
I0(lab2, n...	spice	spice	*schematic hspice symbol*
V2(analo...	hspice		*schematic hspice symbol*
V4(analo...	hspice		*schematic hspice symbol*
V5(analo...	hspice		*schematic hspice symbol*

Figure 19. Detail in config

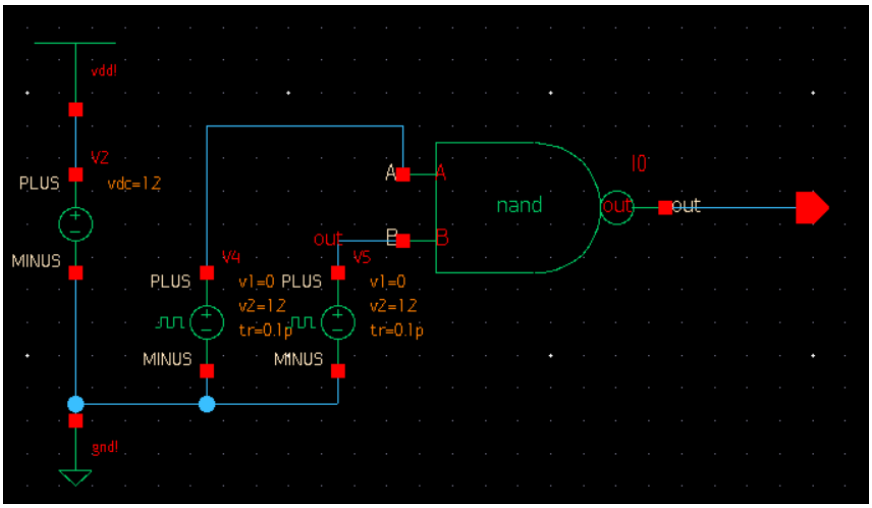

Figure 20. Schematic of config

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*|DSPF 1.3
*|DESIGN nand
*|DATE "Sat May 21 15:24:23 2017"
*|VENDOR "Synopsys"
*|PROGRAM "StarRC"
*|VERSION "D-2010.06"
*|DIVIDER |
*|DELIMITER :
*|OPERATING_TEMPERATURE 25
*|GLOBAL_TEMPERATURE 25
**FORMAT SPF
*

** COMMENTS

** TCAD_GRD_FILE /home/eda/pdk/synopsys/PDK/starrc/reference_90nm_9lm_typ.nxtgrd
**   TCAD_TIME_STAMP Mon Apr 6 20:59:52 2009
**   TCADGRD_VERSION 64


.SUBCKT nand out B A

*|GROUND_NET 0
```

Figure 21. Content in output.sp

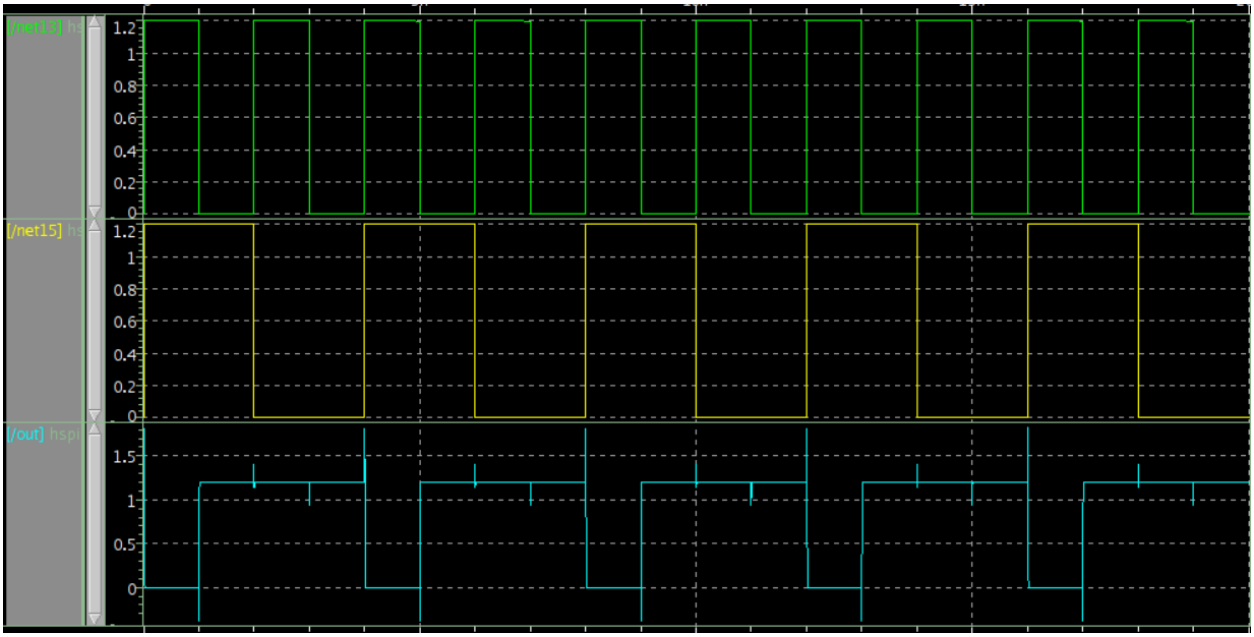

Figure 22. Waveform of post layout

Rise time	Fall time
8.04p	8.5p

Table 6. Rise time and Fall time of out signal

CHAPTER 2. DESIGN FULL ADDER-1 BIT

1. Theory of the Full Adder

1.1.Introduction

A Full Adder (FA) is a digital circuit that computes the sum of three binary bits: two significant bits and a carry-in bit. It produces a sum bit and a carry-out bit. Full Adders are fundamental components in binary addition, commonly used in arithmetic logic units (ALUs) and various digital computing systems to perform multi-bit binary addition.

1.2. Truth table

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 7. True table of FA

In this table:

- A and B are the input bits.
- Cin is the carry-in bit.
- Sum is the sum output bit.
- Cout is the carry-out bit.

2. Design schematic,symbol

Since the Full Adder (FA) will use the MOSFETs described in Chapter 1 (specifically NAND gates), we won't need to look up the W/L ratios for PMOS and NMOS transistors again.

2.1. Schematic

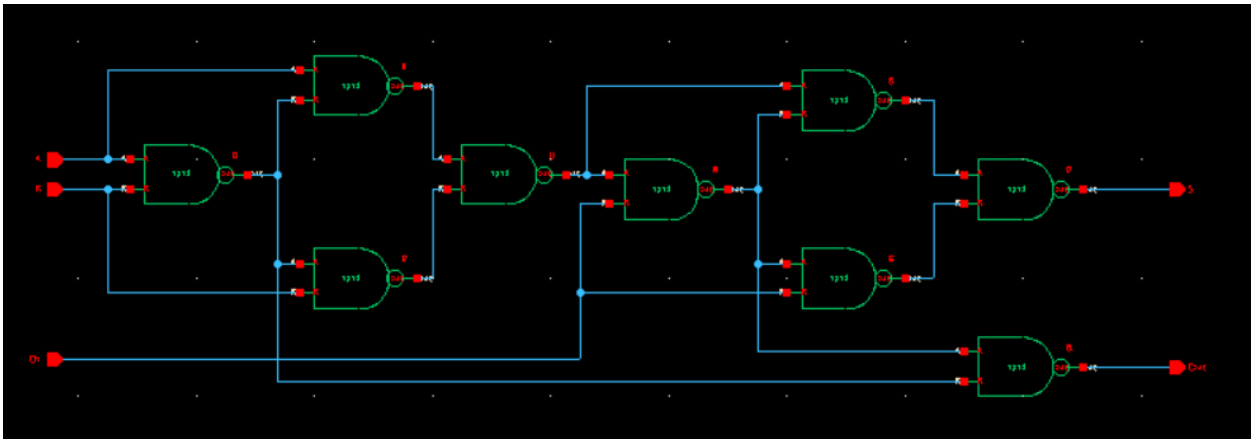

Figure 23. Schematic of FA 1 bit

2.2.Symbol

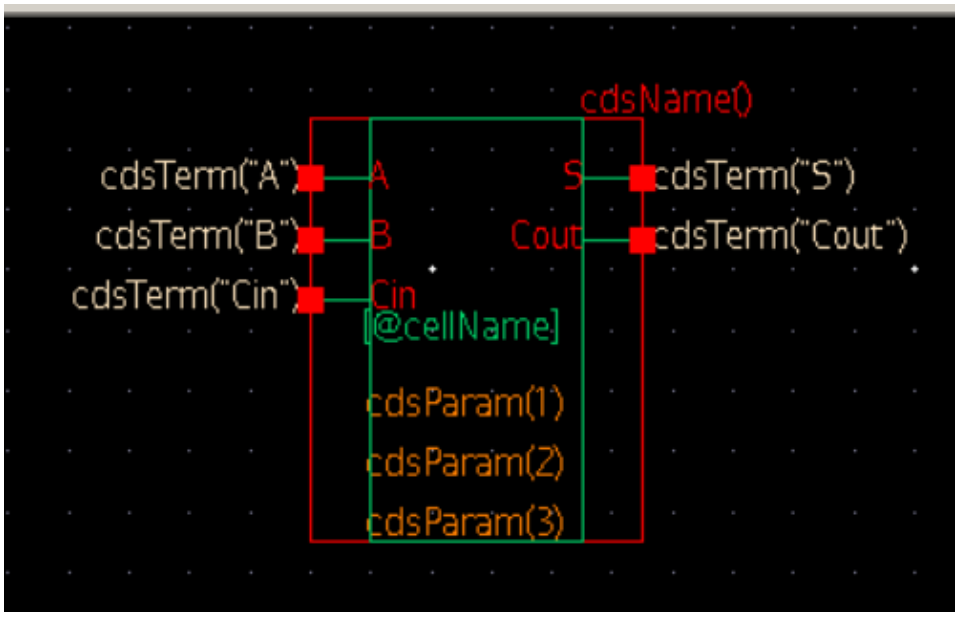

Figure 24. Symbol of FA 1 bit

2.3.Testbench

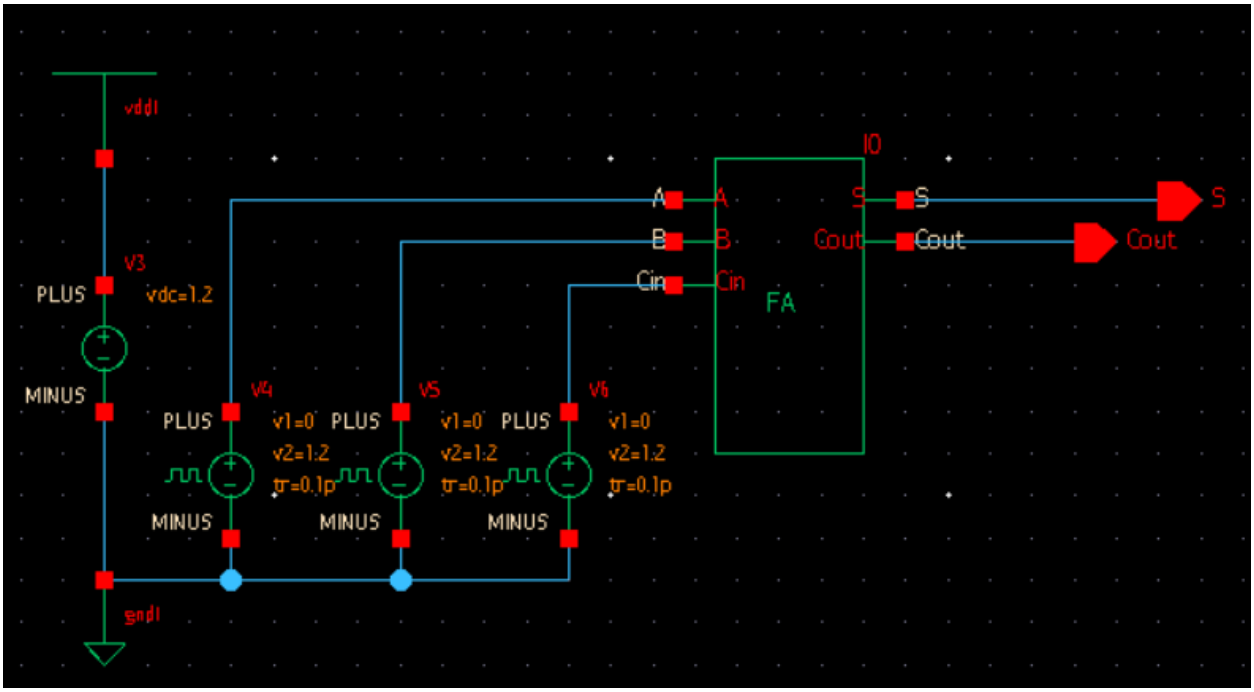

Figure 25. Testbench of FA 1 bit

2.4.Waveform

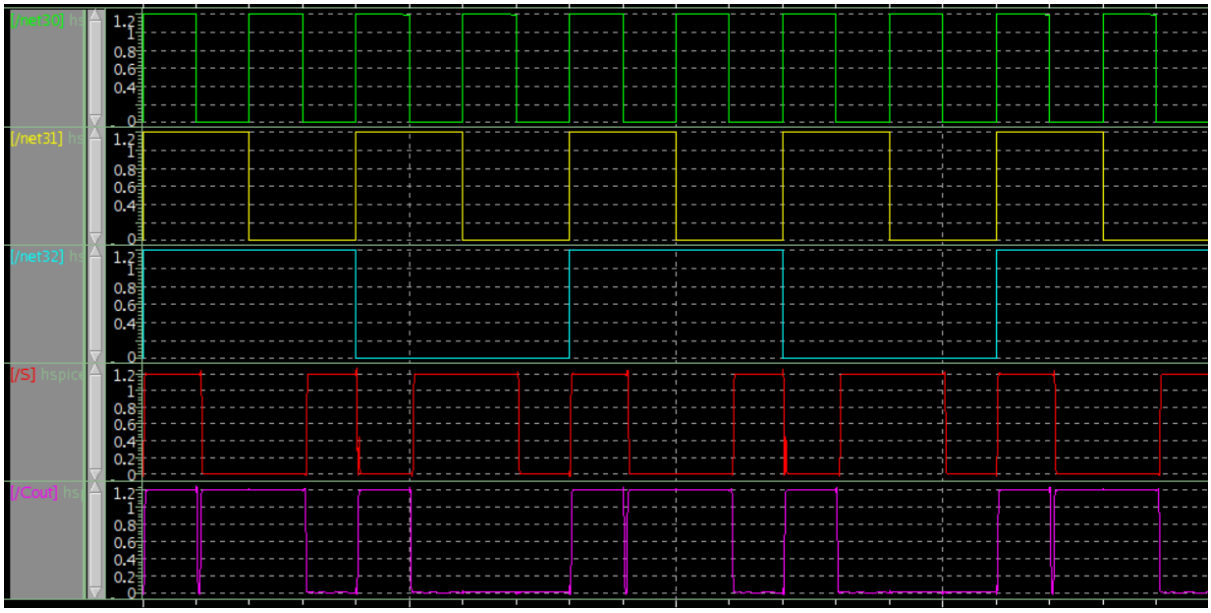

Figure 26. Waveform of FA 1 bit

3. Layout FA 1 BIT

3.1. Layout

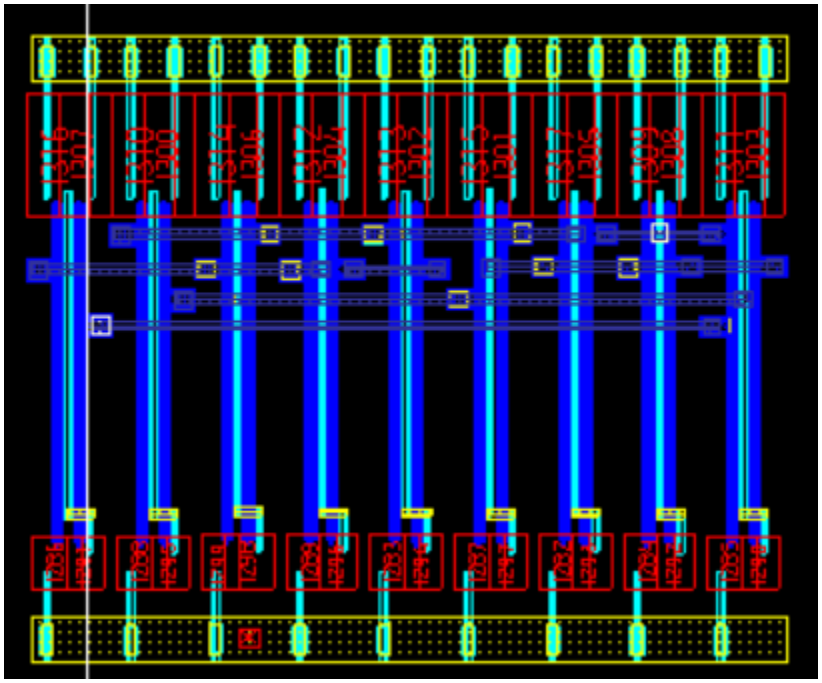

Figure 27. Layout of FA 1 bit

3.2. DRC

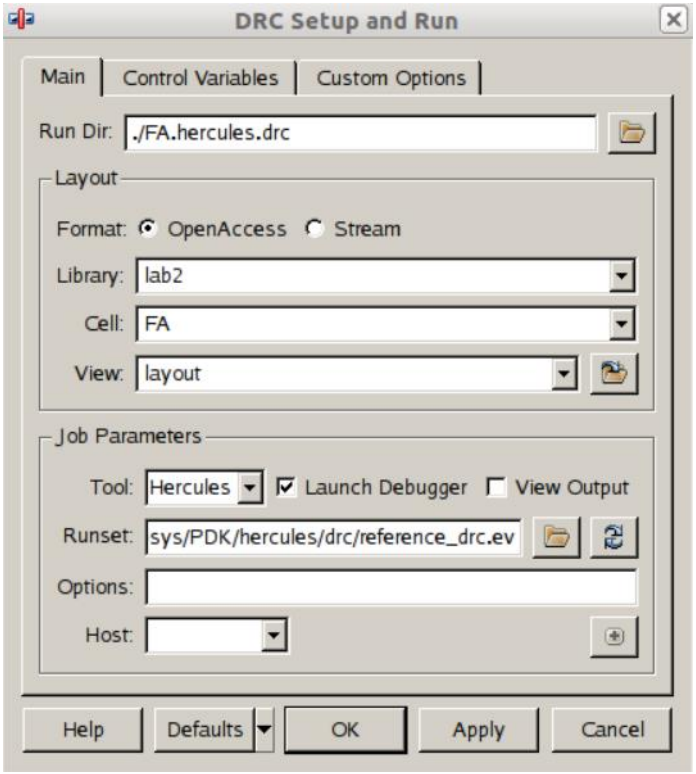

Figure 28. DRC main of FA 1 bit

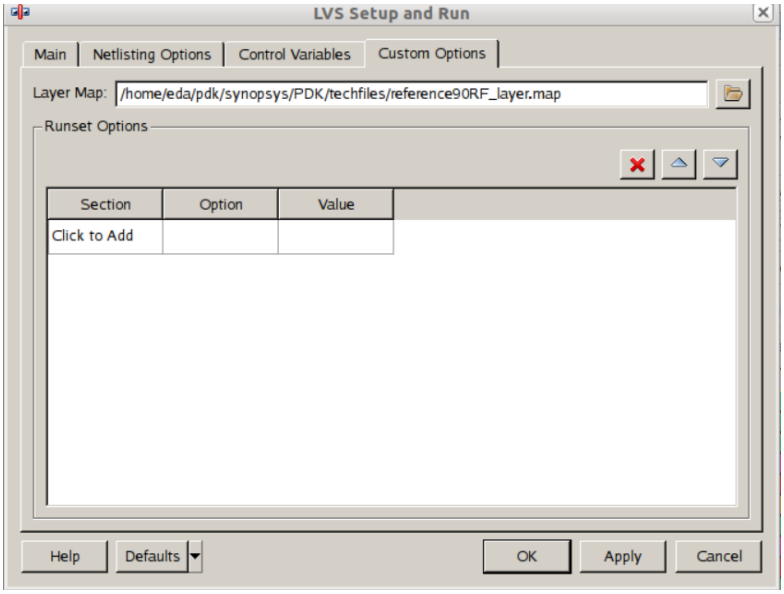

Figure 29. DRC Custom option of FA 1 bit

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JobID: hercules_drc_9
Completed with no errors.
==============================
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Figure 30. DRC result of FA 1 bit

LAYOUT ERRORS RESULTS

CLEAN

Hercules (R) Hierarchical Design Verification, IA.32 Release B-2008.09.SP3.24010 2010/08/27
Hercules Run: Time= 0:00:02 User=0.11 System=0.54

DRC Error Statistics

Library name: lab2
Structure name: FA

DRC Errors:

Figure 31. DRC debug of FA 1 bit

3.3. LVS

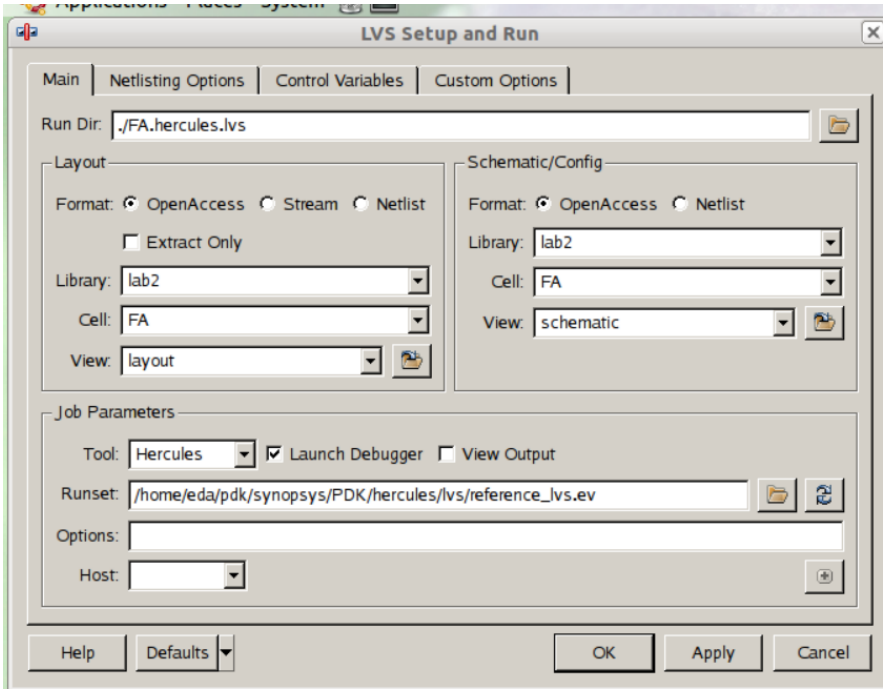

Figure 32. LVS main of FA 1 bit

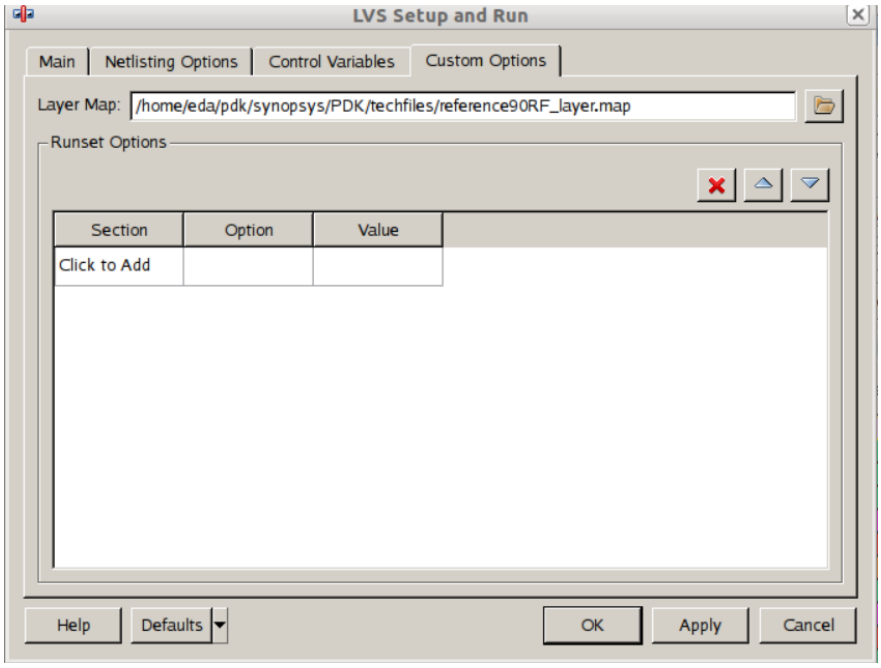

Figure 33. LVS Custom option of FA 1 bit

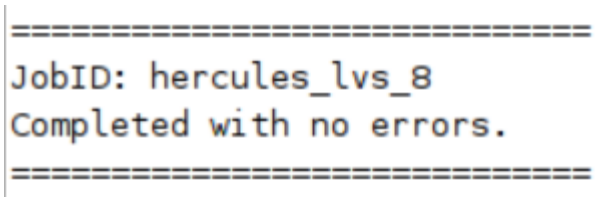

Figure 34. LVS result of FA 1 bit

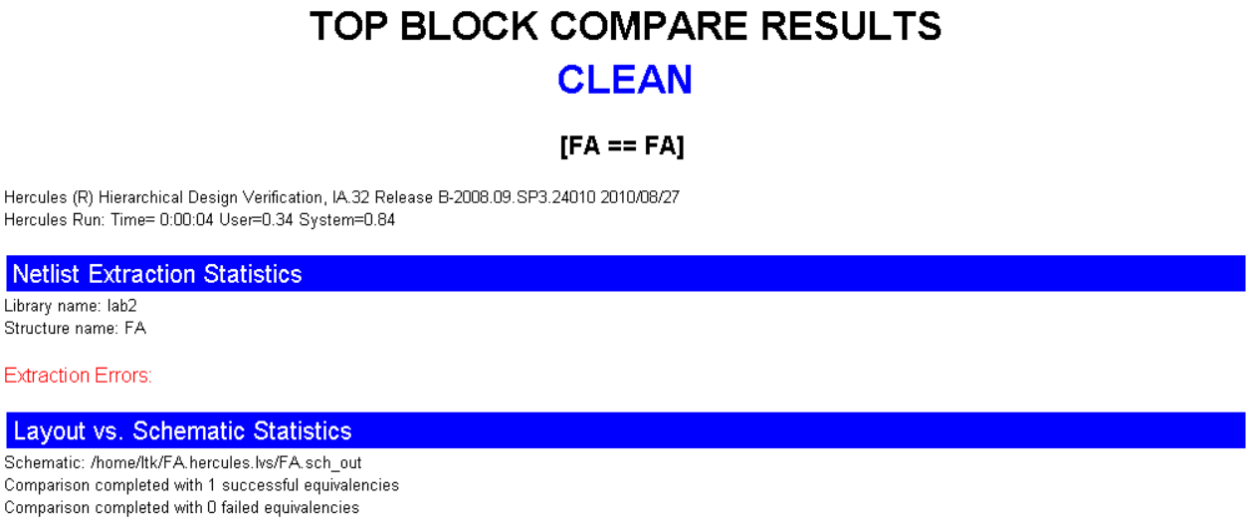

Figure 35. LVS debug of FA 1 bit

3.4. LPE

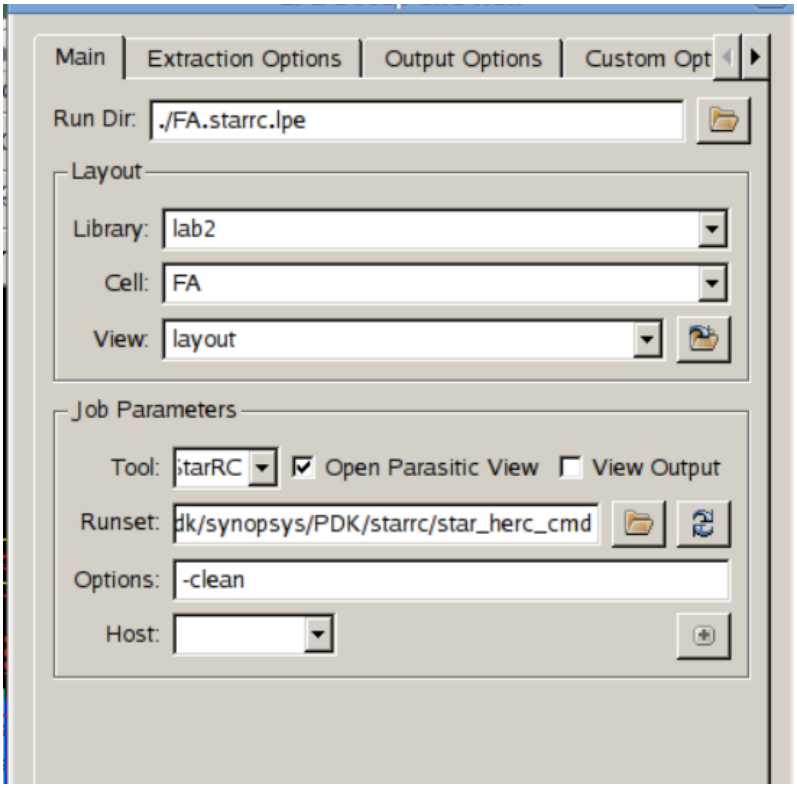

Figure 36. LPE main of FA 1 bit

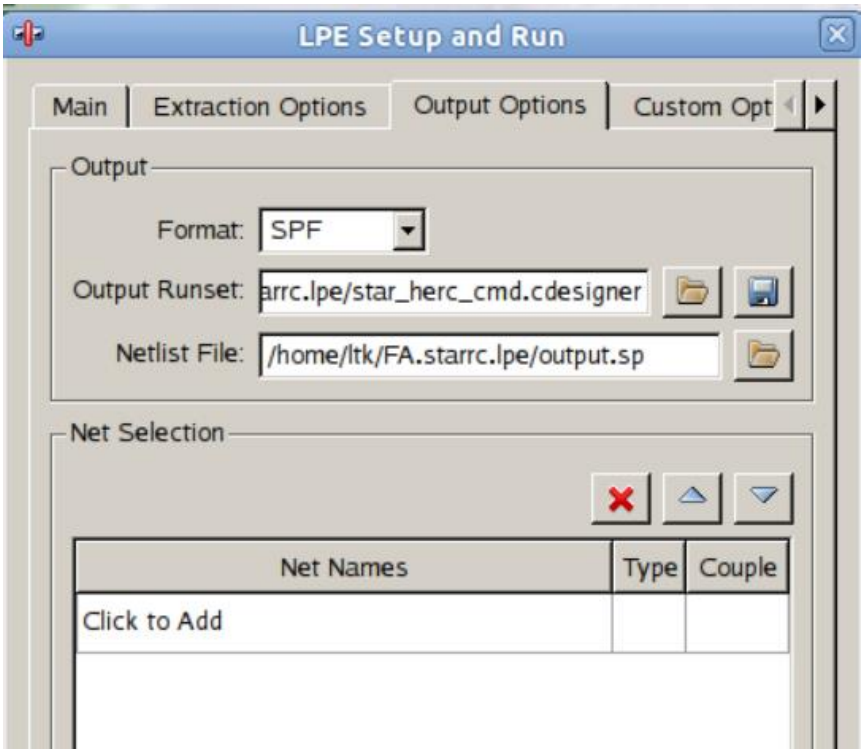

Figure 37. LPE Ouput custom of FA 1 bit

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JobID: starrc_lpe_4
Completed with no errors.
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Figure 38. LPE result of FA 1 bit

3.5. Post layout

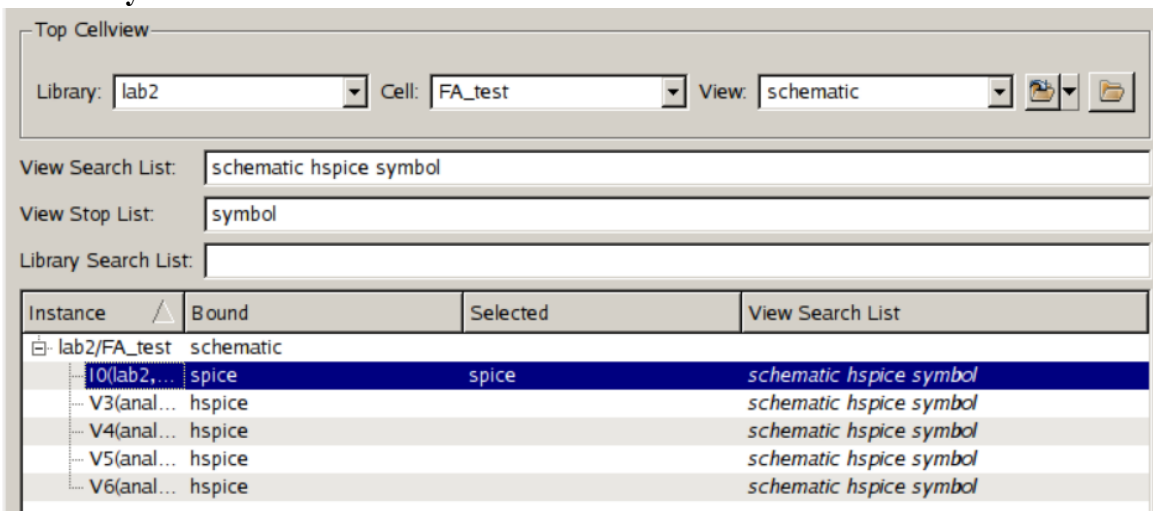

Figure 39. Detail in config

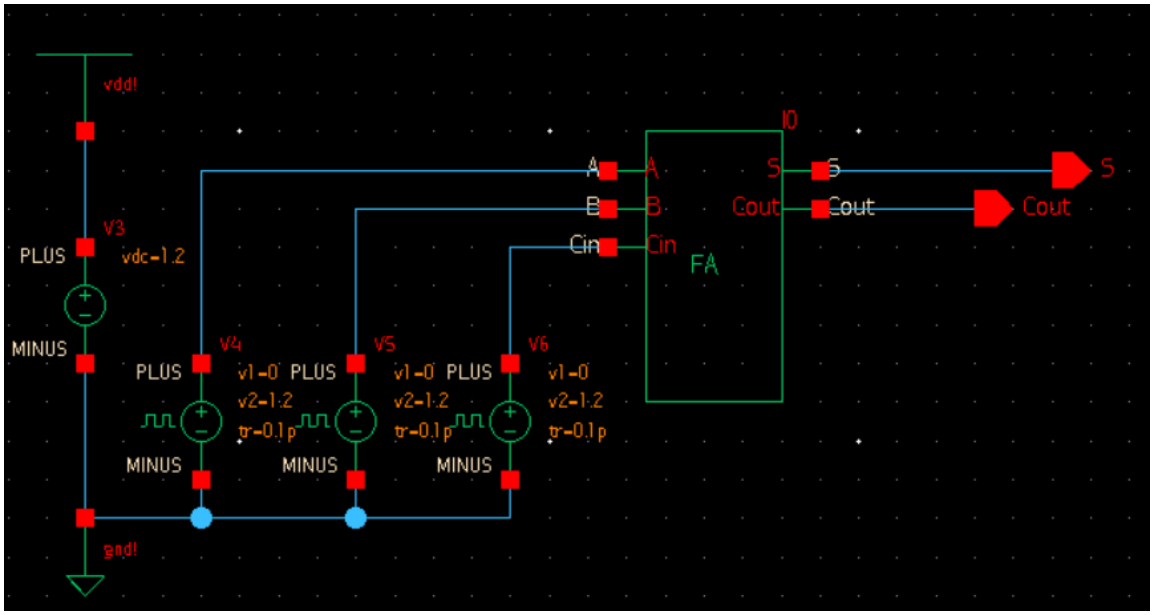

Figure 40. Schematic of config

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*|PROGRAM "StarRC"
*|VERSION "D-2010.06"
*|DIVIDER |
*|DELIMITER :
*|OPERATING_TEMPERATURE 25
*|GLOBAL_TEMPERATURE 25
**FORMAT SPF
*

** COMMENTS

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**   TCAD_TIME_STAMP Mon Apr 6 20:59:52 2009
**   TCADGRD_VERSION 64


.SUBCKT FA Cout S B A Cin

*|GROUND_NET 0
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Figure 41. content in output.sp

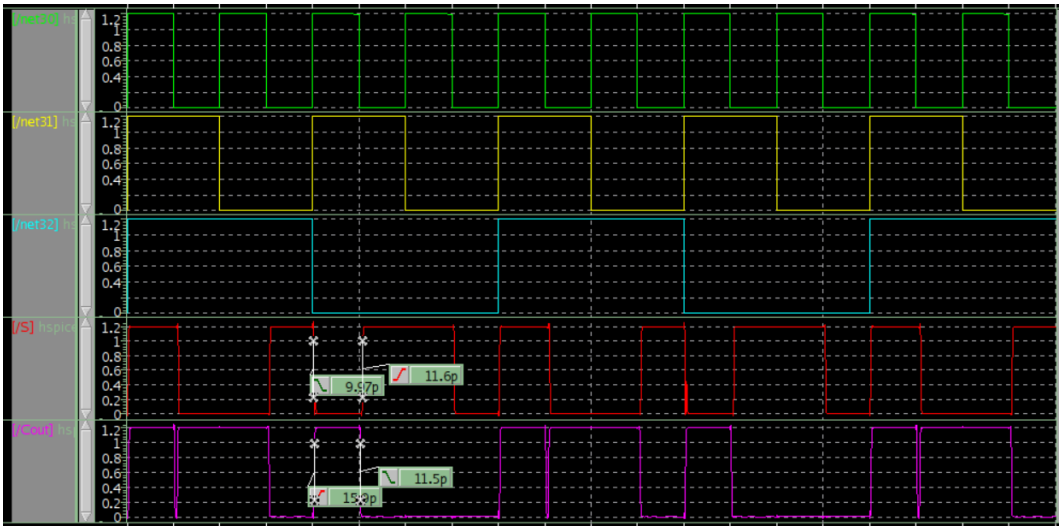

Figure 42. Final waveform

OUTPUT	Fall time	Rise time
S	9.5ps	11.6ps
Cout	11.5ps	15ps

Table 8. Fall time and Rise time of FA

Note: The method for balancing fall time and rise time has been discussed in section 2.4 of chapter 1.

CHAPTER 3. DESIGN FULL ADDER-2 BIT

1. Theory of the Full Adder

To create a 2-bit Full Adder (FA) from two 1-bit Full Adders, you need to connect them in series, where the carry-out of the first 1-bit FA is used as the carry-in for the second 1-bit FA. Here's a step-by-step explanation:

1.First 1-bit Full Adder (FA1):

- Inputs: A0, B0 (least significant bits of the two numbers to be added) and Cin (initial carry-in, usually 0 for the least significant bit).
- Outputs: Sum0 and Cout1.

2.Second 1-bit Full Adder (FA2):

- inputs: A1, B1 (next significant bits of the two numbers to be added) and Cout1 (carry-out from FA1).
- Outputs: Sum1 and Cout2 (final carry-out).

2. Design schematic,symbol

2.1.Schematic

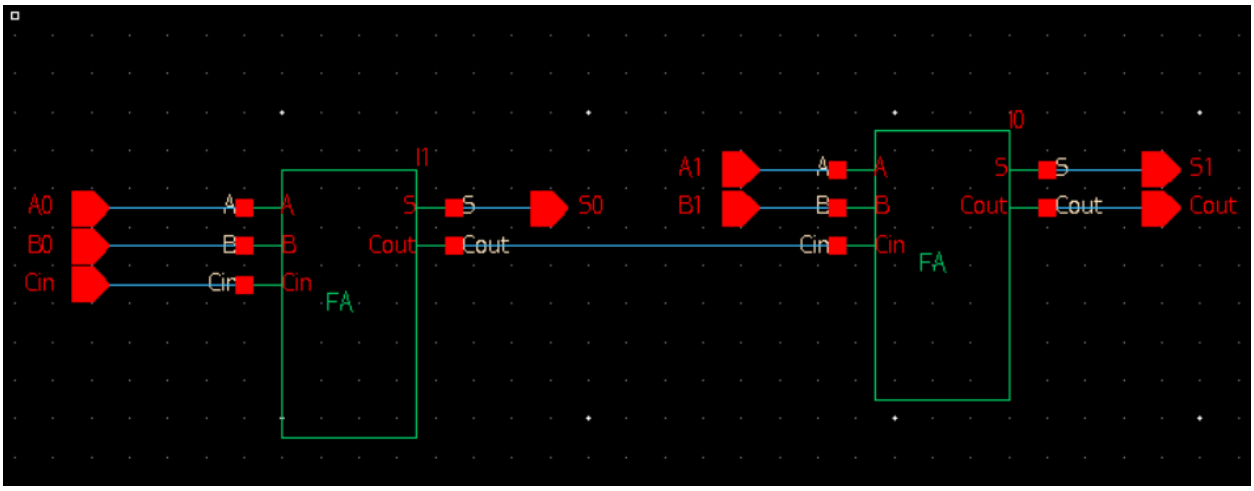

Figure 43. Schematic of FA 2 BIT

2.2. Symbol

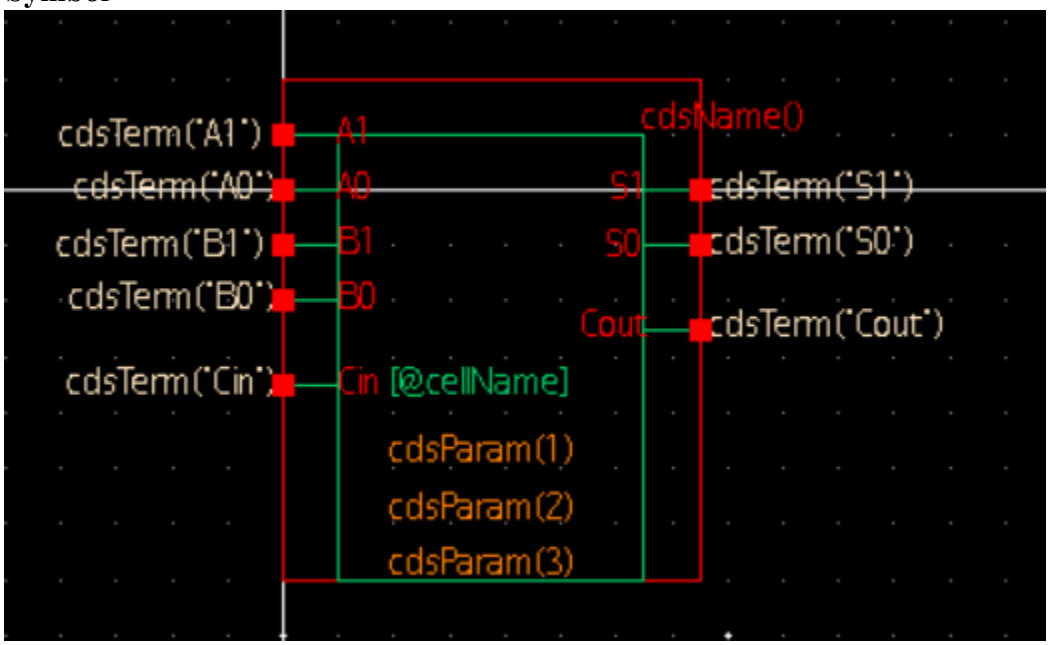

Figure 44. Symbol of FA 2 BIT

2.3. Testbench

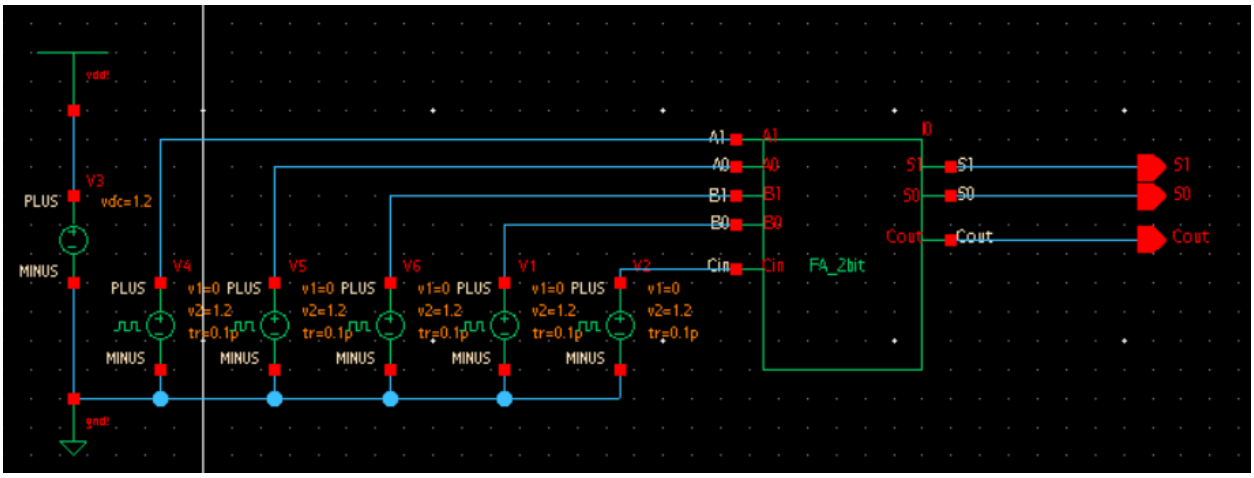

Figure 45. Testbench of FA 2 BIT

3. Layout FA 2 BIT

3.1. Layout

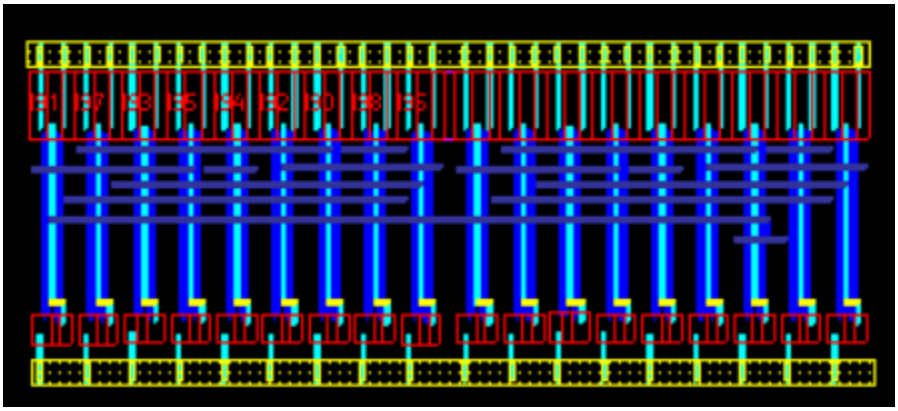

Figure 46. Layout of FA 2 BIT

3.2. DRC

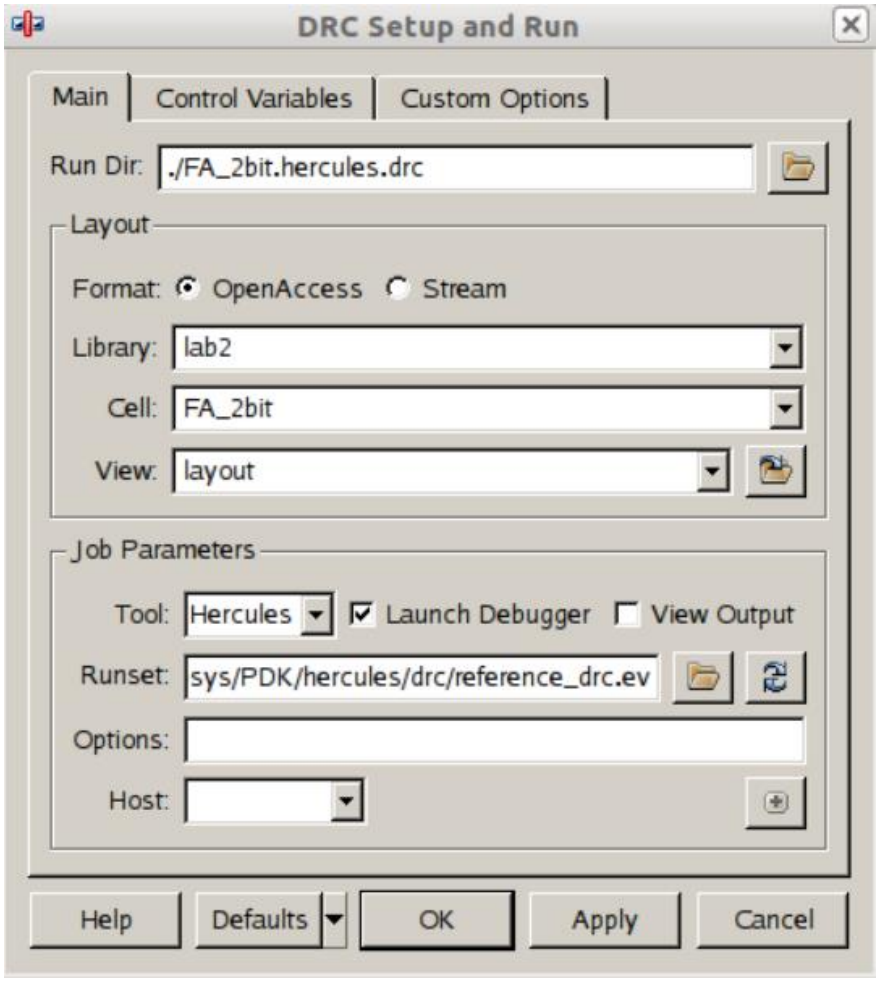

Figure 47. DRC main of FA 2 bit

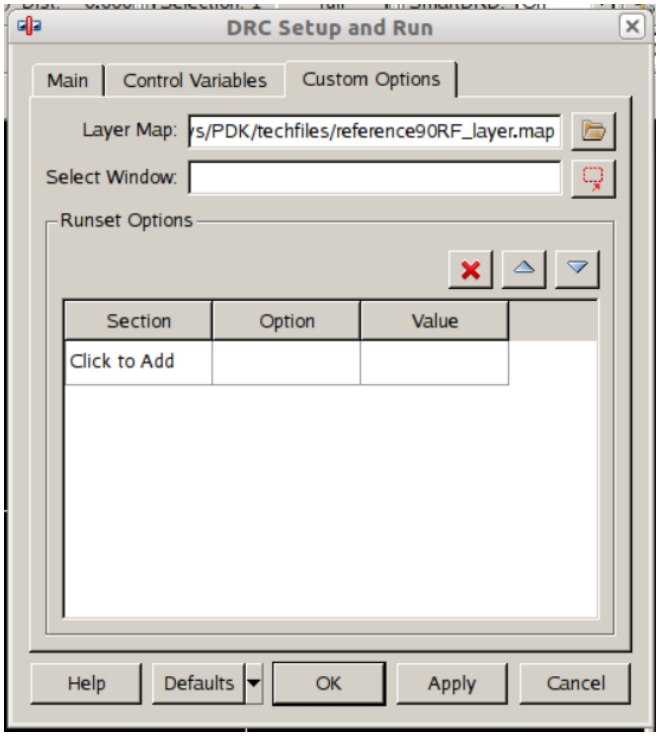

Figure 48. DRC custom option of FA 2 bit

```
==============================
JobID: hercules_drc_17
Completed with no errors.
==============================
```

Figure 49. DRC result of FA 2 bit

LAYOUT ERRORS RESULTS

CLEAN

Hercules (R) Hierarchical Design Verification, IA.32 Release B-2008.09.SP3.24010 2010/08/27
Hercules Run: Time= 0:00:01 User=0.13 System=0.12

DRC Error Statistics

Library name: lab2
Structure name: FA_2bit

DRC Errors:

Figure 50. DRC debug of FA 2 BIT

3.3. LVS

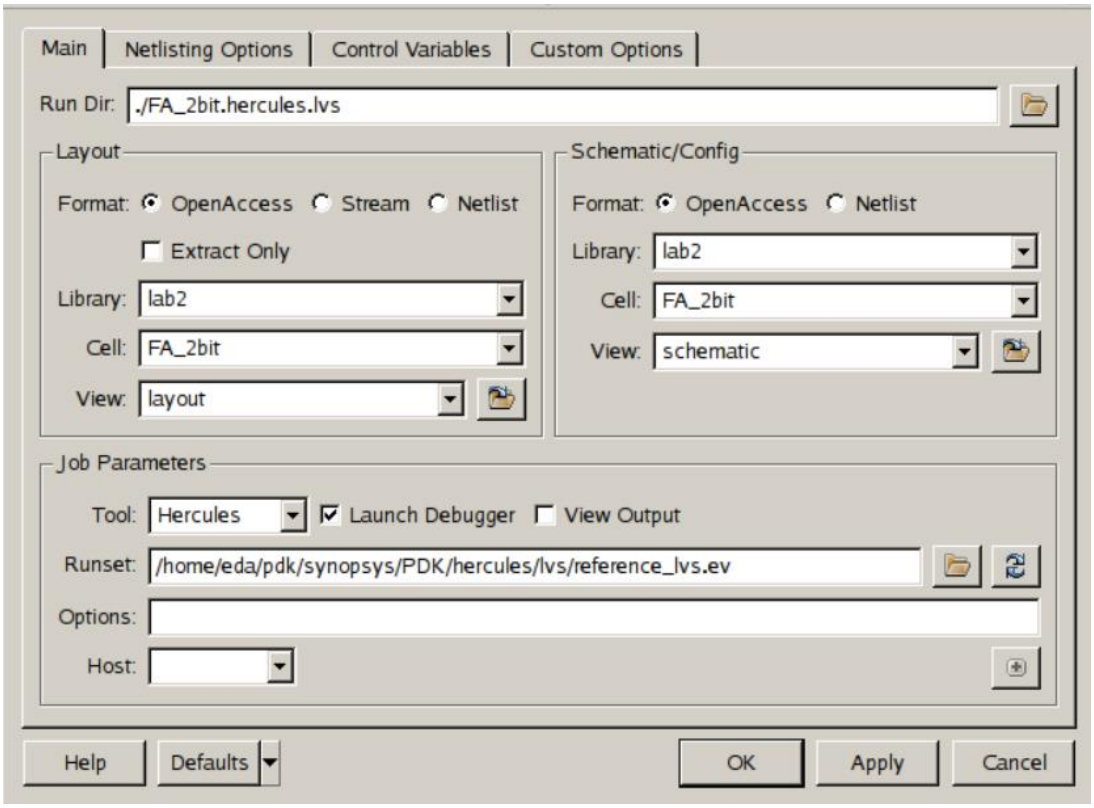

Figure 51. LVS main of FA 2 bit

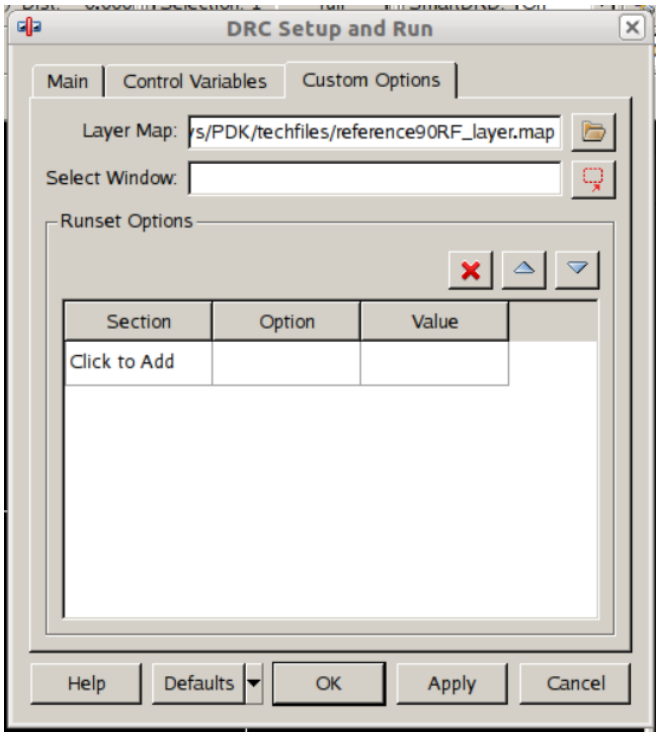

Figure 52. LVS custom option of FA 2 bit

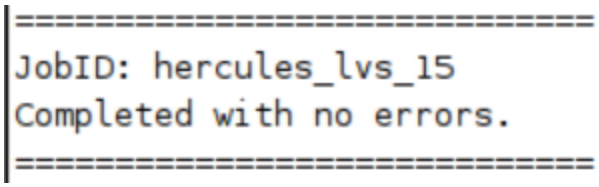

Figure 53. LVS result of FA 2 bit

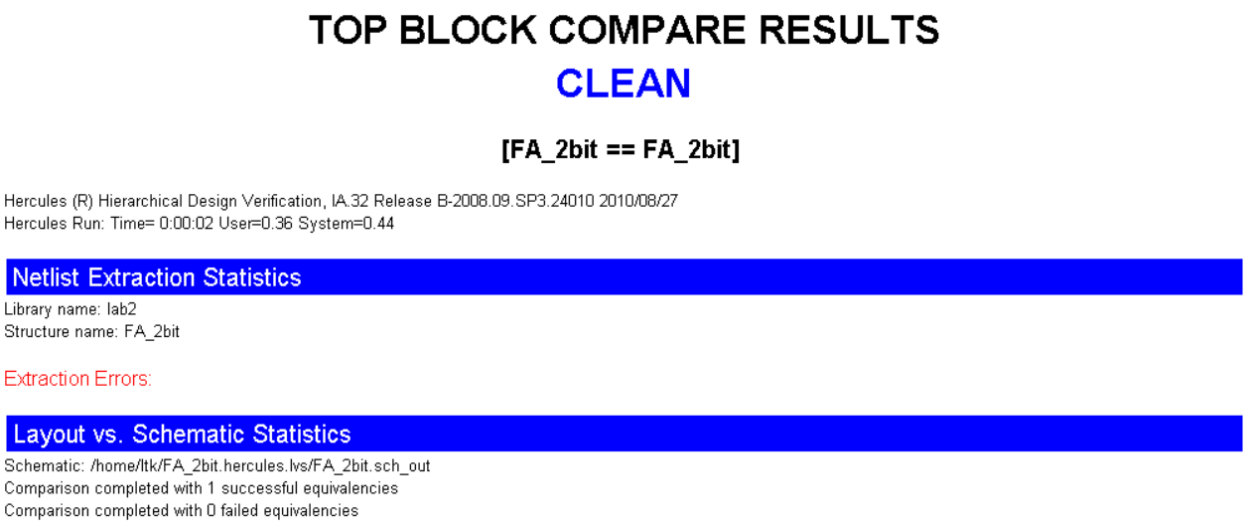

Figure 54. LVS debug of FA 2 BIT

3.4. LPE

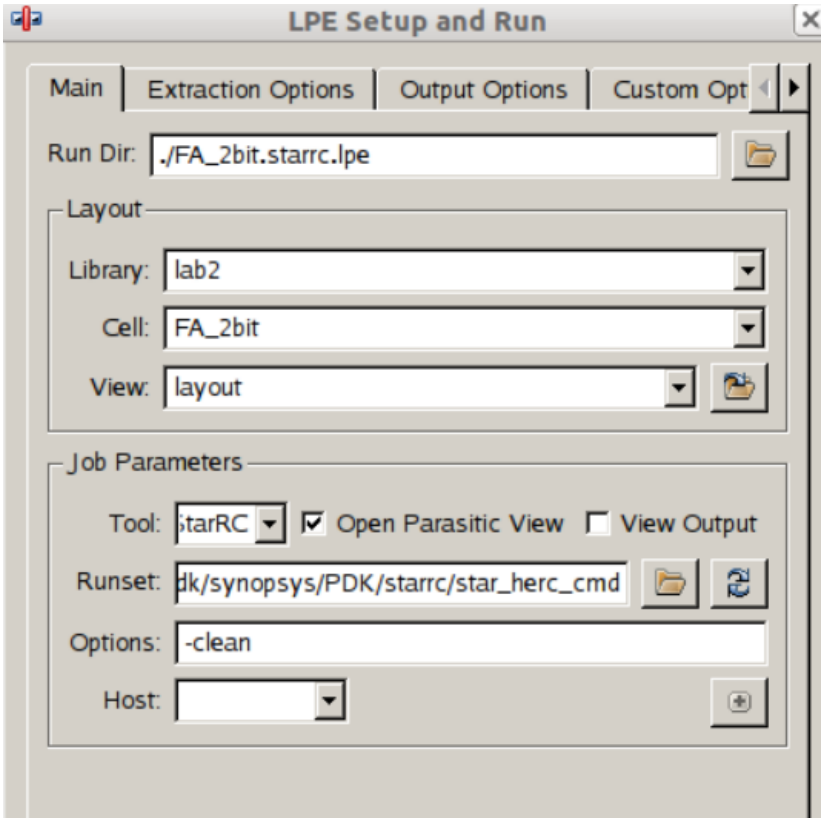

Figure 55. LPE main of FA 2 bit

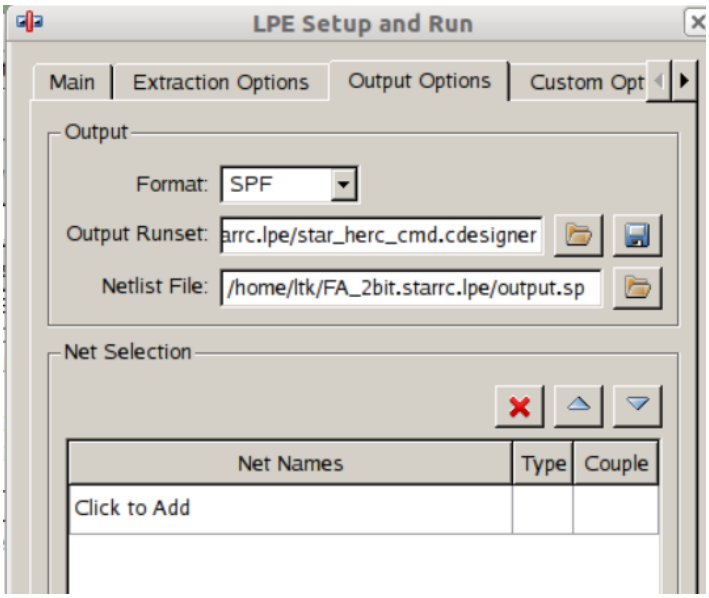

Figure 56. LPE output option of FA 2 bit

```
==============================
JobID: starrc_lpe_4
Completed with no errors.
==============================
```

Figure 57. LPE result of FA 2 BIT

4. Post Layout

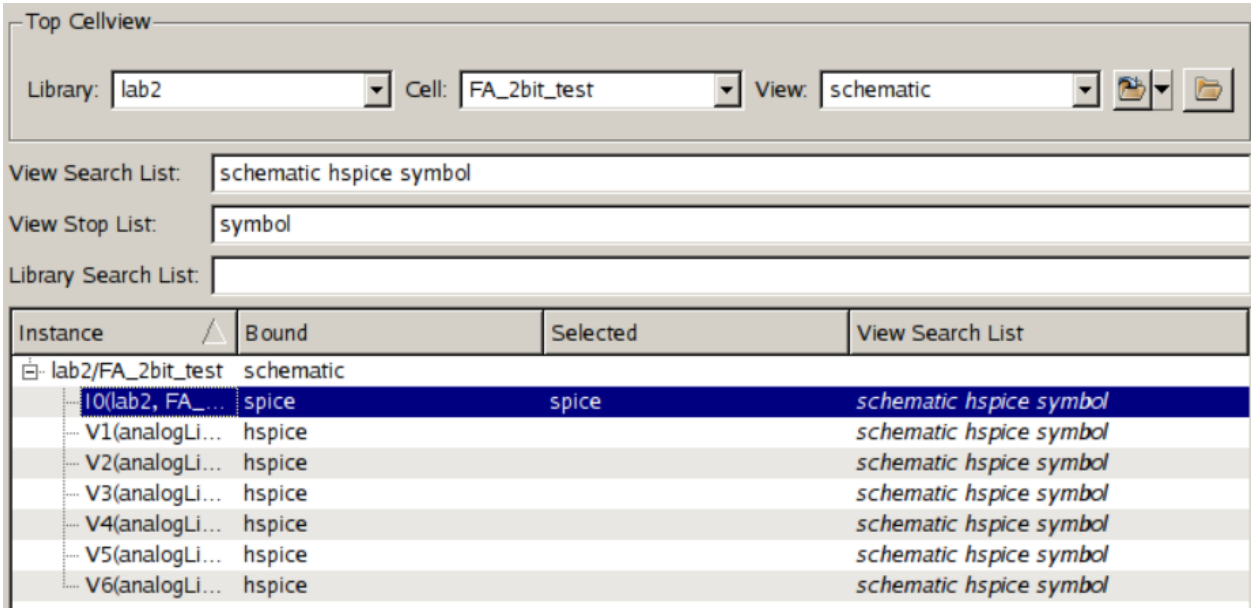

Figure 58. Config detail

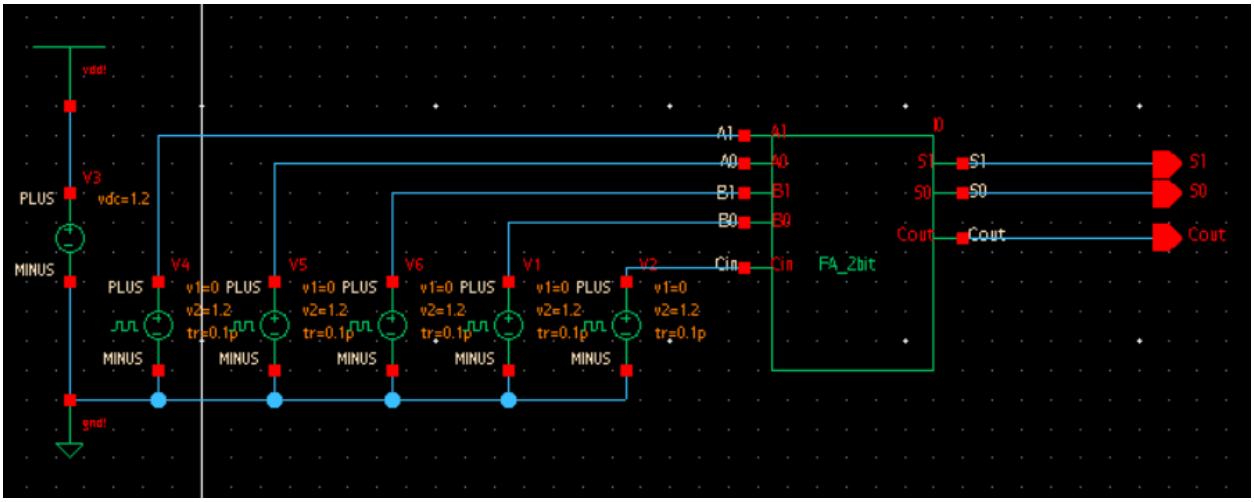

Figure 59. Schematic of FA 2 BIT after config

```
*
*|DSPF 1.3
*|DESIGN FA_2bit
*|DATE "Tue May 23 23:24:00 2017"
*|VENDOR "Synopsys"
*|PROGRAM "StarRC"
*|VERSION "D-2010.06"
*|DIVIDER |
*|DELIMITER :
*|OPERATING_TEMPERATURE 25
*|GLOBAL_TEMPERATURE 25
**FORMAT SPF
*

** COMMENTS

** TCAD_GRD_FILE /home/eda/pdk/synopsys/PDK/starrc/reference_90nm_9lm_typ.nxtgrd
**   TCAD_TIME_STAMP Mon Apr 6 20:59:52 2009
**   TCADGRD_VERSION 64


.SUBCKT FA_2bit S0 B0 A0 Cin Cout S1 B1 A1

*|GROUND_NET 0
```

Figure 60. content of output.sp

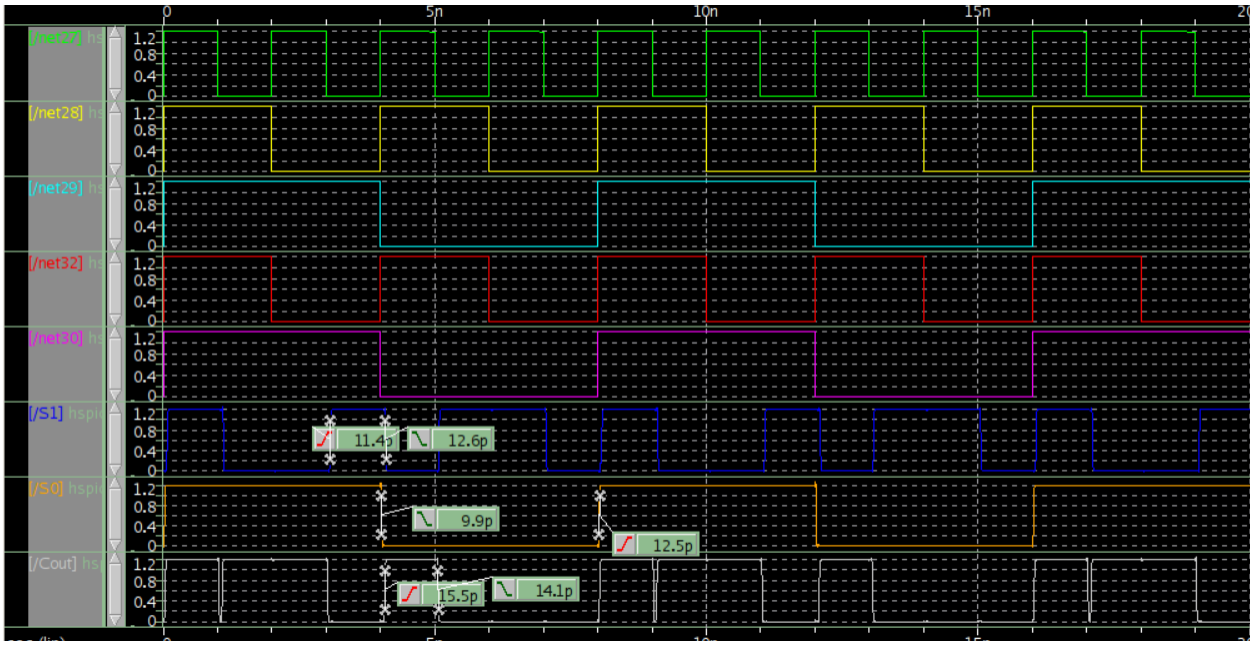

Figure 61. Waveform

Output	Rise time	Fall time
S1	11.4ps	12.6ps
S0	12.5ps	9.9ps
Cout	15.5ps	14.1ps

Table 9. Fall time and Rise time of FA 2 BIT

Output.sp FILE : Here

Note: The method for balancing fall time and rise time has been discussed in section 2.4 of chapter 1.

END