VIETNAM NATIONLA UNIVERSITY, HO CHI MINH CITY
UNIVERSITY OF INFORMATION TECHNOLOGY
FACULTY OF COMPUTER ENGINEERING
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DIGITAL CIRCUIT DESIGN- CE222.O23.MTCL

REPORT LAB 01

GETTING ACQUAINTED WITH CUSTOM DESIGNER AND INVERTER GATE DESIGN

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Lecturer: Tạ Trí Đức

Pictures

CHAPTER 1. DESIGN SCHEMATIC AND SIMULATE INVERTER (FRONT-END)

1. DESIGN SCHEMATIC

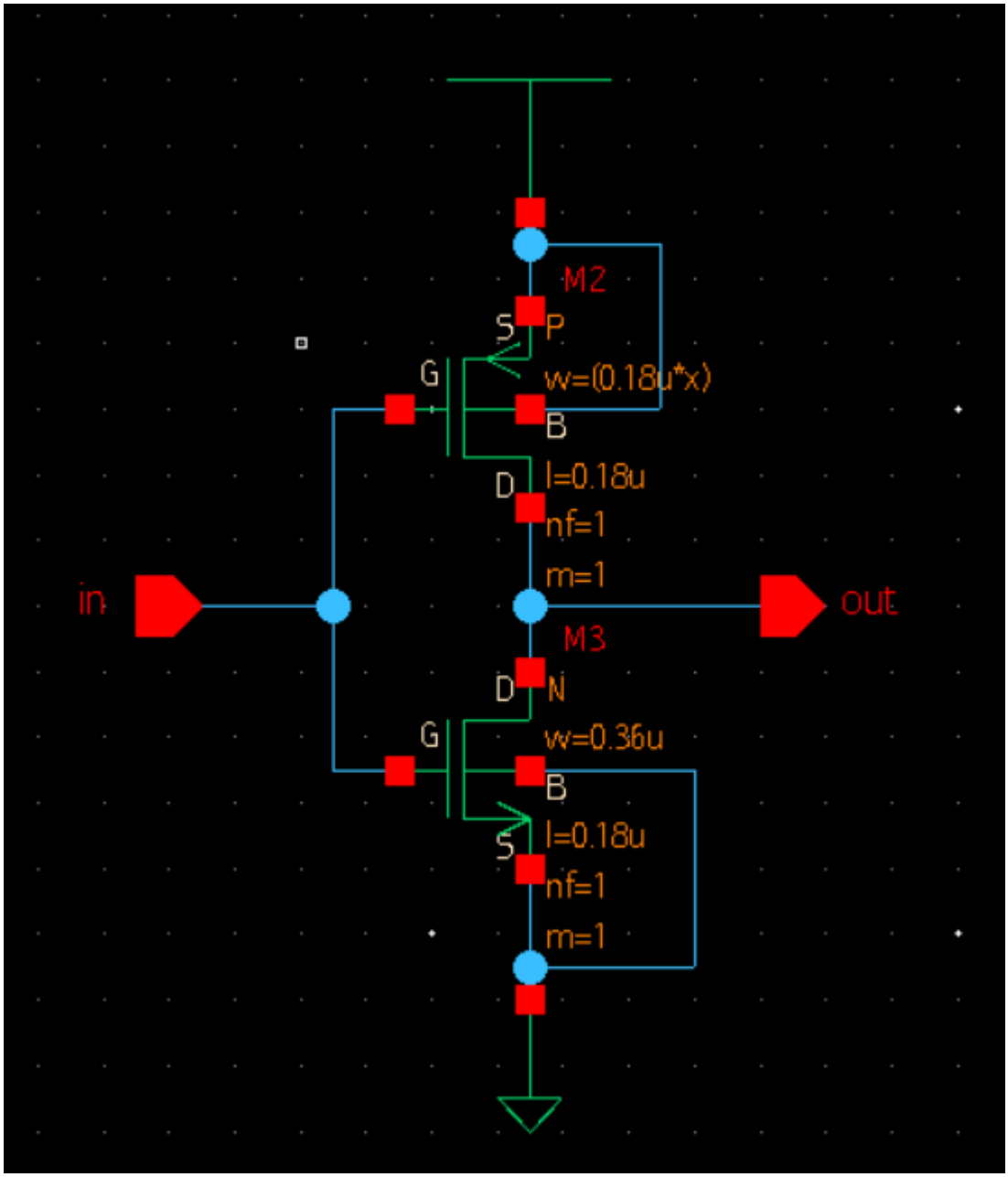

Figure 1. Inverter Schematic

1.1. Calculate the W/L ratio of PMOS and NMOS

By default, we will fix the NMOS with specific dimensions: L=0.18um and W=0.36um. We will calculate the W parameters of the PMOS (where L of PMOS and NMOS are equal) for an appropriate Switching Threshold (Trip-point). Referring to the two figures below:

$$\beta_r = \frac{\beta_n}{\beta_p} = \frac{\mu_n \frac{W_N}{L_N}}{\mu_p \frac{W_P}{L_P}}$$

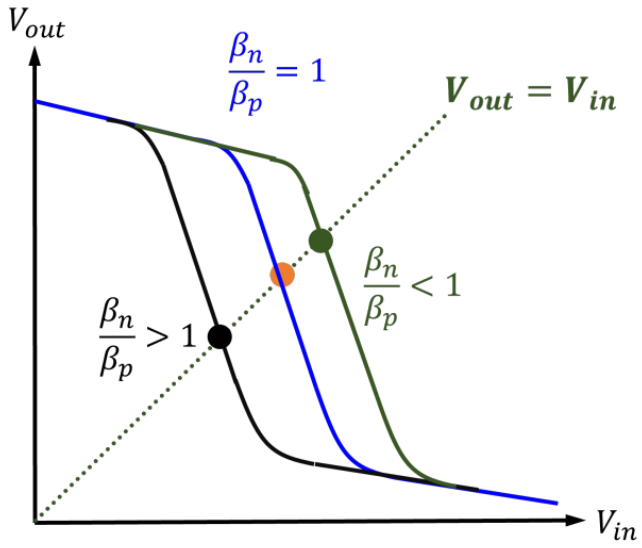

Figure 2. Switching Threshold & β Ratio

Specifically, we will calculate βr=1 based on the mobility of the holes and electrons.

Theory: Typically, μn (electron mobility) is around 2.5-3 times greater than μp (hole mobility). Therefore, the ratio of Wp to Wn (for βr=1) is usually given by $\frac{Wp}{Wn} = \frac{\mu n}{\mu p}$,meaning the width of the PMOS is typically 2.5-3 times wider than the width of the NMOS.

According to the 90nm reference library:

$\frac{Wp}{Wn} = \frac{\mu n}{\mu p} = \frac{4.031486^{-2}}{8.391744^{-3}} \approx 4.8$

⇨ Meaning the width of the PMOS is 4.8 times wider than the width of the NMOS.

1.2. Utilize a tool to assist in finding the W/L ratio

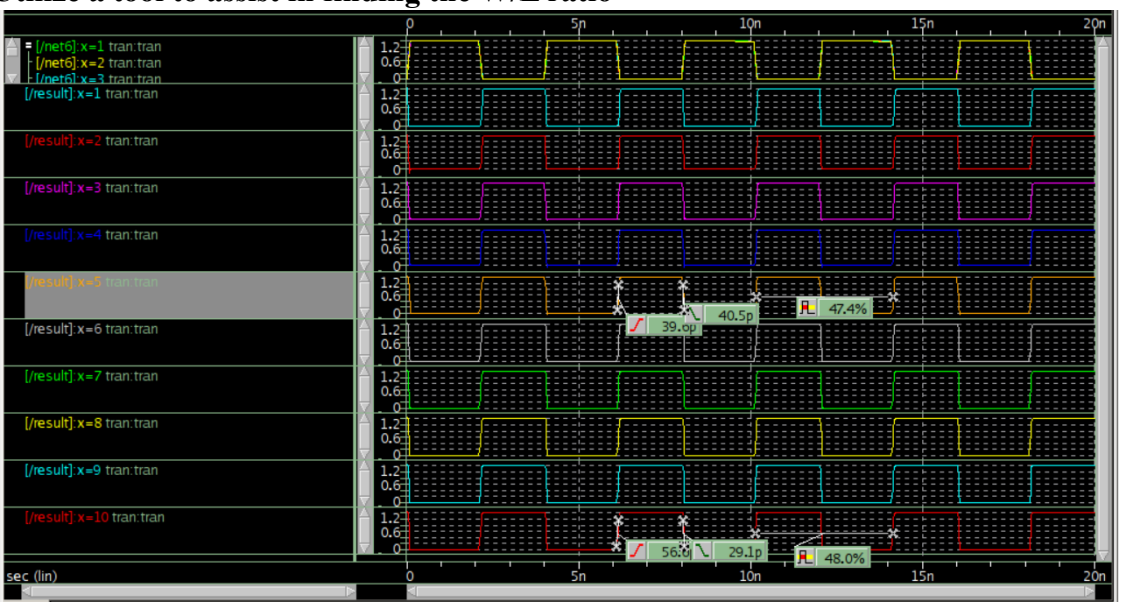

Figure 3.Result of SAE

We will focus on two parameters: False time and rise time, as well as the Duty cycle. We observe that at x=5, where Wp=0.18x5=0.9 um (Wp is 2.5 times Wn), the rise time and false time are nearly equal, making the inverter easier to control, with a duty cycle approximately 47.4%, slightly smaller than at x=10 but not significantly so.

⇨ We will choose Wp to be 2.5 times Wn.

⇨

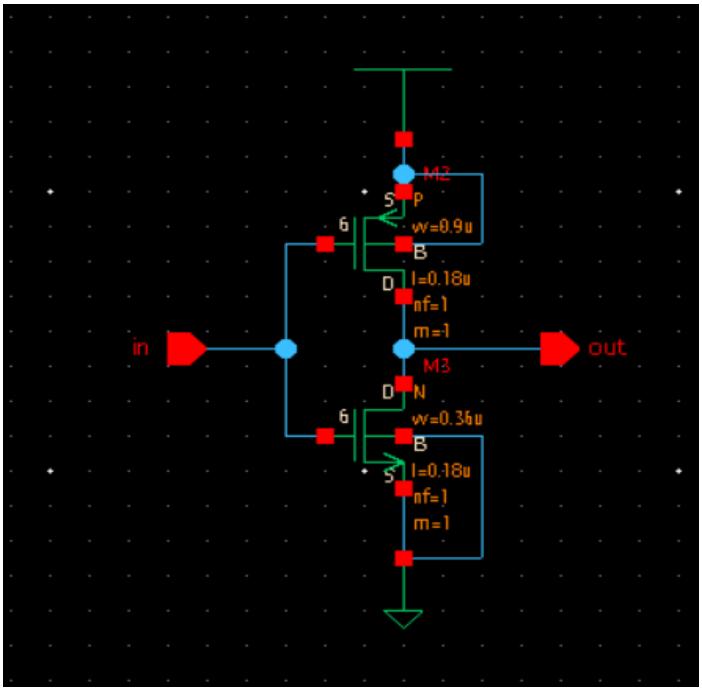

Figure 4. Final Schematic

2. SIMULATE

2.1.Testbench

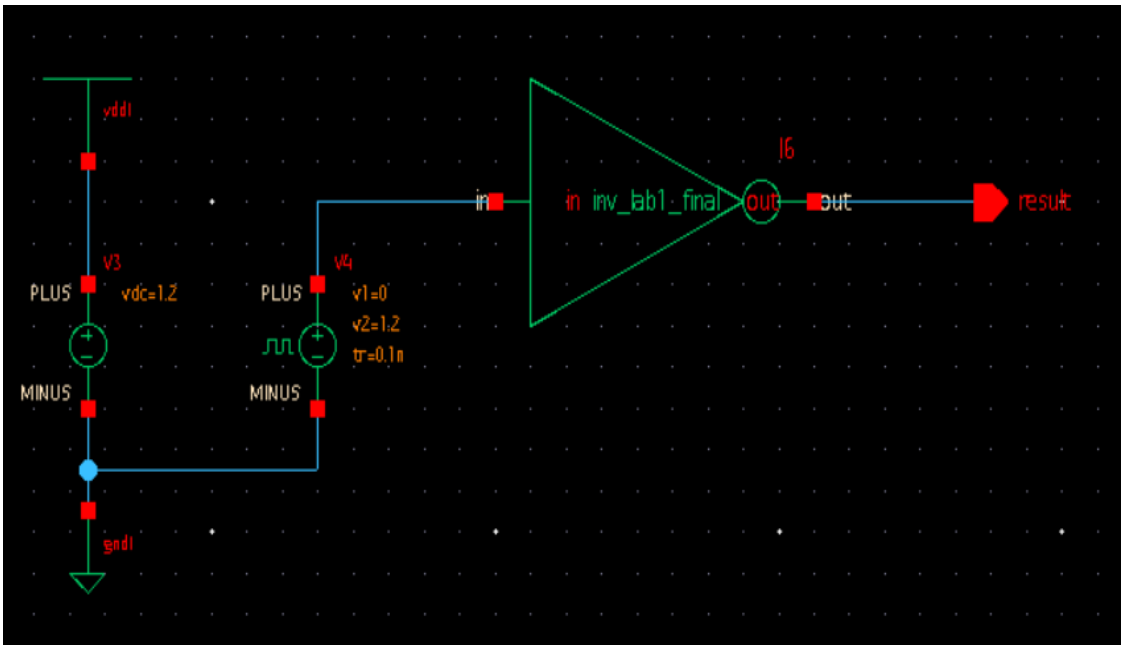

Figure 5. Test schematic

2.2. Waveform of SAE

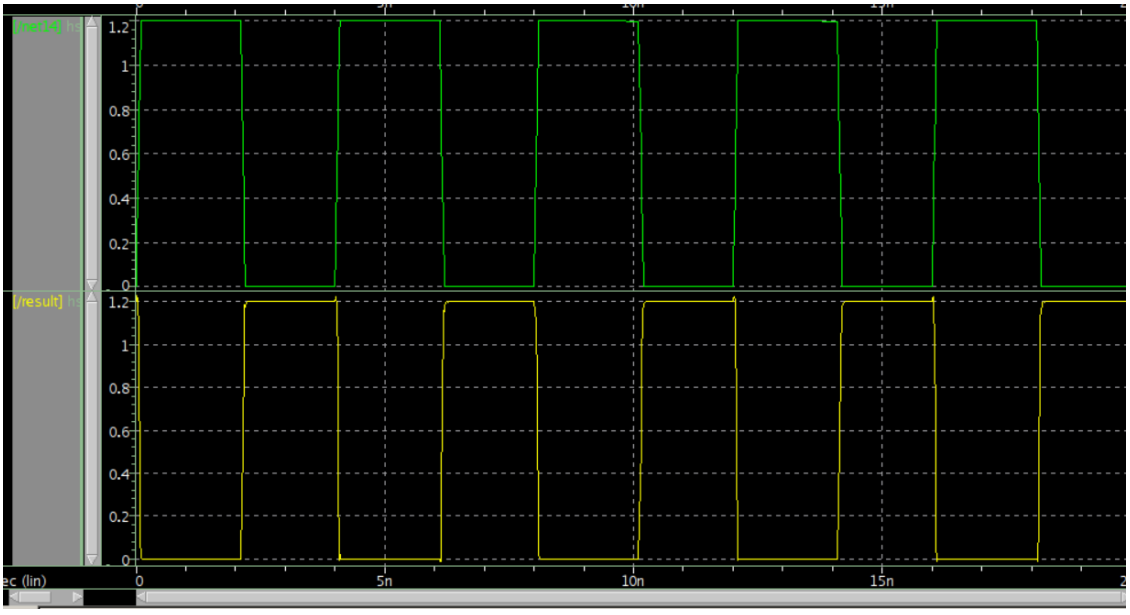

Figure 6. Result of SAE

- Green line: Vin
- Yellow line : Vout

3. SPICE

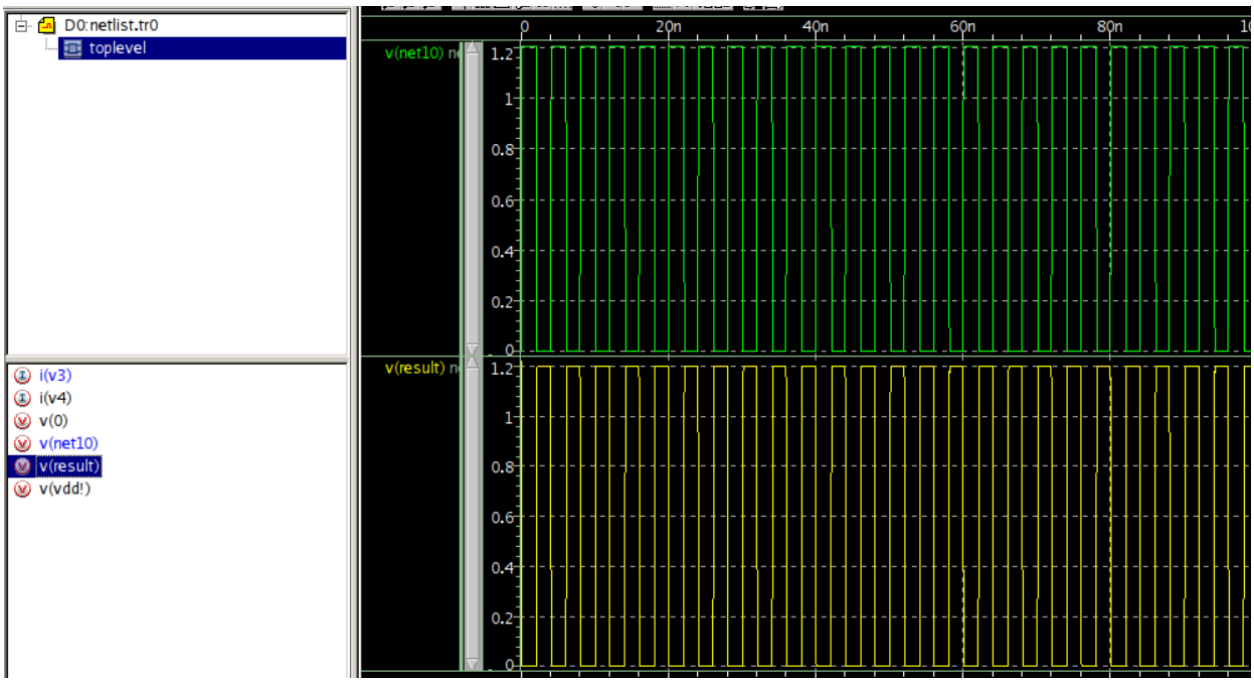

Figure 7. SPICE

- Green line: Vin
- Yellow line : Vout

CHAPTER 2. LAYOUT INVERTER (BACK-END)

1. LAYOUT

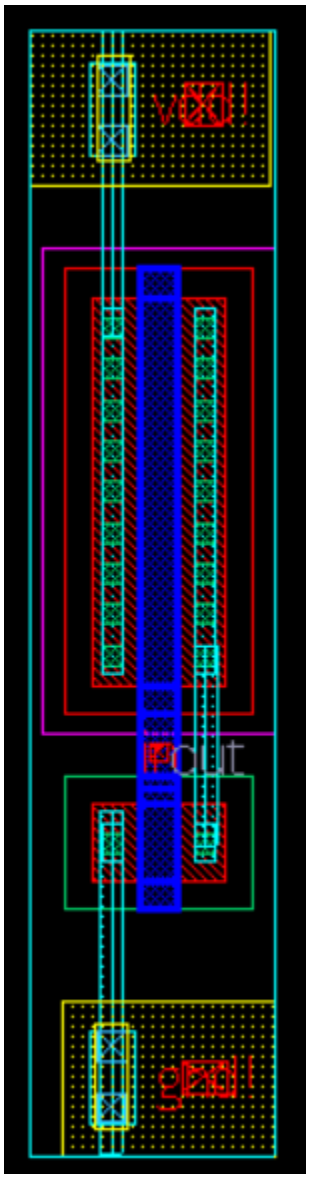

Figure 8. Layout

1.1. Design Rules Check - DRC

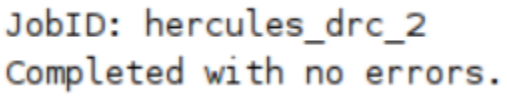

Figure 9. DRC result

1.2. Layout Versus Schematic - LVS

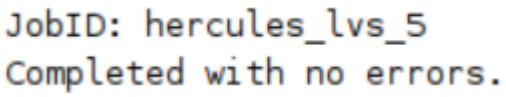

Figure 10. LVS result

1.3. Layout Parasitic Extraction – LPE

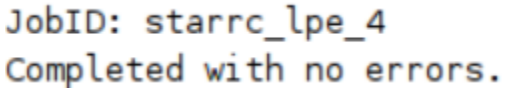

Figure 11. LPE result

2. POST LAYOUT

2.1. SPICE

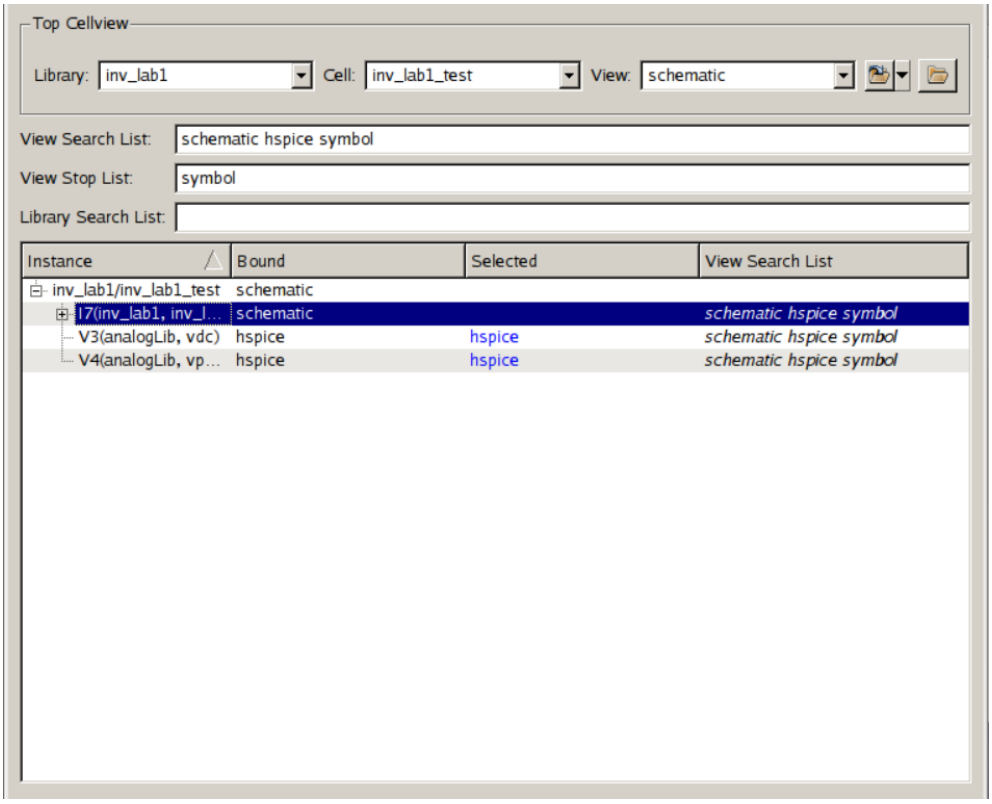

Figure 12. Config of SPICE

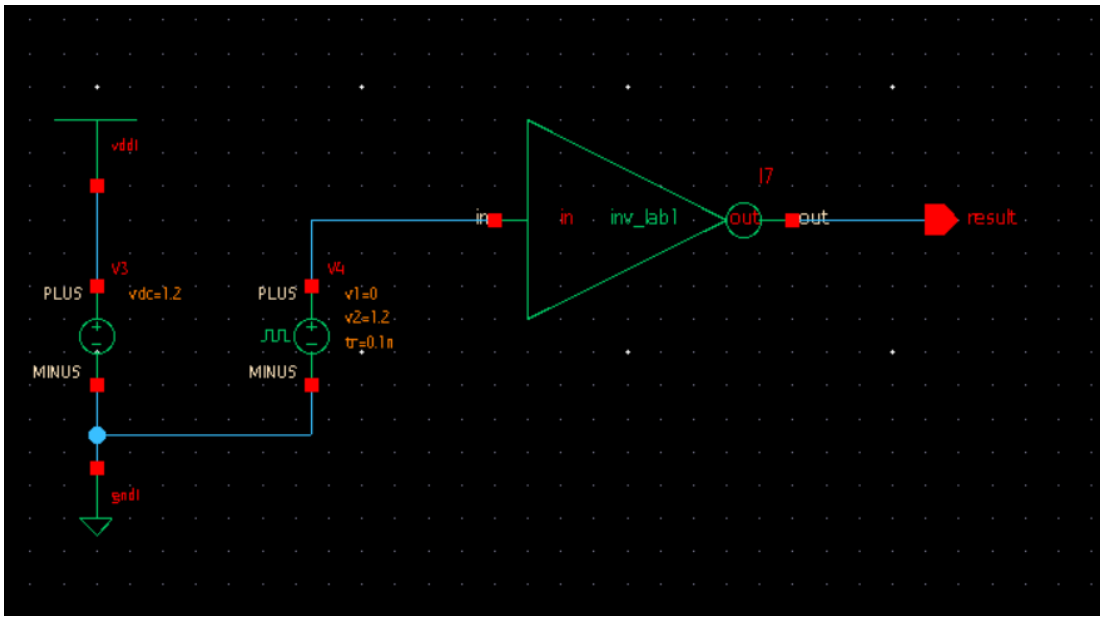

Figure 13. Schematic of config

```
*|DSPF 1.3
*|DESIGN inv_lab1
*|DATE "Wed May  3 01:41:41 2017"
*|VENDOR "Synopsys"
*|PROGRAM "StarRC"
*|VERSION "D-2010.06"
*|DIVIDER |
*|DELIMITER :
*|OPERATING_TEMPERATURE 25
*|GLOBAL_TEMPERATURE 25
**FORMAT SPF
*

** COMMENTS

** TCAD_GRD_FILE /home/eda/pdk/synopsys/PDK/starrc/reference_90nm_9lm_typ.nxtgrd
**   TCAD_TIME_STAMP Mon Apr 6 20:59:52 2009
**   TCADGRD_VERSION 64


.SUBCKT inv_lab1 out in

*|GROUND_NET 0

*LAYER_MAP
```

Figure 14. Content of symbol

2.2. HSPICE

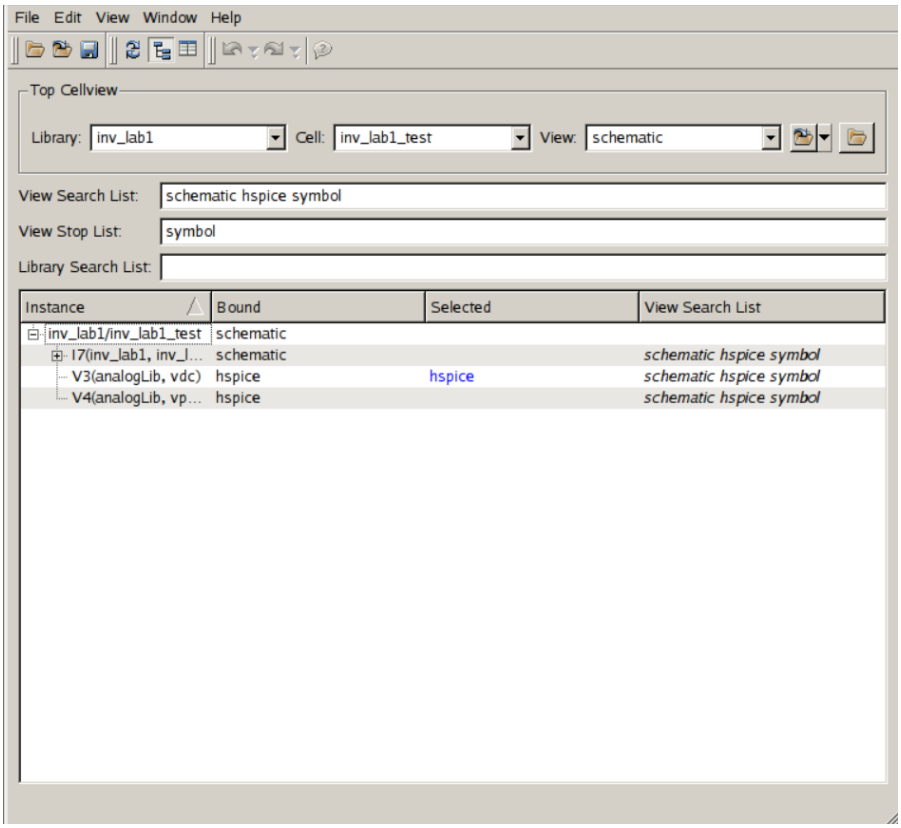

Figure 15. Config of HSPICE

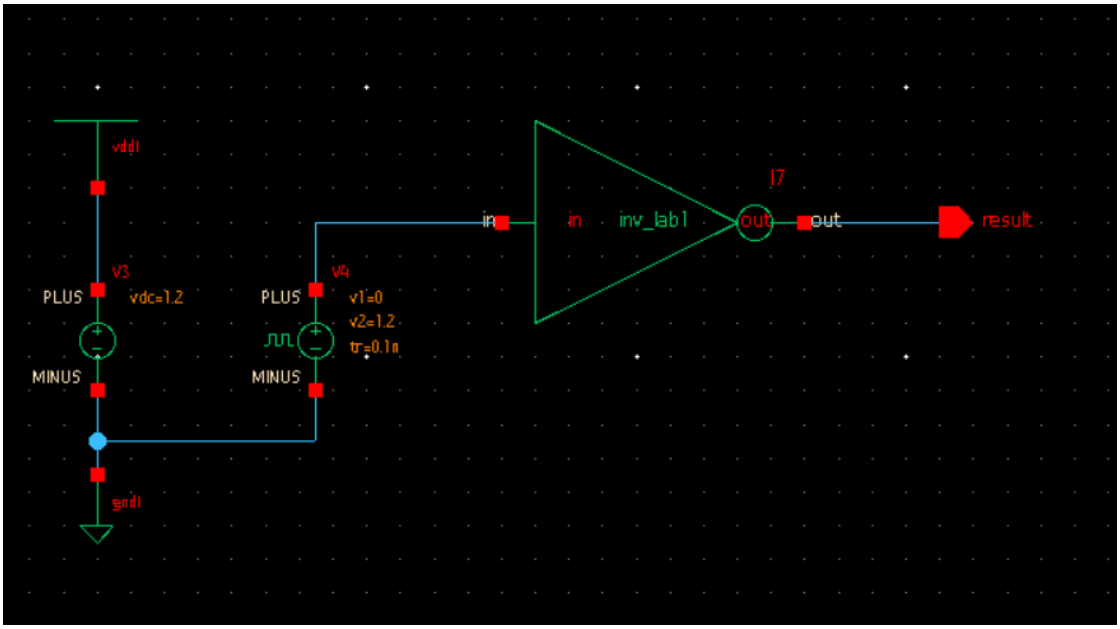

Figure 16. Schematic of config

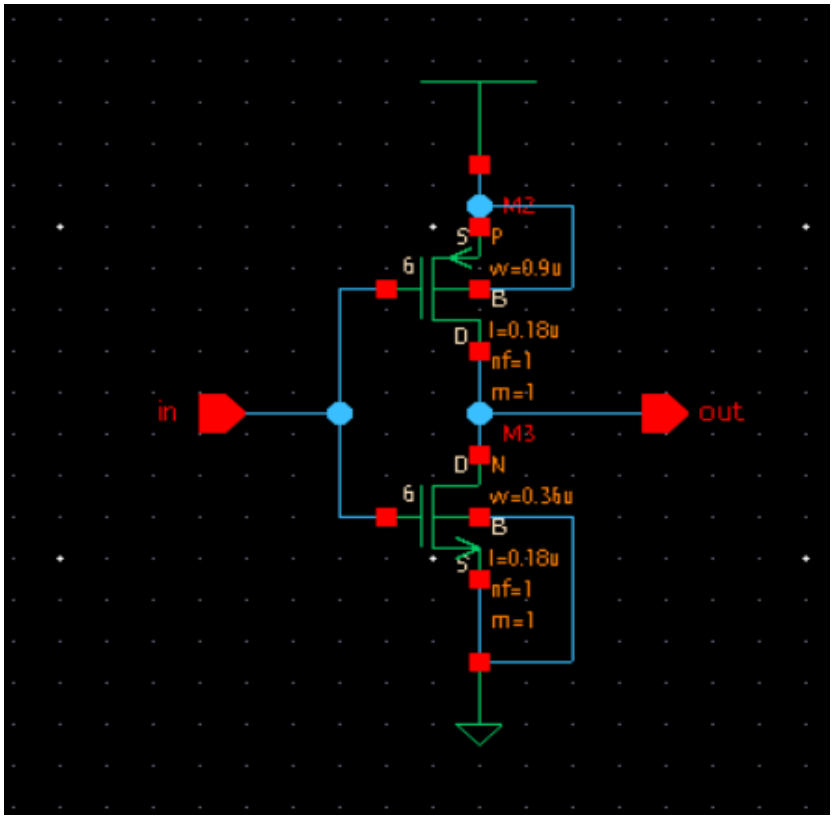

Figure 17. Content of symbol

2.3. SIMULATION

Both have the same waveform and only differ when clicking on the symbol.

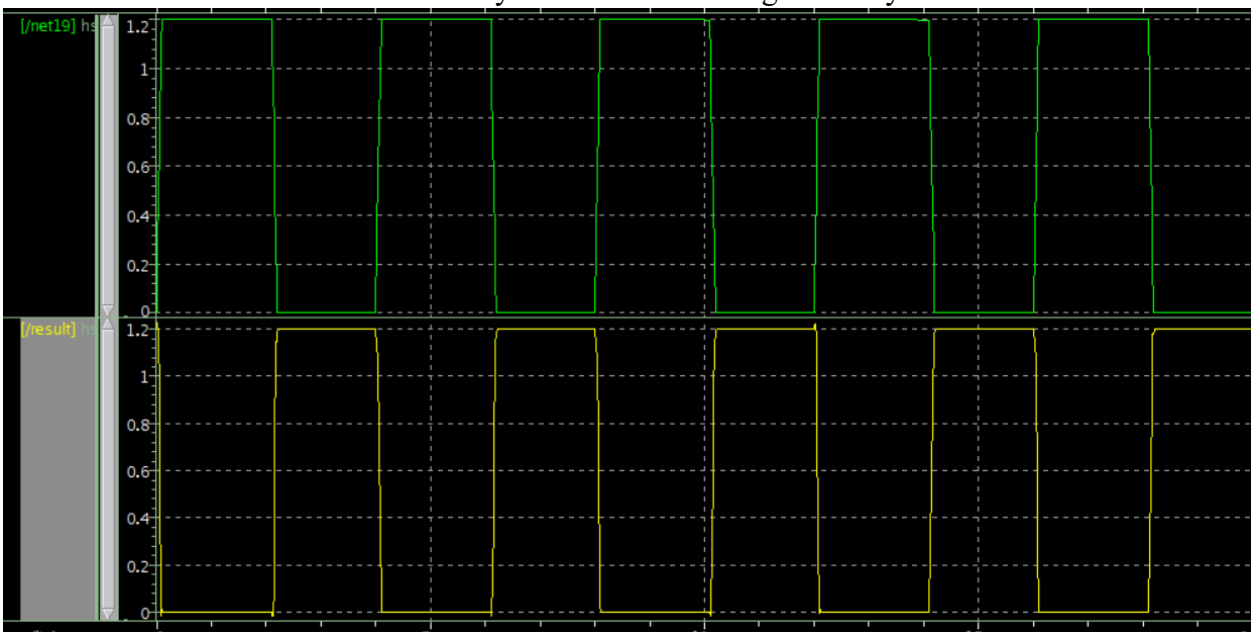

Figure 18. Waveform of POST LAYOUT