# SmartFusion Evaluation Kit

## User's Guide

Actel
POWER MATTERS

**Actel Corporation, Mountain View, CA 94043**



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## Trademarks

# Table of Contents

# Introduction

The RoHS-compliant SmartFusion™ Evaluation Kit (A2F-EVAL-KIT) enables designers to develop applications that involve one or more of the following:

- Microcontroller applications
- Embedded ARM® Cortex™-M3–based systems

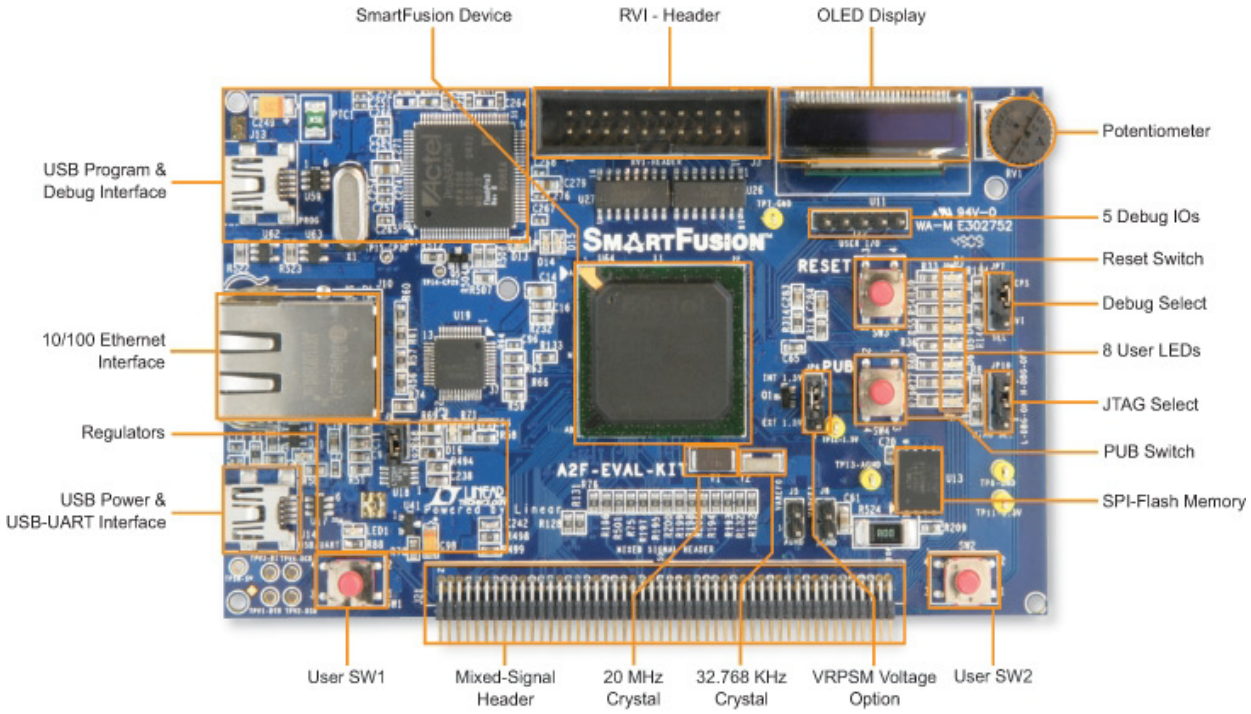



***Figure 1 •*** **A2F-EVAL-KIT**

## Kit Contents

Table 1 lists the contents of the SmartFusion Evaluation Kit..

***Table 1 •*** **A2F-EVAL-KIT Contents**

| Quantity | Description |
|---|---|
| 1 | SmartFusion Evaluation Board with SmartFusion A2F200M3F-FGG484ES device |
| 2 | USB 2.0 A to mini-B cable |
| 1 | Quickstart card |

# Board Description

The SmartFusion Evaluation Kit board is designed to provide a development platform for users to evaluate all the features of the world's only FPGA with a hard ARM Cortex-M3 powered microcontroller subsystem (MSS) along with programmable analog.

The board supports a SmartFusion device in an FG484 package. To enable the MSS, analog, and features for evaluation, the board includes the following:

- Ethernet and USB-to-UART interface for communication with the Ethernet and UART peripherals of the SmartFusion MSS
- SPI flash that interfaces with the SPI peripherals of the SmartFusion MSS
- Organic light-emitting diode (OLED) that interfaces with the $I^2C$ peripheral of the SmartFusion MSS
- $I^2C$ Interface
- Current monitoring and temperature monitoring circuits
- RVI header for application programming and debug from either Keil® U-LINK® Or IAR J-Link, integrated integrated low-cost programmer to enable programming and debugging from Actel design tools, FlashPoint and Soft Console

Table 2 describes the SmartFusion Development Kit board components.

***Table 2 •*** **SmartFusion Evaluation Kit Board Components**

| Name | Description |
|---|---|
| A2F200M3F-FGG484ES | Actel SmartFusion FPGA with hard ARM Cortex-M3 |
| OLED DISPLAY | Organic 96×16 pixel blue OLED PMO13701 with option to interface either interfacing with I2C0 port of SmartFusion MSS |
| SPI FLASH | 8 MByte SPI flash Atmel AT25DF641-MWH-T connected to SPI port 0 of the SmartFusion MSS |
| OSC-20 | 20 MHz / 20 PPM clock oscillator |
| OSC-32 | 32.768 KHz low-power oscillator |
| USB/UART | USB-to-UART adapter chip CP2102 and connector interfacing with UART port 0 of the SmartFusion MSS |
| ETHERNET | RJ45 connector (Ethernet jack with magnetics) interfacing with National Semiconductor 10/100 PHY chip DP83848C in RMII mode interfacing with Ethernet port of SmartFusion MSS (on-chip MAC and external PHY) |
| CURRENT | Current monitoring using thumbwheel POT (RV1) |
| TEMP | Temperature monitoring with temperature diode |
| RVI HEADER | RVI header for application programming and debug from Keil U-LINK or IAR J-Link |
| FP3_PROG | Integrated low-cost programmer |
| PUSH-BUTTON SWITCHES | Two push-button switches connected to GPIOs, which can be used as test and navigation switches |
| LEDS | Eight active low LEDs that can be connected to user I/O for debug to power on the board |
| USER I/Os | Five general purpose user I/Os that can be used for Direct-C signaling, interfacing and debugging purposes |
| PUSH-BUTTON RESET | Push-button system reset for SmartFusion FPGA System6 |
| MIXED_CONN100 | Mixed-signal header |

# 1 – Installation and Settings

## Software Installation

Download and install the latest release of Actel Libero® Integrated Design Environment (IDE) (v9.0 or later) from the Actel website and register for your free Gold license. For instructions on how to install Libero IDE and SoftConsole, refer to the Libero IDE Installation and Licensing Guide, available on the Actel website: www.actel.com/documents/install_ug.pdf.

Refer to the Installing IP Cores and Drivers User's Guide for downloading and installing Actel DirectCores, SGCores, and Driver firmware cores that must be localized on the personal computer where Libero IDE is installed when designing with Actel FPGAs.

Actel has partnered with key industry leaders in the microcontroller space to provide a robust SmartFusion ecosystem. Actel SmartFusion is supported by IAR Systems latest release, IAR Embedded Workbench for ARM. Refer to Designing SmartFusion with IAR Systems for more information.

Actel SmartFusion is also supported by Keil's latest release, MDK-ARM Microcontroller Development Kit. Refer to Designing SmartFusion with Keil for more information.

## Jumpers, Switches, and LED Settings

The recommended default jumpers, switches, LEDs, and DIP switch settings are defined in Table 1 through Table 4 on page 8. Connect the jumpers with the default settings to enable the pre-programmed demonstration design to function correctly.

The available headers and their usage are detailed in Table 5 and Table 6 on page 9.

***Table 1 •*** **SmartFusion Evaluation Kit Jumper Settings**

| Jumper | Function | Default Setting | Notes |
|---|---|---|---|
| J6 | Jumper to select second 3.3 V (V3P3_F2) power supply for board | Closed | |
| JP6 | Jumper to select either 1.5 V external regulator or SmartFusion 1.5 V internal regulator | | |
| | Pin 1–2 = 1.5 V internal | Closed | |
| | Pin 2–3 = 1.5 V external | Open | |
| JP7 | Jumper to select between RVI header or LCP header for application debug | | |
| | Pin 1–2 = USB programming and SoftConsole | Closed | |
| | Pin 2–3 = RVI for Keil U-LINK/IAR J-ink | Open | |
| JP10 | Jumper to select JTAGSEL | | Allows selection of A2F2 programming or Cortex-M3 debug with integrated low-cost programmer |
| | Pin 1–2 = FPGA, allows A2F2 programming | Closed | |
| | Pin 2–3 = M3, allows Cortex-M3 debug | Open | |

***Table 2 •*** **SmartFusion Evaluation Kit Push-Button Switches**

| Push-Button Switch | SmartFusion FPGA Pin | Comment |
|---|---|---|
| SW1 | G19 | Test and navigation switch |
| SW2 | G20 | Test and navigation switch |
| SW3 | W7(PU_N) | Push-button switch for PUB. This negative active switch is connected to the PUB pin, which is a digital input to the FPGA. PUB is the connection for the external momentary switch used to turn on the 1. 5 V voltage regulator. |
| SW4 | R1 (MSS_SYSRESET) | System Reset for DUT |

***Table 3 •*** **SmartFusion Evaluation Kit LEDs**

| LED | SmartFusion FPGA Pin | Comment |
|---|---|---|
| D1 | B19 | Test LED for user application |
| D2 | B20 | Test LED for user application |
| D3 | C19 | Test LED for user application |
| D4 | H17 | Test LED for user application |
| D5 | H20 | Test LED for user application |
| D6 | C21 | Test LED for user application |
| D7 | D21 | Test LED for user application |
| D8 | G21 | Test LED for user application |
| D11 | N/A | UART over USB link indicator LED |
| D14 | N/A | Programmer activitiy indicator LED |
| D15 | N/A | Programmer ON indicator LED |
| D16 | N/A | SPEED LED. The LED is ON when device is in 100 Mbps mode and OFF when in 10 Mbps mode. |
| LED1 | N/A | USB power supply indicator LED. This GREEN LED is ON when the board is powered on. |

***Table 4 •*** **Test Points**

| Test Point | Comment |
|---|---|
| TP7, TP8 | Digital ground (GND) |
| TP11 | 3.3 V supply for SmartFusion |
| TP12 | 1.5 V supply for SmartFusion |
| TP13 | Analog ground (AGND) |

***Table 5 •*** **J22 Header Strip – User I/Os**

| Pin | SmartFusion FPGA I/O |
|---|---|
| 1 | J19 |
| 2 | J20 |
| 3 | J21 |
| 4 | J22 |
| 5 | K19 |

***Table 6 •*** **Header for VAREF Monitoring**

| Jumper | Description |
|---|---|
| J5 | Used to monitor VAREF0 driven from VAREFOUT output of A2F |
| J8 | Used to monitor VAREF1 driven from VAREFOUT output of A2F |

Note: Never put a jumper on these headers. These are provided to measure and monitor VAREF0 and VAREF1

# Testing the Hardware

If the board is shipped directly from Actel, it contains a test program that determines whether the board works properly. If while using the board you suspect that the board is damaged, you can rerun the "Manufacturing Test" to verify functionality of the key components of the board.

# 2 – Hardware Components

## FPGA Description and Connections

The SmartFusion Development Kit Board is populated with a SmartFusion A2F200-FG484, the world's only FPGA with hard ARM Cortex-M3. The key features of SmartFusion are listed below.

The microcontroller subsystem (MSS) consists of the following:

- 100 MHz 32-bit ARM Cortex-M3
  - 1.25 DMIPS/MHz throughput from zero wait state memory
- Internal memories
  - Embedded flash memory (eNVM), 64 Kbytes to 512 Kbytes
  - Embedded high-speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, implemented in two physical blocks to enable simultaneous access from two different masters
- Multi-layer AHB communications matrix
  - Provides up to 16 Gbps of on-chip memory bandwidth
- 10/100 Ethernet MAC with RMII interface
- Programmable external memory controller, which supports the following:
  - Asynchronous memories
  - NOR flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two $I^2C$ peripherals
- Two 16550 compatible UARTs
- Two SPI peripherals
- Two 32-bit timers
- 32-bit watchdog timer
- 8-channel DMA controller
- Clock sources
  - 1.5 MHz to 20 MHz main oscillator
  - Battery-backed 32 KHz low-power oscillator with real-time counter (RTC)
  - 100 MHz embedded RC oscillator 1% accuracy
  - Embedded PLL with 4 output phases
- High-performance FPGA
- Based on Actel's proven ProASIC® FPGA fabric
- Analog front-end (AFE)
- Up to three 12-bit SAR analog-to-digital converters (ADCs)
- One first-order $\Sigma\Delta$ (sigma delta) digital-to-analog converter (DAC) per ADC
- Up to 5 new high-performance analog signal conditioning blocks (SCB) per device
- Two high-speed comparators
- Analog compute engine (ACE)
  - Offloads CPU from analog initialization and processing of ADC, DAC, and SCBs
  - Sample sequencing engine for ADC and DAC parameter setup
  - Post-processing engine (PPE) for functions such as low-pass filtering and linear transformation

***Table 1 •*** **A2F200 Key Features**

| Feature | Specification |
|---|---|
| System gates | 200,000 |
| Tiles (D-flip-flops) | 4,608 |
| RAM blocks (4,608 bits) | 8 |
| Flash (Kbytes) | 256 |
| SRAM (Kbytes) | 64 |
| Cortex-M3 with MPU | 1 |
| 10/100 Ethernet MAC | Yes |
| External memory controller (EMC) | 26-bit address, 16-bit data |
| DMA | 8 Ch |
| $I^2C$ | 2 |
| SPI | 2 |
| 16550 UART | 2 |
| 32-bit timer | 2 |
| PLL | 1 |
| 32 KHz low-power oscillator | 1 |
| 100 MHz on-chip RC oscillator | 1 |
| Main oscillator | 1 |
| ADCs (12-bit SAR) | 2 |
| DACs (1-bit sigma-delta) | 2 |
| Signal conditioning blocks (SCBs) | 4 |
| Comparators* | 8 |
| Current monitors* | 4 |
| Temperature monitors* | 4 |
| HV bipolar voltage monitors* | 8 |
| Direct analog inputs to ADC* | 18 |

*Note: *The maximum available resources have dependencies. For additional information on SmartFusion, refer to the SmartFusion datasheet..*

***Table 2 •*** **A2F200 I/Os**

| I/Os | FG484 |
|---|---|
| Direct analog input | 8 |
| Total analog input | 24 |
| Total analog output | 2 |
| MSS I/Os[1,2] | 41 |
| FPGA I/Os | 94 |
| Total I/Os | 161 |

*Notes:*

1. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, and 3.3 V) standards.*
2. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5/1.8/2.5, and 3.3 V standards.*

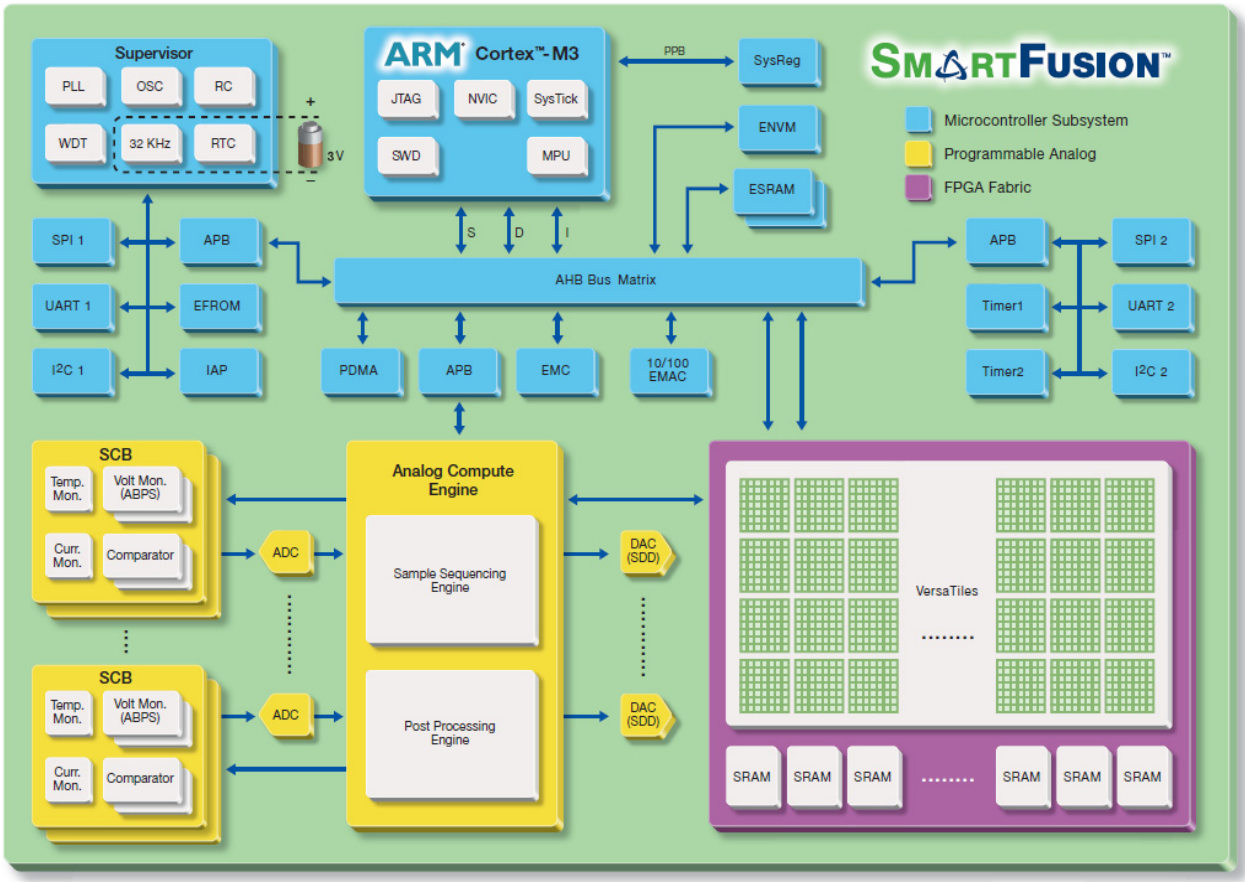



***Figure 1 •*** **SmartFusion MSS Block Diagram**

# I/O Pin Connections

The A2F200M3F-FGG484ES pin list is provided in the chapter "Pin List".

# SmartFusion FPGA Hard ARM Cortex-M3

The SmartFusion FPGA comes with a hard Cortex-M3 advanced processor-based MSS. The ARM Cortex-M3 microcontroller is a low-power processor that features low gate count, low predictable interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response features. SmartFusion devices use the R1P1 version of the Cortex-M3 core. Some of the important subsystems are listed below:

- Memory protection unit (MPU)
- Single cycle multiplication, hardware divide
- JTAG debug (4 wire), Serial Wire Debug (SWD – 2 wire) and Serial Wire Viewer (SWV) interfaces

The evaluation board is populated with components to enable development using the MSS. These components include SPI flash, OLED, and communication interfaces such as Ethernet and USB-to-UART.

# Power Sources

## SmartFusion FPGA Power Sources

The evaluation kit board is powered through USB. The USB power will supply power to three voltage rails: 3.3 V, 1.5 V, and 10 V.

- Linear LT1963AES8 (1.5 A), supplies 3.3 V rails
- Linear LT3080 (1.1 A), supplies 1.5 V rails
- Linear LT1615 step-up converter supplies 10 V, 100 mA typical, for driving the OLED

Note: The USB can provide a maximum current of 500 mA. If the application requires a daughter board, the user must use an independent power supply source.

# 3 – Component Descriptions and Connections

## VAREF Connections

The SmartFusion device has one external VAREF input pin for each of the ADCs in the device. These are VAREF0 for ADC0 and VAREF1 for ADC1 (Figure 1). The internal VAREF is brought out as an output. This is available as the VAREFOUT output pin.

On the A2F-EVAL-KIT board, the VAREF0 and VAREF1 inputs are hardwired to the VAREFOUT output of the SmartFusion device (Figure 2). This means the user should not drive these inputs from any external source. Two headers, J5 and J8, are provided to monitor the VAREF0 and VAREF1 for any debug purposes.

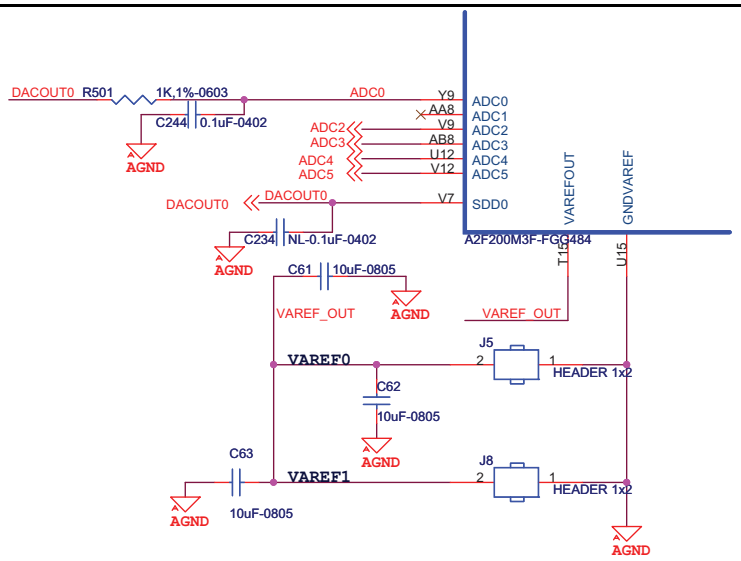



***Figure 1 •*** **VAREFOUT to VAREF0 and VAREF1**


***Figure 2 •*** **VAREF0 and VAREF1 Inputs of FPGA**

## Current Sensing Circuit

A current sensing circuit is provided on the SmartFusion Evaluation Kit board for applications using the embedded current monitor. Current monitoring is performed across the AC0 and AT0 pins. The current sensing circuit is for the 3.3 V voltage rail, as shown in Figure 3.

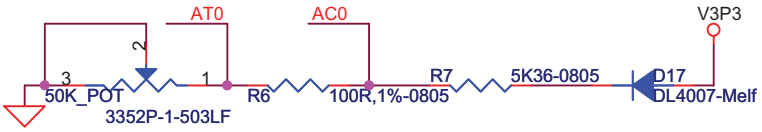



***Figure 3 •*** **Current Sensing**

# PWM Circuit

The PWM RC circuit depicted in Figure 4 and Figure 5 can be used with Actel CorePWM instantiated in the FPGA fabric to generate various voltage waveforms. These voltage waveforms can be displayed on the OLED or used via the mixed-signal header. In addition, one PWM RC circuit source is routed to the AV input pin of an analog quad. This AV pin can be used to monitor the generated voltage with high accuracy, depending on the ADC resolution configured in the FPGA.

Figure 5 shows the A2F200 pins driving PWM and the PWM circuit.

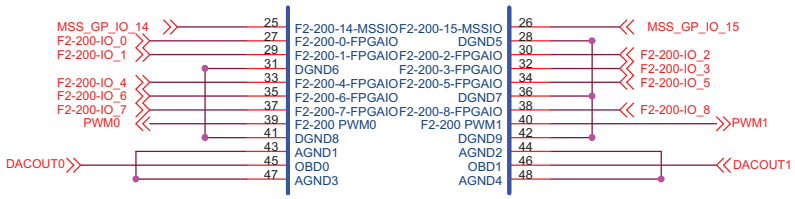



***Figure 4* • PWM Pins**

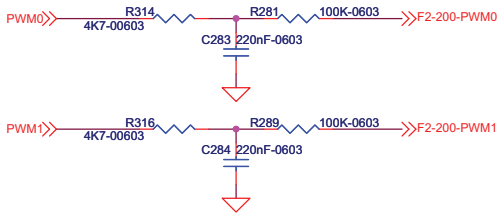



***Figure 5* • PWM Circuit**

# Push-Button System Reset

A push-button system reset switch with a Schmitt trigger is provided on the board (Figure 6). The Schmitt trigger reduces noise on the system reset push-button. SmartFusion MSS reset is synchronized with this reset.

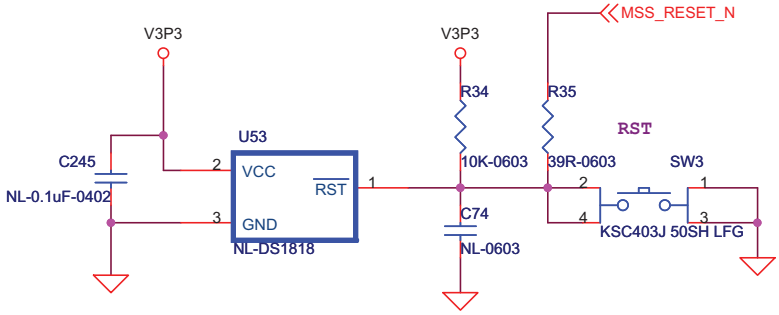



***Figure 6* • Push-Button System Reset**

# Push-Button Switches and User LEDs

Push-button switches and user LEDs (Figure 7) can also be used for debug and for various applications, such as gaming.

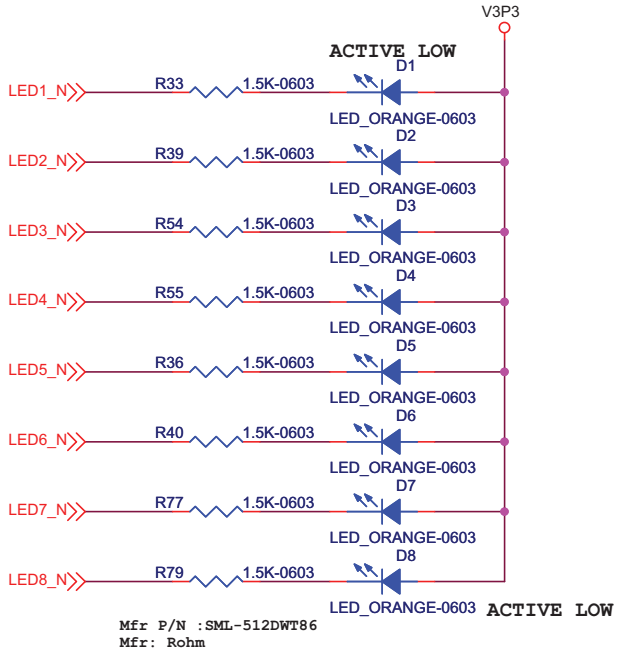



***Figure 7* • Test LEDs**

The board provides users access to eight active Low LEDs (Figure 8), which are connected to SmartFusion pins B19, B20, C19, H17, H20, C21, D21, and G21. In addition, the board includes two push-button switches (Figure 9 on page 18) that are connected to pins G19 and G20 of the SmartFusion FPGA.

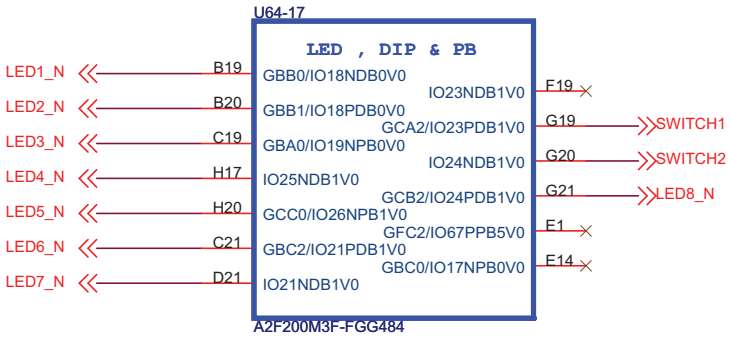



***Figure 8* • LEDs**

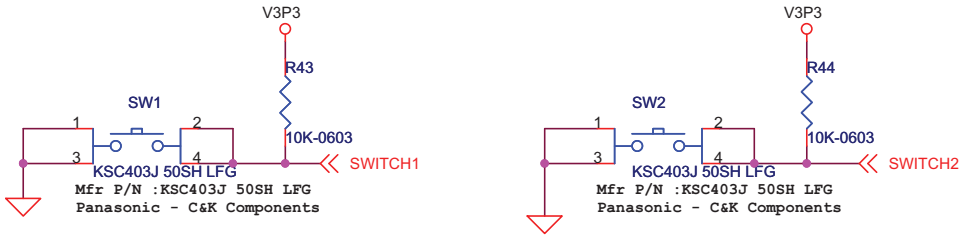



***Figure 9* • Push-Button Switches**

## User I/Os

The board comes with the provision of five user I/Os brought out to jumper J22 (Figure 10). These can be used as general purpose user I/Os. One of the potential applications is DirectC signaling where these five pins can be used for JTAG signals (TDI, TDO, TMS, TCK, and TRSTN). Other possible uses are for interfacing with other boards and debugging.

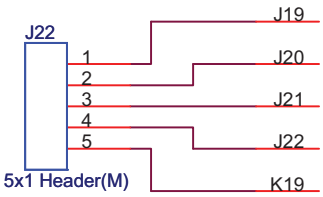



***Figure 10* • User I/Os**

# OLED Display

A 9616-pixel low-power OLED is made available on the board for display (EQ 11 on page 19). This low-power device, BLUE OLED, requires 3.3 V and 10 V power supplies. The OLED is interfaced with the SmartFusion MSS I2C0 port (Figure 12 on page 19). The OLED displays sharp gaming images or text. For example, the SmartFusion RTC current time or time between two events can be displayed on the OLED. The OLED inputs OLED_BS1, OLED_BS2, and OLED_CSN are tied off and OLED_D/C# is pulled down as required to work with $I^2C$ mode.

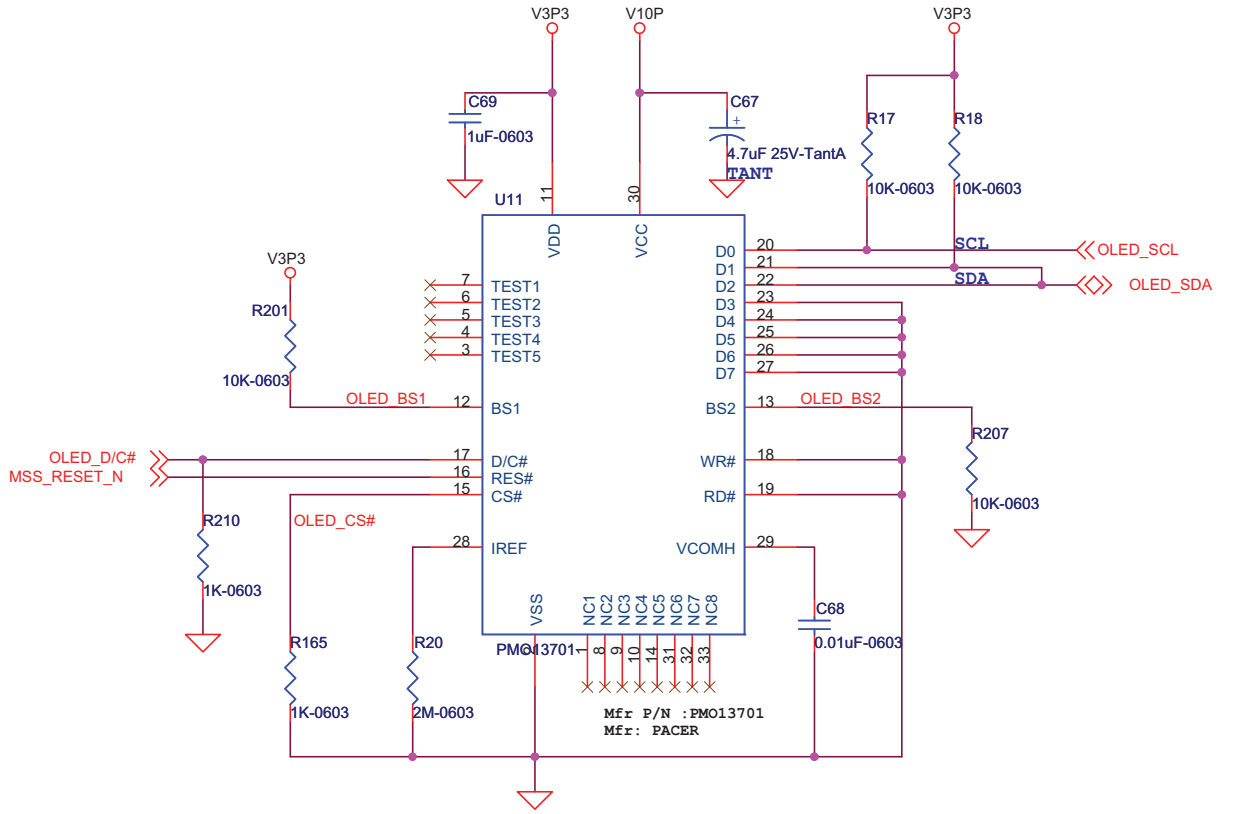



***Figure 11* • OLED Connections**

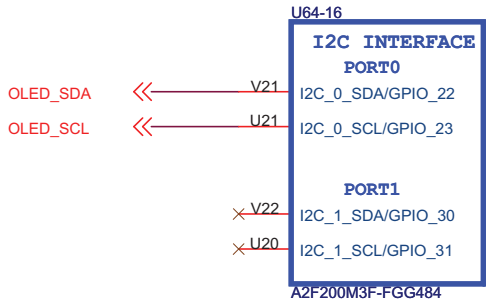



***Figure 12* • SmartFusion MSS I2C0 Interface**

# SPI Flash

One 8 MByte SPI flash Atmel AT25DF641-MWH-T is also offered on the board (Figure 13). This is interfaced with the SmartFusion MSS SPI0 port (Figure 14). The WP# and HOLD# inputs are pulled High on the board.

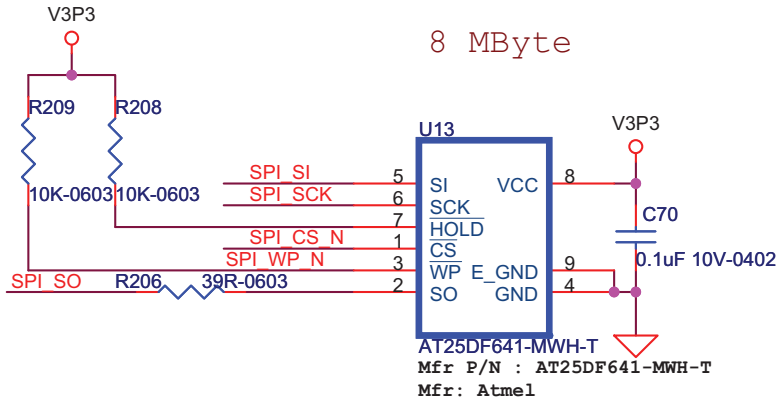



***Figure 13* • SPI Flash**

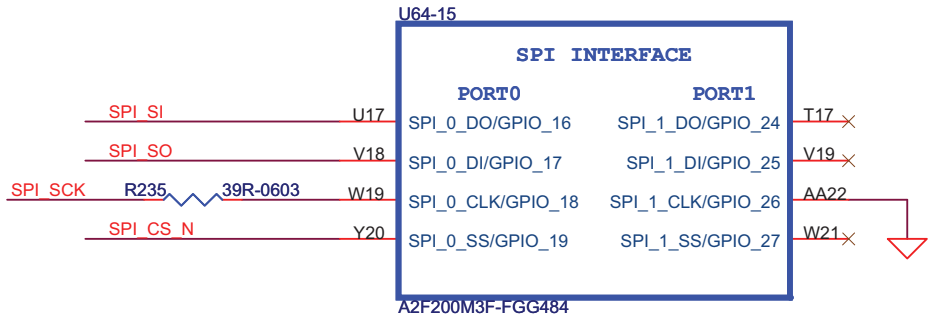



***Figure 14* • SmartFusion MSS SPI0 Port**

# 20 MHz Oscillator

A 20 MHz resonator of 20 PPM is placed across the MAINXIN and MAINXOUT pins of the SmartFusion FPGA with the appropriate 18 PF capacitors (Figure 15 on page 21). This is used to generate a high precision clock for Ethernet MAC and is also used in real-time counter (RTC) based applications.

# 32.768 KHz (low power) Oscillator

A 32.768 KHz Resonator CM519 is placed across the LPXIN and LPXOUT pins of the SmartFusion FPGA with the appropriate 30 PF capacitors (Figure 15). This low power resonator is useful in real-time counter (RTC) based applications.

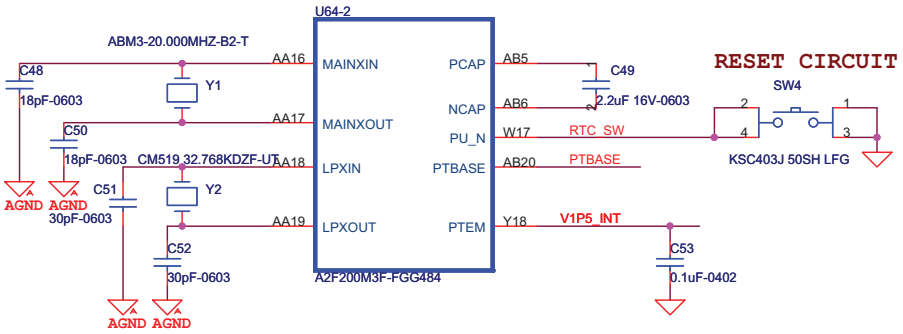



***Figure 15 •*** **20 MHz and 32.768 KHz Oscillators**

# USB-to-UART Interface

Included on the evaluation board is a USB-to-UART interface with ESD protection (Figure 16 on page 22). This interface includes an integrated USB-to-UART bridge controller (U16) to provide a standard UART connection with the SmartFusion MSS UART0 port.

One application of the USB-to-UART interface is to allow HyperTerminal on a PC to communicate with the SmartFusion FPGA. HyperTerminal is a serial communications application program that can be installed in the Windows® operating system. A basic HyperTerminal program is usually distributed with Windows. With a USB driver properly installed, and the correct COM port and communication settings selected, you can use the HyperTerminal program to communicate with a design running on the SmartFusion FPGA device.

Table 1 lists the supported UART parameters for HyperTerminal applications.

***Table 1 •*** **UART HyperTerminal Settings**

| **Supported HyperTerminal Parameters** | | | |
|---|---|---|---|
| **Baud Rates** | **Data Bits** | **Parity Types** | **STOP BIT** |
| 110 | 5,6,7,8 | NO/ODD/EVEN/MARK(1)/SPACE(0) | ONE/ONE-HALF/TWO |
| 300 | | | |
| 1200 | | | |
| 2400 | | | |
| 4800 | | | |
| 9600 | | | |
| 19200 | | | |
| 38400 | | | |
| 57600 | | | |
| 115200 | | | |
| 230400 | | | |
| 460800 | | | |
| 921600 | | | |

Figure 16 shows the USB-to-UART connections and Figure 17 shows the UART0 port.

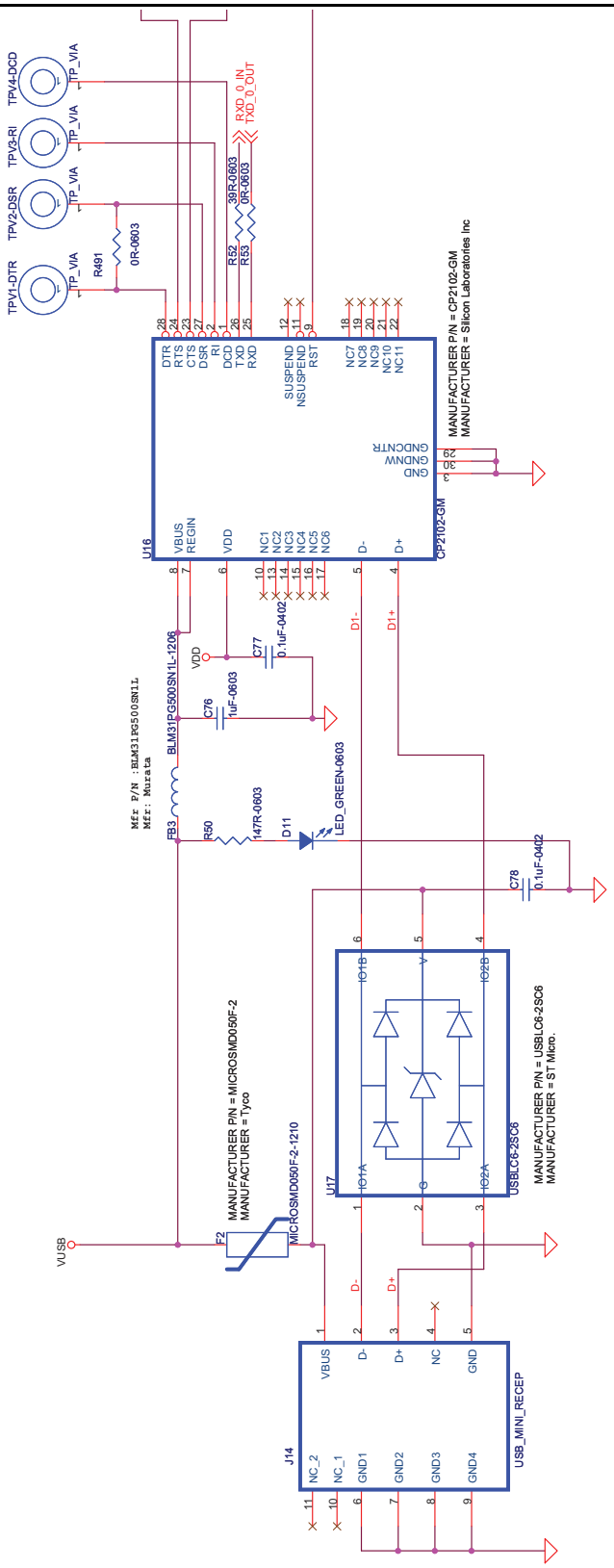



***Figure 16* • USB to UART**

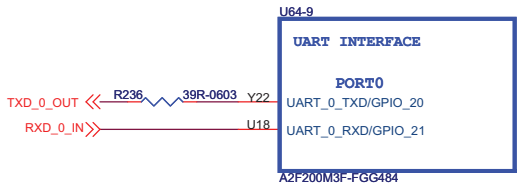



***Figure 17 •*** **UART Port 0**

# Ethernet Interface

One Ethernet interface, configured for RMII Full Duplex mode, and a low-power 10/100 Mbps single-port Ethernet physical layer transceiver (U19) are provided on-board (Figure 19 on page 24). The Ethernet physical layer features integrated sub-layers to support both 10BASE-T and 100BASE-TX Ethernet protocols. These sub-layers ensure compatibility and interoperability with many other standards-based Ethernet solutions.

The Ethernet RJ45 interface and physical layer interface with the SmartFusion MSS Ethernet media access controller (MAC), which supports RMII, serve many purposes. For example, these interfaces can be used to access the SmartFusion FPGA to monitor the ADC data over a network. The embedded system memory and control registers can be accessed and processed remotely to support system management.

## Clocking Scheme for RMII CLK

The 10/100 MAC RMII interface requires a 50 MHz clock. The PHY device also requires a 50 MHz 20 PPM clock for proper operation. While there are several possible ways of providing the clock, the following clocking scheme has been tested on the board.

- The 20 MHz oscillator feeds the CCC input. The CCC, GLC output is configured as 50 MHz.
- The GLC feeds the MAC_CLK (pin T6) input of the 10/100 MAC peripheral of the SmartFusion MSS.
- The same GLC is routed through the fabric and feeds the X1 input of the Ethernet PHY device on the board.

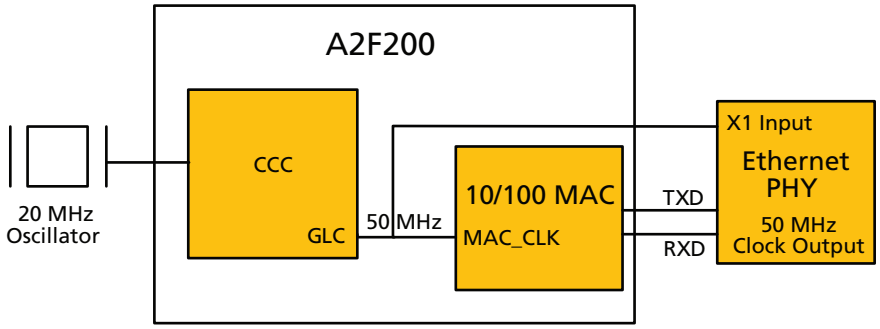



***Figure 18 •*** **Ethernet Clocking Scheme**

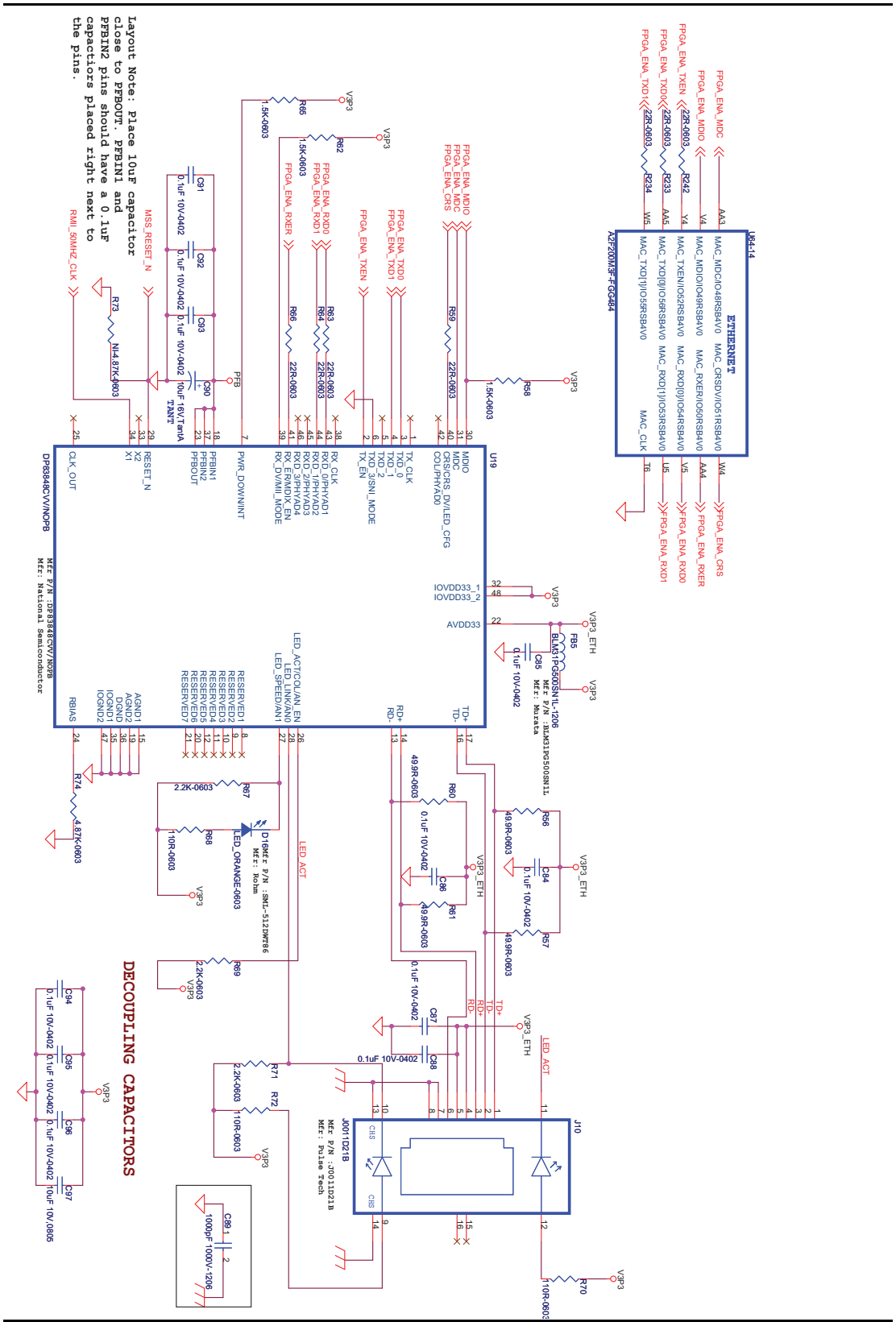



***Figure 19 •*** **Ethernet Interface**

# RealView Header

One 10x2 RealView® Header is provided on the board for debugging (Figure 20). This header allows plugging with the Keil U-LINK debugger or IAR J-Link debugger to easily debug or configure the hard ARM Cortex-M3 processor during board power-up.

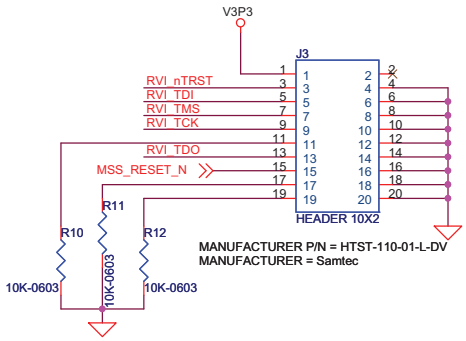



***Figure 20 •*** **RealView Header**

The jumper settings shown in Table 2 are needed for debug with Keil U-LINK or IAR J-Link.

***Table 2 •*** **RVI Header Jumper Settings**

| To Debug with Keil U-link or IAR J-link | | | |
|---|---|---|---|
| **Jumper** | **Pin** | **Pin** | **Connection Details** |
| JP7 | 2 | 3 | To select RealView® JTAG header |
| JP10 | 2 | 3 | To select Cortex-M3 debug |

# Integrated Low-Cost Programmer (LCP)

The board comes with a built-in programmer to program the SmartFusion device and debug software with SoftConsole.

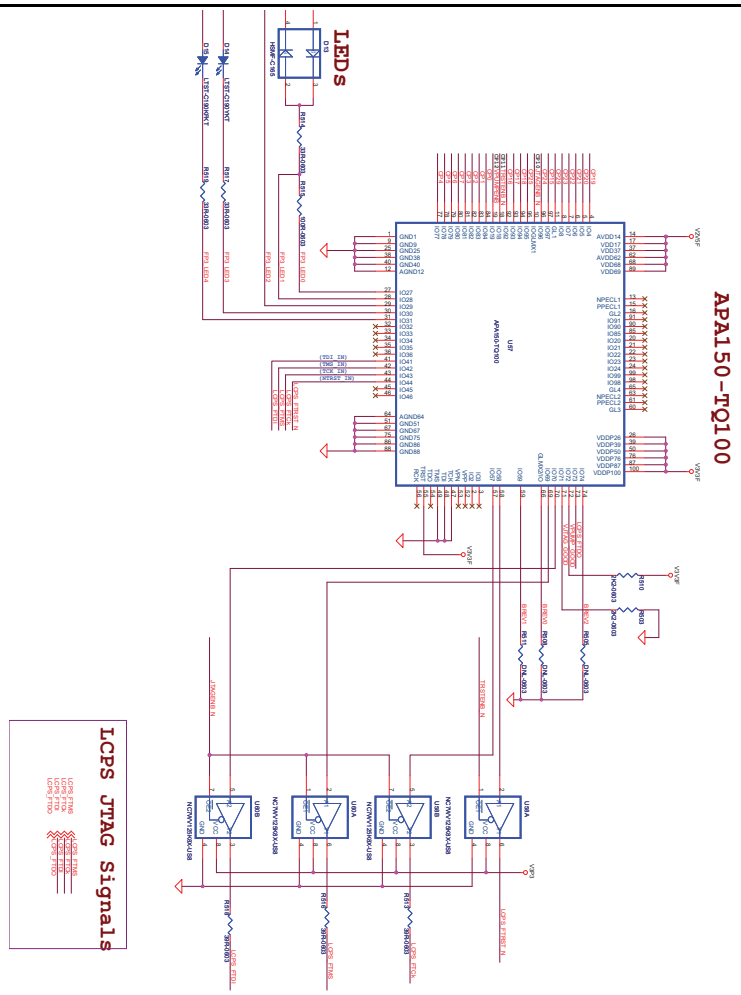



***Figure 21 •*** **Integrated Low-Cost Programmer**

***Table 3 •*** **Jumper Settings to Debug with SoftConsole**

| To Debug with SoftConsole | | | |
|---|---|---|---|
| **Jumper** | **Pin** | **Pin** | **Connection Details** |
| JP7 | 1 | 2 | To select the the integrated low-cost programmer (LCP) |
| JP10 | 2 | 3 | To select the Cortex-M3 debug |

***Table 4 •*** **Jumper Settings for A2F200 Programming**

| To Program with Built-In LCP | | | |
|---|---|---|---|
| **Jumper** | **Pin** | **Pin** | **Connection Details** |
| JP7 | 1 | 2 | To select the integrated LCP |
| JP10 | 1 | 2 | To select the SmartFusion device |

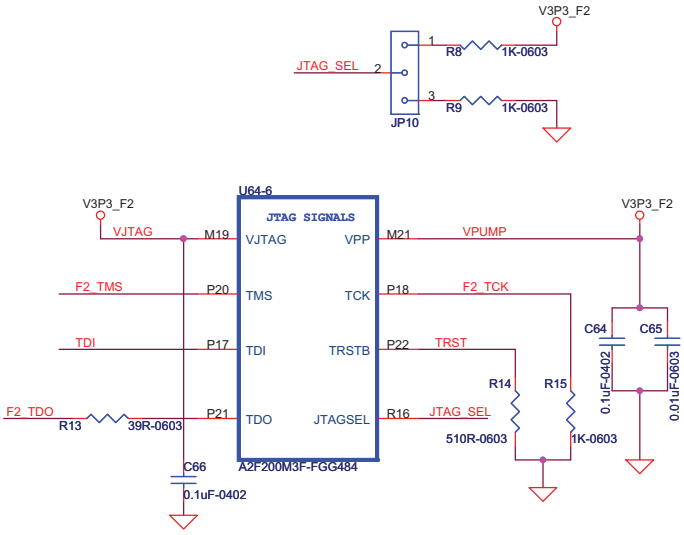



***Figure 22 •*** **A2F200 JTAG Connections**

# Temperature Diode

A temperature diode is provided on the board to measure ambient temperature (Figure 23). This is used in battery charging and MPM applications. This diode is connected to the AT1 input of SmartFusion FPGA.

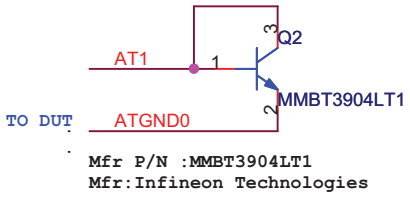



***Figure 23 •*** **Temperature Diode**

# Mixed-Signal Header

The mixed-signal header can be obtained from Samtec, using the following part numbers:

Mother Board Header 2X50 50 mil pitch: Samtec FTSH-150-04-L-D-RA (populated in the evaluation board)

Daughter Board Header 2X50 50 mil pitch: Samtec CLP-150-02-L-DH

The detailed instructions given below must be followed to ensure the correct orientation and insertion into the mother board.

Figure 24 (top view) indicates the orientation of the mixed-signal headers on the mother board and daughter board.

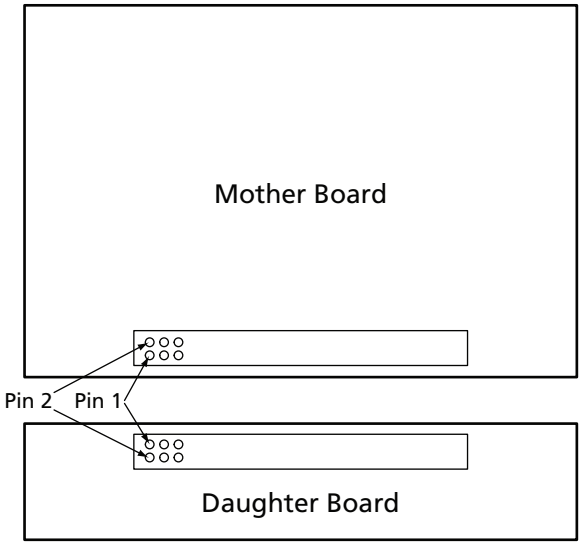
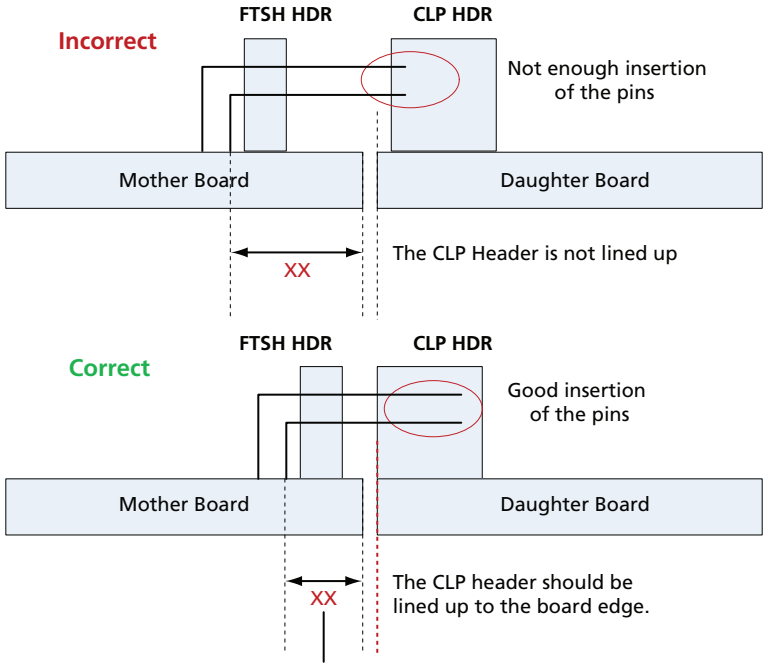



***Figure 24 •*** **Top View of Mixed-Signal Headers Correct Orientation**

Ensure that the header is placed such that a full insertion is possible between the two headers (Figure 25).




*Note: XX is the critical length. Ensure that the connector is placed close enough so there is a good connection with the mating connector. This is applicable when designing the daughter board or the mother board.*

***Figure 25 •*** **Correct Insertion of Daughter Board**

When designing a daughter board to plug into an A2F-EVAL-KIT:

- Ensure the CLP header edge is lined up against the edge of the board.
- This will provide maximum insertion into the SmartFusion evaluation board.

When designing a mother board for an existing daughter board (MPM DB, for example):

- Ensure that the length, denoted by XX, is kept less than 150 mils.
- Use the SmartFusion Evaluation Kit PCB files (www.actel.com/download/rsc/?f=A2F_EVAL_KIT_BF).

## Pinout Definition

Table 5 provides the pinout definition for the mixed-signal header.

***Table 5 •*** **Pinout Definition**

| J21-Pin | Net Name | Pin Number | Description | J21-Pin | Net Name | Pin Number | Description |
|---|---|---|---|---|---|---|---|
| 1 | 5V | Power | Power | 2 | 5V | Power | Power |
| 3 | 5V | Power | Power | 4 | 5V | Power | Power |
| 5 | DGND | DGND | Digital ground | 6 | DGND | DGND | Digital ground |
| 7 | MSS_GP_IO_0 | V1 | MSS I/Os[1] | 8 | MSS_GP_IO_1 | R3 | MSS I/Os[1] |
| 9 | MSS_GP_IO_2 | W1 | MSS I/Os[1] | 10 | MSS_GP_IO_3 | Y1 | MSS I/Os[1] |
| 11 | MSS_GP_IO_4 | AA1 | MSS I/Os[1] | 12 | DGND | DGND | Digital ground |
| 13 | MSS_GP_IO_5 | U2 | MSS I/Os[1] | 14 | MSS_GP_IO_6 | V2 | MSS I/Os[1] |
| 15 | DGND | DGND | Digital ground | 16 | MSS_GP_IO_7 | W2 | MSS I/Os[1] |
| 17 | MSS_GP_IO_8 | T3 | MSS I/Os[1] | 18 | MSS_GP_IO_9 | V3 | MSS I/Os[1] |
| 19 | MSS_GP_IO_10 | U3 | MSS I/Os[1] | 20 | DGND | DGND | Digital ground |
| 21 | MSS_GP_IO_11 | T4 | MSS I/Os[1] | 22 | MSS_GP_IO_12 | AA2 | MSS I/Os[1] |
| 23 | DGND | DGND | Digital ground | 24 | MSS_GP_IO_13 | AB2 | MSS I/Os[1] |
| 25 | MSS_GP_IO_14 | AB3 | MSS I/Os[1] | 26 | MSS_GP_IO_15 | Y3 | MSS I/Os[1] |
| 27 | F2-200-IO_0 | E3 | FPGA I/Os[1] | 28 | DGND | DGND | Digital ground |
| 29 | F2-200-IO_1 | F3 | FPGA I/Os[1] | 30 | F2-200-IO_2 | G4 | FPGA I/Os[1] |
| 31 | DGND | DGND | Digital ground | 32 | F2-200-IO_3 | H5 | FPGA I/Os[1] |
| 33 | F2-200-IO_4 | H6 | FPGA I/Os[1] | 34 | F2-200-IO_5 | J6 | FPGA I/Os[1] |
| 35 | F2-200-IO_6 | B22 | FPGA I/Os[1] | 36 | DGND | | Digital ground |
| 37 | F2-200-IO_7 | C22 | FPGA I/Os[1] | 38 | F2-200-IO_8 | F1 | FPGA I/Os[1] |
| 39 | PWM0 | E22 | Has External RC*[1] | 40 | PWM1 | F22 | Has External RC*[1] |
| 41 | DGND | DGND | Digital ground | 42 | DGND | DGND | Digital ground |
| 43 | AGND | AGND | Analog ground | 44 | AGND | AGND | Analog ground |
| 45 | DACOUT0 | V7 | SDD0[2] | 46 | DACOUT1 | Y17 | SDD1[2] |

*Notes:*

1. *Digital signal.*
2. *Analog signal.*

***Table 5 •*** **Pinout Definition**

| J21-Pin | Net Name | Pin Number | Description | J21-Pin | Net Name | Pin Number | Description |
|---|---|---|---|---|---|---|---|
| 47 | AGND | AGND | Analog ground | 48 | AGND | AGND | Analog ground |
| 49 | AC2 | AB13 | CM2[2] | 50 | AT2 | AB12 | TM2[2] |
| 51 | AGND | AGND | Analog ground | 52 | ATGND1 | | GNDTM1[2] |
| 53 | AC3 | AA11 | CM3[2] | 54 | AT3 | Y12 | TM3[2] |
| 55 | AGND | AGND | Analog ground | 56 | AGND | | Analog ground |
| 57 | NC | NC | NC | 58 | NC | NC | NC |
| 59 | AGND | AGND | Analog ground | 60 | ATGND2 | | GNDTM2[2] |
| 61 | AV1_1 | W9 | ABPS2[2] | 62 | AV2_1 | AB7 | ABPS3[2] |
| 63 | AGND | AGND | Analog ground | 64 | AGND | AGND | Analog ground |
| 65 | AV1_3 | W12 | ABPS6[2] | 66 | AV2_3 | Y11 | ABPS7[2] |
| 67 | AGND | AGND | Analog ground | 68 | AGND | AGND | Analog ground |
| 69 | NC | NC | NC | 70 | NC | NC | NC |
| 71 | AGND | AGND | Analog ground | 72 | AGND | AGND | Analog ground |
| 73 | ADC2 | V9 | ADC2 | 74 | ADC3 | AB8 | ADC3 |
| 75 | AGND | AGND | Analog ground | 76 | AGND | AGND | Analog ground |
| 77 | ADC4 | U12 | ADC4 | 78 | ADC5 | V12 | ADC5 |
| 79 | AGND | AGND | Analog ground | 80 | AGND | AGND | Analog ground |
| 81 | ADC6 | V11 | ADC6[2] | 82 | ADC7 | T12 | ADC7[2] |
| 83 | AGND | AGND | Analog ground | 84 | AGND | AGND | Analog ground |
| 85 | ADC8 | V14 | ADC8[2] | 86 | ADC9 | AA14 | ADC9[2] |
| 87 | AGND | AGND | Analog ground | 88 | AGND | AGND | Analog ground |
| 89 | ADC10 | AA13 | ADC10[2] | 90 | ADC11 | U14 | ADC11[2] |
| 91 | AC1 | U9 | CM1[2] | 92 | AGND | AGND | Analog ground |
| 93 | AGND | AGND | Analog ground | 94 | AGND | AGND | Analog ground |
| 95 | DGND | DGND | Digital ground | 96 | DGND | DGND | Digital ground |
| 97 | 3.3V | Power | Power | 98 | 3.3V | Power | Power |
| 99 | 3.3V | Power | Power | 100 | 3.3V | Power | Power |

*Notes:*

1. *Digital signal.*
2. *Analog signal.*

# 4 – Pin List

Below is the pin list applicable to the SmartFusion A2F200M3F-FGG484ES device.

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| A1 | GND1 | GND |
| A2 | NC2 | NC |
| A3 | NC5 | NC |
| A4 | GND7 | GND |
| A5 | EMC_CS0_N/GAB0/IO01NDB0V0 | NC |
| A6 | EMC_CS1_N/GAB1/IO01PDB0V0 | NC |
| A7 | GND8 | GND |
| A8 | EMC_AB[0]/IO04NDB0V0 | NC |
| A9 | EMC_AB[1]/IO04PDB0V0 | NC |
| A10 | GND2 | GND |
| A11 | NC1 | NC |
| A12 | EMC_AB[7]/IO07PDB0V0 | NC |
| A13 | GND3 | GND |
| A14 | EMC_AB[12]/IO10NDB0V0 | NC |
| A15 | EMC_AB[13]/IO10PDB0V0 | NC |
| A16 | GND4 | GND |
| A19 | GND5 | GND |
| A20 | NC3 | NC |
| A21 | NC4 | NC |
| A22 | GND6 | GND |
| AA1 | GPIO_4/IO43RSB4V0 | MSS_GP_IO_4 |
| AA2 | GPIO_12/IO37RSB4V0 | MSS_GP_IO_12 |
| AA3 | MAC_MDC/IO48RSB4V0 | FPGA_ENA_MDC |
| AA4 | MAC_RXER/IO50RSB4V0 | FPGA_ENA_RXER |
| AA5 | MAC_TXD[0]/IO56RSB4V0 | FPGA_ENA_TXD0 |
| AA6 | ABPS0 | V10P |
| AA7 | TM1 | AT1 |
| AA8 | ADC1 | NC |
| AA9 | GND15ADC1 | AGND |
| AA10 | GND33ADC10 | AGND |
| AA11 | CM3 | AC3 |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| AA12 | GNDTM1 | ATGND1 |
| AA13 | ADC10 | NC |
| AA14 | ADC9 | NC |
| AA16 | MAINXIN | AGND (Y1,C48) |
| AA17 | MAINXOUT | AGND (Y1,C50) |
| AA18 | LPXIN | AGND (Y2,C51) |
| AA19 | LPXOUT | AGND (Y2,C52) |
| AA20 | NC6 | NC |
| AA21 | NC7 | NC |
| AA22 | SPI_1_CLK/GPIO_26 | GND |
| AB1 | GND9 | GND |
| AB2 | GPIO_13/IO36RSB4V0 | MSS_GP_IO_13 |
| AB3 | GPIO_14/IO35RSB4V0 | MSS_GP_IO_14 |
| AB4 | GND11 | GND |
| AB5 | PCAP | C49 |
| AB6 | NCAP | C49 |
| AB7 | ABPS3 | AV2_1 |
| AB8 | ADC3 | ADC3 |
| AB9 | GND15ADC0 | AGND |
| AB10 | VCC33ADC1 | V3P3A |
| AB11 | VAREF1 | VAREF_OUT |
| AB12 | TM2 | AT2 |
| AB13 | CM2 | AC2 |
| AB14 | ABPS4 | V3P3 |
| AB15 | GNDAQ1 | AGND |
| AB16 | GNDMAINXTAL | AGND |
| AB17 | GNDLPXTAL | AGND |
| AB18 | VCCLPXTAL | V3P3A |
| AB19 | VDDBAT | GND |
| AB20 | PTBASE | PTBASE |
| AB21 | NC8 | NC |
| AB22 | GND10 | GND |
| B1 | EMC_DB[15]/GAA2/IO71PDB5V0 | NC |
| B2 | GND12 | GND |
| B5 | VCCFPGAIOB0_3 | V3P3_F2 |
| B6 | EMC_RW_N/GAA1/IO00PDB0V0 | NC |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| B8 | VCCFPGAIOB0_4 | V3P3_F2 |
| B9 | EMC_BYTEN[0]/GAC0/IO02NDB0V0 | NC |
| B10 | EMC_AB[2]/IO05NDB0V0 | NC |
| B11 | EMC_AB[3]/IO05PDB0V0 | NC |
| B12 | EMC_AB[6]/IO07NDB0V0 | NC |
| B13 | EMC_AB[14]/IO11NDB0V0 | NC |
| B14 | EMC_AB[15]/IO11PDB0V0 | NC |
| B15 | VCCFPGAIOB0_1 | V3P3_F2 |
| B16 | EMC_AB[18]/IO13NDB0V0 | NC |
| B17 | EMC_AB[19]/IO13PDB0V0 | NC |
| B18 | VCCFPGAIOB0_2 | V3P3_F2 |
| B19 | GBB0/IO18NDB0V0 | LED1_N |
| B20 | GBB1/IO18PDB0V0 | LED2_N |
| B21 | GND13 | GND |
| B22 | GBA2/IO20PDB1V0 | F2-200-IO_6 |
| C1 | EMC_DB[14]/GAB2/IO71NDB5V0 | NC |
| C2 | NC9 | NC |
| C3 | NC11 | NC |
| C6 | EMC_CLK/GAA0/IO00NDB0V0 | NC |
| C9 | EMC_BYTEN[1]/GAC1/IO02PDB0V0 | NC |
| C10 | EMC_OEN1_N/IO03PDB0V0 | NC |
| C11 | GND14 | GND |
| C12 | VCCFPGAIOB0_5 | V3P3_F2 |
| C13 | EMC_AB[8]/IO08NDB0V0 | NC |
| C14 | EMC_AB[16]/IO12NDB0V0 | NC |
| C15 | EMC_AB[17]/IO12PDB0V0 | NC |
| C16 | EMC_AB[24]/IO16NDB0V0 | NC |
| C17 | EMC_AB[22]/IO15NDB0V0 | NC |
| C18 | EMC_AB[23]/IO15PDB0V0 | NC |
| C19 | GBA0/IO19NPB0V0 | LED3_N |
| C20 | NC10 | NC |
| C21 | GBC2/IO21PDB1V0 | LED6_N |
| C22 | GBB2/IO20NDB1V0 | F2-200-IO_7 |
| D1 | GND15 | GND |
| D2 | EMC_DB[12]/IO70NDB5V0 | NC |
| D3 | EMC_DB[13]/GAC2/IO70PDB5V0 | NC |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| D4 | NC14 | NC |
| D5 | NC15 | NC |
| D6 | GND19 | GND |
| D9 | GND20 | GND |
| D10 | EMC_OEN0_N/IO03NDB0V0 | NC |
| D11 | EMC_AB[10]/IO09NDB0V0 | NC |
| D12 | EMC_AB[11]/IO09PDB0V0 | NC |
| D13 | EMC_AB[9]/IO08PDB0V0 | NC |
| D14 | GND16 | GND |
| D15 | GBC1/IO17PPB0V0 | OLED_D/C# |
| D16 | EMC_AB[25]/IO16PDB0V0 | NC |
| D17 | GND17 | GND |
| D18 | GBA1/IO19PPB0V0 | NC |
| D19 | NC12 | NC |
| D20 | NC13 | NC |
| D21 | IO21NDB1V0 | LED7_N |
| D22 | GND18 | GND |
| E1 | GFC2/IO67PPB5V0 | NC |
| E2 | VCCFPGAIOB5_1 | V3P3_F2 |
| E3 | GFA2/IO68PDB5V0 | F2-200-IO_0 |
| E4 | GND22 | GND |
| E5 | NC18 | NC |
| E6 | GNDQ1 | GND |
| E7 | VCCFPGAIOB0_12 | V3P3_F2 |
| E9 | NC19 | NC |
| E10 | VCCFPGAIOB0_6 | V3P3_F2 |
| E11 | EMC_AB[4]/IO06NDB0V0 | NC |
| E12 | EMC_AB[5]/IO06PDB0V0 | NC |
| E13 | VCCFPGAIOB0_13 | V3P3_F2 |
| E14 | GBC0/IO17NPB0V0 | NC |
| E15 | NC16 | NC |
| E16 | VCCFPGAIOB0_7 | V3P3_F2 |
| E17 | VCOMPLA1 | NC |
| E19 | GND21 | GND |
| E20 | NC17 | NC |
| E21 | VCCFPGAIOB1_1 | V3P3_F2 |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| E22 | IO22NDB1V0 | F2-200-PWM0 |
| F1 | GFB1/IO65PPB5V0 | F2-200-IO_8 |
| F2 | IO67NPB5V0 | RMII_50MHZ_CLK |
| F3 | GFB2/IO68NDB5V0 | F2-200-IO_1 |
| F4 | EMC_DB[10]/IO69NPB5V0 | NC |
| F5 | VCCFPGAIOB5_2 | V3P3_F2 |
| F6 | VCCPLLA | V1P5_DUT (VCCPLA) |
| F7 | VCOMPLA | GND |
| F8 | NC23 | NC |
| F9 | NC24 | NC |
| F10 | NC20 | NC |
| F11 | NC21 | NC |
| F12 | NC22 | NC |
| F13 | EMC_AB[20]/IO14NDB0V0 | NC |
| F14 | EMC_AB[21]/IO14PDB0V0 | NC |
| F15 | GNDQ2 | GND |
| F16 | VCCPLA | NC |
| F18 | VCCFPGAIOB1_2 | V3P3_F2 |
| F19 | IO23NDB1V0 | NC |
| F22 | IO22PDB1V0 | F2-200-PWM1 |
| G1 | GND23 | GND |
| G2 | GFB0/IO65NPB5V0 | NC |
| G3 | EMC_DB[9]/GEC1/IO63PDB5V0 | NC |
| G4 | GFC1/IO66PPB5V0 | F2-200-IO_2 |
| G5 | EMC_DB[11]/IO69PPB5V0 | NC |
| G6 | GNDQ4 | GND |
| G7 | NC25 | NC |
| G8 | GND28 | GND |
| G9 | VCCFPGAIOB0_11 | V3P3_F2 |
| G10 | GND24 | GND |
| G11 | VCCFPGAIOB0_8 | V3P3_F2 |
| G12 | GND25 | GND |
| G13 | VCCFPGAIOB0_9 | V3P3_F2 |
| G14 | GND26 | GND |
| G15 | VCCFPGAIOB0_10 | V3P3_F2 |
| G16 | GNDQ3 | GND |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| G19 | GCA2/IO23PDB1V0 | SWITCH1 |
| G20 | IO24NDB1V0 | SWITCH2 |
| G21 | GCB2/IO24PDB1V0 | LED8_N |
| G22 | GND27 | GND |
| H1 | EMC_DB[7]/GEB1/IO62PDB5V0 | NC |
| H2 | VCCFPGAIOB5_3 | V3P3_F2 |
| H3 | EMC_DB[8]/GEC0/IO63NDB5V0 | NC |
| H4 | GND33 | GND |
| H5 | GFC0/IO66NPB5V0 | F2-200-IO_3 |
| H6 | GFA1/IO64PDB5V0 | F2-200-IO_4 |
| H7 | GND34 | GND |
| H8 | VCC4 | V1P5_DUT |
| H9 | GND35 | GND |
| H10 | VCC1 | V1P5_DUT |
| H11 | GND29 | GND |
| H12 | VCC2 | V1P5_DUT |
| H13 | GND30 | GND |
| H14 | VCC3 | V1P5_DUT |
| H15 | GND31 | GND |
| H16 | VCCFPGAIOB1_3 | V3P3_F2 |
| H17 | IO25NDB1V0 | LED4_N |
| H18 | GCC2/IO25PDB1V0 | NC |
| H19 | GND32 | GND |
| H20 | GCC0/IO26NPB1V0 | LED5_N |
| H21 | VCCFPGAIOB1_4 | V3P3_F2 |
| H22 | GCB0/IO27NDB1V0 | NC |
| J1 | EMC_DB[6]/GEB0/IO62NDB5V0 | NC |
| J2 | EMC_DB[5]/GEA1/IO61PDB5V0 | NC |
| J3 | EMC_DB[4]/GEA0/IO61NDB5V0 | NC |
| J4 | EMC_DB[3]/GEC2/IO60PPB5V0 | NC |
| J5 | VCCFPGAIOB5_4 | V3P3_F2 |
| J6 | GFA0/IO64NDB5V0 | F2-200-IO_5 |
| J7 | VCCFPGAIOB5_5 | V3P3_F2 |
| J8 | GND40 | GND |
| J9 | VCC8 | V1P5_DUT |
| J10 | GND36 | GND |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| J11 | VCC5 | V1P5_DUT |
| J12 | GND37 | GND |
| J13 | VCC6 | V1P5_DUT |
| J14 | GND38 | GND |
| J15 | VCC7 | V1P5_DUT |
| J16 | GND39 | GND |
| J18 | VCCFPGAIOB1_5 | V3P3_F2 |
| J19 | GCA0/IO28NDB1V0 | J22.1 |
| J20 | GCA1/IO28PDB1V0 | J22.2 |
| J21 | GCC1/IO26PPB1V0 | J22.3 |
| J22 | GCB1/IO27PDB1V0 | J22.4 |
| K1 | GND41 | GND |
| K2 | EMC_DB[0]/GEA2/IO59NDB5V0 | NC |
| K3 | EMC_DB[1]/GEB2/IO59PDB5V0 | NC |
| K5 | EMC_DB[2]/IO60NPB5V0 | NC |
| K7 | GND46 | GND |
| K8 | VCC12 | V1P5_DUT |
| K9 | GND47 | GND |
| K10 | VCC9 | V1P5_DUT |
| K11 | GND42 | GND |
| K12 | VCC10 | V1P5_DUT |
| K13 | GND43 | GND |
| K14 | VCC11 | V1P5_DUT |
| K15 | GND44 | GND |
| K16 | VCCFPGAIOB1_6 | V3P3_F2 |
| K18 | GDA1/IO31PDB1V0 | NC |
| K19 | GDA0/IO31NDB1V0 | J22.5 |
| K20 | GDC1/IO29PDB1V0 | NC |
| K21 | GDC0/IO29NDB1V0 | NC |
| K22 | GND45 | GND |
| L4 | GND52 | GND |
| L7 | VCCFPGAIOB5_10 | V3P3_F2 |
| L8 | GND53 | GND |
| L9 | VCC16 | V1P5_DUT |
| L10 | GND48 | GND |
| L11 | VCC13 | V1P5_DUT |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| L12 | GND49 | GND |
| L13 | VCC14 | V1P5_DUT |
| L14 | GND50 | GND |
| L15 | VCC15 | V1P5_DUT |
| L16 | GND51 | GND |
| L17 | GNDQ5 | GND |
| L18 | GDA2/IO33NDB1V0 | NC |
| L19 | VCCFPGAIOB1_7 | V3P3_F2 |
| L20 | GDB1/IO30PDB1V0 | NC |
| L21 | GDB0/IO30NDB1V0 | NC |
| L22 | GDC2/IO32PDB1V0 | NC |
| M3 | VCCFPGAIOB5_6 | V3P3_F2 |
| M5 | GNDQ6 | GND |
| M7 | GND58 | GND |
| M8 | VCC20 | V1P5_DUT |
| M9 | GND59 | GND |
| M10 | VCC17 | V1P5_DUT |
| M11 | GND54 | GND |
| M12 | VCC18 | V1P5_DUT |
| M13 | GND55 | GND |
| M14 | VCC19 | V1P5_DUT |
| M15 | GND56 | GND |
| M16 | VCCFPGAIOB1_8 | V3P3_F2 |
| M17 | NC26 | NC |
| M18 | GDB2/IO33PDB1V0 | NC |
| M19 | VJTAG | VJTAG |
| M20 | GND57 | GND |
| M21 | VPP | VPUMP |
| M22 | IO32NDB1V0 | NC |
| N1 | GND60 | GND |
| N5 | VCCFPGAIOB5_7 | V3P3_F2 |
| N7 | VCCFPGAIOB5_8 | V3P3_F2 |
| N8 | GND65 | GND |
| N9 | VCC24 | V1P5_DUT |
| N10 | GND61 | GND |
| N11 | VCC21 | V1P5_DUT |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| N12 | GND62 | GND |
| N13 | VCC22 | V1P5_DUT |
| N14 | GND63 | GND |
| N15 | VCC23 | V1P5_DUT |
| N17 | NC27 | NC |
| N18 | VCCFPGAIOB1_9 | V3P3_F2 |
| N20 | GNDENVM | GND |
| N21 | NC28 | NC |
| N22 | GND64 | GND |
| P3 | GNDRCOSC | GND |
| P4 | GND70 | GND |
| P5 | NC29 | NC |
| P6 | NC30 | NC |
| P7 | GND71 | GND |
| P8 | VCC28 | V1P5_DUT |
| P9 | GND72 | GND |
| P10 | VCC25 | V1P5_DUT |
| P11 | GND66 | GND |
| P12 | VCC26 | V1P5_DUT |
| P13 | GND67 | GND |
| P14 | VCC27 | V1P5_DUT |
| P15 | GND68 | GND |
| P16 | VCCFPGAIOB1_10 | V3P3_F2 |
| P17 | TDI | TDI |
| P18 | TCK | F2_TCK |
| P19 | GND69 | GND |
| P20 | TMS | F2_TMS |
| P21 | TDO | F2_TDO |
| P22 | TRSTB | TRST |
| R1 | MSS_RESET_N | MSS_RESET_N |
| R2 | VCCFPGAIOB5_9 | V3P3_F2 |
| R3 | GPIO_1/IO46RSB4V0 | MSS_GP_IO_1 |
| R4 | NC35 | NC |
| R5 | NC36 | NC |
| R6 | NC37 | NC |
| R7 | NC38 | NC |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| R8 | GND76 | GND |
| R9 | VCC32 | V1P5_DUT |
| R10 | GND73 | GND |
| R11 | VCC29 | V1P5_DUT |
| R12 | GND74 | GND |
| R13 | VCC30 | V1P5_DUT |
| R14 | GND75 | GND |
| R15 | VCC31 | V1P5_DUT |
| R16 | JTAGSEL | JTAG_SEL |
| R17 | NC31 | NC |
| R18 | NC32 | NC |
| R19 | NC33 | NC |
| R21 | VCCFPGAIOB1_11 | V3P3_F2 |
| R22 | NC34 | NC |
| T1 | GND77 | GND |
| T3 | GPIO_8/IO39RSB4V0 | MSS_GP_IO_8 |
| T4 | GPIO_11/IO57RSB4V0 | MSS_GP_IO_11 |
| T5 | GND80 | GND |
| T6 | MAC_CLK | GND |
| T8 | VCC33SDD0 | V3P3A |
| T9 | VCC15A | V1P5A |
| T10 | GNDAQ0 | AGND |
| T11 | GND33ADC01 | AGND |
| T12 | ADC7 | ADC7 |
| T13 | AT4 | NC |
| T14 | VAREF2 | NC |
| T15 | VAREFOUT | VAREF_OUT |
| T17 | SPI_1_DO/GPIO_24 | NC |
| T18 | GND78 | GND |
| T22 | GND79 | GND |
| U1 | GND81 | GND |
| U2 | GPIO_5/IO42RSB4V0 | MSS_GP_IO_5 |
| U3 | GPIO_10/IO58RSB4V0 | MSS_GP_IO_10 |
| U5 | MAC_RXD[1]/IO53RSB4V0 | FPGA_ENA_RXD1 |
| U6 | NC39 | NC |
| U7 | VCC33AP | V3P3A |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| U8 | VCC33N | AGND |
| U9 | CM1 | AC1 |
| U10 | VAREF0 | VAREF_OUT |
| U11 | GND33ADC11 | AGND |
| U12 | ADC4 | ADC4 |
| U13 | ATGND_02 | NC |
| U14 | ADC11 | NC |
| U15 | GNDVAREF | AGND |
| U16 | VCC33SDD1 | V3P3A |
| U17 | SPI_0_DO/GPIO_16 | SPI_SI |
| U18 | UART_0_RXD/GPIO_21 | RXD_0_IN |
| U20 | I2C_1_SCL/GPIO_31 | NC |
| U21 | I2C_0_SCL/GPIO_23 | OLED_SCL |
| U22 | GND82 | GND |
| V1 | GPIO_0/IO47RSB4V0 | MSS_GP_IO_0 |
| V2 | GPIO_6/IO41RSB4V0 | MSS_GP_IO_6 |
| V3 | GPIO_9/IO38RSB4V0/ADC3 | MSS_GP_IO_9 |
| V4 | MAC_MDIO/IO49RSB4V0 | FPGA_ENA_MDIO |
| V5 | MAC_RXD[0]/IO54RSB4V0 | FPGA_ENA_RXD0 |
| V6 | GND84 | GND |
| V7 | SDD0 | DACOUT0 |
| V8 | ABPS1 | V1P5 |
| V9 | ADC2 | ADC2 |
| V10 | VCC33ADC0 | V3P3A |
| V11 | ADC6 | ADC6 |
| V12 | ADC5 | ADC5 |
| V13 | ABPS5 | AV2_2 |
| V14 | ADC8 | NC |
| V16 | NC40 | NC |
| V17 | GND83 | GND |
| V18 | SPI_0_DI/GPIO_17 | SPI_SO |
| V19 | SPI_1_DI/GPIO_25 | NC |
| V20 | UART_1_TXD/GPIO_28 | NC |
| V21 | I2C_0_SDA/GPIO_22 | OLED_SDA |
| V22 | I2C_1_SDA/GPIO_30 | NC |
| W1 | GPIO_2/IO45RSB4V0 | MSS_GP_IO_2 |

| A2F200 Pin Number | A2F200 Pin Name | Board Signal Name |
|---|---|---|
| W2 | GPIO_7/IO40RSB4V0 | MSS_GP_IO_7 |
| W3 | GND86 | GND |
| W4 | MAC_CRSDV/IO51RSB4V0 | FPGA_ENA_CRS |
| W5 | MAC_TXD[1]/IO55RSB4V0 | FPGA_ENA_TXD1 |
| W6 | NC41 | NC |
| W7 | GNDA0 | AGND |
| W8 | TM0 | AT0 |
| W9 | ABPS2 | AV1_1 |
| W10 | GND33ADC02 | AGND |
| W11 | VCC15ADC1 | V1P5A |
| W12 | ABPS6 | AV1_3 |
| W13 | AC4 | NC |
| W14 | AV2_4 | NC |
| W16 | GNDA1 | AGND |
| W17 | PU_N | RTC_SW |
| W18 | GNDSDD1 | AGND |
| W19 | SPI_0_CLK/GPIO_18 | SPI_SCK |
| W20 | GND85 | GND |
| W21 | SPI_1_SS/GPIO_27 | NC |
| W22 | UART_1_RXD/GPIO_29 | NC |
| Y1 | GPIO_3/IO44RSB4V0 | MSS_GP_IO_3 |
| Y3 | GPIO_15/IO34RSB4V0 | MSS_GP_IO_15 |
| Y4 | MAC_TXEN/IO52RSB4V0 | FPGA_ENA_TXEN |
| Y7 | CM0 | AC0 |
| Y8 | GNDTM0 | ATGND0 |
| Y9 | ADC0 | ADC0 |
| Y10 | VCC15ADC0 | V1P5A |
| Y11 | ABPS7 | AV2_3 |
| Y12 | TM3 | AT3 |
| Y13 | AV1_4 | NC |
| Y16 | VCCMAINXTAL | V3P3A |
| Y17 | SDD1 | DACOUT1 |
| Y18 | PTEM | V1P5_INT |
| Y19 | VCC33A | V3P3A |
| Y20 | SPI_0_SS/GPIO_19 | SPI_CS_N |
| Y22 | UART_0_TXD/GPIO_20 | TXD_0_OUT |

# 5 – Board Stackup

## Board Stack-Up

The SmartFusion Evaluation Kit board is built on a 6-layer printed circuit board (PCB). The silkscreen is provided in Figure 2 on page 44. The full PCB design layout is provided on the SmartFusion Evaulation Kit page of the Actel website:

www.actel.com/products/hardware/devkits_boards/smartfusion_eval.aspx.

To view the PCB design layout files, you can use Allegro Free Physical Viewer, which can be downloaded from the Cadence website Allegro Download page:

www.cadence.com/products/pcb/Pages/Downloads.aspx.

The layers are arranged in the following order:

Layer1: Top Signal

Layer2: GND1

Layer3: PWR1

Layer4: PWR2

Layer5: GND2

Layer6: Bottom Signal

Figure 1 shows the stack-up:

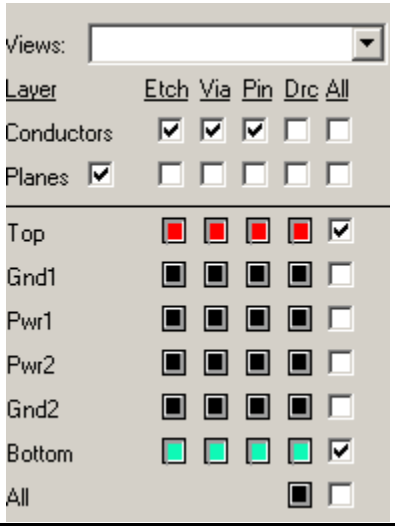



***Figure 1* • A2F-EVAL-KIT PCB Layer Stack up**

Figure 2 shows the silkscreen top view.

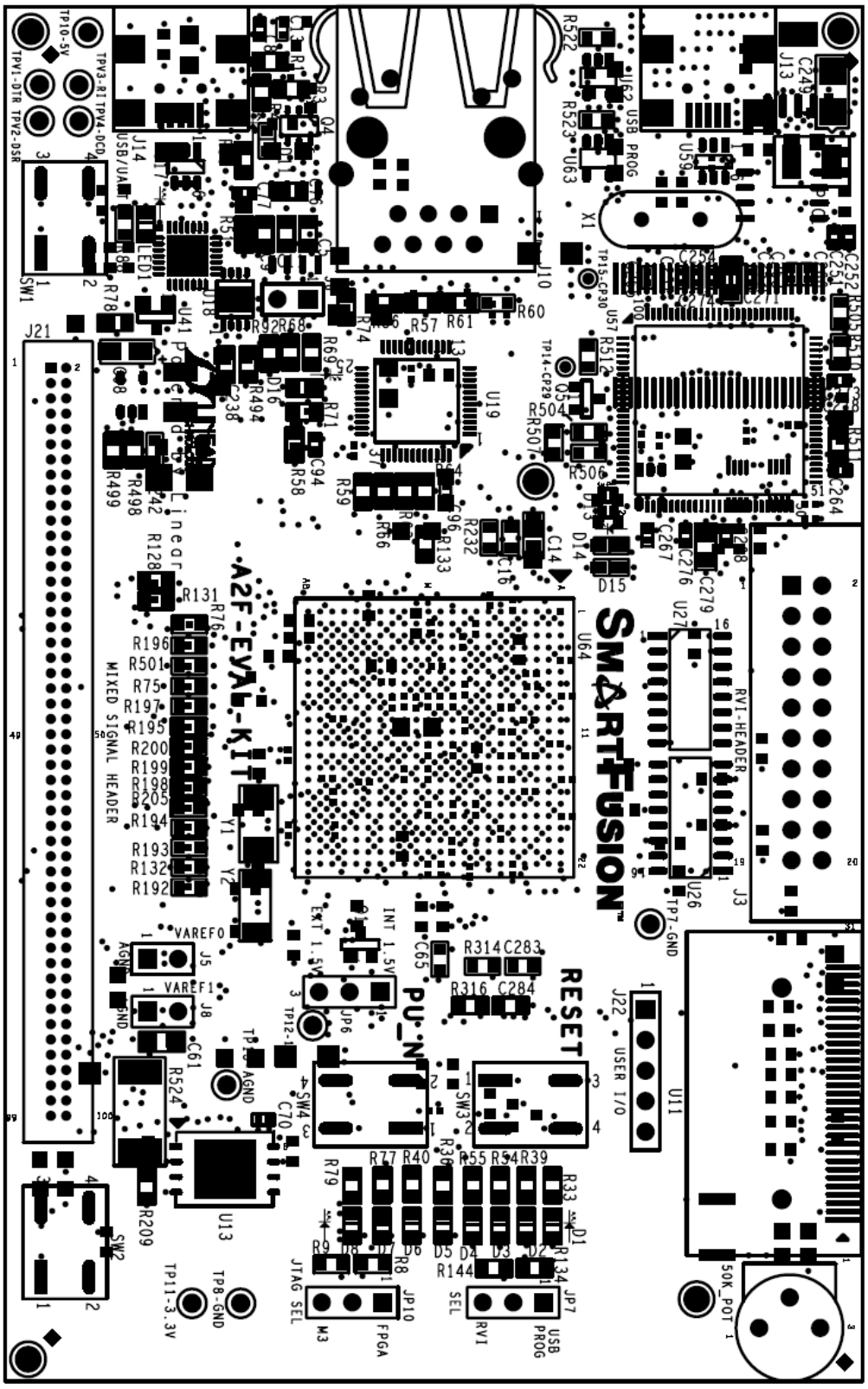



***Figure 2* • A2F-EVAL-KIT Top Silk-Screen**

# 6 – Demo Design

This chapter describes how to run the Webserver demo design on the SmartFusion Evaluation Kit. The SmartFusion Evaluation Kit comes with a preloaded Webserver demo design. If the board is not preprogrammed, the programming file and the source files for the demo are provided on the SmartFusion Evaluation Kit page:

www.actel.com/products/hardware/devkits_boards/smartfusion_eval.aspx.

The programming file for the demo is provided as a standalone zip file under the SmartFusion Evaluation Kit Quickstart Card. The source files are provided with the SmartFusion Webserver Demo Using uIP and FreeRTOS User's Guide.

## Jumper Settings for Demo Design

Prior to powering up the A2F-EVAL-KIT for the first time, make sure the jumpers are set as shown in the Table 1.

***Table 1 •*** **Manufacturing Test Jumper Settings**

| Jumper | Location | Settings |
|---|---|---|
| J6 | 2 pins next to the Ethernet jack | 1–2 |
| JP6 | Next to the PUB switch | 2-3 |
| JP7 | Below the POT | 1–2 |
| JP10 | Below JP7 | 1–2 |

## Running the Demo Design

Connect one end of the USB mini B cable to the USB connection, J14 (labeled as USB2) on the A2F-EVAL-KIT board. Connect the other end of the USB cable to the PC you will use for testing. The board receives power from USB. LED1 lights up, indicating the board is powered up. The D11 LED also lights up, indicating UART link establishment. Connect an Ethernet cable from the local area network to J10, the A2F-EVAL-KIT Ethernet jack.

This demo provides you the flexibility to select demo options using switches or serial terminal emulation programs like HyperTermianl or PuTTy. With a USB driver properly installed, and correct COM port and communication settings selected, you can use the serial terminal emulation program to communicate with a design running on SmartFusion FPGA device.

Configure the serial terminal emulation program which is available on your PC with the following settings:

- Bits per second: 57600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Refer to the Configuring Serial Terminal Emulation Programs Tutorial for configuring the HyperTerminal, Tera Term, or PuTTY.

Press switch SW3 (RESET) to start the demo. If the board is programmed correctly, a welcome message is displayed on the OLED as shown in Figure 1 on page 46.


***Figure 1* • SmartFusion Welcome display on OLED**

The OLED then displays the SmartFusion Menu as shown in Figure 2.


***Figure 2* • SmartFusion Menu Display on OLED**

If you cannot see the display on OLED, recheck the jumper settings, and if required, program the SmartFusion device with the provided programming file.

The message on OLED (see Figure 2) indicates that you can either press switch SW1 on the kit to select Multimeter mode, or press switch SW2 to scroll the menu on OLED.

The serial terminal emulation program displays a welcome message and the SmartFusion Play Menu for user selection as shown in Figure 3. Use the keyboard to press '0' to select the Multimeter mode, '1' to select Webserver mode, or '2' to select LED Test. .

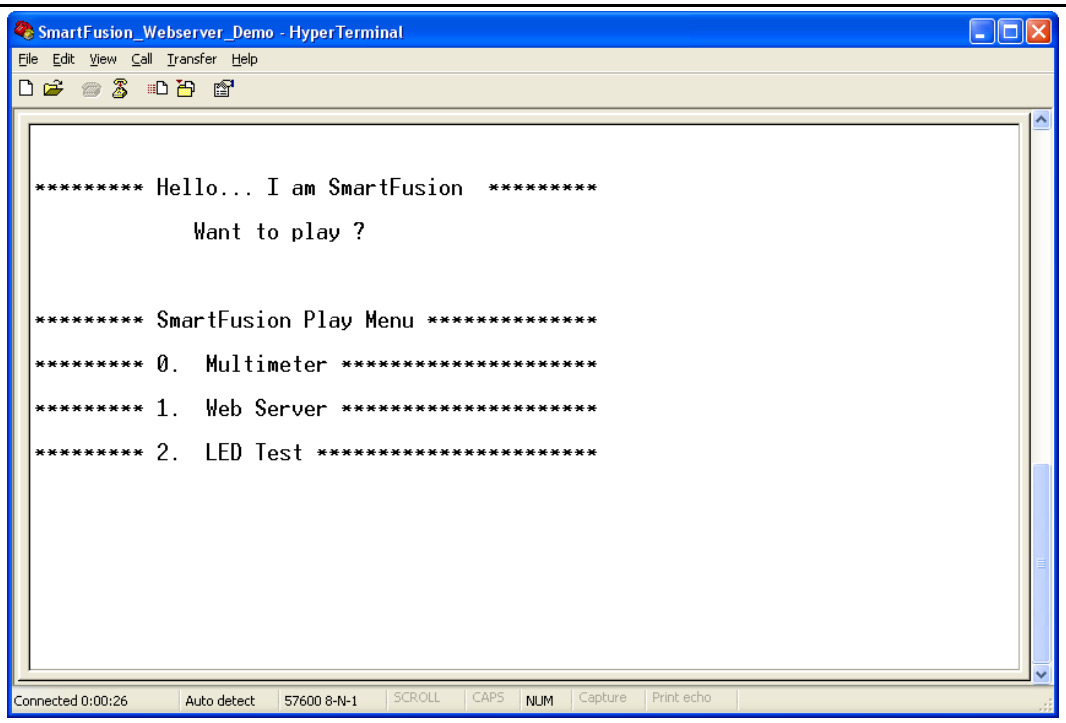



***Figure 3* • Serial Terminal Emulation Program (HyperTerminal) Window**

# Multimeter Mode

Press switch SW1 to select the Multimeter mode. OLED displays the values of the POT voltage, POT current, and external temperature read by the analog computing engine (ACE) of SmartFusion. Rotate the POT provided on the SmartFusion Evaluation board to observe the change in the POT values displayed on the OLED. Press SW1 to go back to the main menu.

The same Multimeter mode can be selected by pressing '0' in serial terminal emulation program. This displays the values of the POT voltage, POT current, and external temperature on the serial terminal emulation program like HyperTerminal.

# Webserver Mode

Press switch SW2 to scroll the menu and then press switch SW1 to select the Webserver mode. This displays the IP address captured by DHCP from the network on OLED and the serial terminal emulation program.

The Webserver mode can also be selected by pressing '1' in the serial terminal emulation program.

Note: To capture the dynamic IP from network, the local area network must be running a DHCP server that assigns an IP address to the Webserver on the board. The network firewalls must not block the board webserver.

Enter the captured IP address in the Internet Explorer address bar and press **Enter** to browse the Webserver utility. Figure 4 shows the SmartFusion Webserver home page.

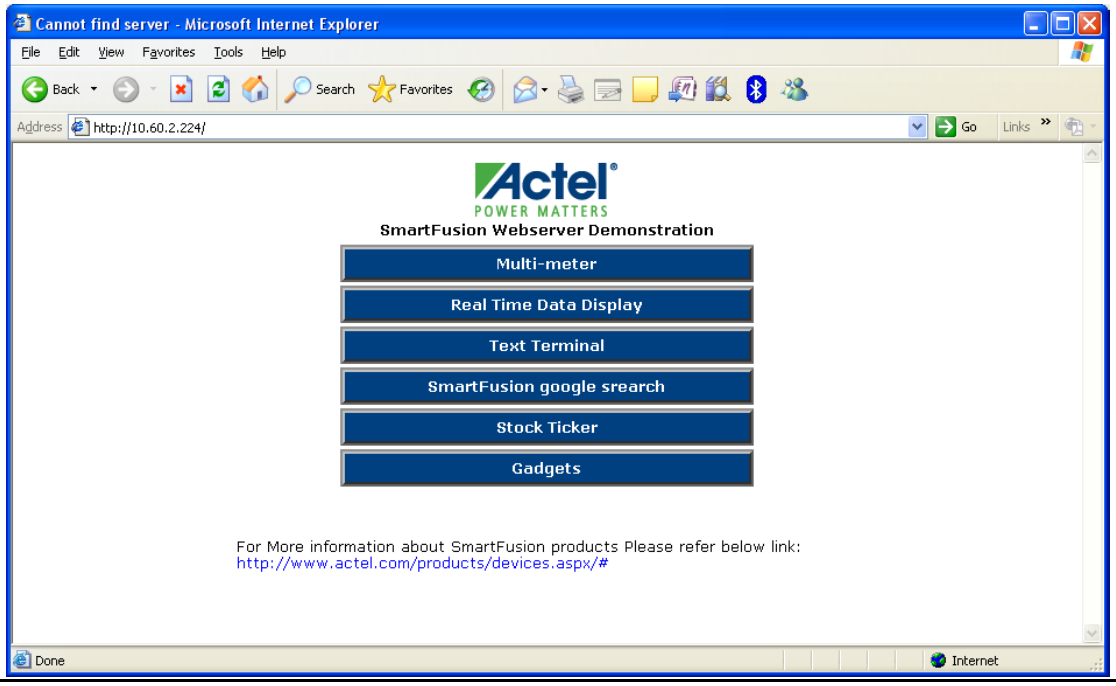



***Figure 4* • SmartFusion Webserver Home page**

Note: Internet Explorer version 6.0 should be used to run the Webserver utility with proper web page visibility. Also the PC Ethernet card link speed should be in Auto Detect mode or fixed to 100 Mbps speed.

# Real Time Data Display

Select **Real Time Data Display** on the Webserver home page. It displays the voltage, current, and temperature values in real time. The web page refreshes periodically, and displays the updated values of voltage, current, and temperature. Vary the potentiometer on the board and observe the change in the voltage and current values. Click the **Home** button to go back to Home page. Figure 5 shows the SmartFusion Webserver Real Time Display web page.

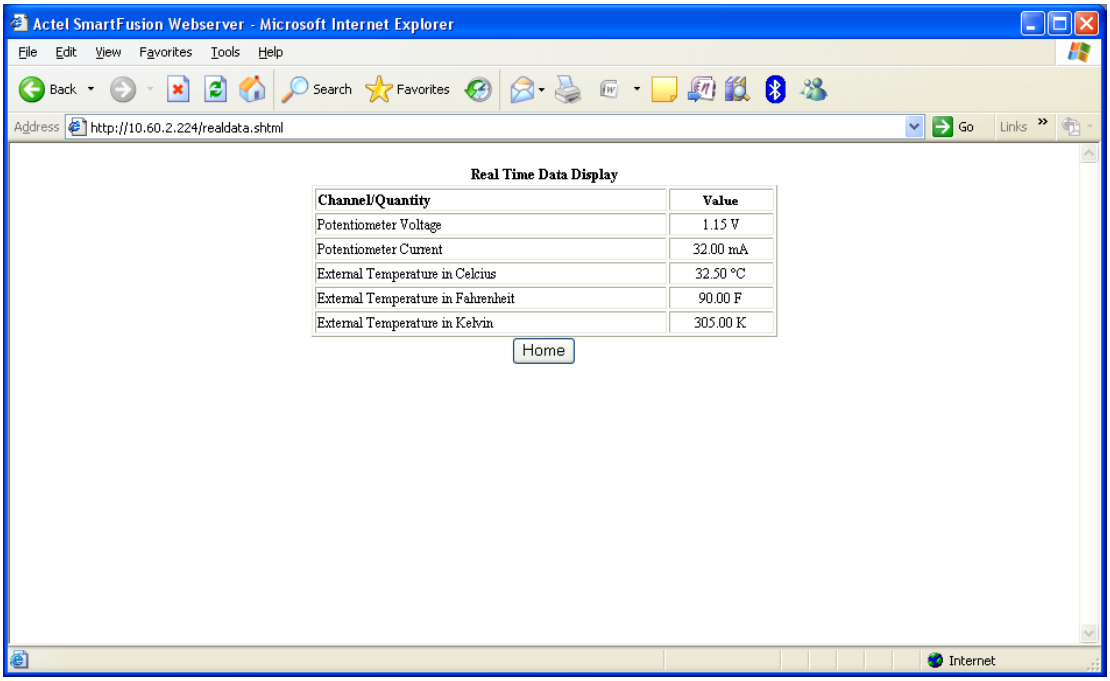



***Figure 5* • SmartFusion Webserver Real Time Display Web Page**

# LED Test

Press switch SW2 to scroll the menu and then press SW1 to select LED test. Observe the blinking of LEDs available on the SmartFusion Evaluation Kit.

Refer to the SmartFusion Webserver Demo Using uIP and FreeRTOS User's Guide for step by step procedure to run the demo and for complete features of webserver demo.

# 7 – Manufacturing Test

## A2F-EVAL-KIT Board Testing Procedures

This chapter defines and describes the specific A2F-EVAL-KIT board testing procedures. Instructions for running the ACTEL A2F-EVAL-KIT board tests and the steps needed to set up the test environment are outlined in the following sections.

Associated files for this procedure can be downloaded from the Actel website: www.actel.com/download/rsc/?f=A2F_EVAL_KIT_Mfg_PF.

### Jumper Settings for the Board Test

Table 1 lists all the jumpers that need to be set on the board for performing the tests. In case any of the tests in the following section do not work as expected, double-check Table 1.

***Table 1 •*** **Manufacturing Test Jumper Settings**

| Jumper | Pin (From) | Pin (To) |
|---|---|---|
| JP6 | 2 | 3 |
| JP7 | 1 | 2 |
| JP10 | 1 | 2 |

### Installing the A2F-EVAL-KIT Board USB Serial Driver

1. Download and extract all the files stored in the CP210x_driver.zip archive from the Actel website.
2. Double-click on the file named **CP210x_VCP_Win2K_XP_S2K3.exe**.
3. Choose the Install option in the Install Wizard and select **Yes** for the licensing agreement.
4. Restart the computer on which the driver was installed. After restart, the driver can be used to communicate with A2F-EVAL-KIT board.

### Hooking up the Board and UART Cable

Connect one end of USB mini B cable to the USB connection, J14 (labeled as USB2 in Figure 1 on page 50) on the A2F-EVAL-KIT board. Connect the other end of the USB cable to the PC you will use for testing.

The board receives power from USB. LED1 lights up, indicating the board is powered up. The D11 LED also lights up, indicating UART link establishment.

## Hooking Up the Board and Ethernet Cable

Connect an Ethernet cable from the local area network to J10, the A2F-EVAL-KIT Ethernet jack.

Note: For the board Ethernet test to pass, the local network must be running a DHCP server that assigns an IP address to the web server on the board. Network firewalls must not block the web server.

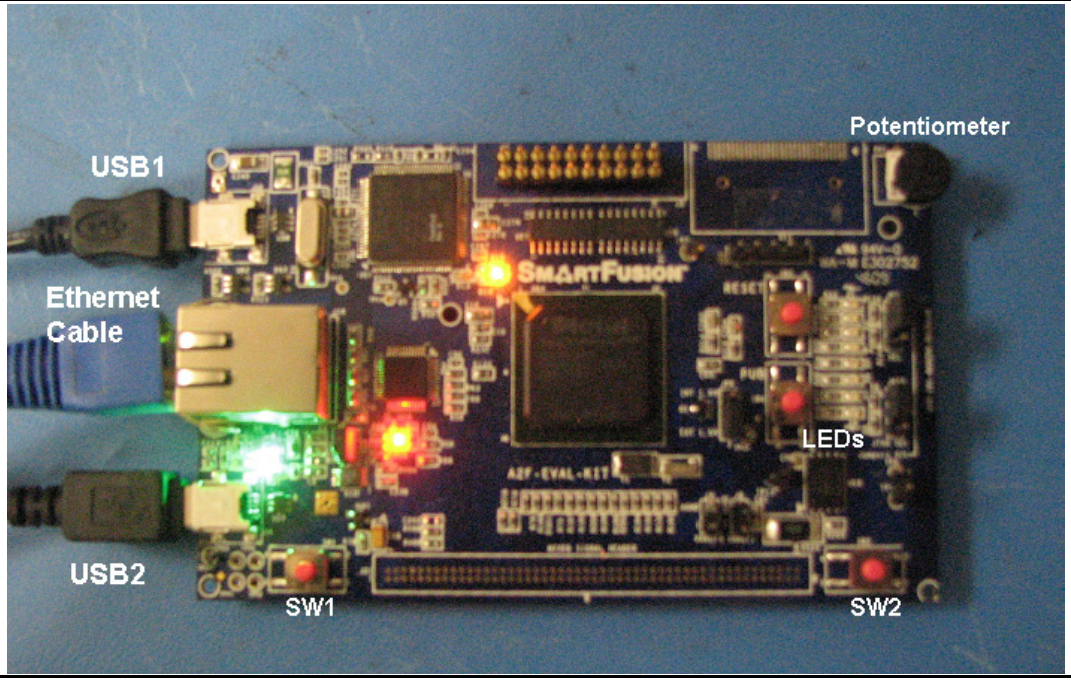



***Figure 1* • Board Manufacturing Test Setup**

## Hooking up the A2F-EVAL-KIT Board Built-in Programmer to PC

Connect the second mini USB cable to connection J13 on the board (labeled USB1 in Figure 1). Plug in the second side of the cable to the PC USB port. This establishes connection to the built-in programming circuit (FlashPro3) on the board, programming the A2F-EVAL-KIT board (SmartFusion device).

1. Open the FlashPro programming software (Figure 2).

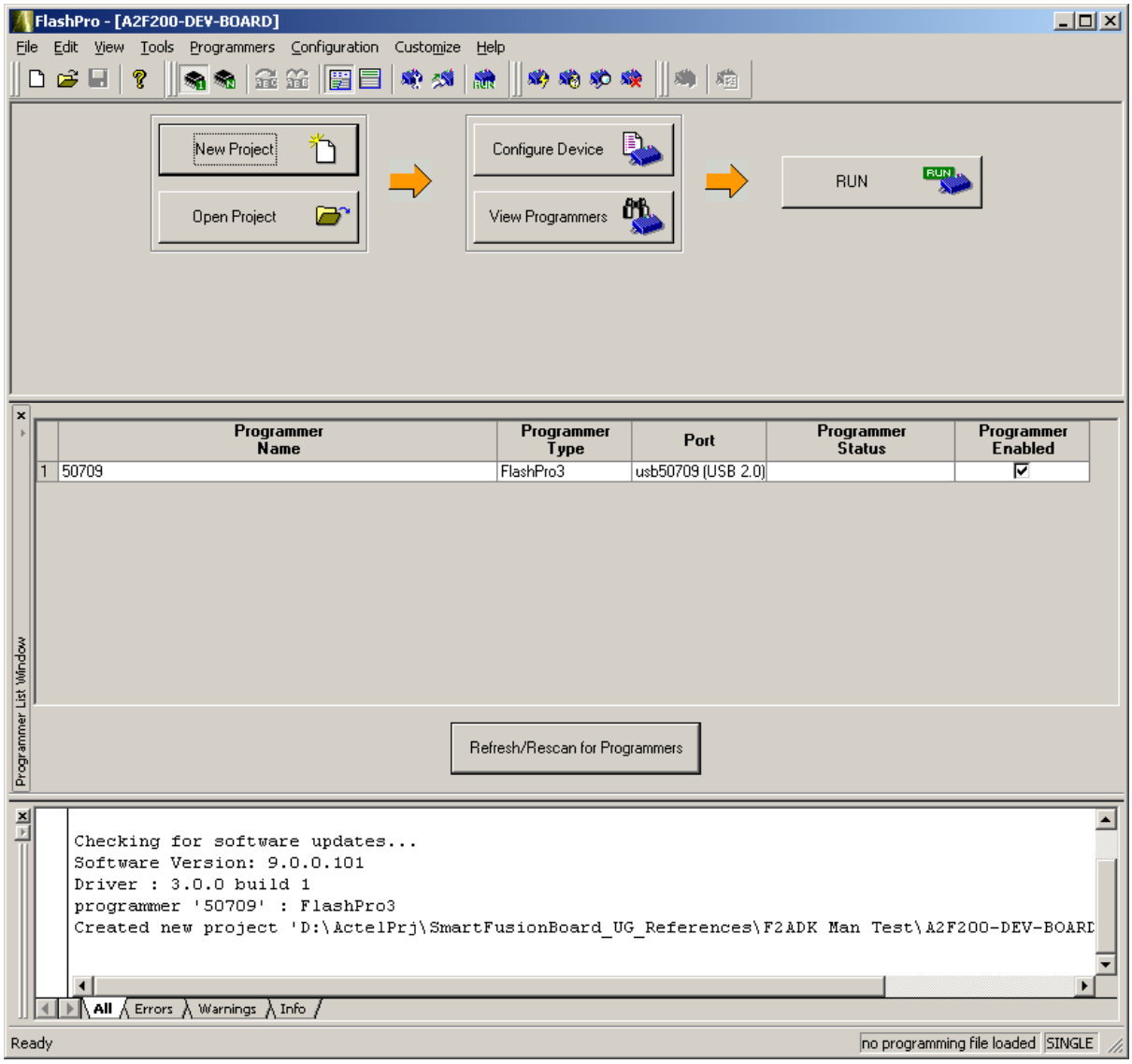



***Figure 2* • FlashPro New Project Setup**

2. Create a new programming project (Figure 3).

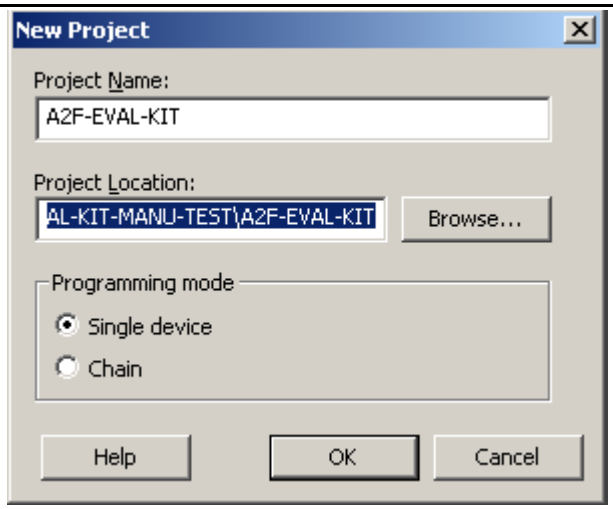



***Figure 3* • New Project Creation**

3. Select the option **Single Device** when choosing the programming mode
4. Click the **Configure Programmer** button. This makes the **Load Existing Programming File** button available.
5. Browse the PC file system to find the A2F-EVAL-KIT.stp programming file. Click **Open** to select the A2F-EVAL-KIT.stp file (Figure 4).

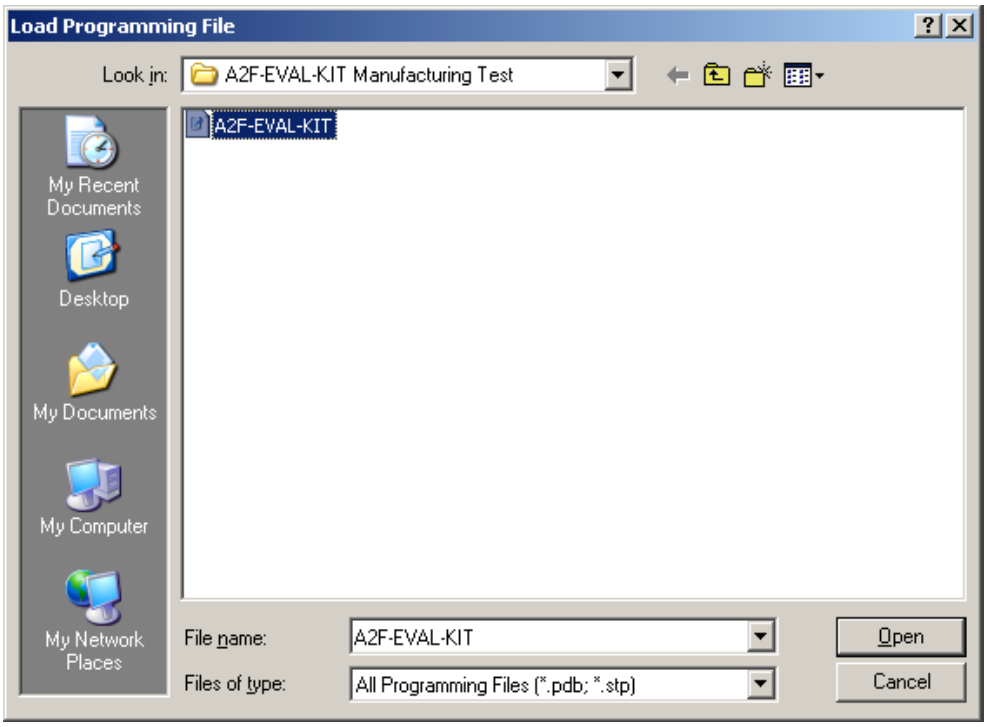



***Figure 4* • Selecting Manufacturing Test STAPL File**

6. Click the **Program** button to program the A2F-EVAL-KIT board.

## Setting Up the Test Terminal

1. Open the Windows start menu. Select **All** > **Programs** > **Accessories** > **Communications** and select the HyperTerminal program (Figure 5). This opens HyperTerminal.

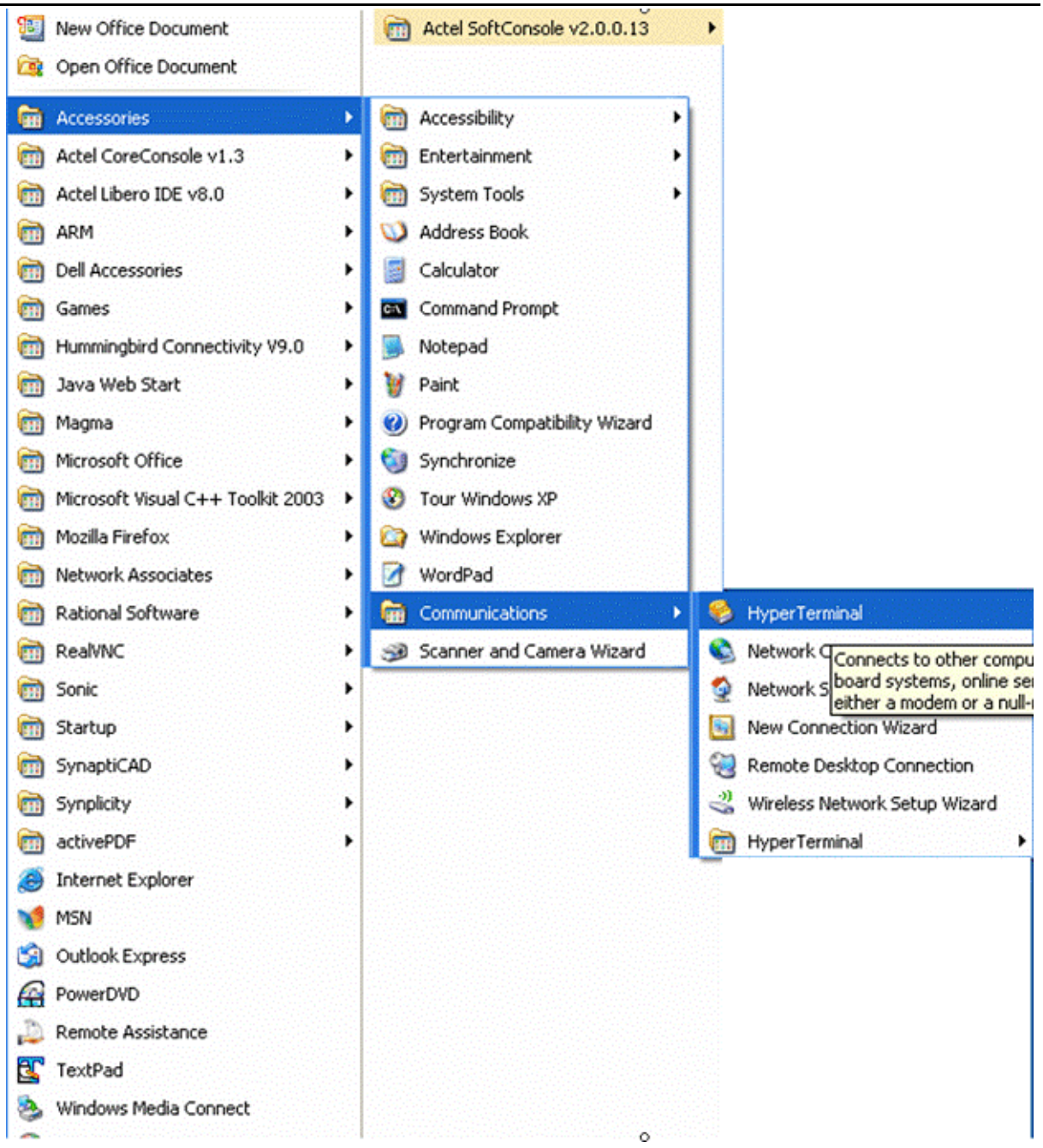



***Figure 5* • HyperTerminal Program Setup**

The Connection Description window is displayed (Figure 6). Type in **A2F-EVAL-KIT** as the name of the new HyperTerminal session and click the **OK**.

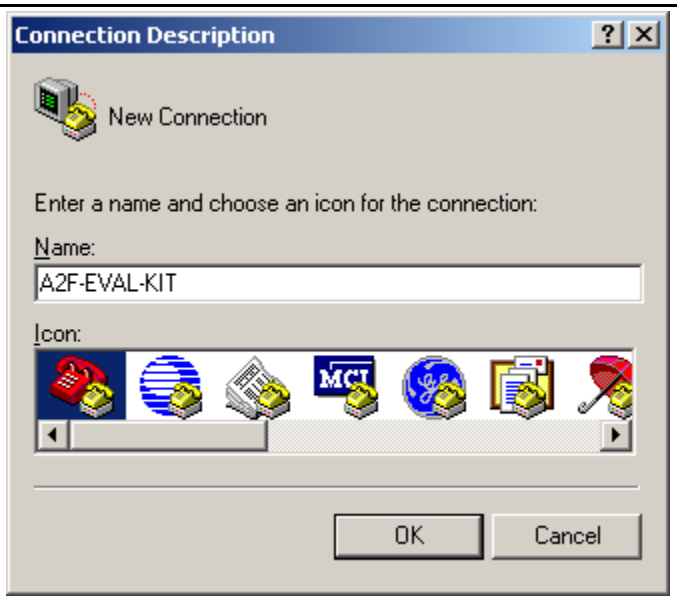



***Figure 6* • HyperTerminal Setup**

2. The Connect To window is displayed. Select the COM4 serial connection (Figure 7).

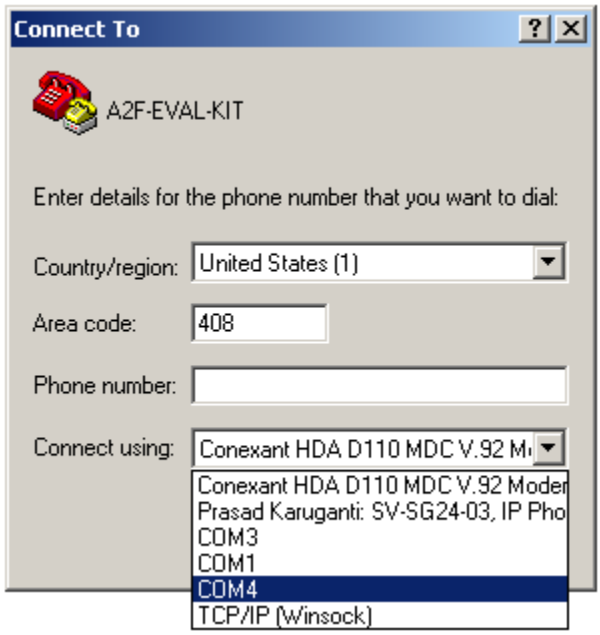



***Figure 7* • HyperTerminal Port Selection**

3. The COM4 Properties window is displayed. Select the following settings (Figure 8):
   Bits per second = 19200
   Data bits = 8
   Parity = None
   Stop bits = 1
   Flow Control = None.

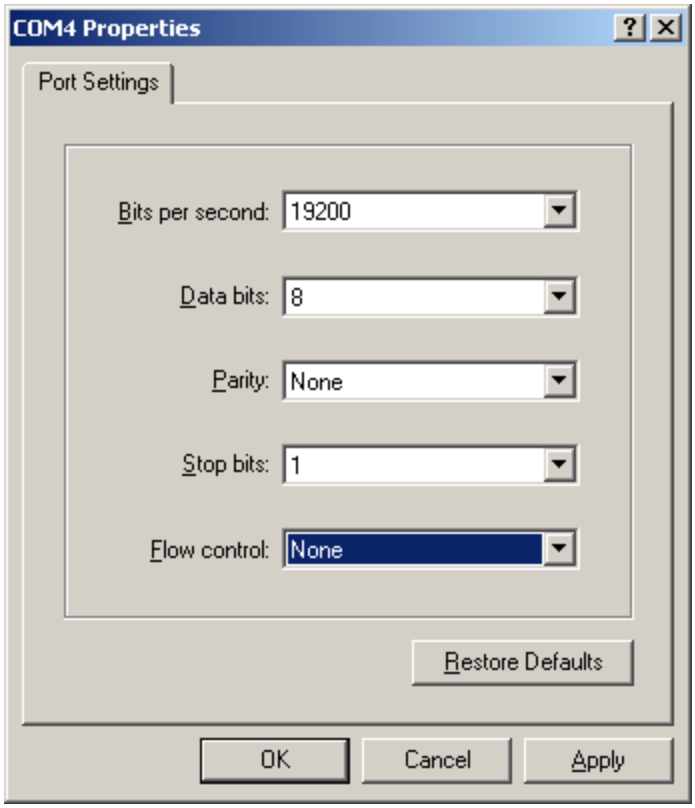



***Figure 8* • HyperTerminal Port Settings**

4. Select **File** > **Properties** in the HyperTerminal window. Choose the **Settings** tab (Figure 9).

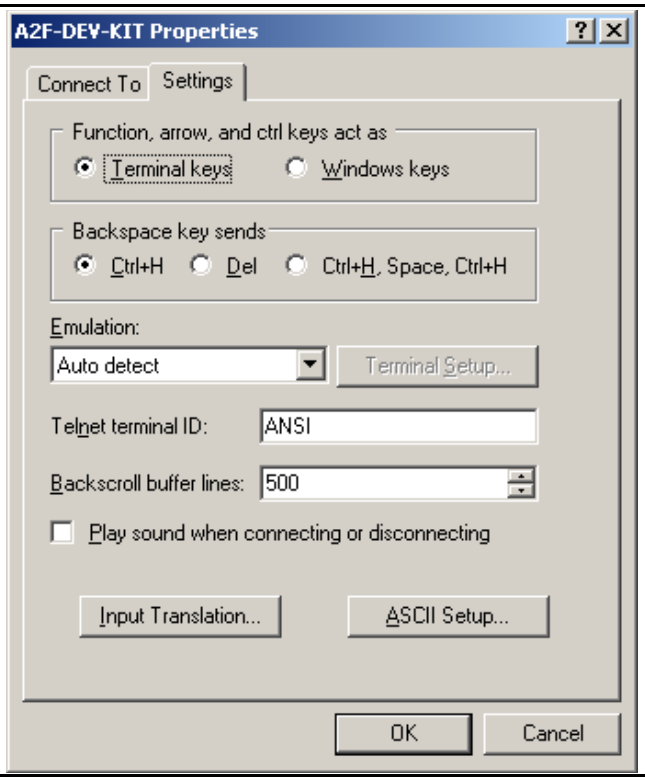



***Figure 9* • HyperTerminal Properties**

5. Click the **ASCII Setup** button. Select the check box labeled **Append line feeds to incoming line ends** (Figure 10).

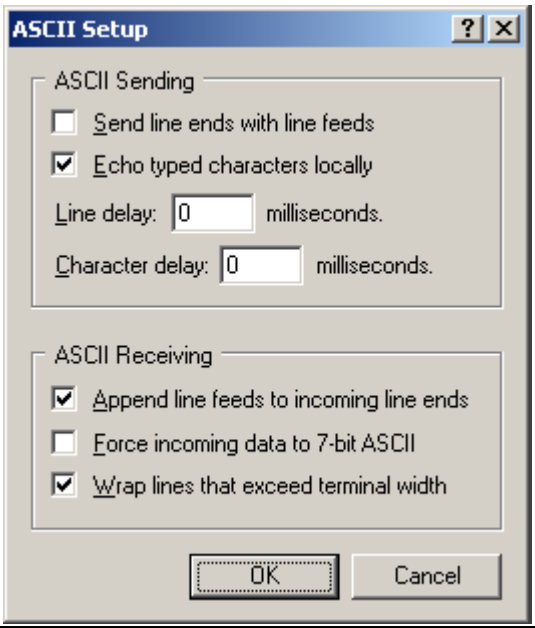



***Figure 10* • ASCII Character Settings**

# Running the A2F-EVAL-KIT Board Test

Press the button labeled **RESET** (SW3) on the A2F-EVAL-KIT board to start the test program.

1. The menu shown in Figure 11 is displayed on the terminal.

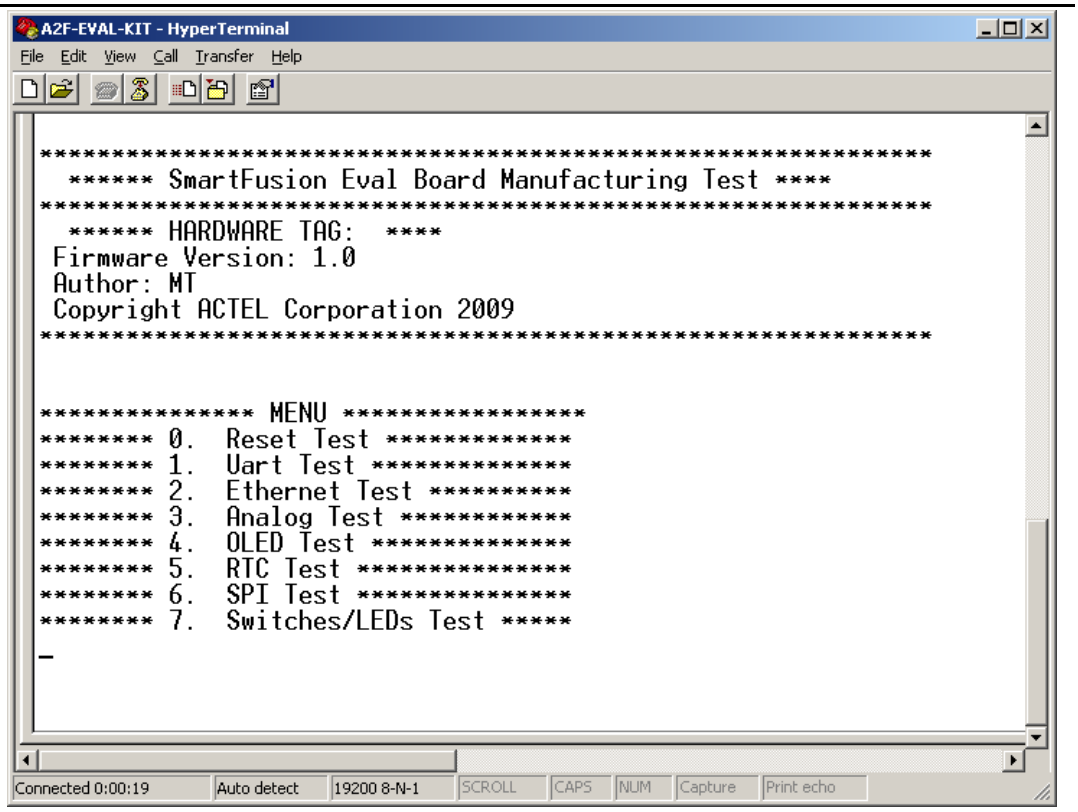



***Figure 11* • Manufacturing Test Menu**

Note: If this message does not appear, try pressing button SW8 again. If the above message still does not appear, refer to the "Setting Up the Test Terminal" section on page 53 and check to see that the terminal has been set up correctly.

## RESET Test

1. Enter **0** into the terminal to begin the reset test. The resulting display should be similar to Figure 12.

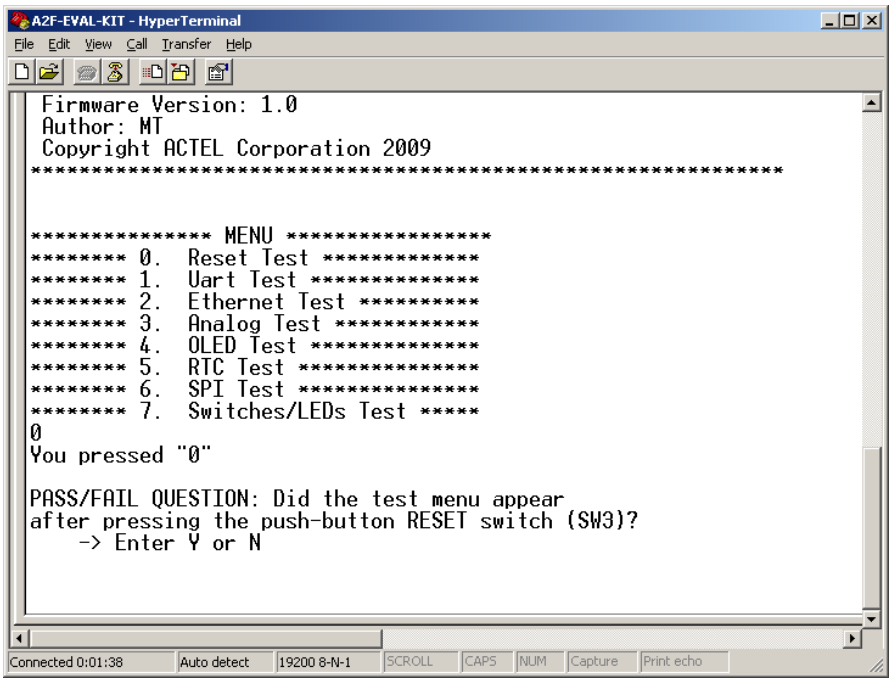



***Figure 12* • Reset Test**

2. If the menu appears correct, enter the character **Y** into the terminal (Figure 13).

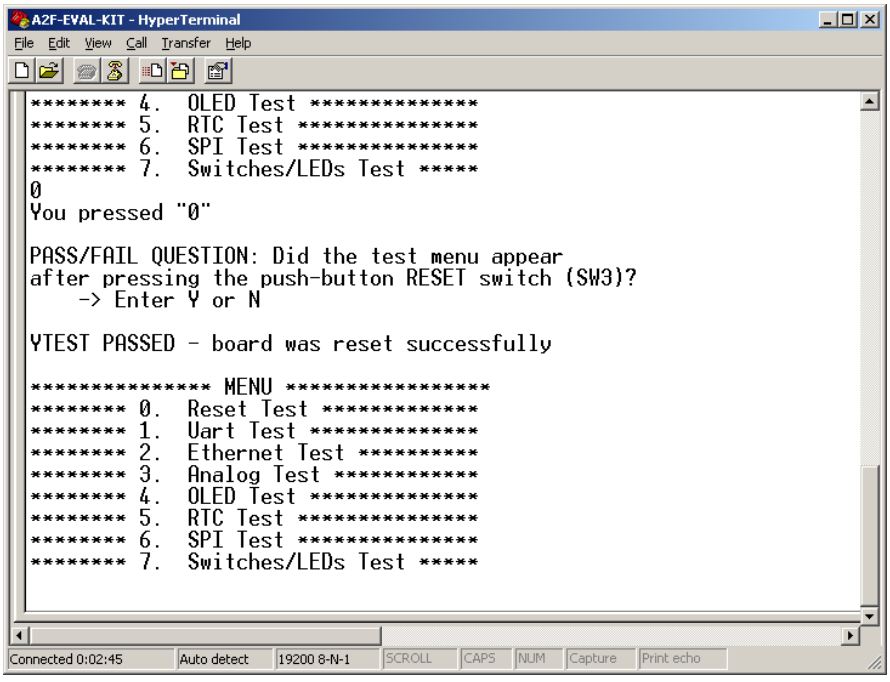



***Figure 13* • Reset Test Result**

## UART Test

1. Enter **1** into the terminal to begin the UART test (Figure 14).

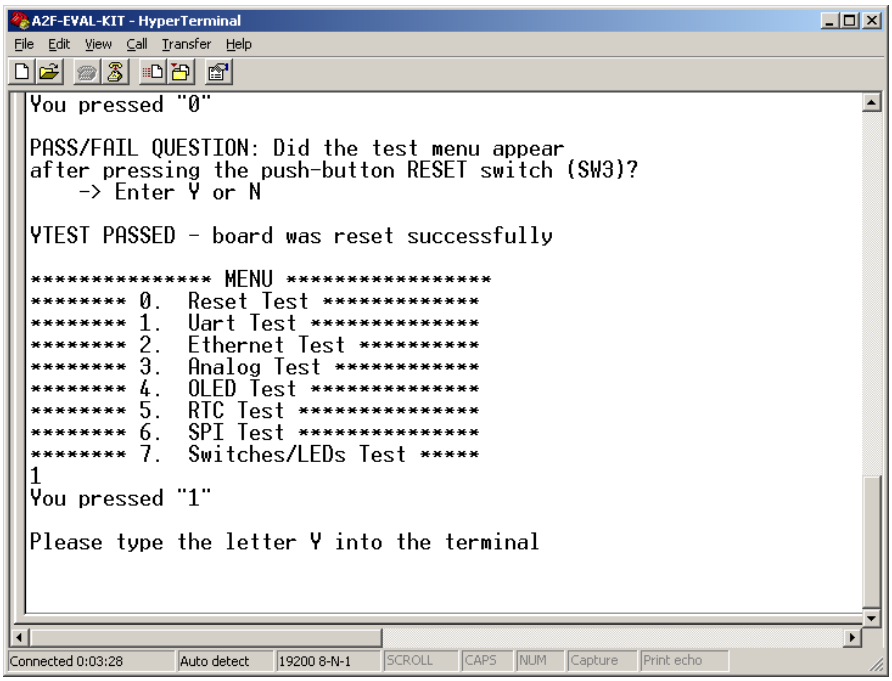



***Figure 14 •*** **UART Test**

2. Type the character **Y** into the terminal. The screen shown in Figure 15 should appear.

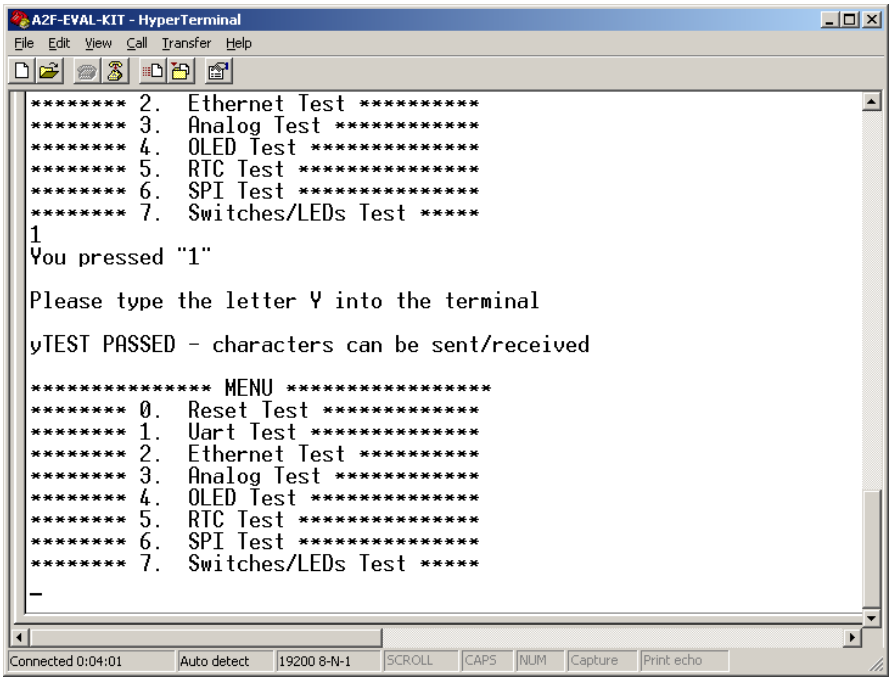



***Figure 15 •*** **UART Test Result**

## Ethernet Test

1. Enter **2** into the terminal to begin the Ethernet test. The screens shown in Figure 16 and Figure 17 should appear.

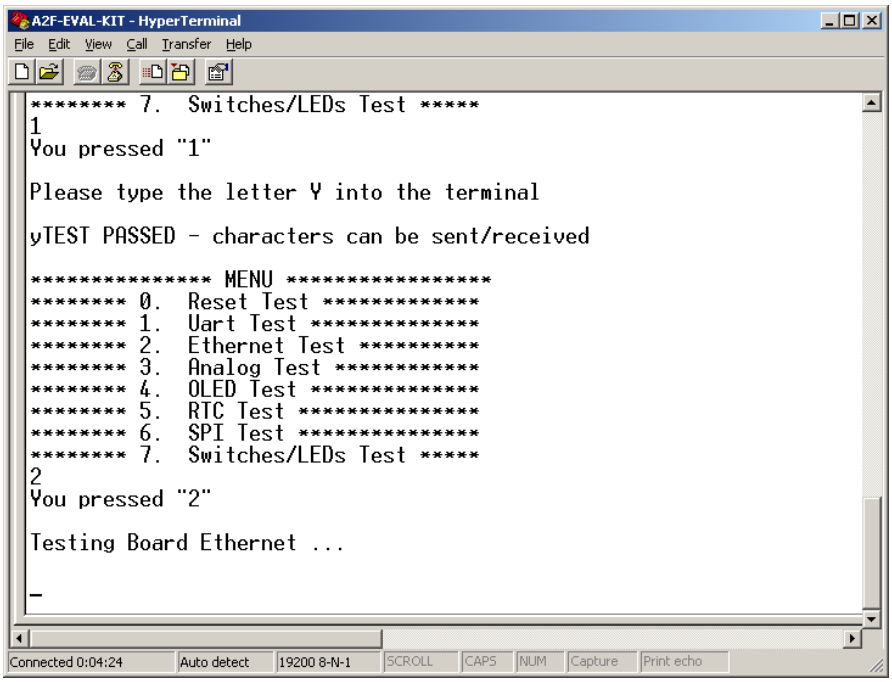



***Figure 16* • Ethernet Test**

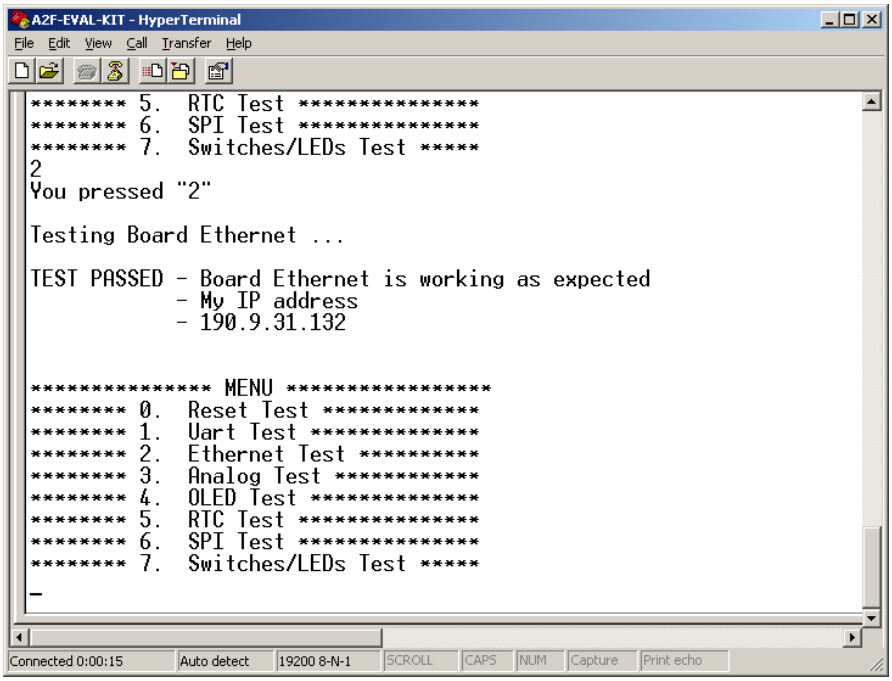



***Figure 17* • Ethernet Test Result**

Note: The IP address may vary in the network setup.

## Analog Test

1. Enter **3** into the terminal to begin the Analog test. The screen shown in Figure 18 should appear.

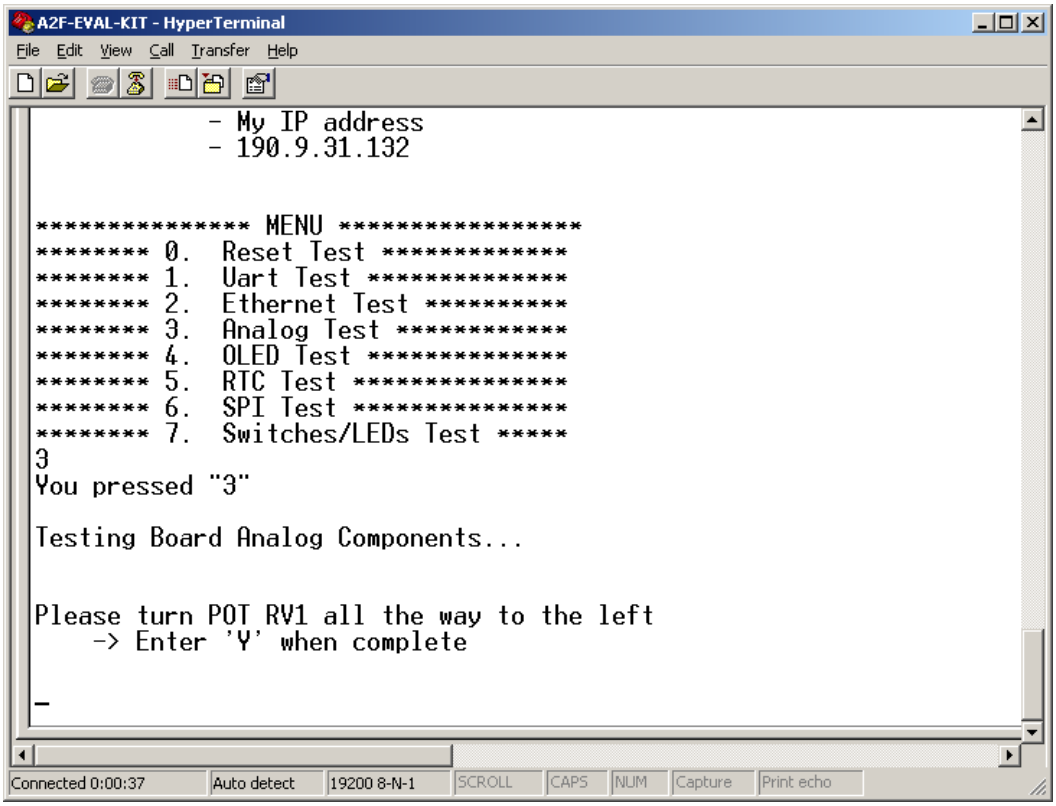



***Figure 18* • Analog Test**

2. Locate POT RV on the bottom, left hand corner of the board. Turn POT RV1 counter-clockwise all the way to the left, as shown in Figure 19.

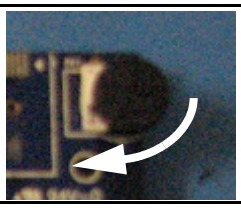


***Figure 19* • POT RV1**

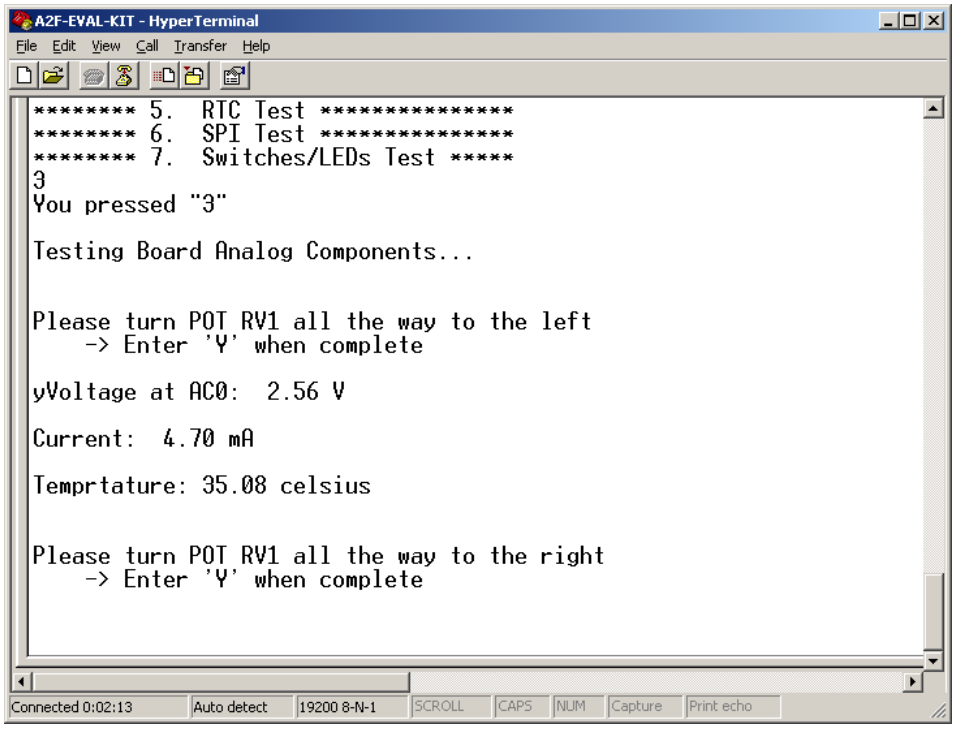



***Figure 20 •*** **Analog Test Starting Results**

3. Turn POT RV clockwise all the way clockwise to the right. The display on the terminal should be similar to Figure 21.

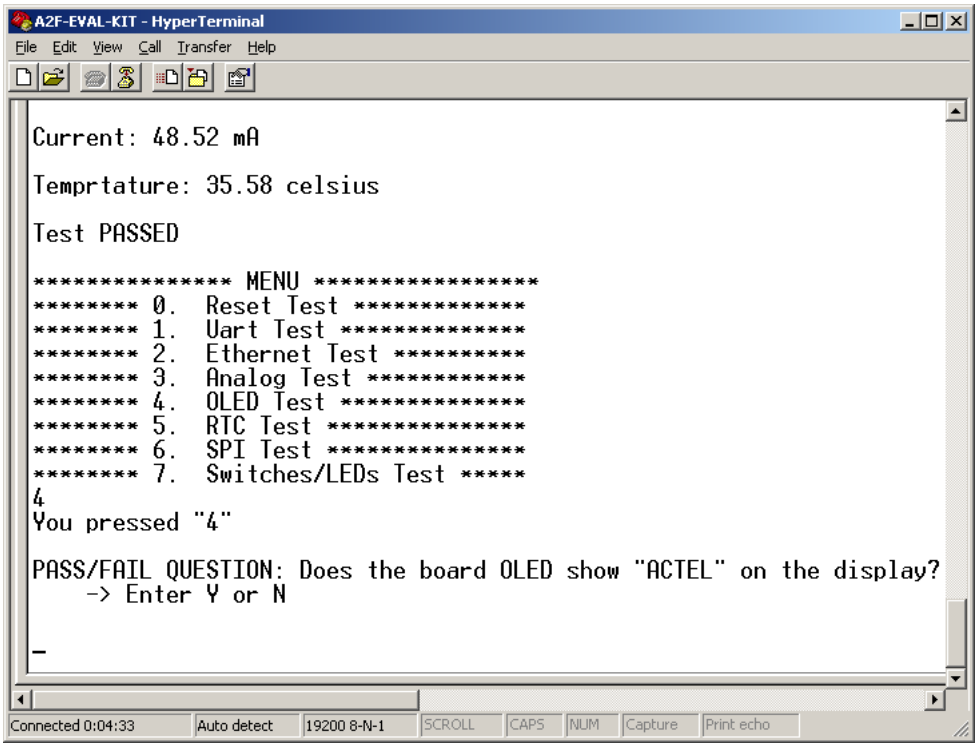



***Figure 21 •*** **Analog Test Ending Results**

## OLED Test

1. Enter **4** into the terminal to begin the OLED test. The screen shown in Figure 22 is displayed.

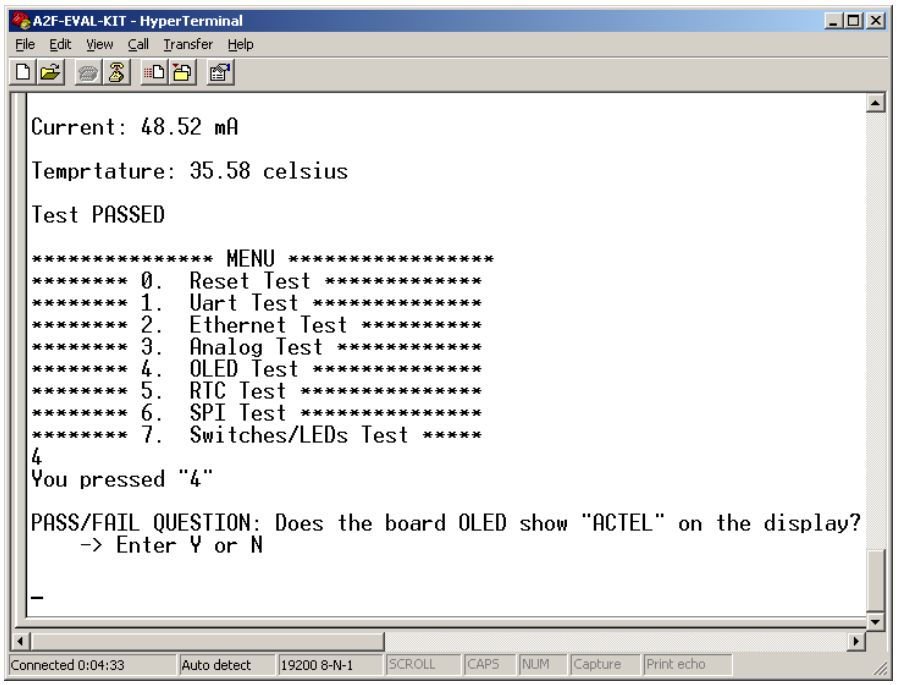



***Figure 22 •*** **OLED Test Setup**

2. Check the board OLED display. If the characters ACTEL MAN TEST are displayed in the OLED, enter **Y** in the terminal; otherwise, enter **N**. If Y was entered, the screen shown in Figure 23 is displayed.

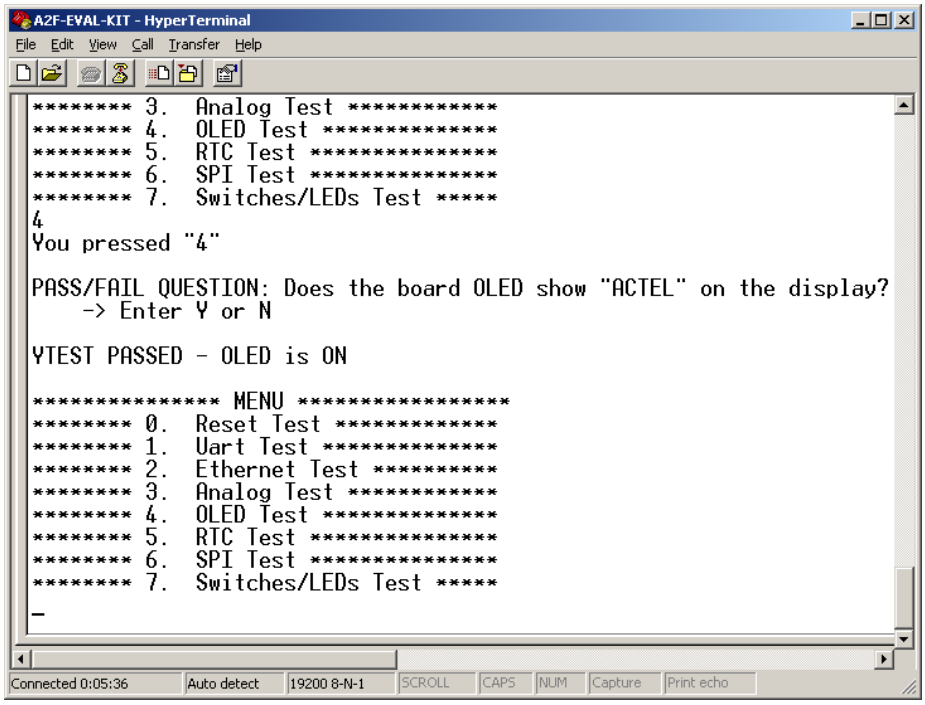



***Figure 23 •*** **OLED Test Results**

## RTC Test

1. Enter **5** into the terminal to begin the RTC test (Figure 24).

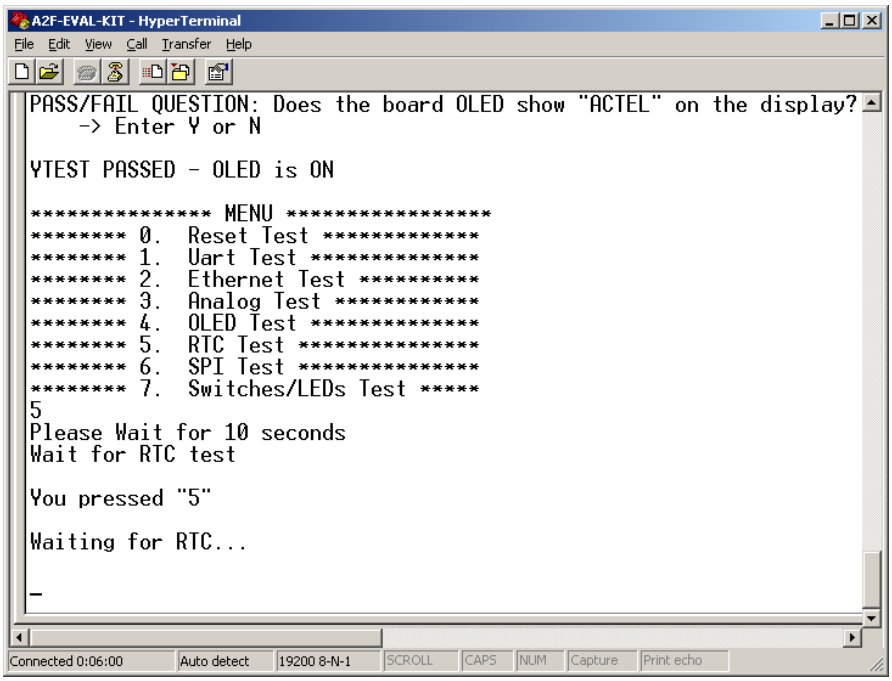



***Figure 24* • RTC Test**

2. After a few seconds, the screen shown in Figure 25 should appear.

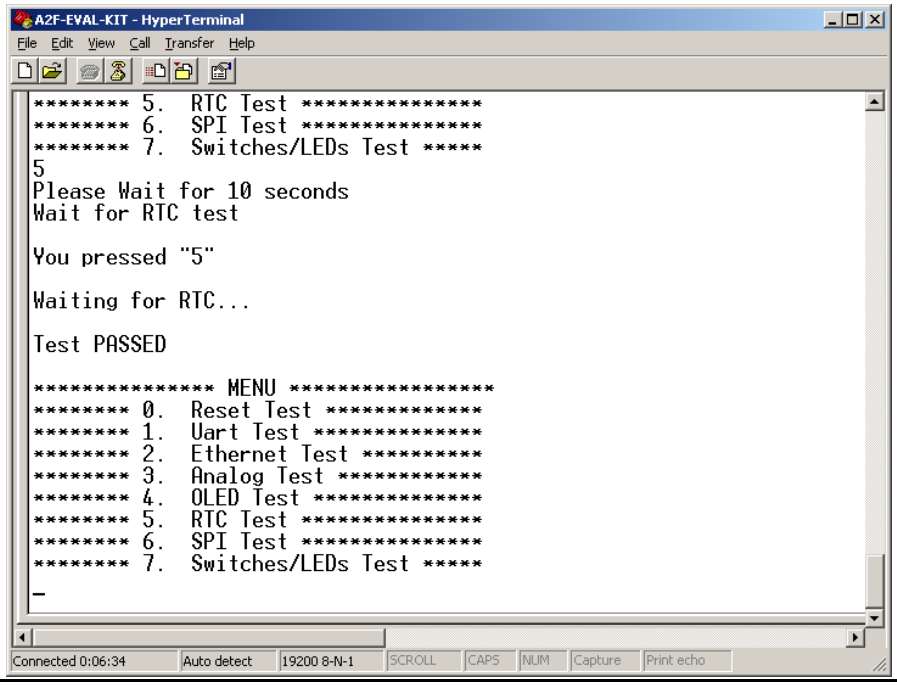



***Figure 25* • RTC Test Passed**

## SPI Test

Enter **6** into the terminal to begin the SPI test. After several seconds, the screen shown in Figure 26 should appear.

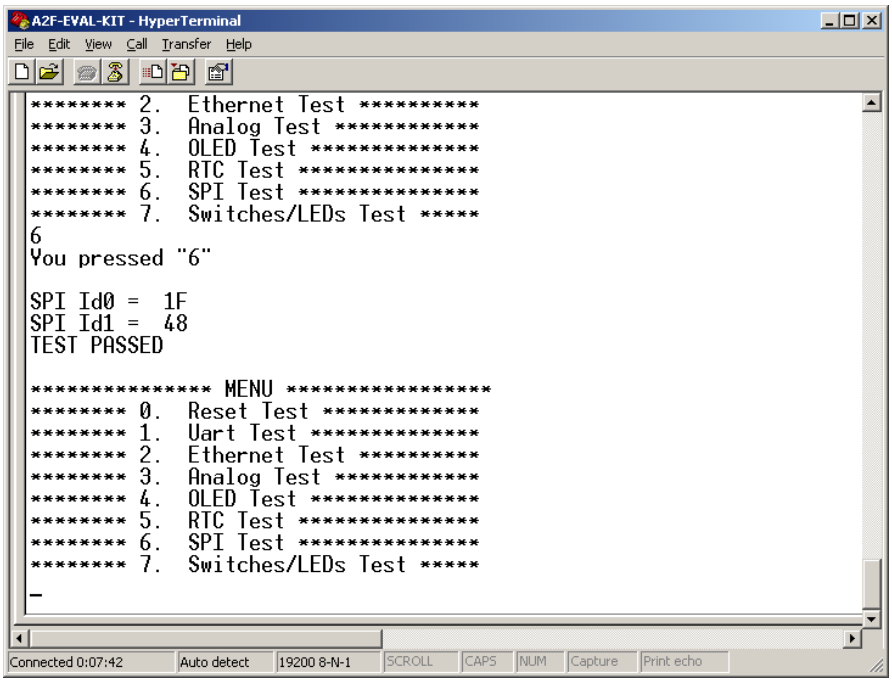



***Figure 26 •*** **SPI Test**

## Switch/LED Test

1. Enter **7** into the terminal to begin the LEDs test. The screen shown in Figure 27 is displayed.

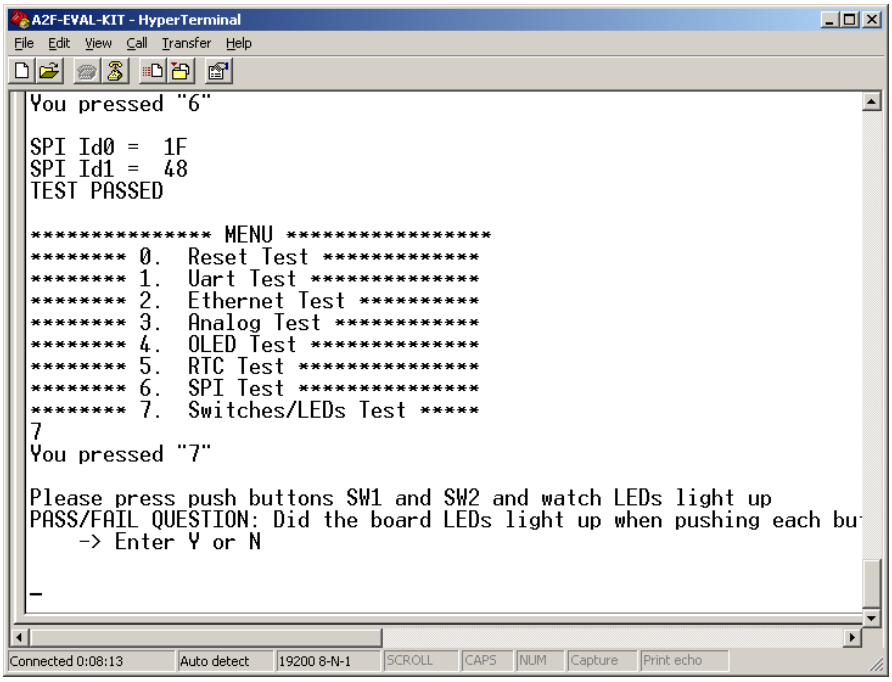



***Figure 27 •*** **LED Test**

2. Press **SW2** and LEDs D1, D2, D3, D4, D5, D6, D7, and D8 must light up. When this has occurred, press **Y** (Figure 28).

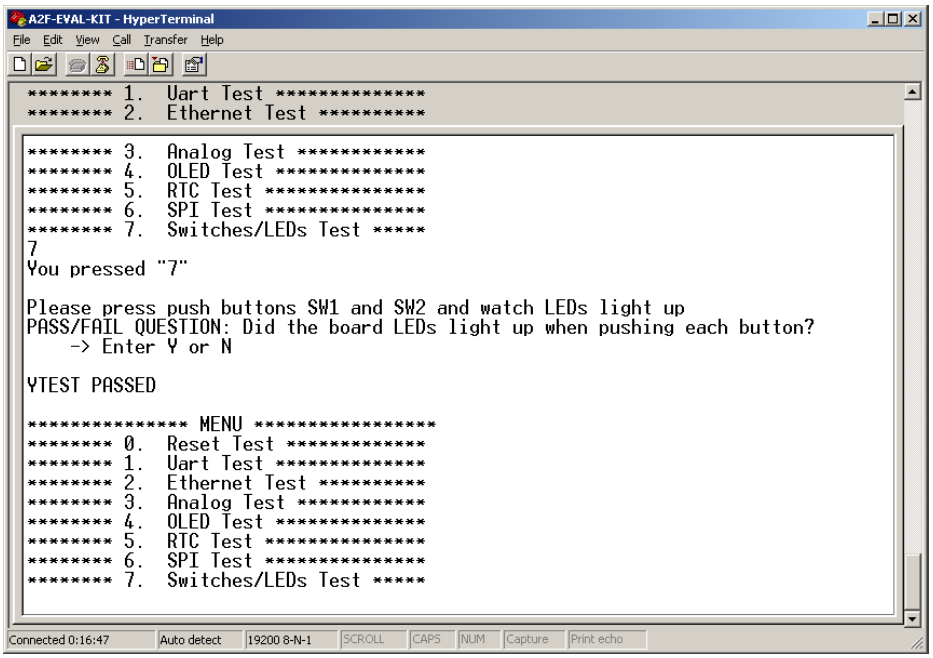



***Figure 28* • Switch Test**

# A2F-EVAL-KIT Board Failures

All Tests outlined in "Running the A2F-EVAL-KIT Board Test" on page 57 should result in the words TEST PASSED being printed on the terminal. If this does not happen, or the words TEST FAILED are printed, the test has failed.

If the A2F-EVAL-KIT board fails any of the tests outlined in "Running the A2F-EVAL-KIT Board Test" on page 57, the board being tested is not functional.

# A – List of Changes

The following table lists critical changes that were made in the current version of the chapter.

| Previous Version | Changes in Current Version* (50200209-4/05.11) | Page |
|---|---|---|
| 50200209-3/10.10 | The "Pinout Definition" table in the "Component Descriptions and Connections" chapter was updated. This fixes SAR# 31533. | 29 |
| 50200209-2/5.10 | The "Demo Design" chapter was added that fixes SAR# 27577. | 45 |
| | Reference added in the "Software Installation" section for IAR and Keil Software support to SmartFusion that fixes SAR# 27579. | 7 |
| 50200209-0/2.10 | The "Mixed-Signal Header" section was added. | 27 |

*Note: *The part number is located on the last page of the document. The digits following the slash indicate the month and year of publication.*

# B – Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

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You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

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The technical support email address is tech@actel.com.

## Phone

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