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TEAM PROJECT

# COUNTER IN GRAY CODE

# GRAY CODE

- A Gray code is an encoding of numbers so that adjacent numbers have a single digit differing by 1. The term Gray code is often used to refer to a "reflected" code, or more specifically still, the binary reflected Gray code.
- Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems.

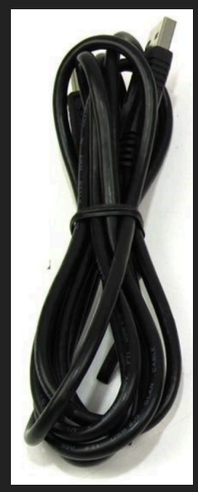
| Decimal | Binary | Gray |
|---|---|---|
| 0 | 0000 | 0000 |
| 1 | 0001 | 0001 |
| 2 | 0010 | 0011 |
| 3 | 0011 | 0010 |
| 4 | 0100 | 0110 |
| 5 | 0101 | 0111 |
| 6 | 0110 | 0101 |
| 7 | 0111 | 0100 |
| 8 | 1000 | 1100 |
| 9 | 1001 | 1101 |
| 10 | 1010 | 1111 |
| 11 | 1011 | 1110 |
| 12 | 1100 | 1010 |
| 13 | 1101 | 1011 |
| 14 | 1110 | 1001 |
| 15 | 1111 | 1000 |

# PROJECT GOALS

- Design a counter in Gray code using VHDL in the ISE software
- Must be a N-bits counter
- Counting Up and Down
- With a Reset signal

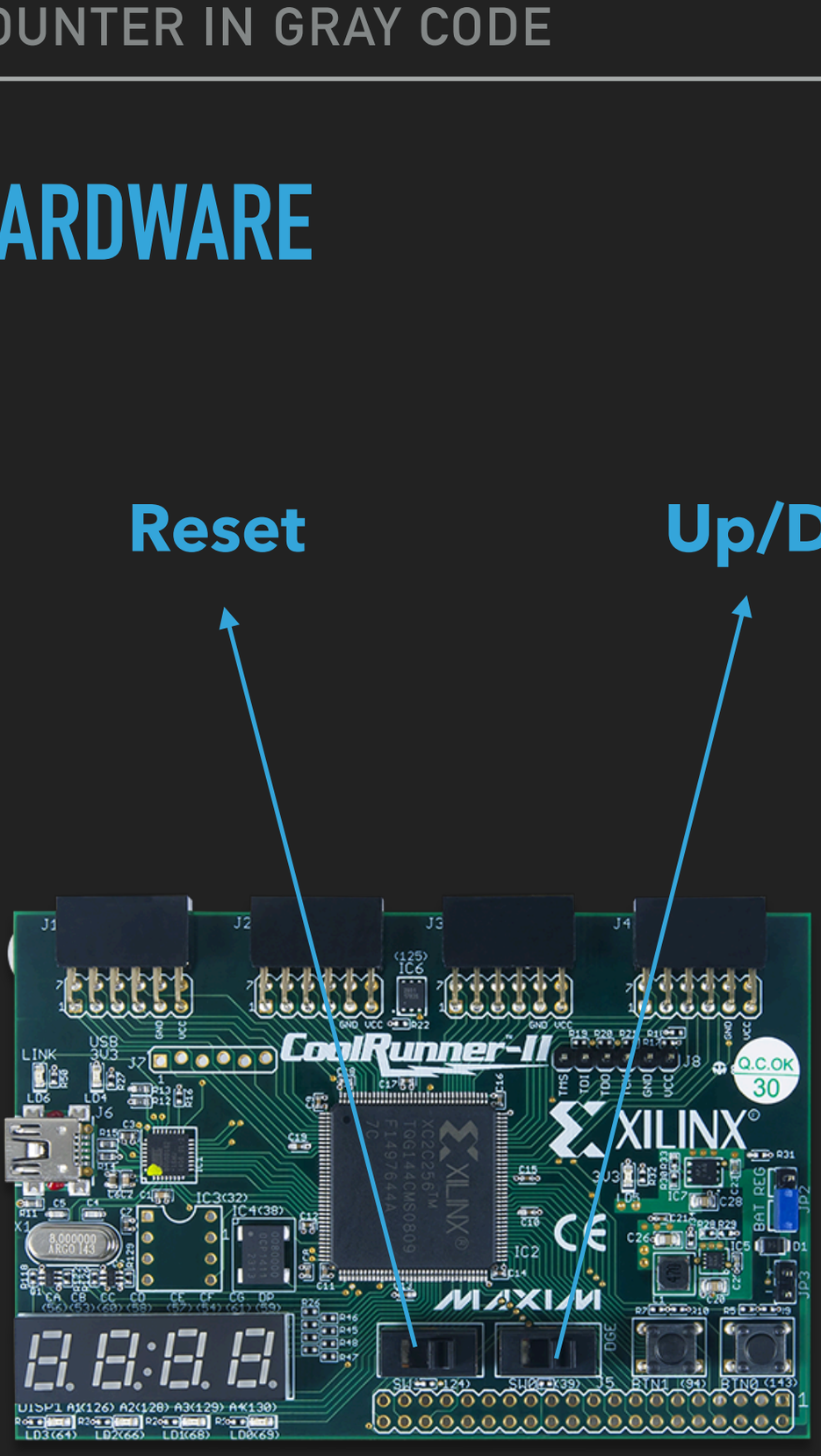
```
44        -- Entity output signals
45       g_out    : out std_logic_vector(16-1 downto 0)
46          );
47
48  end gray_cnt;
49
50  architecture Behavioral of gray_cnt is
51
52      constant PRESC_BIT : integer := 16; --Number of bits for the pr
53      constant c_NBIT : integer := 9; --Number of bits of the N-bits
54      signal s_clk_prescaler : std_logic_vector(PRESC_BIT-1 downto 0)
55      signal s_b_in : std_logic_vector(16-1 downto 0);
56
57  begin
58
59
60   BINCNTPRESC : entity work.bin_cnt_presc
61      generic map (
62          PRESC_BIT => PRESC_BIT          -- N_bit binary counter
63      )
64      port map (
65          clk_i => clk_i,                 -- 10 kHz
66          rst_n_i => '1',                 -- inactive reset
67          bin_cnt_o => s_clk_prescaler    -- output bits
68      );
69
70
71  BINCNT2 : entity work.bin_cnt_2
72      generic map (
73          N_BIT => c_NBIT                  -- N_bit binary counter
74      )
75   port map (
76          b_in => s_b_in,   -- output bits
77          s_up(0) => g_s_up(0),
78          clk_i => s_clk_prescaler(PRESC_BIT-1),--CAMBIAR POR PRESC B
79          rst_n_i => rst_n_i,
80          b_out => s_b_in
81      );
82
83  BIN2GRAY : entity work.bin2gray
84      generic map (
85          N_BIT => c_NBIT                  -- N_bit binary counter
86      )
87      port map (
88          clk_i => clk_i,
```

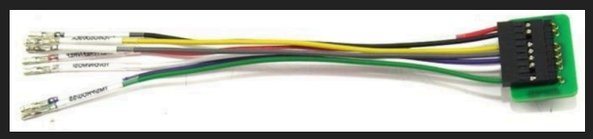
# HARDWARE



**Reset**

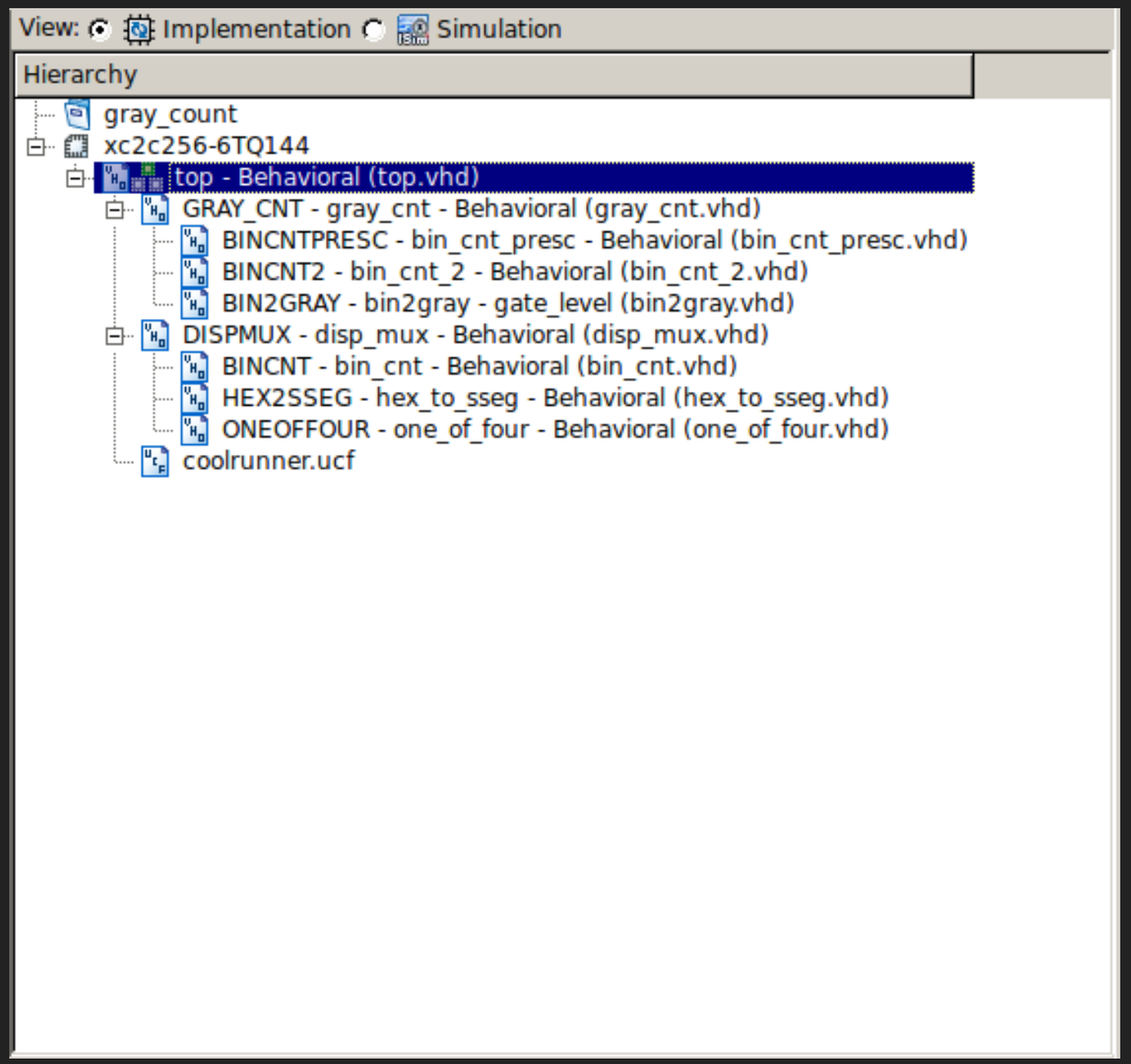
**Up/Down**



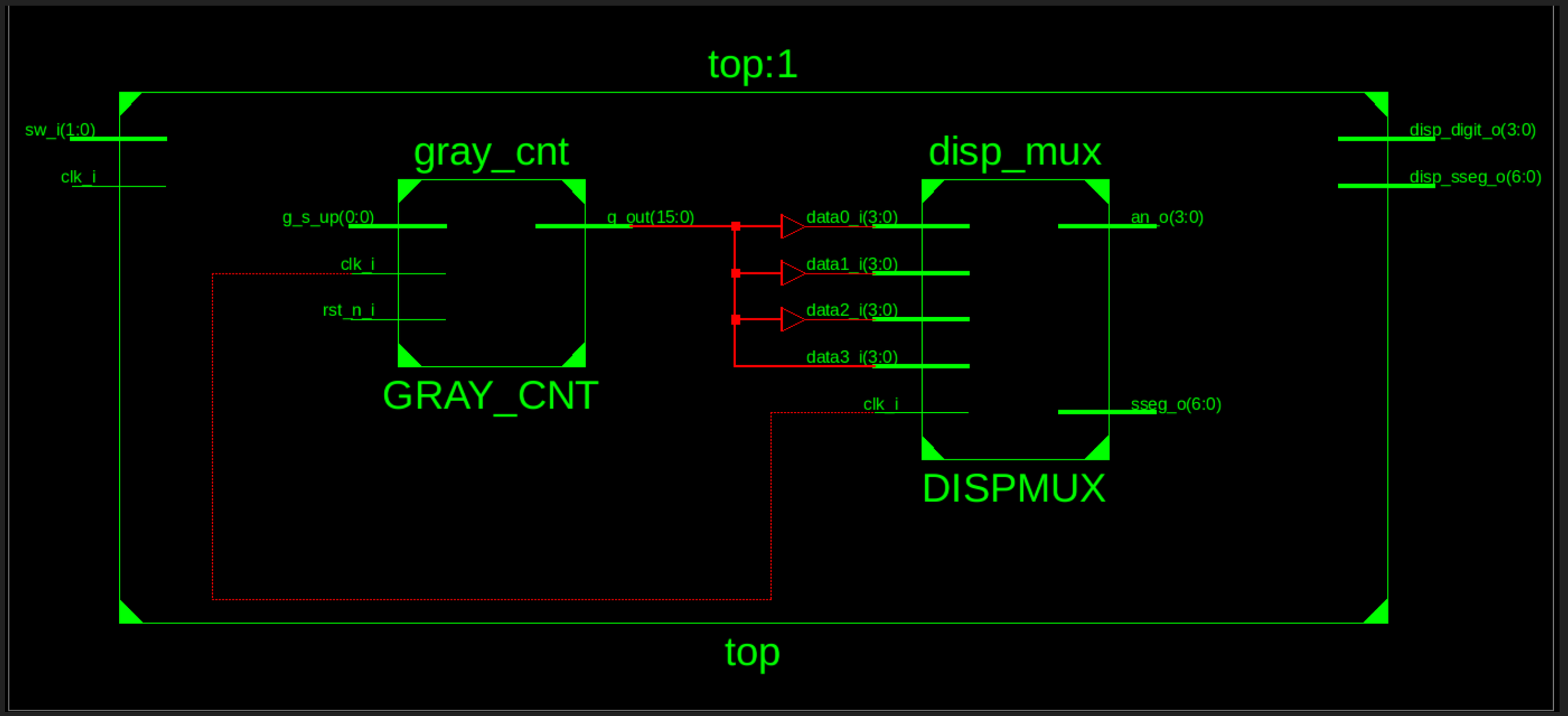



# VHDL MODULES

- gray_cnt
  - bin_cnt_presc
  - bin_cnt_2
  - bin2gray
- disp_mux
  - bin_cnt
  - four_to_one
  - hex_to_sseg
  - one_of_four



# SCHEMATIC


top:1
sw_i(1:0)
clk_i
gray_cnt
g_s_up(0:0)
clk_i
rst_n_i
g_out(15:0)
GRAY_CNT
data0_i(3:0)
data1_i(3:0)
data2_i(3:0)
data3_i(3:0)
clk_i
disp_mux
an_o(3:0)
sseg_o(6:0)
DISPMUX
disp_digit_o(3:0)
disp_sseg_o(6:0)
top

# VIDEO DEMOSTRARON OF THE PROJECT

# RESULTS

- All required project specifications have been checked so we can close the project satisfactorily.

# THANK YOU FOR YOUR ATTENTION

## AND PLEASE

# DON'T ASK TOO MUCH 😄