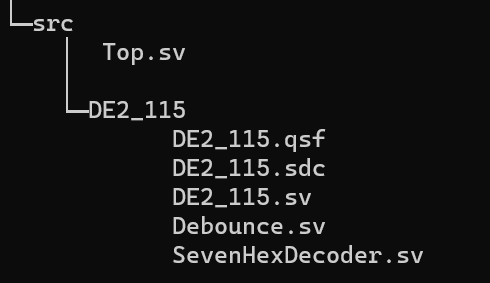
NTUEE DCLAB LAB1

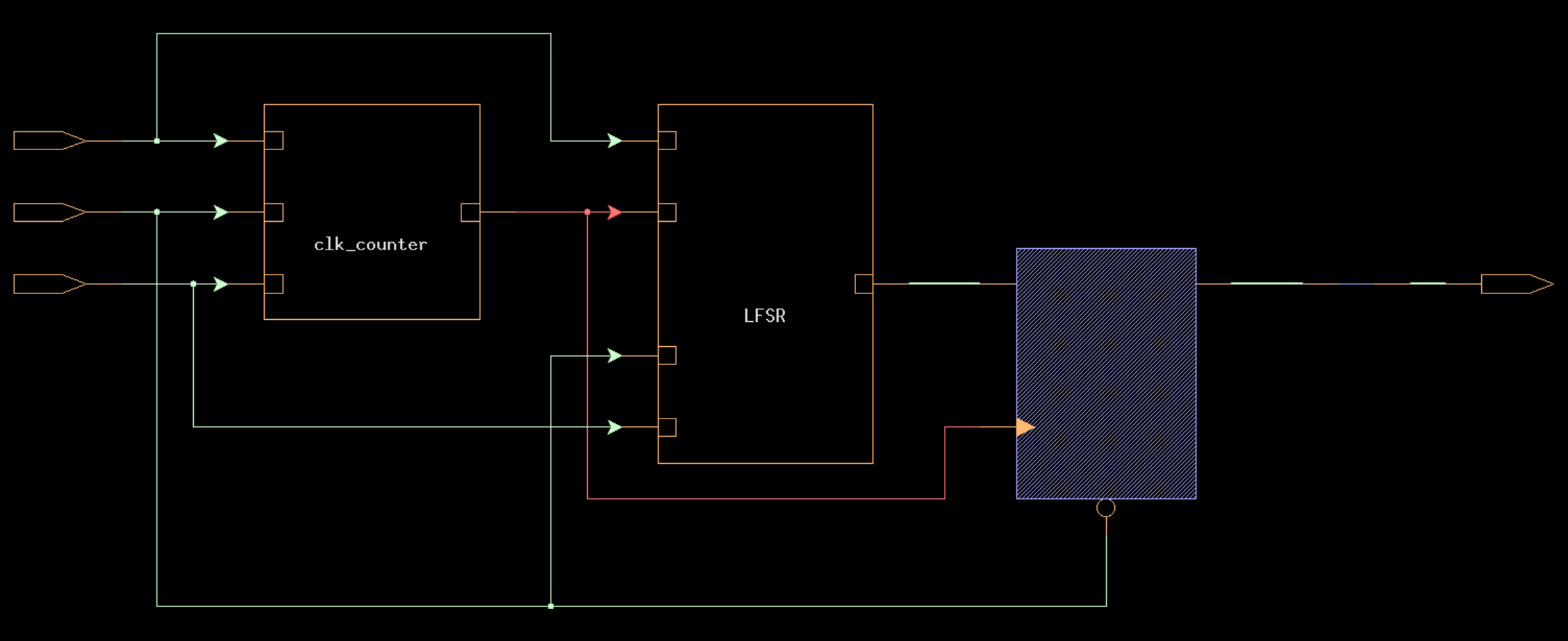
Team 05陳冠穎、陳楚融、梁璿安

**Part 1: File Structure**



**Part 2: System Architecture**

Top:



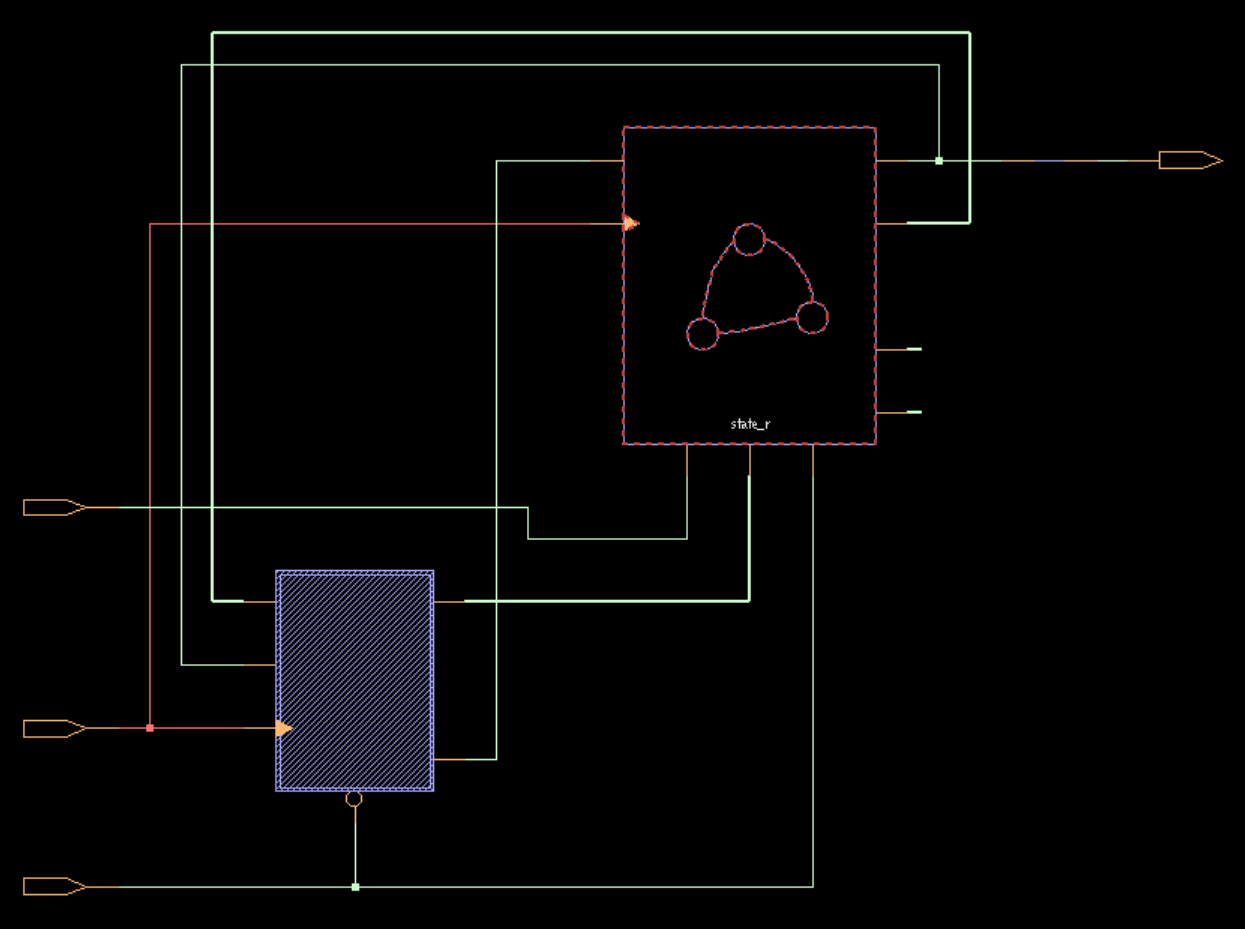
o\_random\_out

i\_clk

i\_rst\_n

i\_start

Clk\_counter



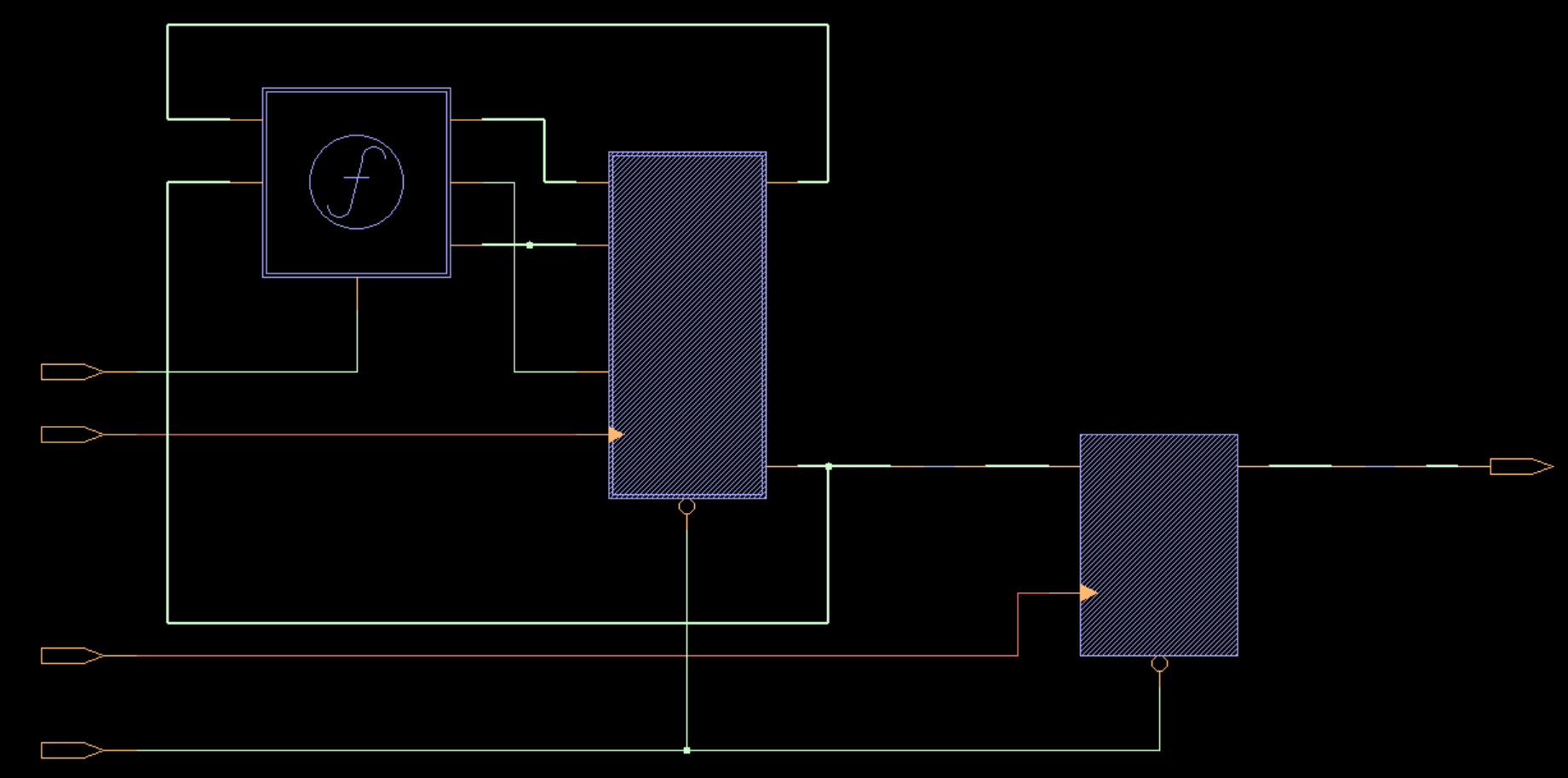
slower\_clk

i\_start

i\_clk

i\_rst\_n

LFSR



result[3:0]

i\_start

i\_clk

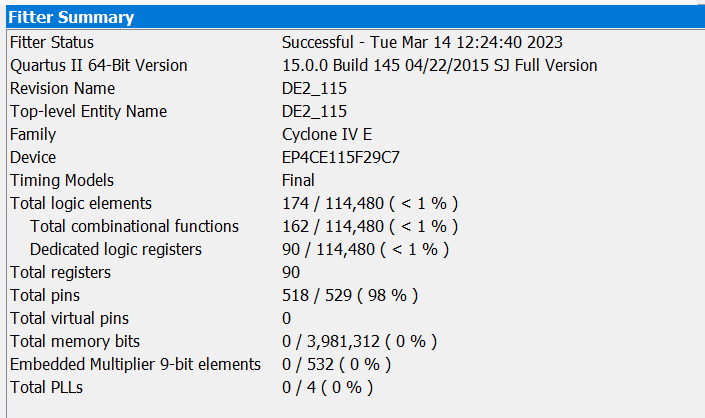
slower\_clk

i\_rst\_n

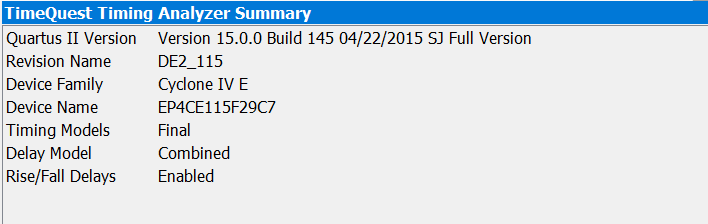
**Part 3: Hardware Scheduling**

****

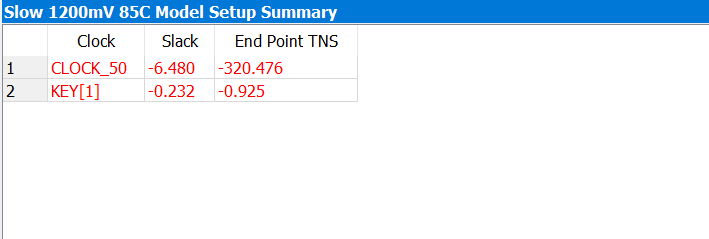
**Part 4: Filter Summary**

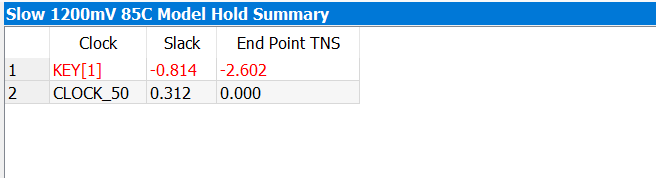
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**Part 5: Timing Analyzer**

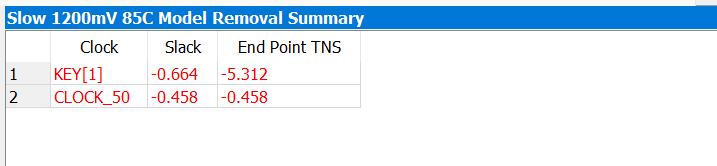


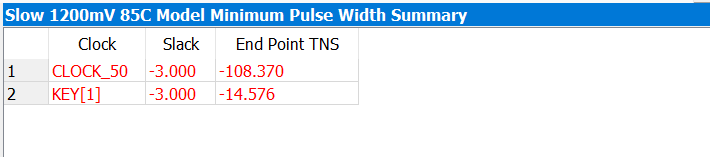
Timing Violation (Slow 1200mV 85C Model)

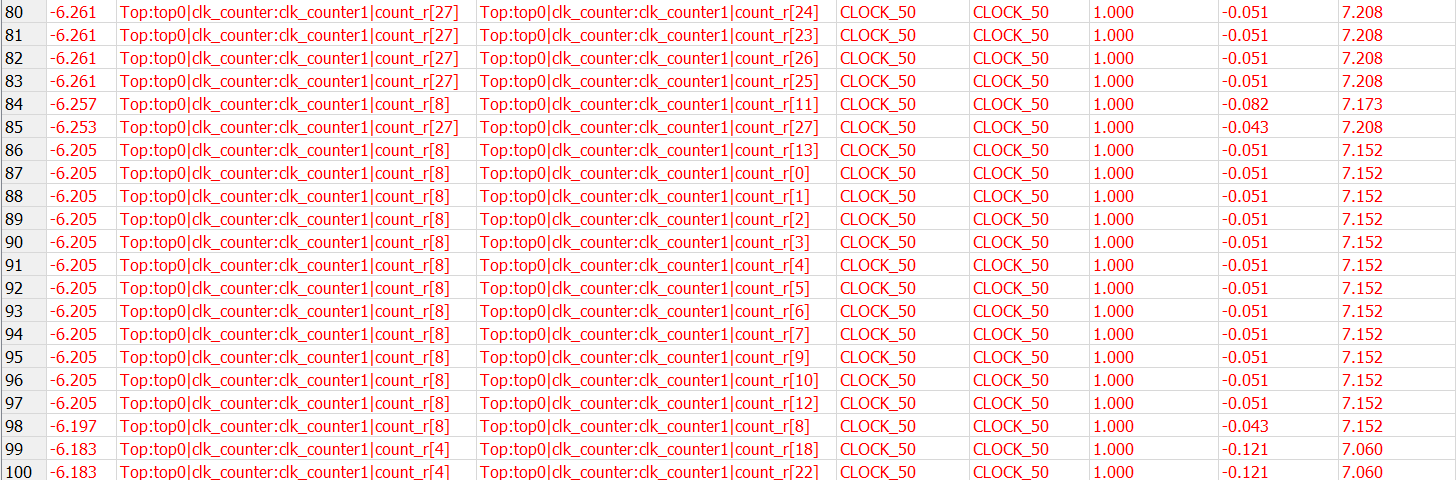
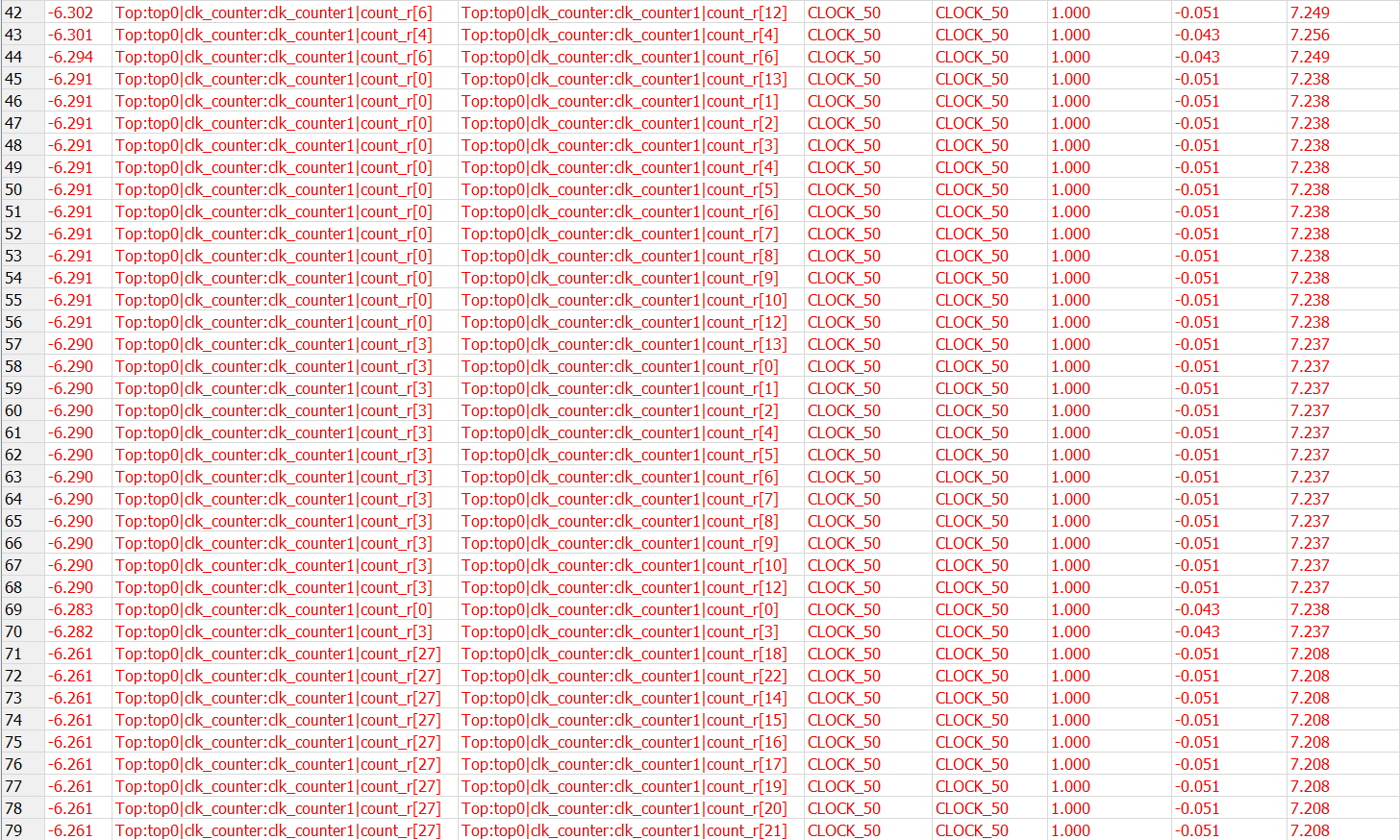
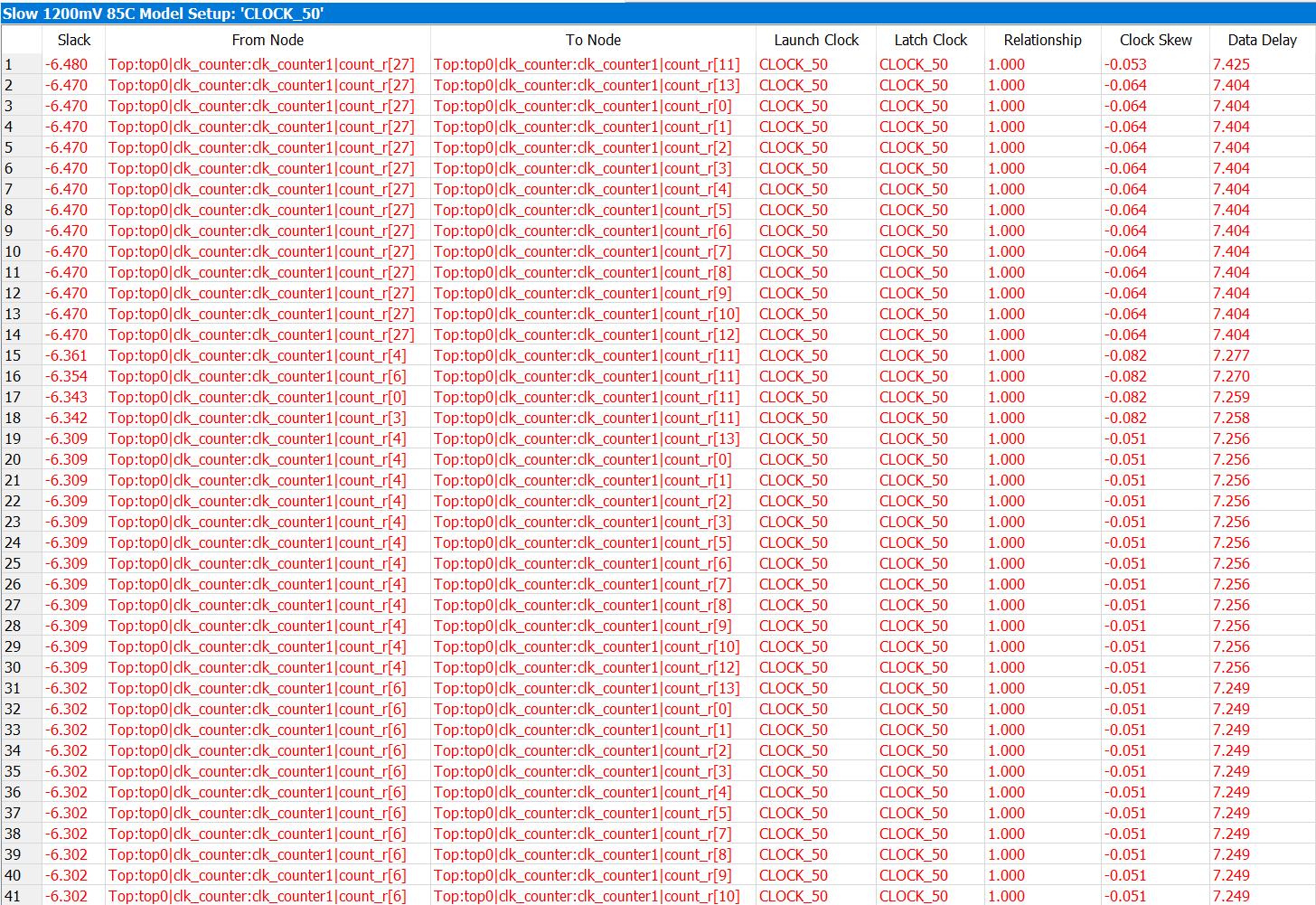


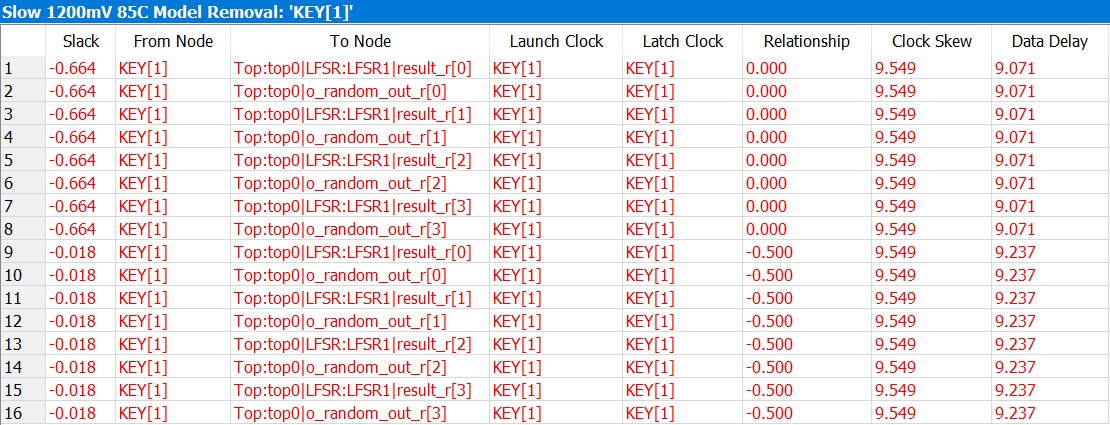
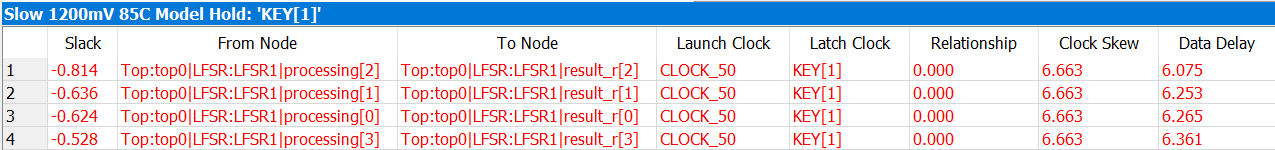
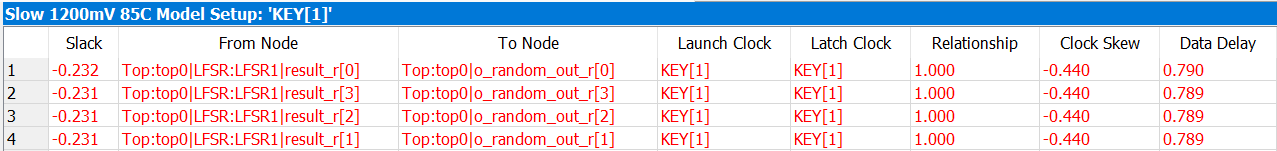
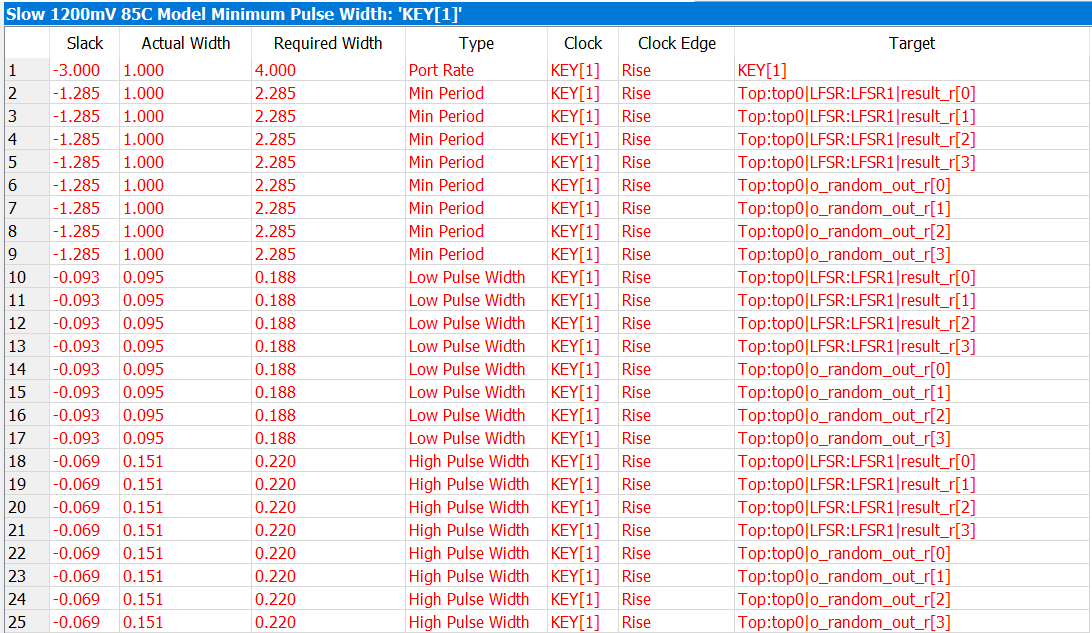
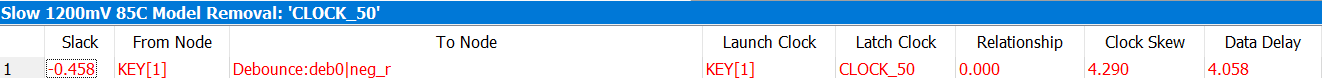


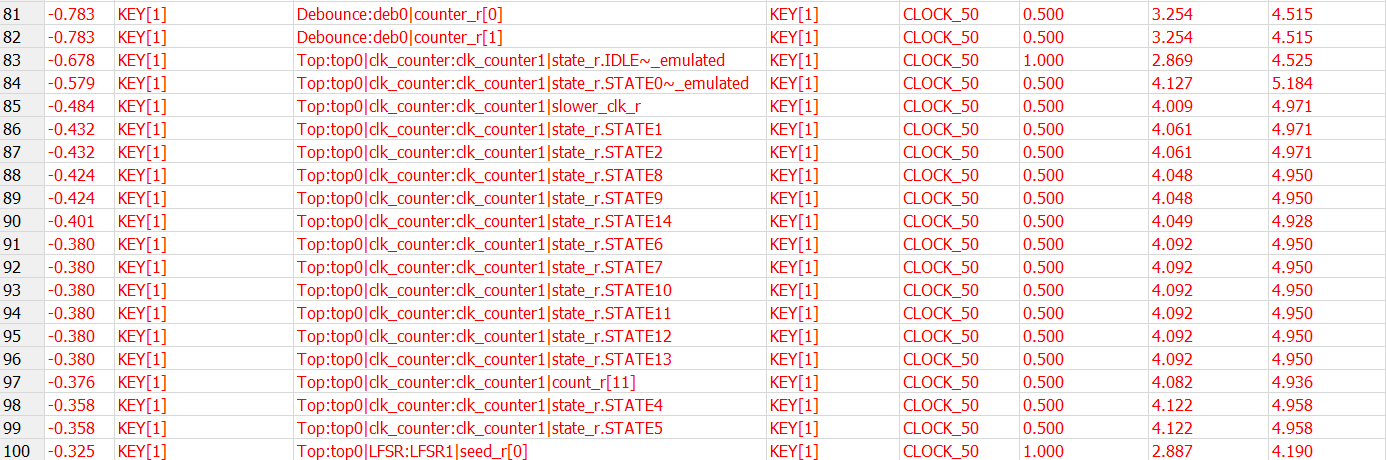
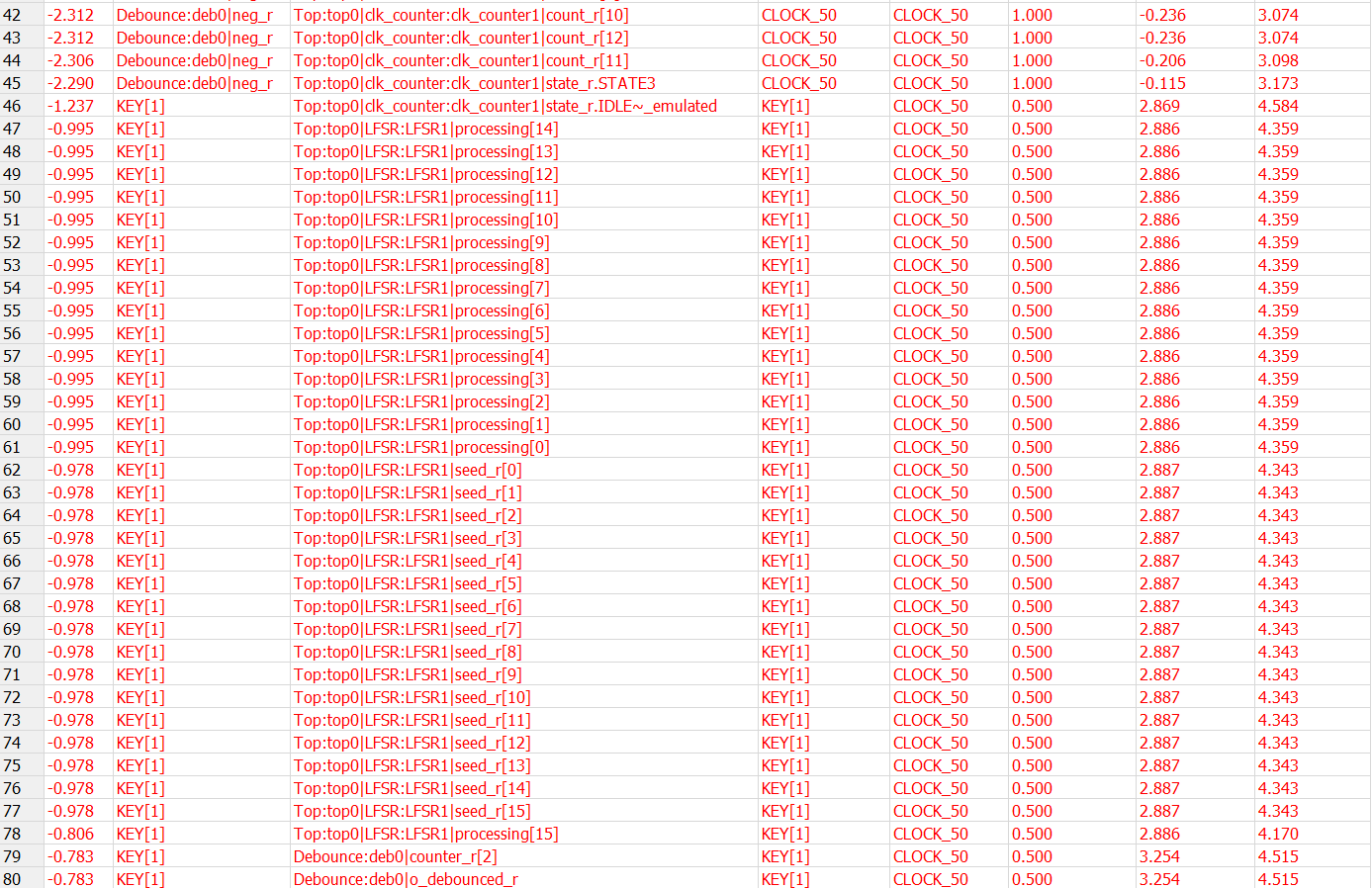
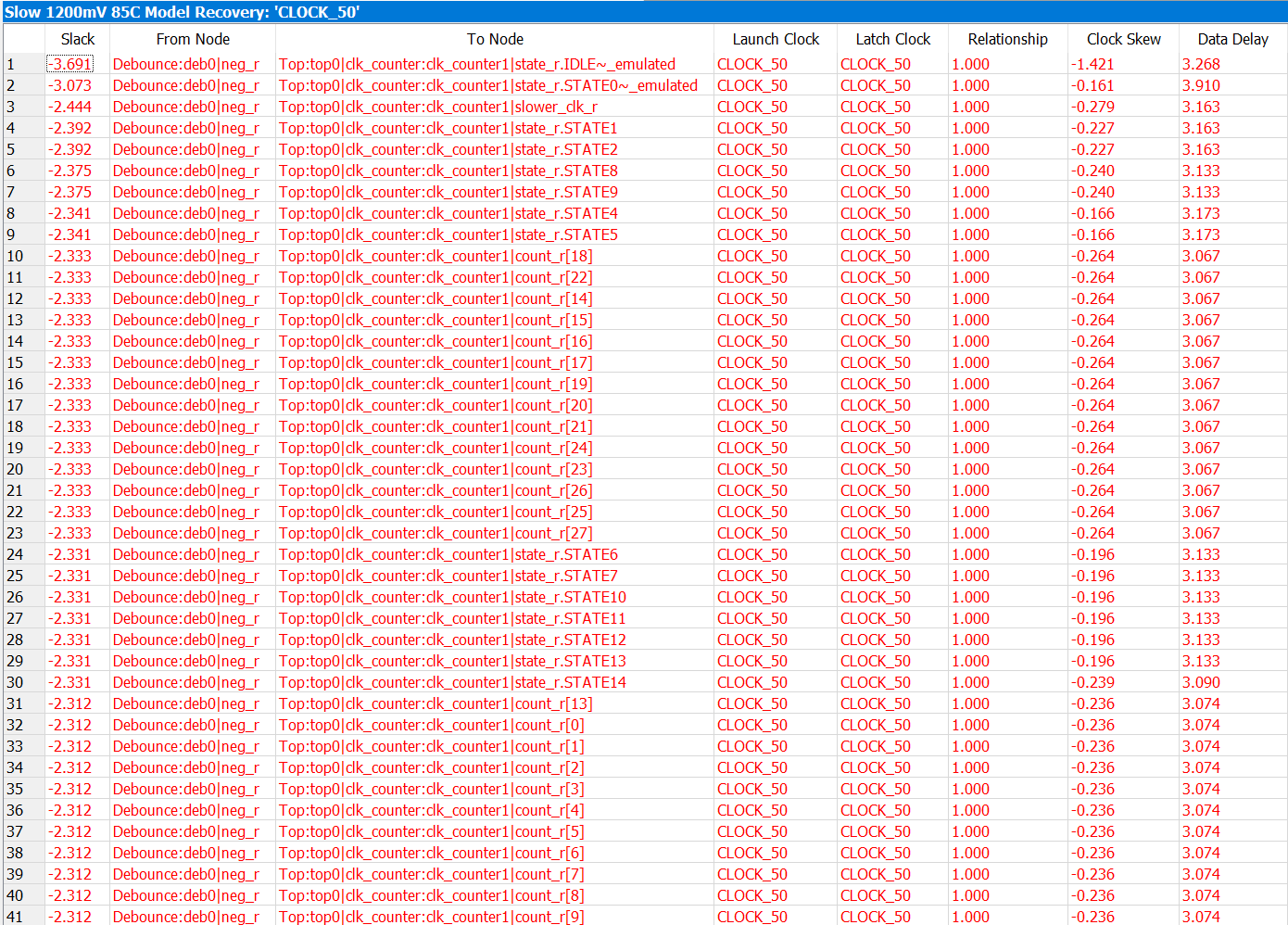


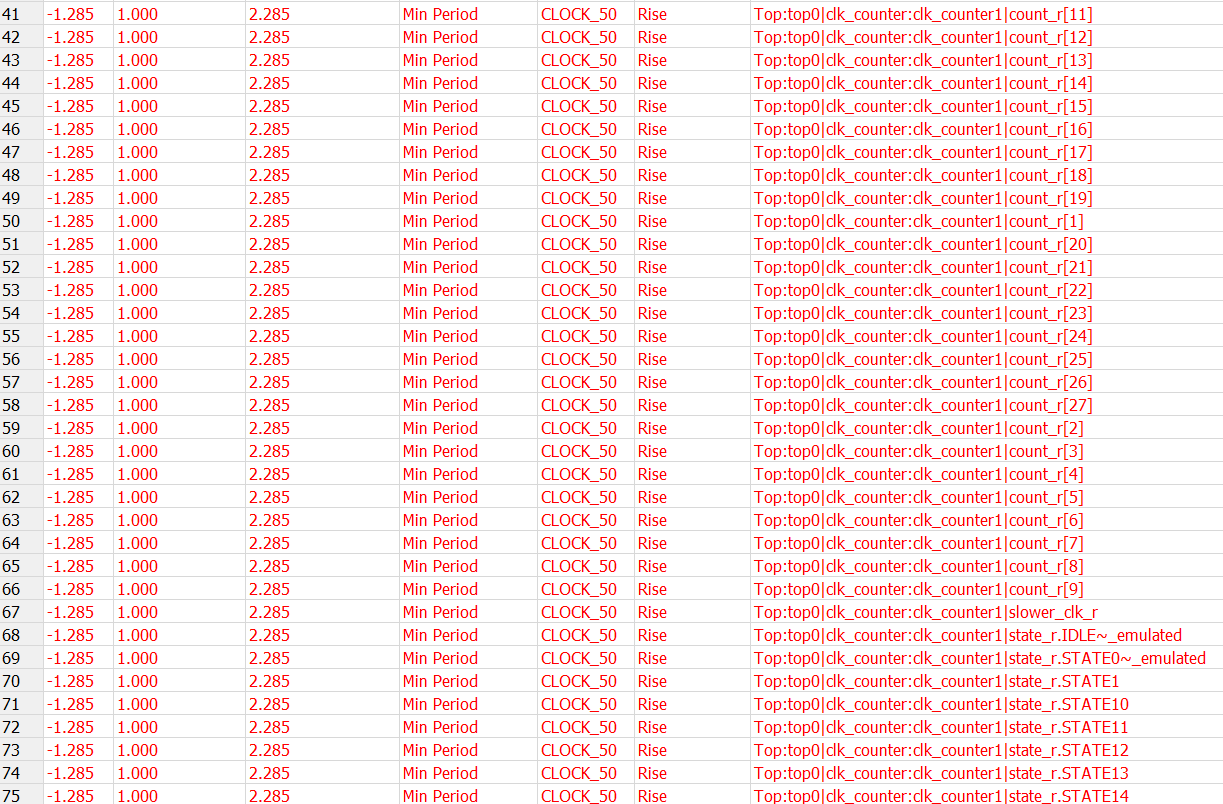
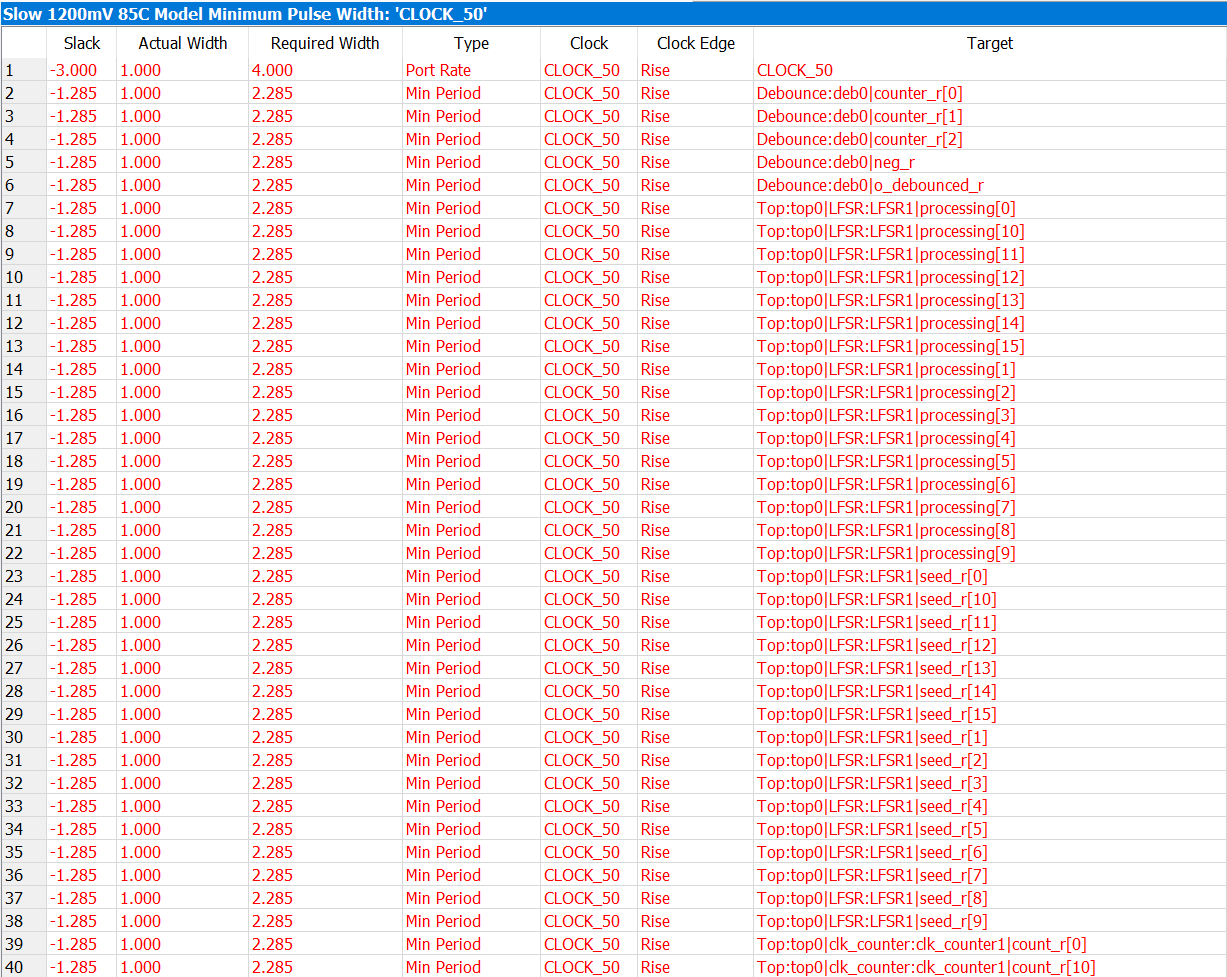
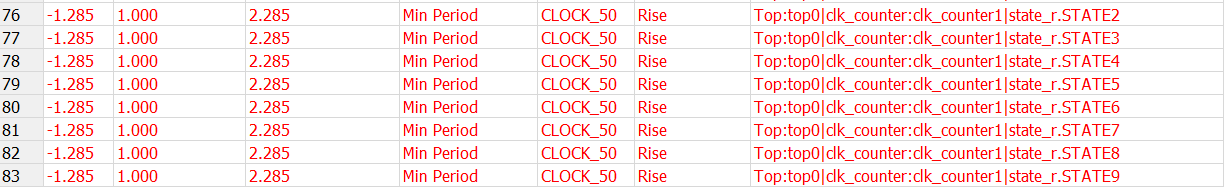


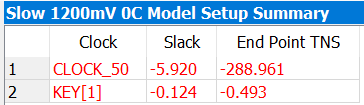




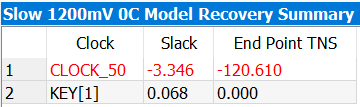
 

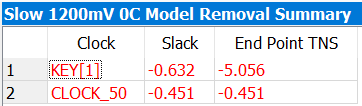


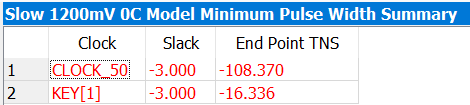
  Timing Violation (Slow 1200mV 0C Model)

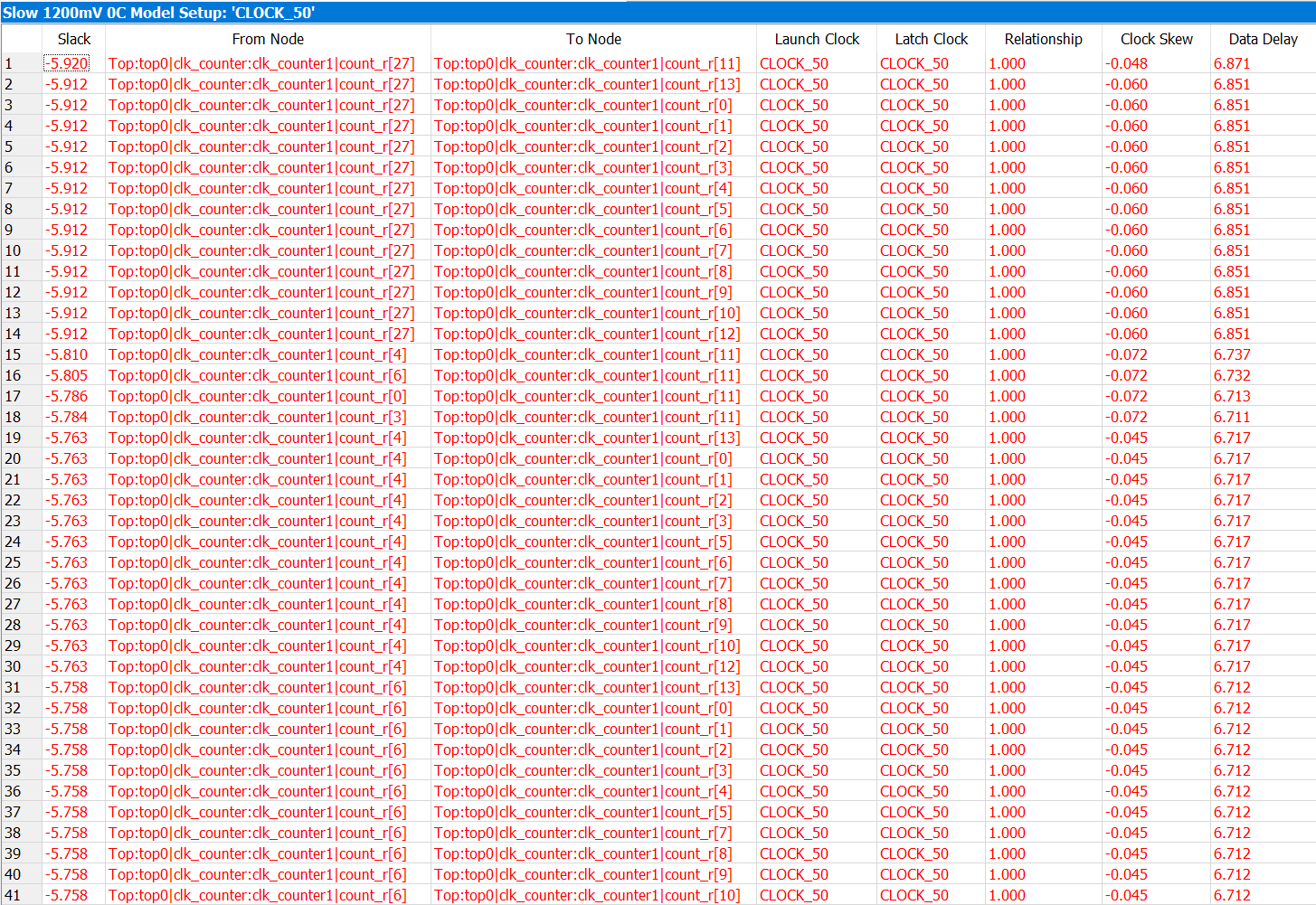
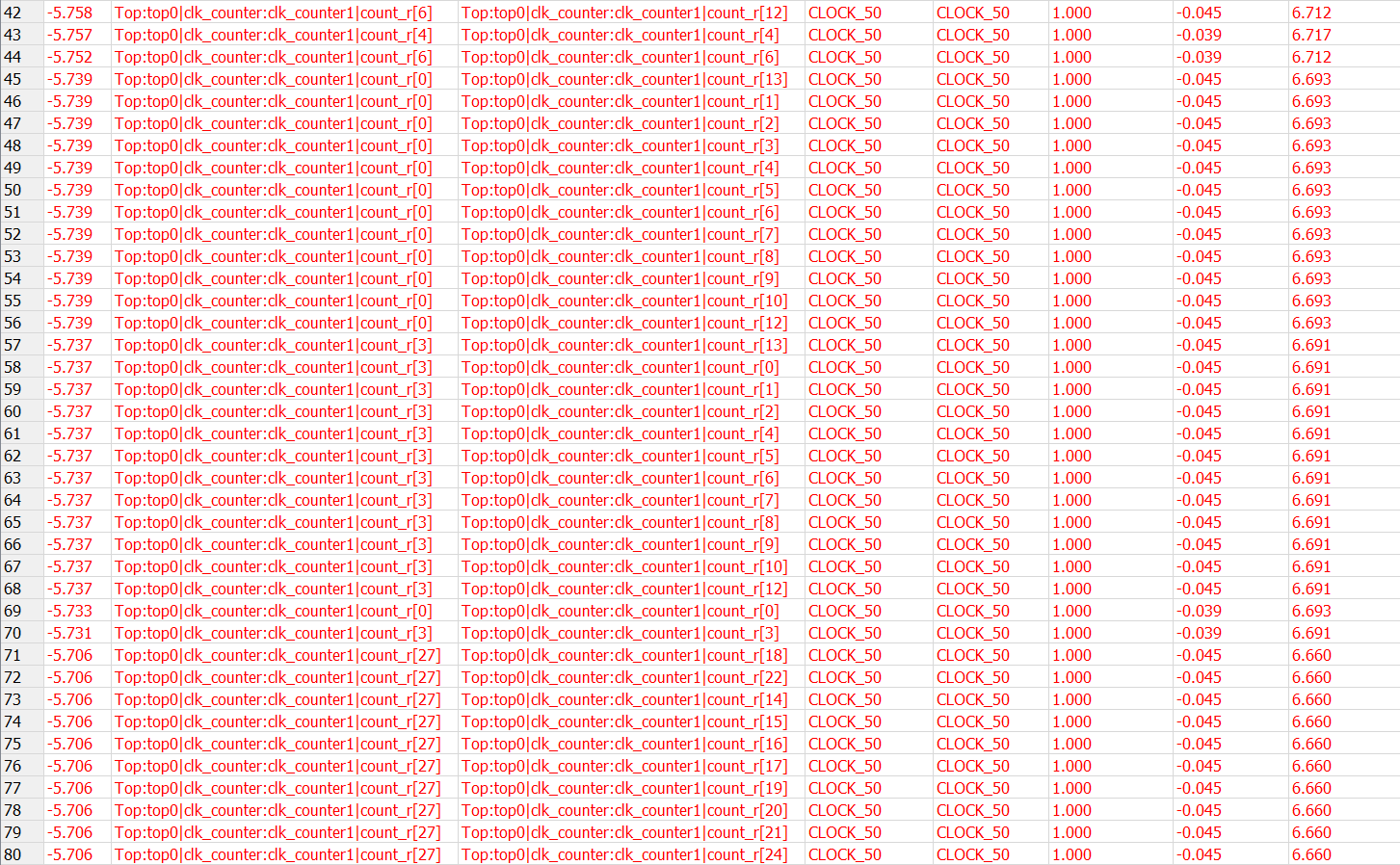
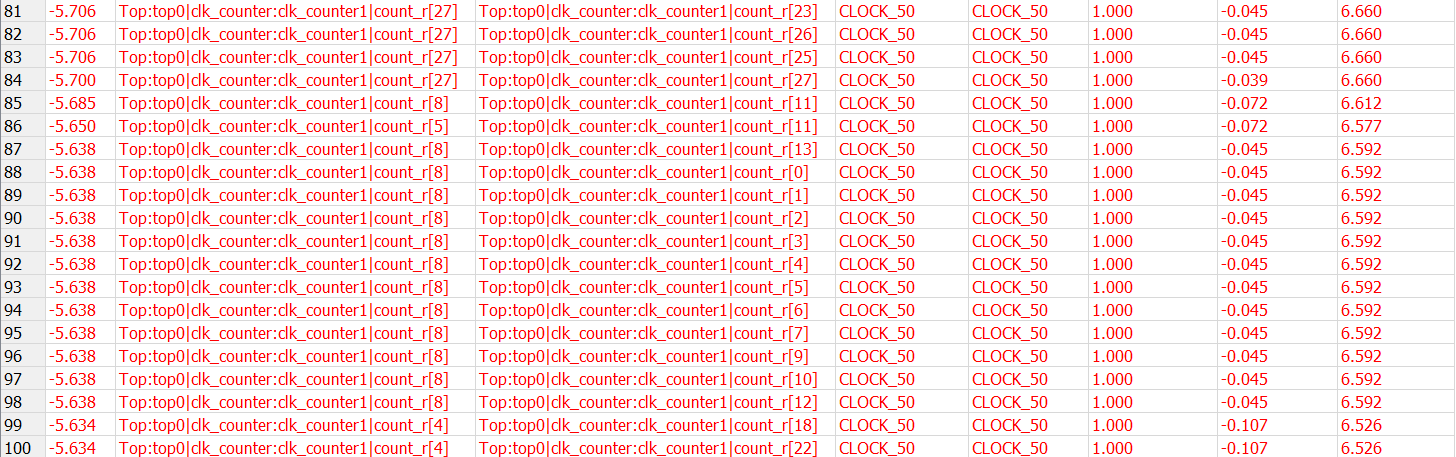


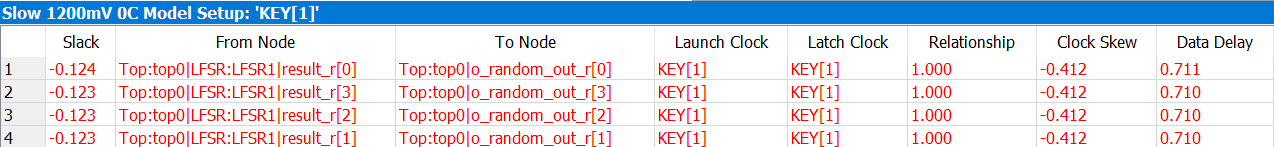
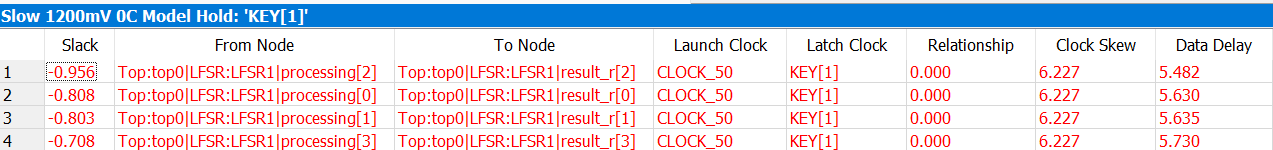
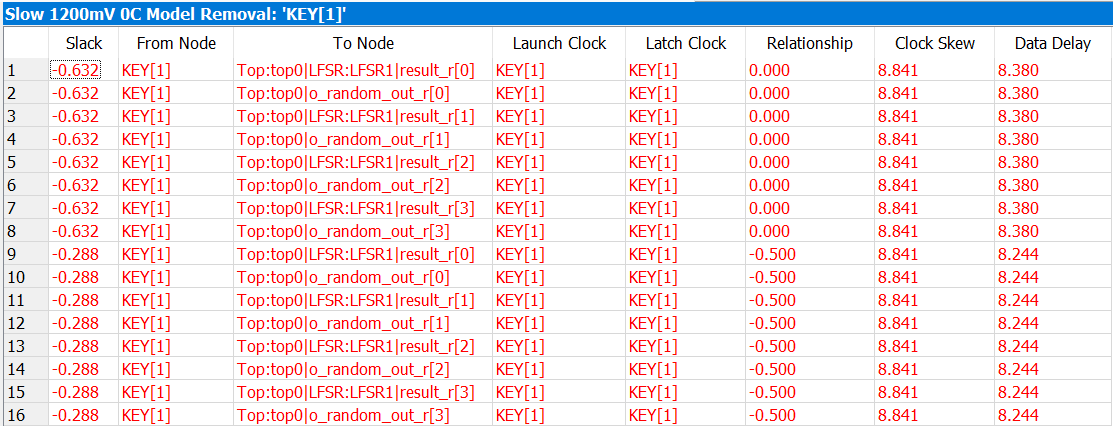
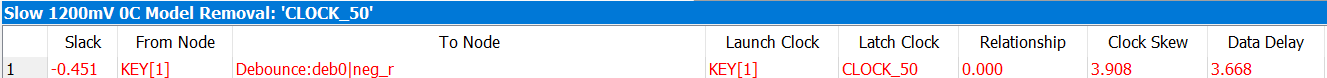
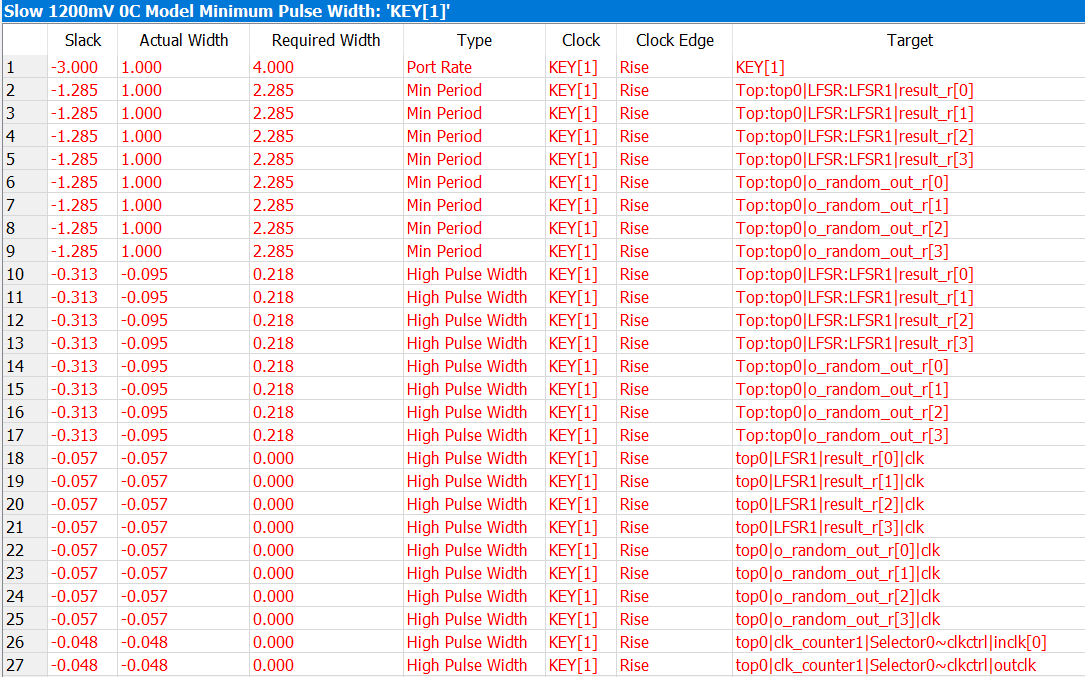


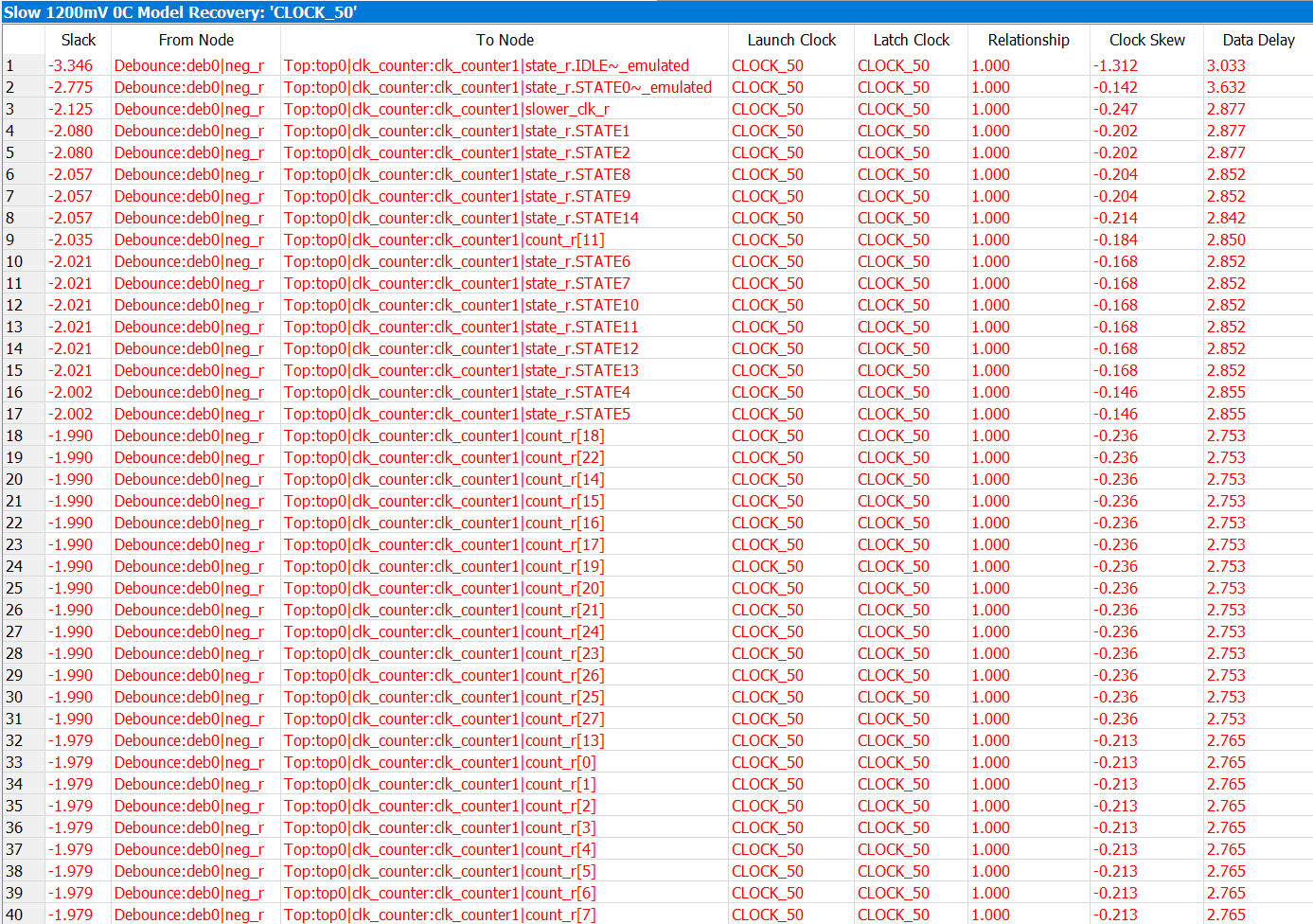
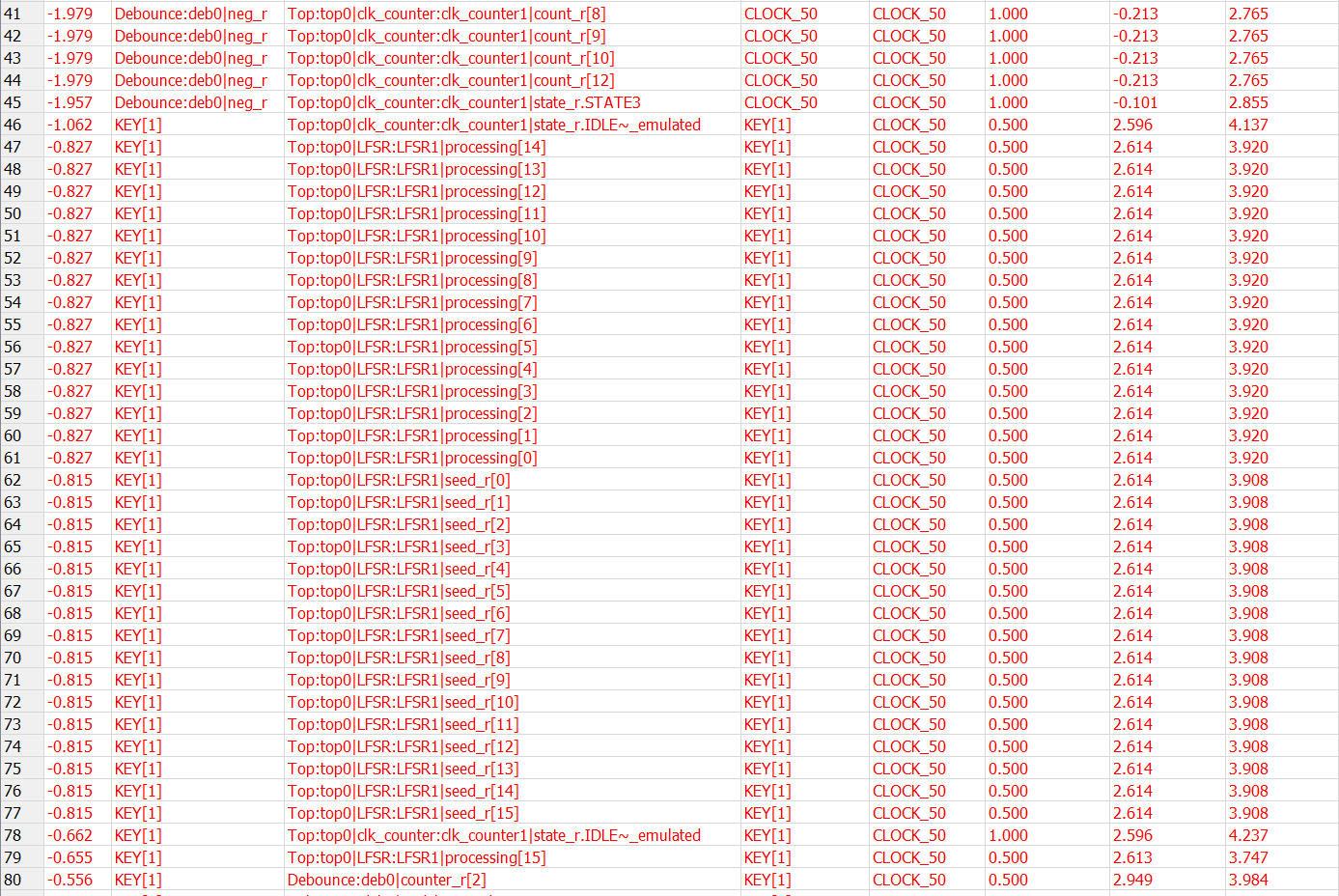
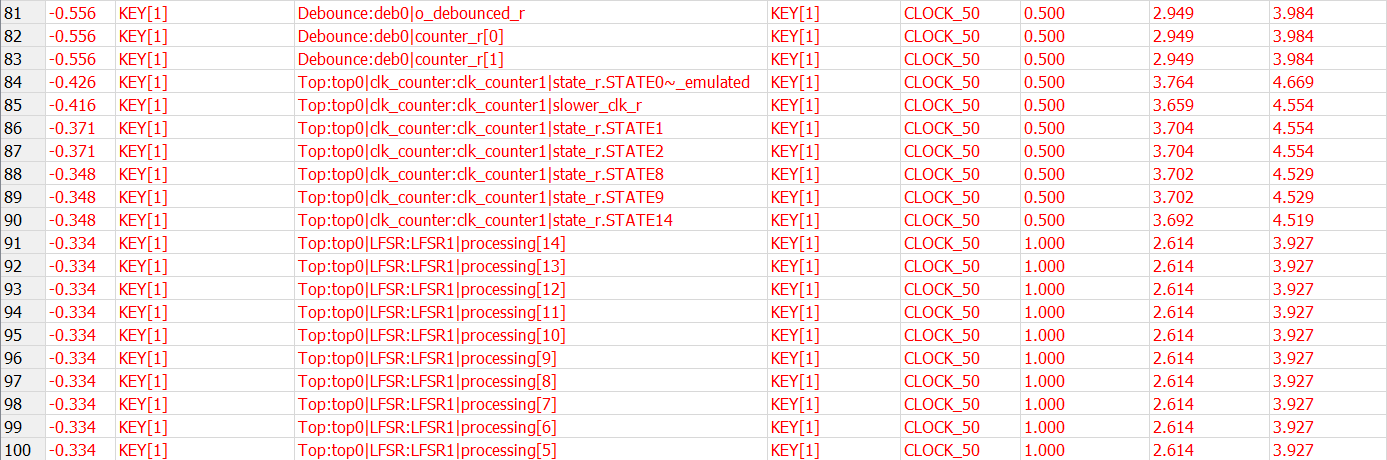


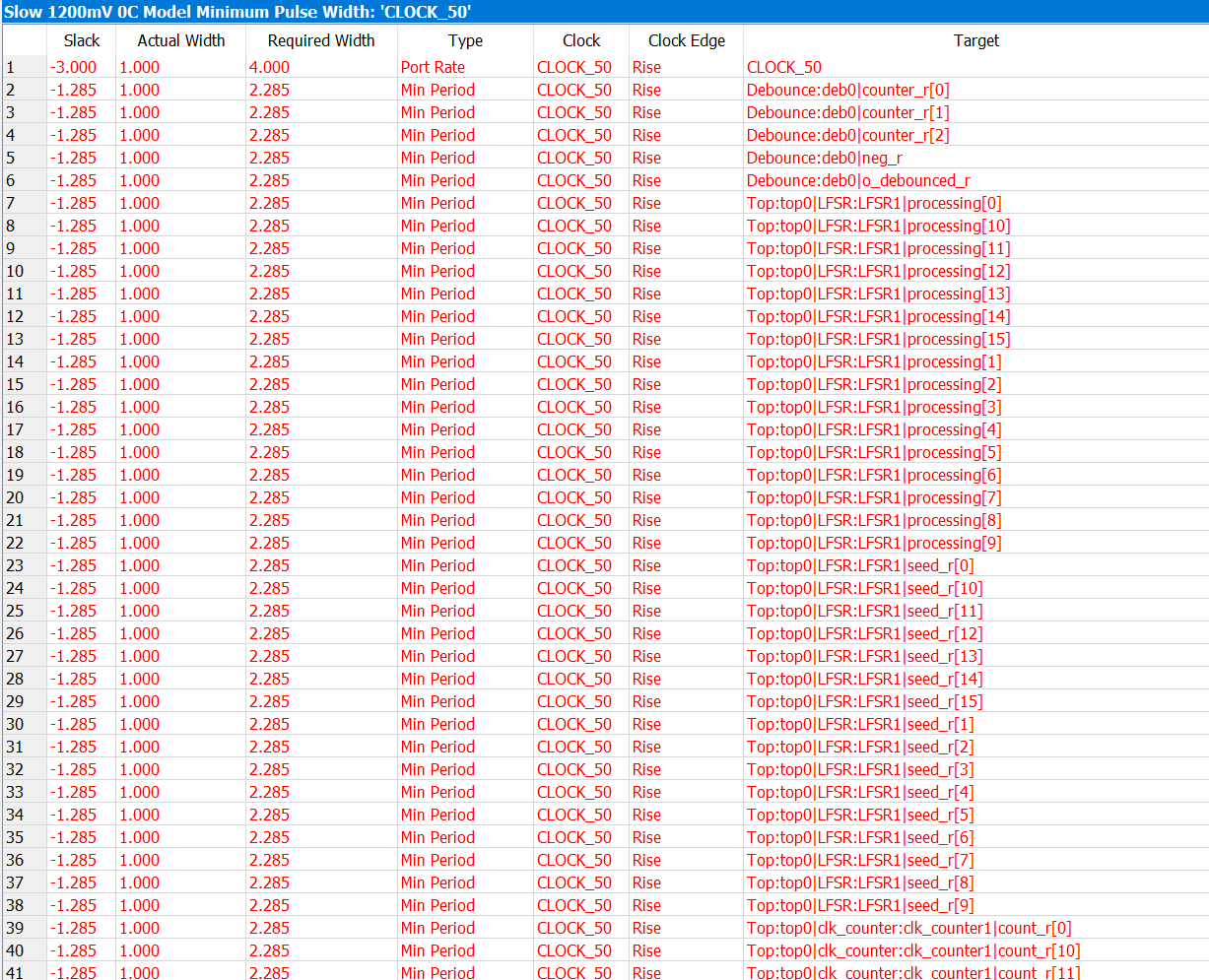




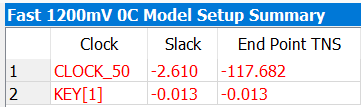
    

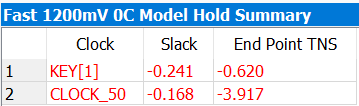
  

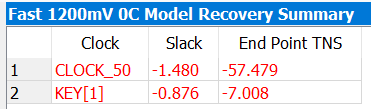
 

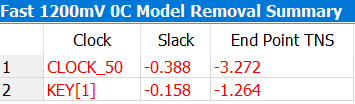


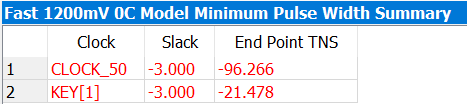
Timing Violation (Fast 1200mV 0C Model)

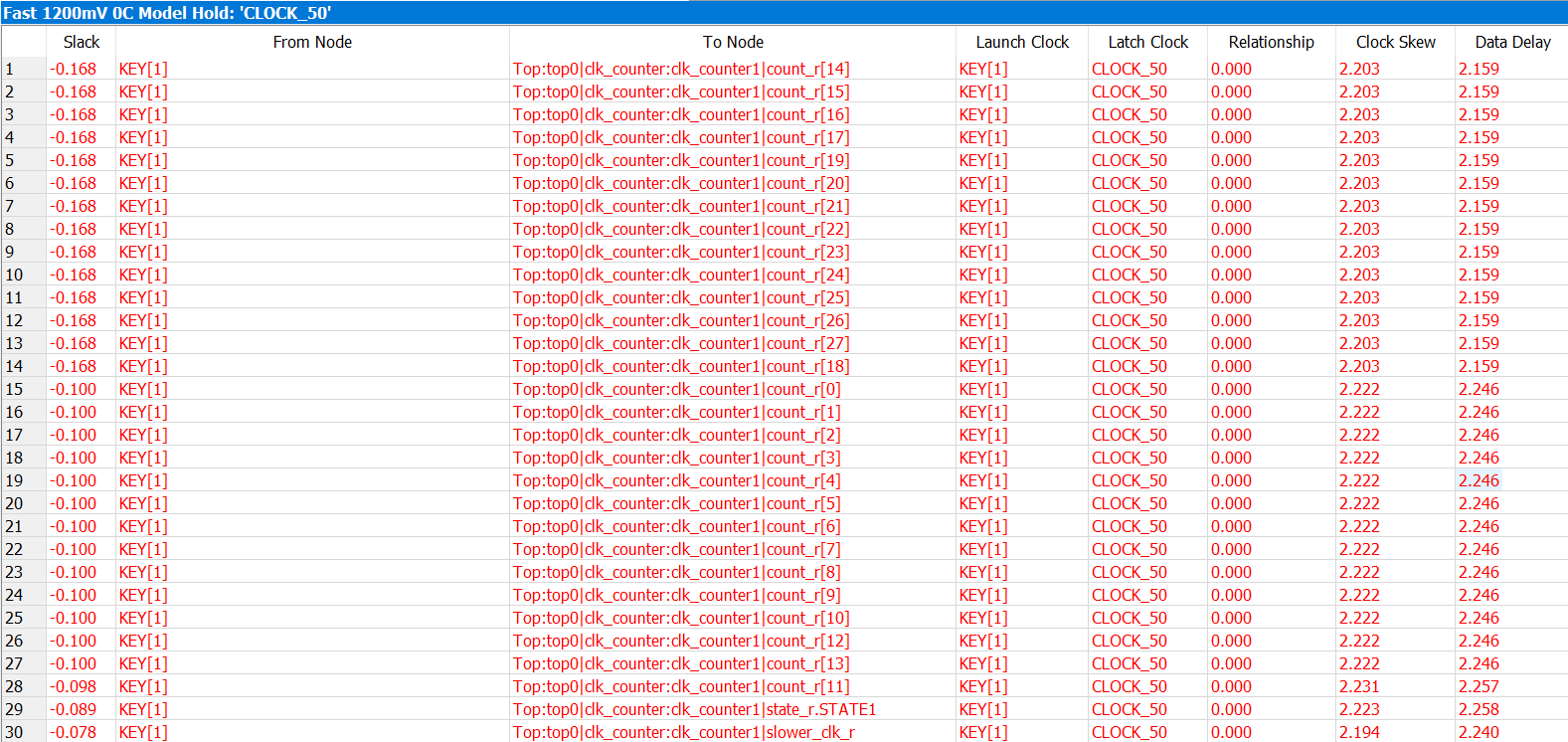


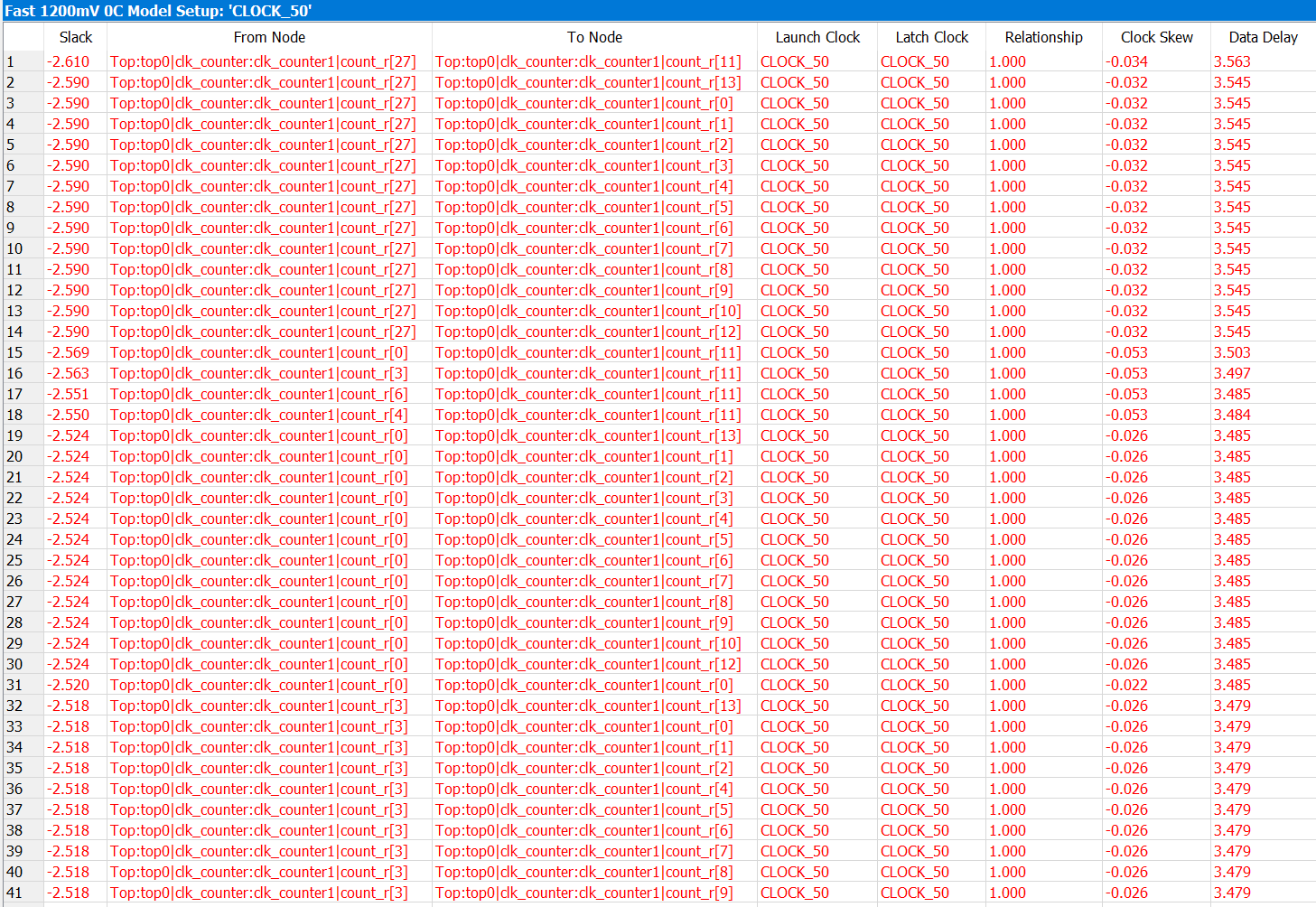
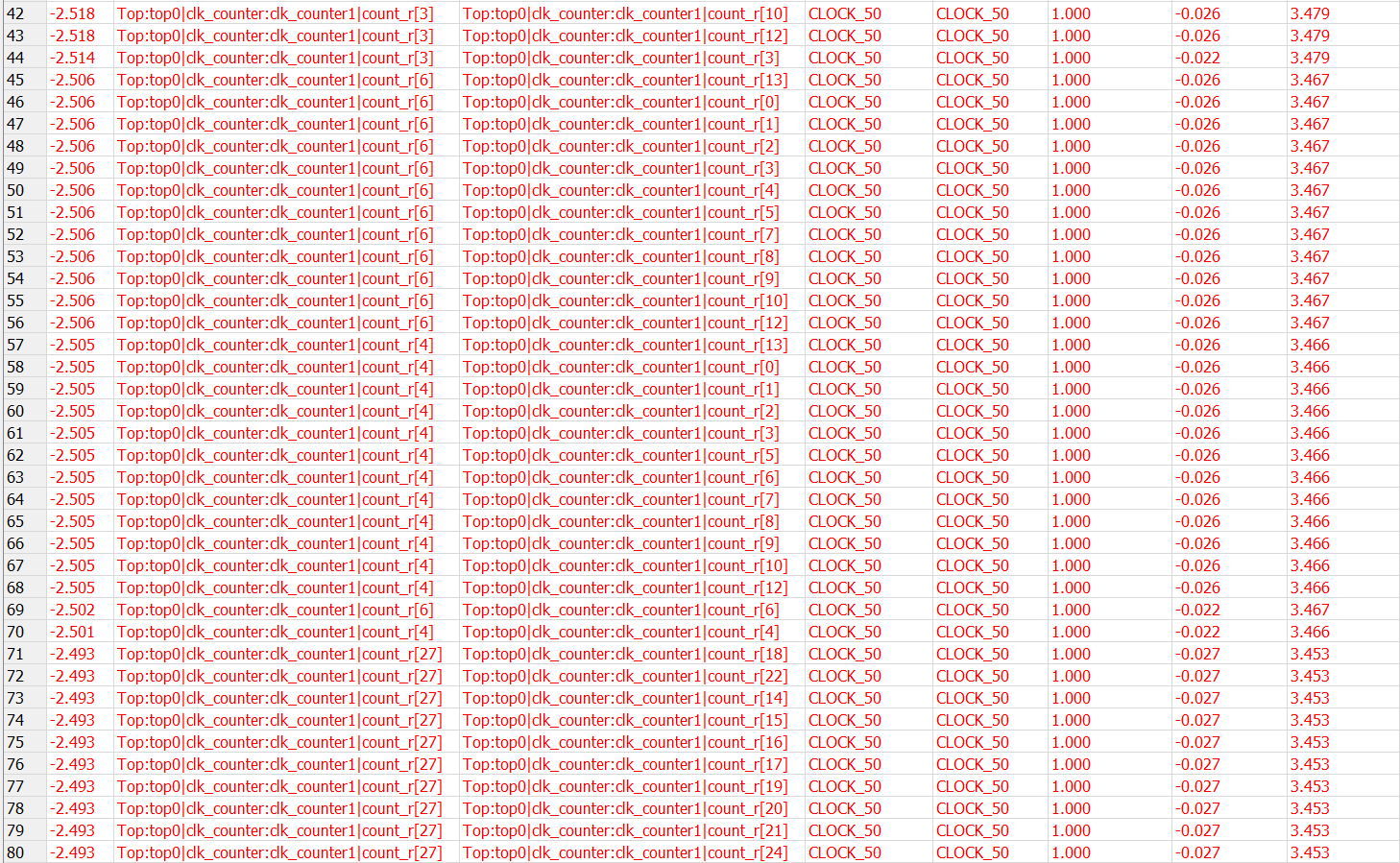
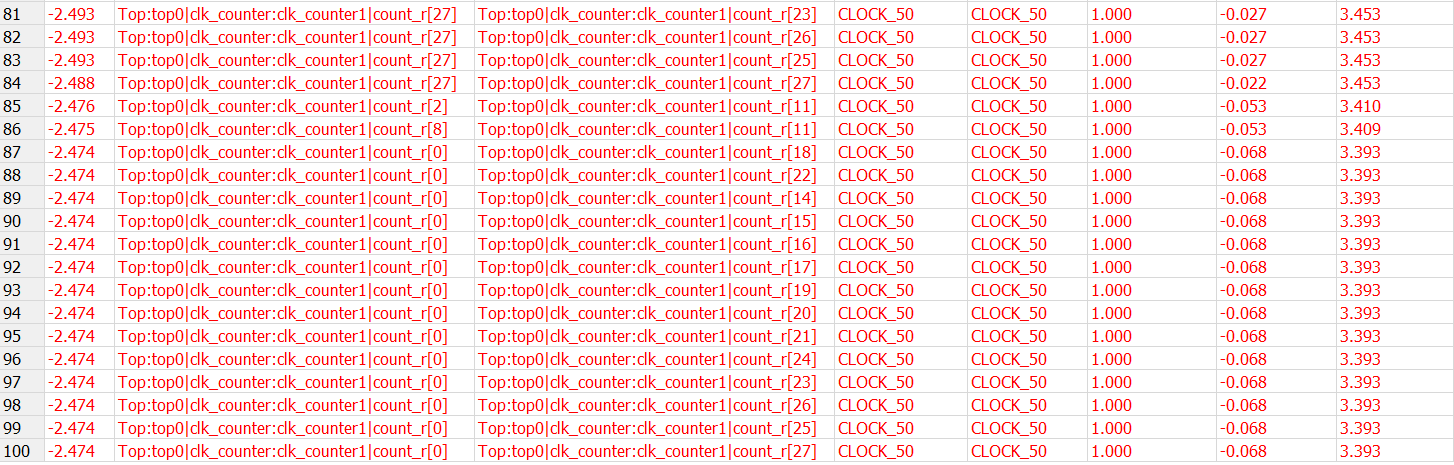


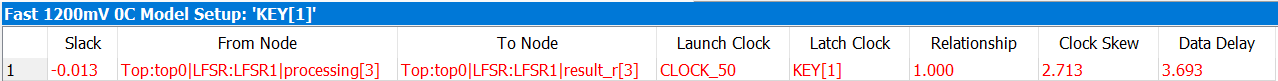
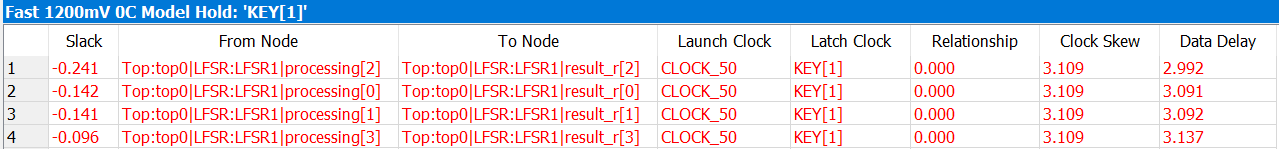
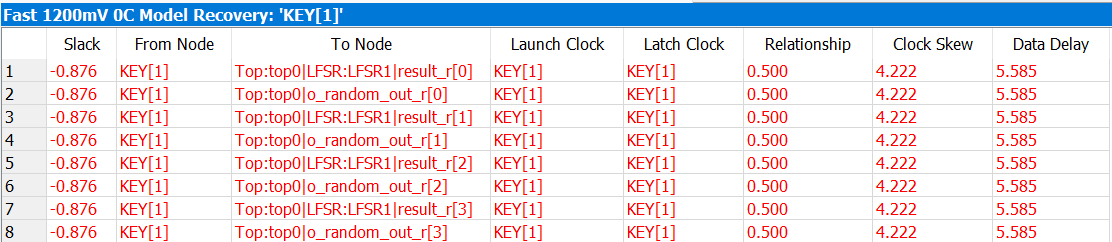
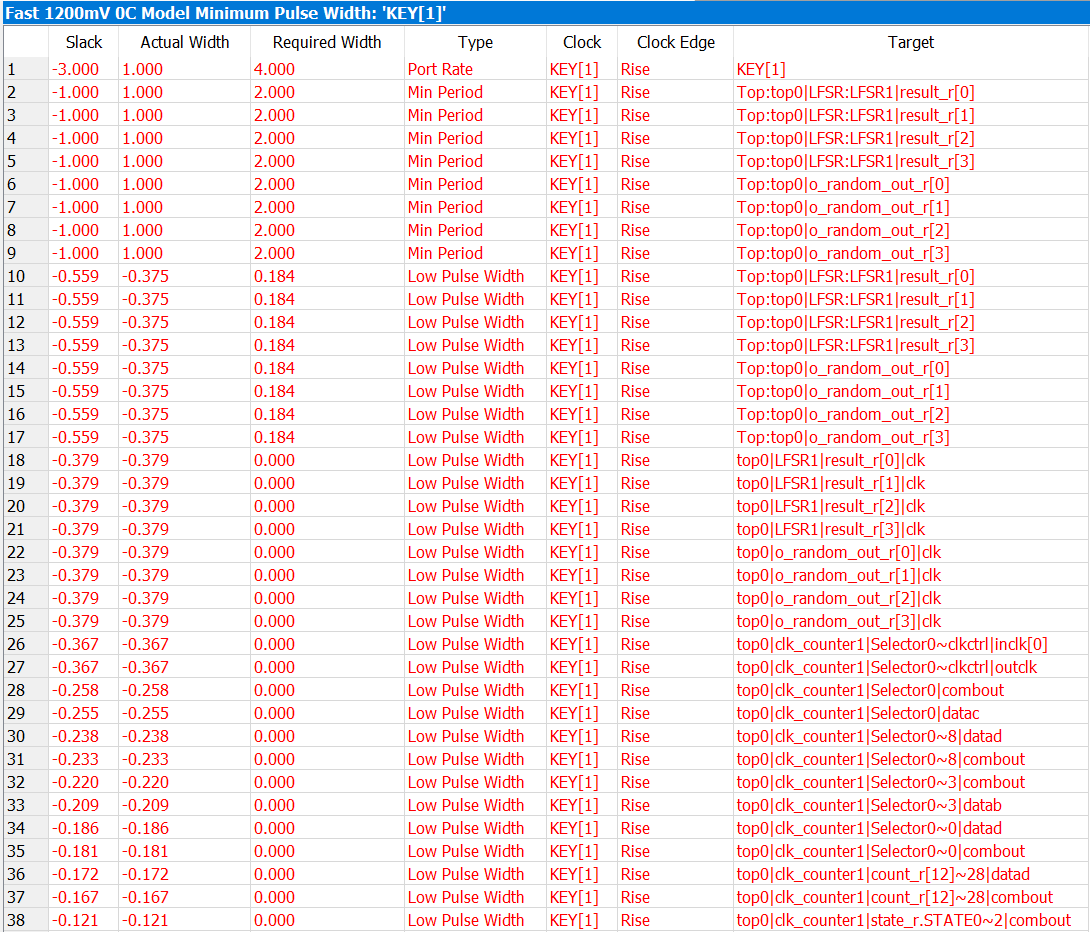


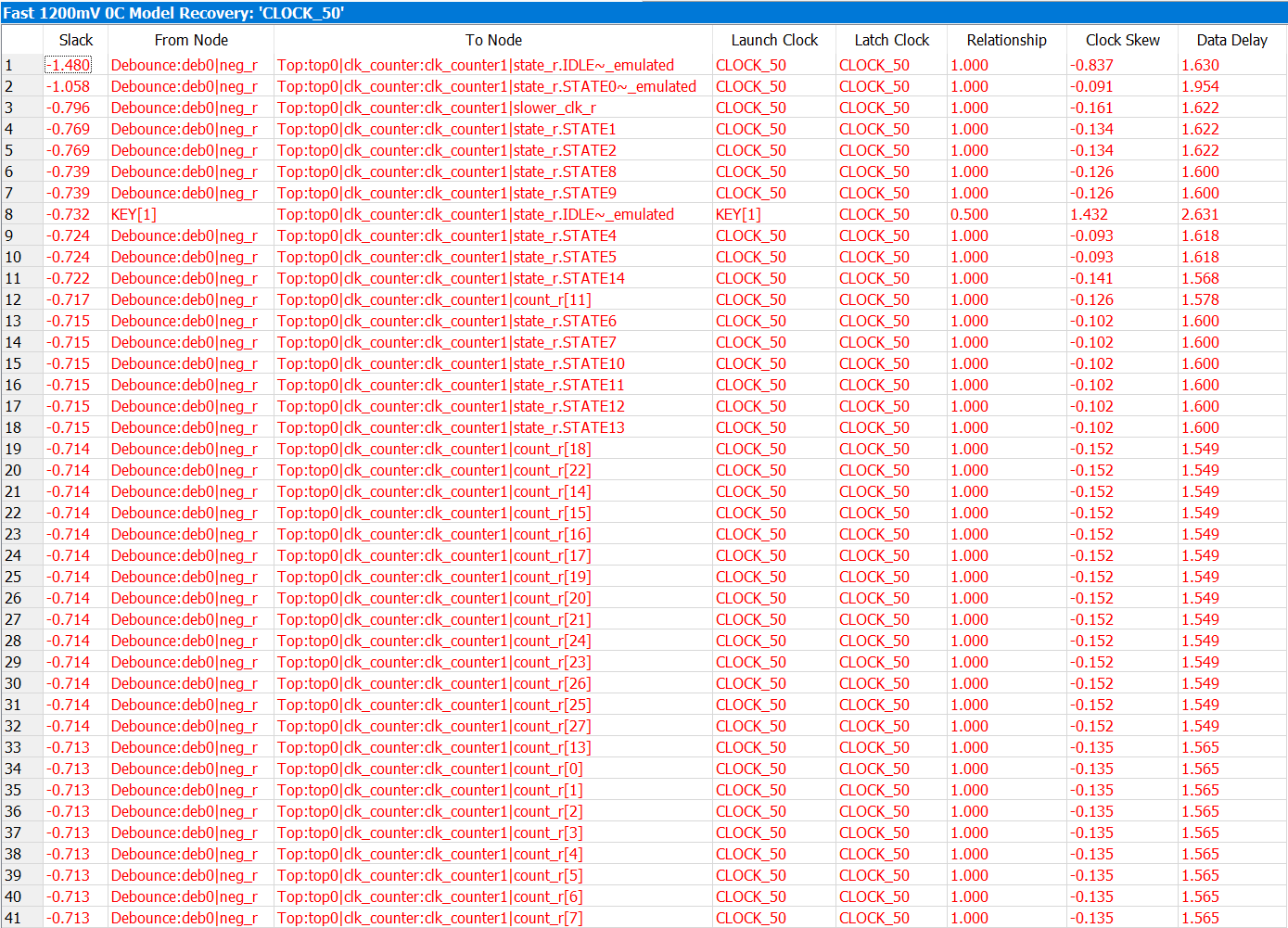
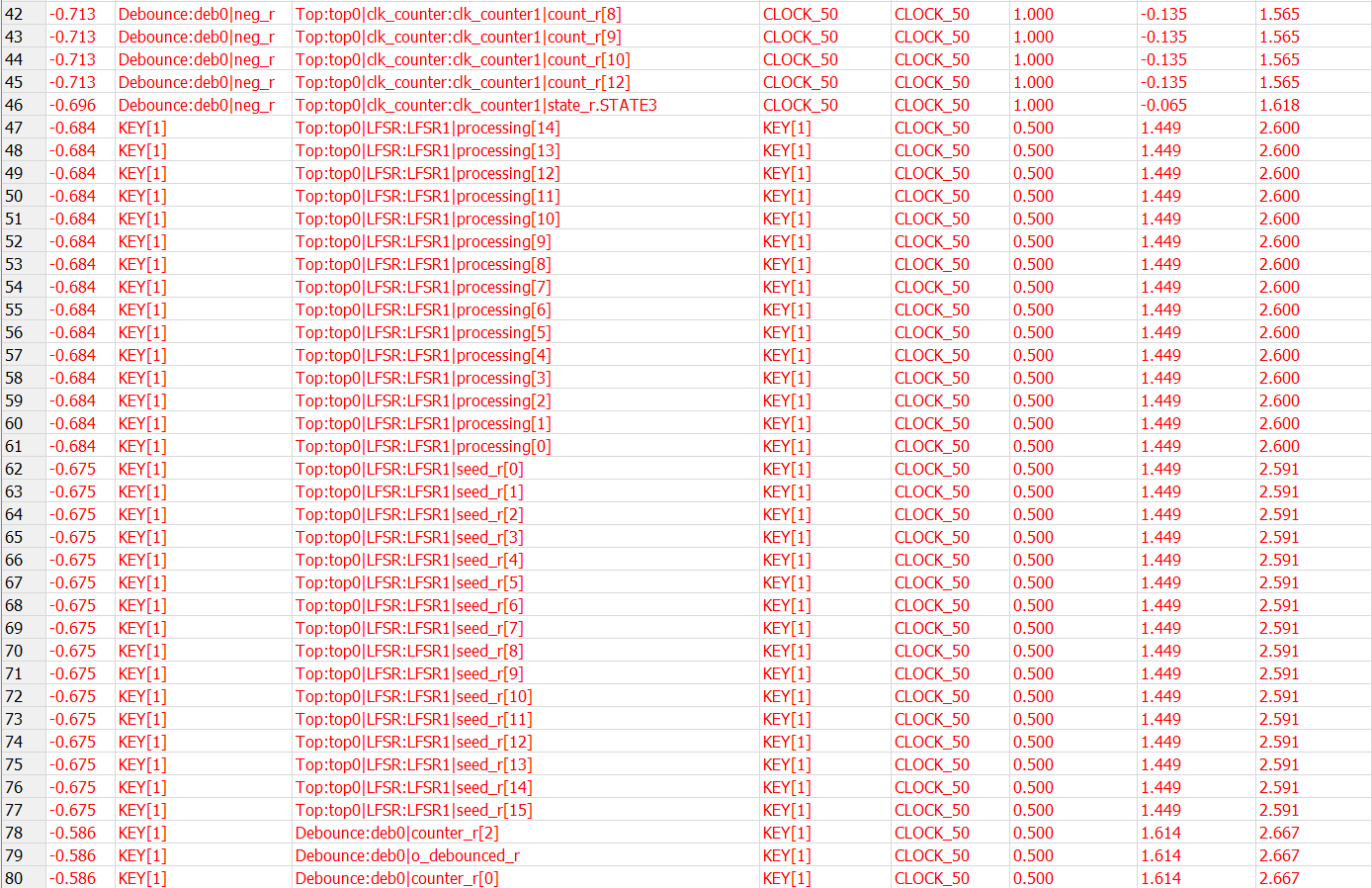
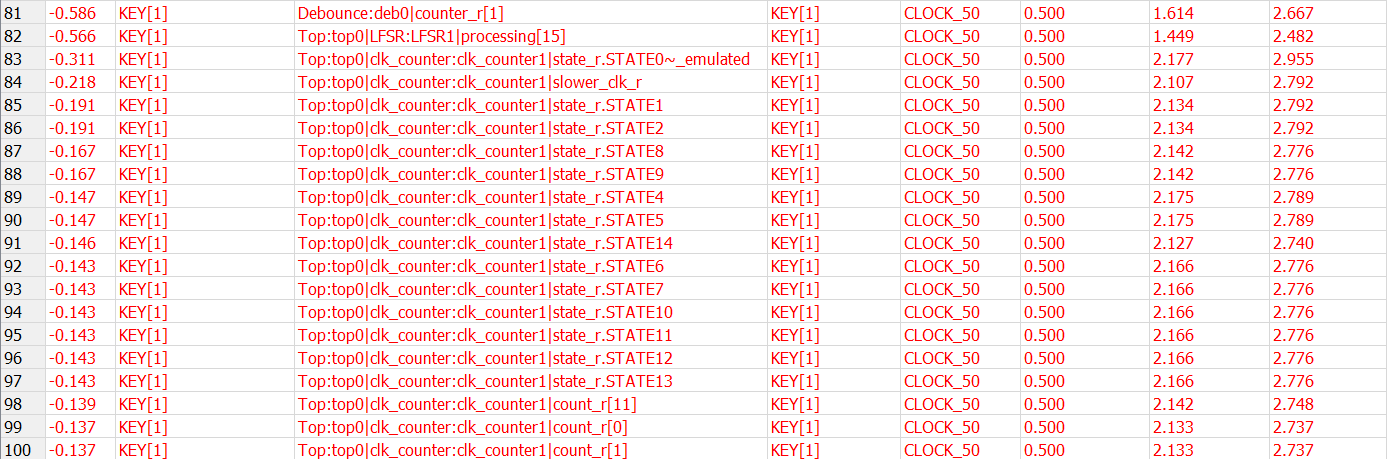


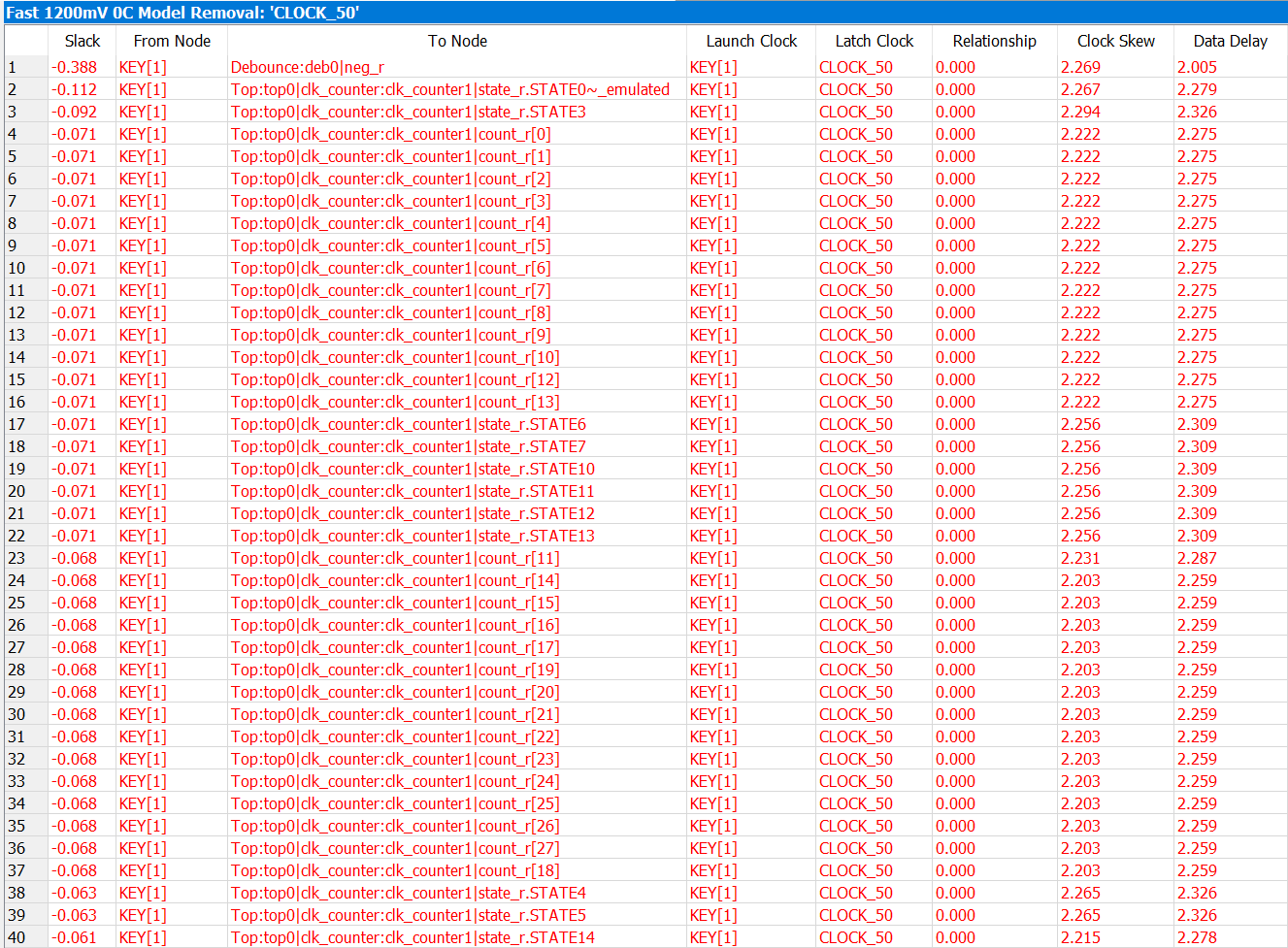
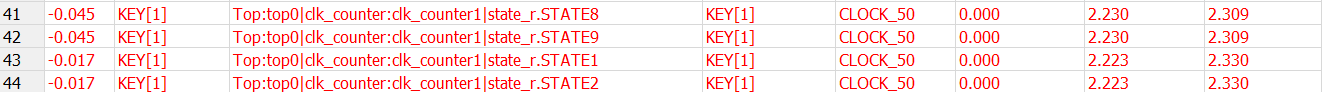


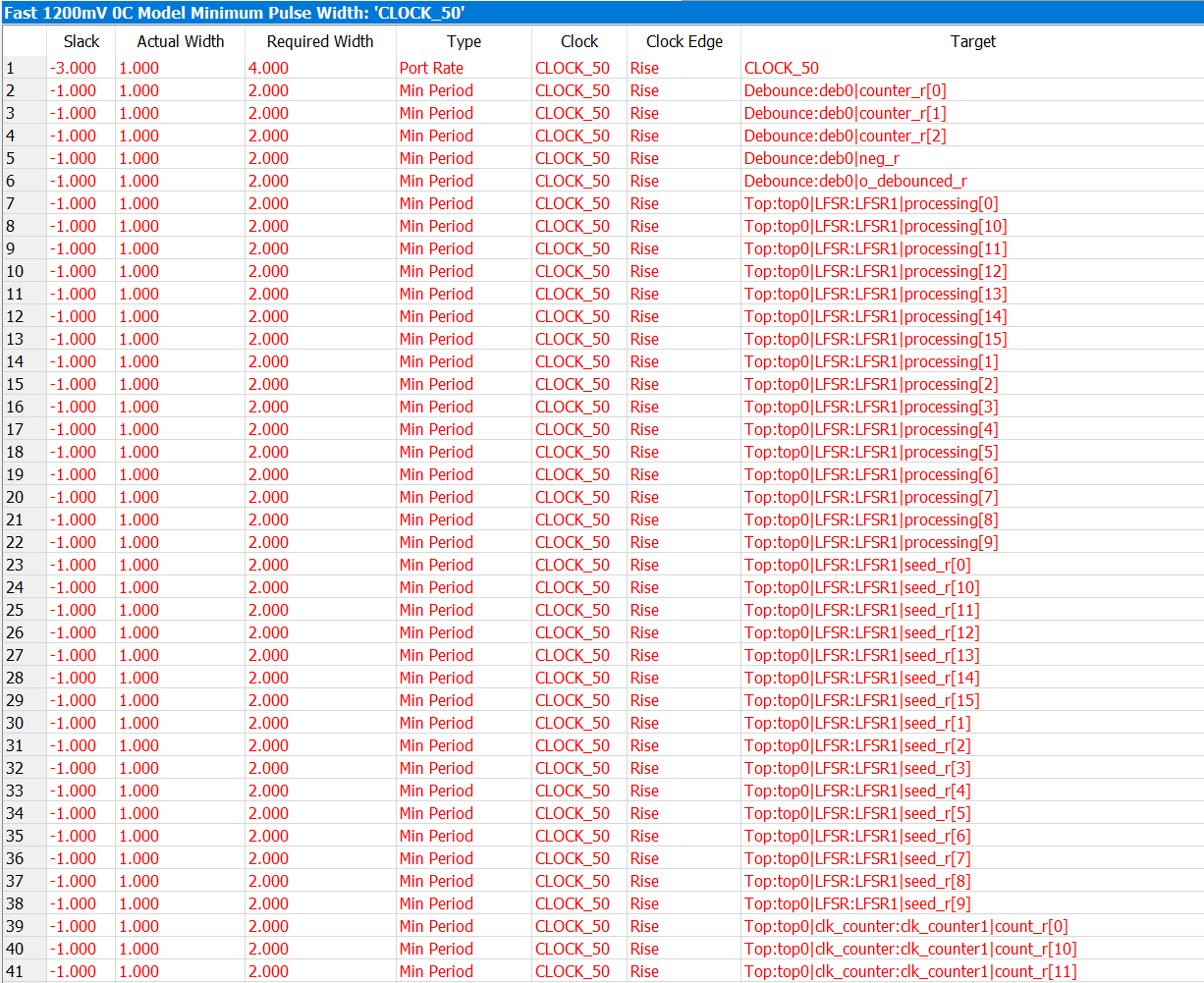
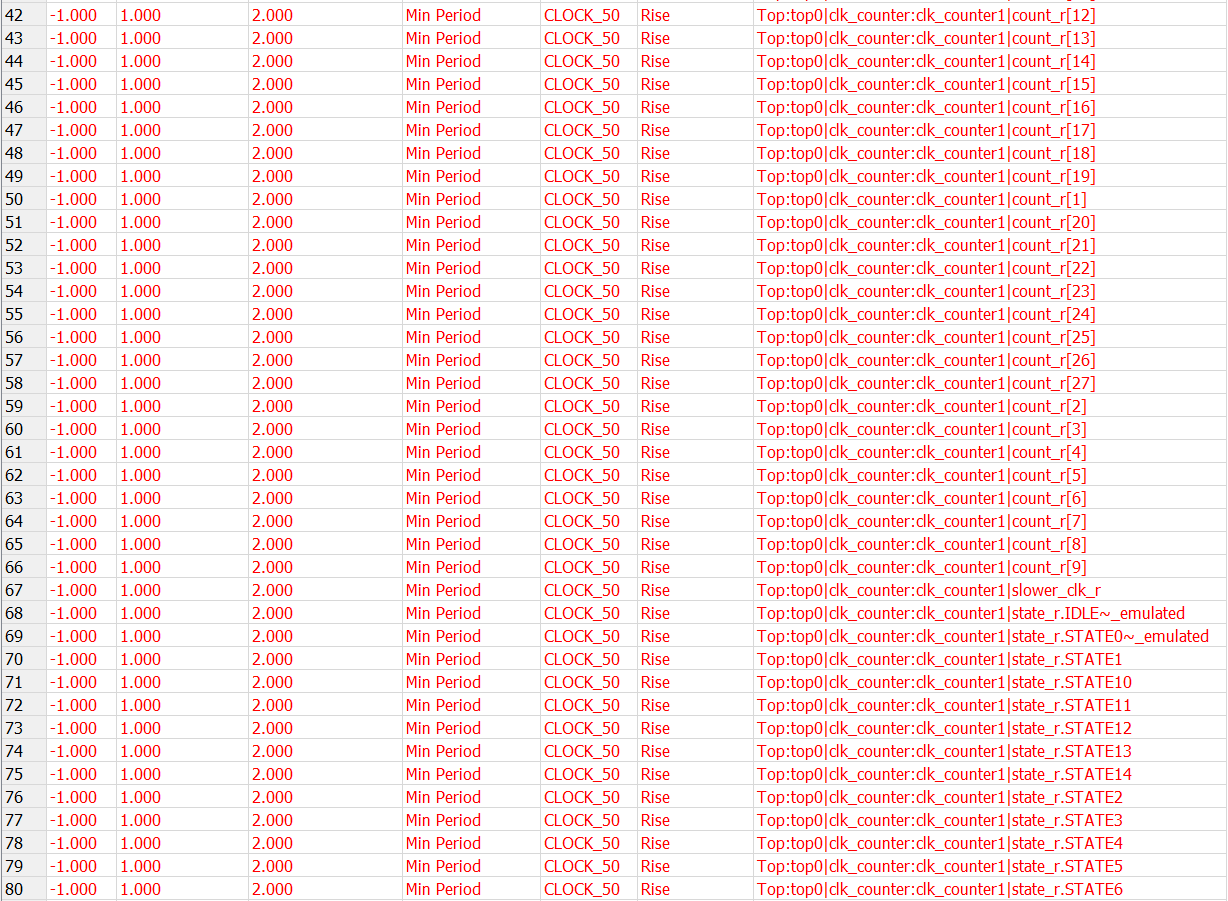




**Part 6: Thoughts**

這次Lab由於我們部分組員對Verilog還在熟悉階段，因此對於許多的硬體設計還沒有很深刻的了解（看看我們timing violation有多少便知），再加上光舞的忙碌情形，使得這次Lab仍有許多改進的地方。我們遇到的最大問題應當是一個值不能同時在兩個不同的always被賦值，以及在一個always當中必須要保證每個state賦值的對稱性。總而言之，這次的Lab讓我們對於硬體的verilog設計有了基本概念，能夠讓下一次的實驗更加順手。