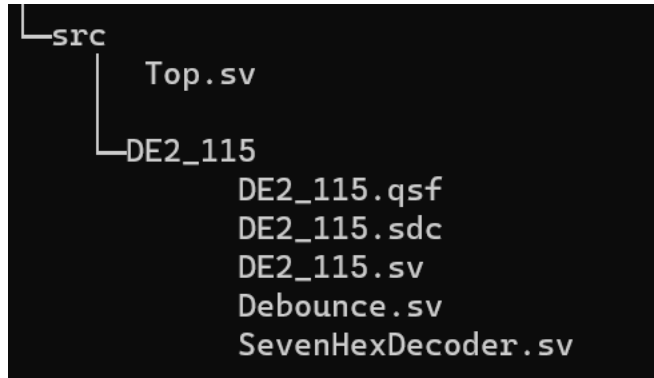


NTUEE DCLAB LAB1

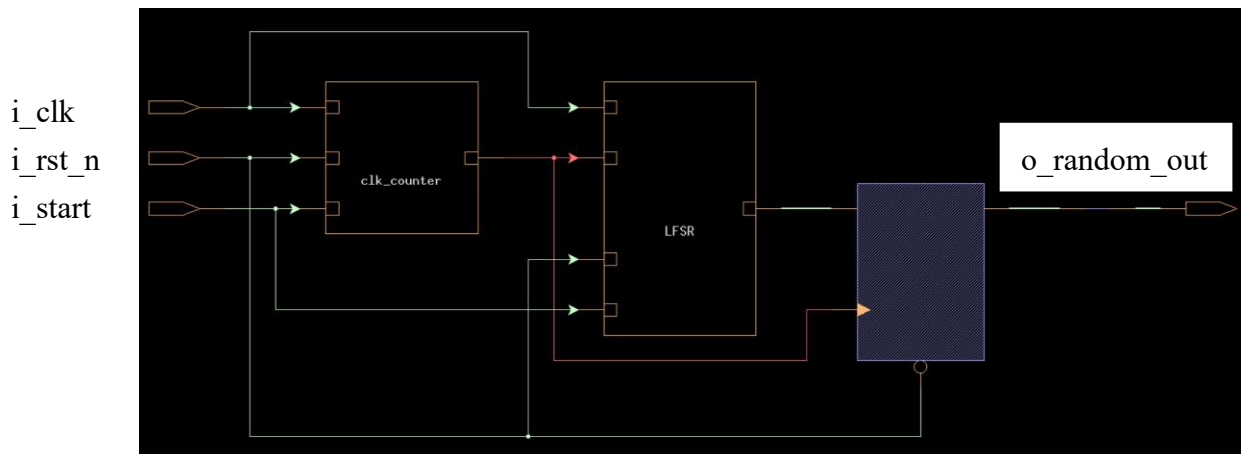
Team 05 陳冠穎、陳楚融、梁璿安

Part 1: File Structure

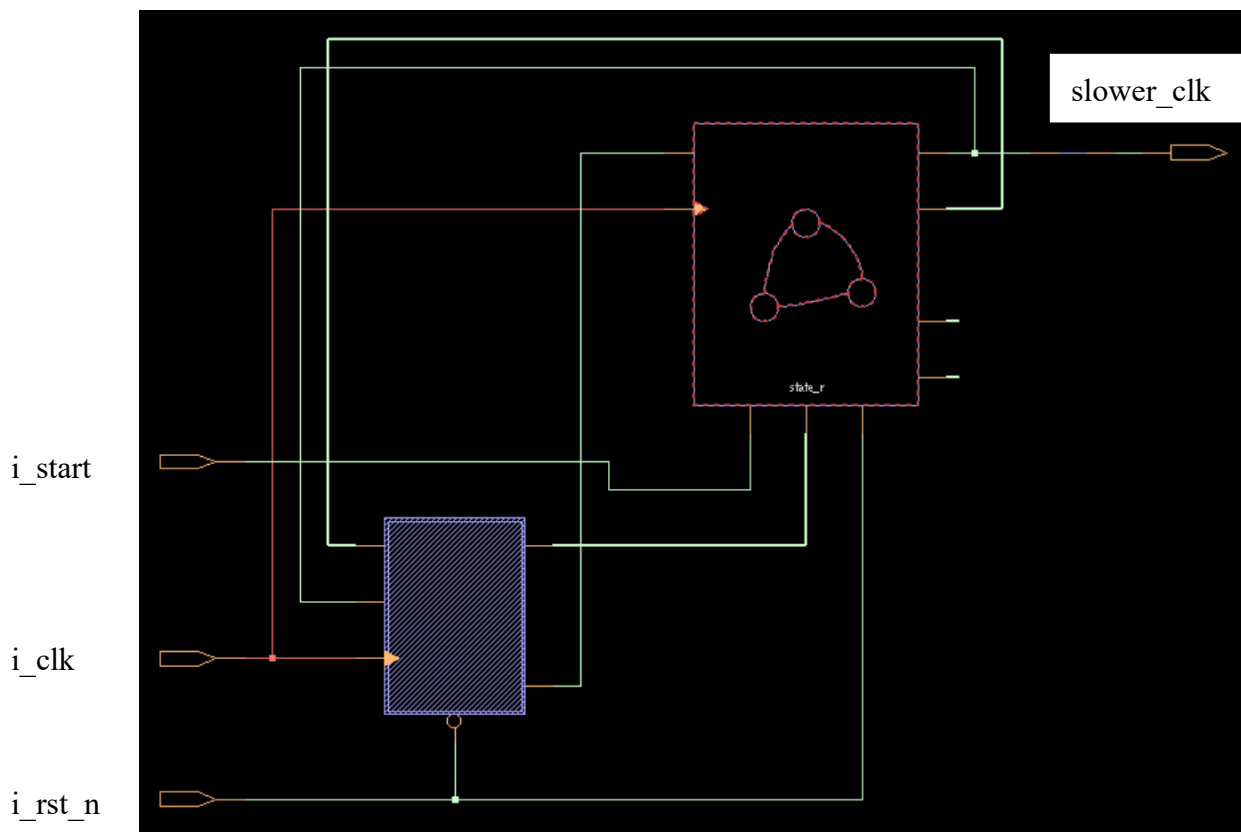


Part 2: System Architecture

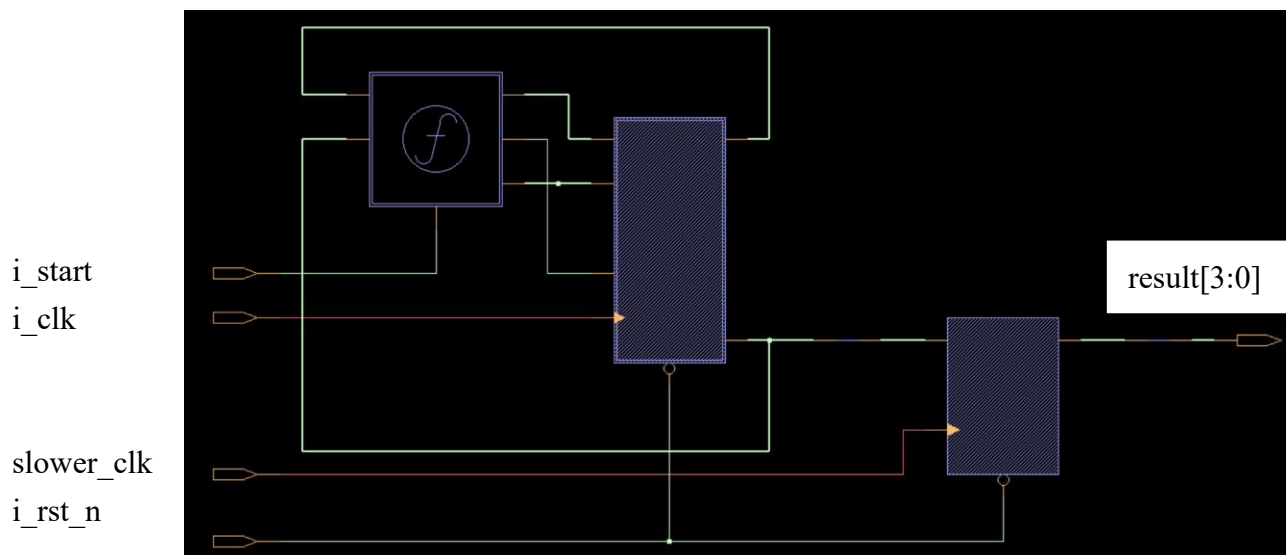
Top:



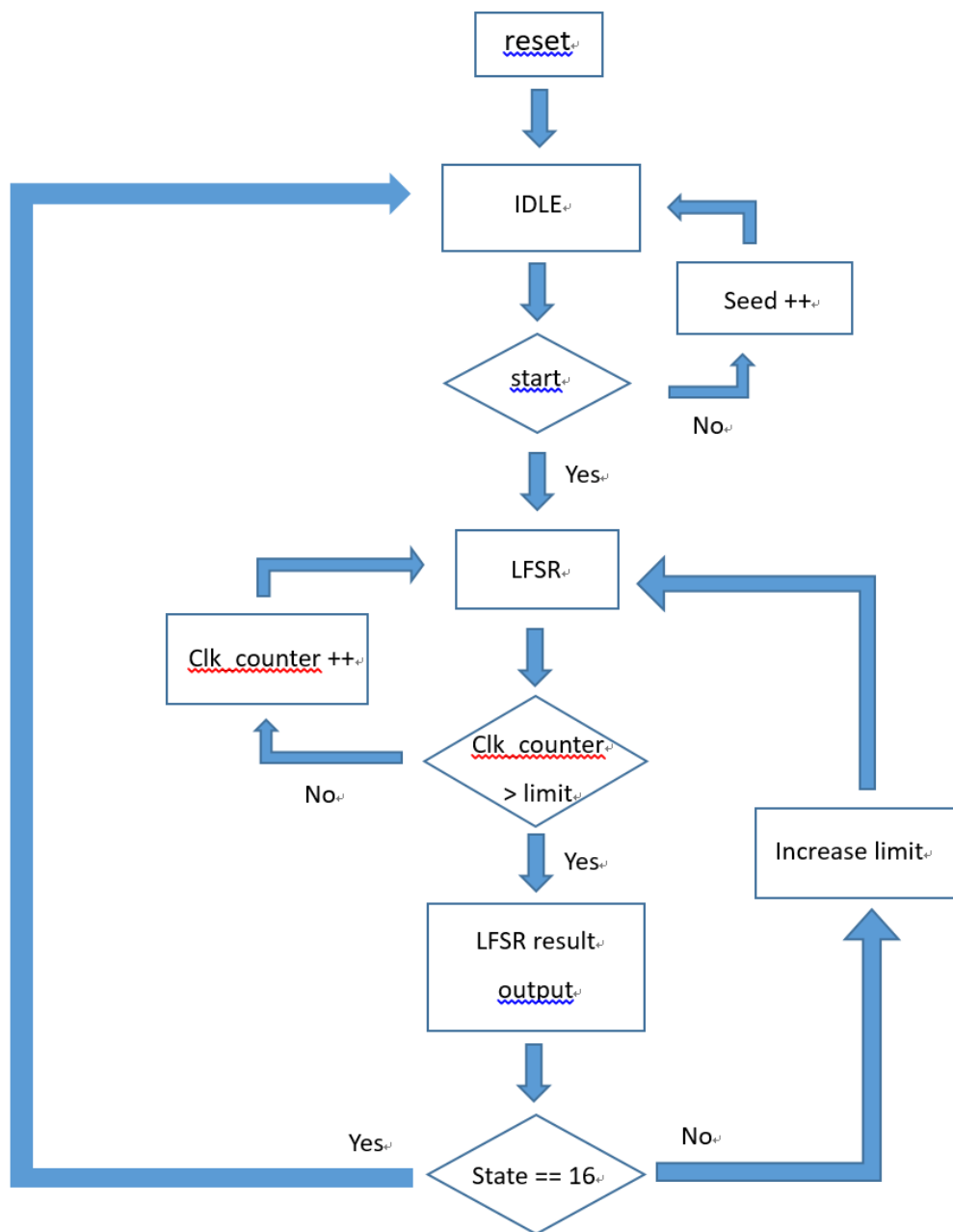
Clk_counter



LFSR



Part 3: Hardware Scheduling



Part 4: Filter Summary

Fitter Summary	
Fitter Status	Successful - Tue Mar 14 12:24:40 2023
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	174 / 114,480 (< 1 %)
Total combinational functions	162 / 114,480 (< 1 %)
Dedicated logic registers	90 / 114,480 (< 1 %)
Total registers	90
Total pins	518 / 529 (98 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Part 5: Timing Analyzer

TimeQuest Timing Analyzer Summary	
Quartus II Version	Version 15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Device Family	Cyclone IV E
Device Name	EP4CE115F29C7
Timing Models	Final
Delay Model	Combined
Rise/Fall Delays	Enabled

Timing Violation (Slow 1200mV 85C Model)

Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-6.480	-320.476
2	KEY[1]	-0.232	-0.925

Slow 1200mV 85C Model Hold Summary

	Clock	Slack	End Point TNS
1	KEY[1]	-0.814	-2.602
2	CLOCK_50	0.312	0.000

Slow 1200mV 85C Model Recovery Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-3.691	-141.566
2	KEY[1]	-0.323	-2.584

Slow 1200mV 85C Model Removal Summary

	Clock	Slack	End Point TNS
1	KEY[1]	-0.664	-5.312
2	CLOCK_50	-0.458	-0.458

Slow 1200mV 85C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-3.000	-108.370
2	KEY[1]	-3.000	-14.576

[illegible]

Slow 1200mV 85C Model Setup: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.232	Top:top0 LFSR:LFSR1 result_r[0]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	1.000	-0.440	0.790
2	-0.231	Top:top0 LFSR:LFSR1 result_r[3]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	1.000	-0.440	0.789
3	-0.231	Top:top0 LFSR:LFSR1 result_r[2]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	1.000	-0.440	0.789
4	-0.231	Top:top0 LFSR:LFSR1 result_r[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	1.000	-0.440	0.789

Slow 1200mV 85C Model Hold: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.814	Top:top0 LFSR:LFSR1 processing[2]	Top:top0 LFSR:LFSR1 result_r[2]	CLOCK_50	KEY[1]	0.000	6.663	6.075
2	-0.636	Top:top0 LFSR:LFSR1 processing[1]	Top:top0 LFSR:LFSR1 result_r[1]	CLOCK_50	KEY[1]	0.000	6.663	6.253
3	-0.624	Top:top0 LFSR:LFSR1 processing[0]	Top:top0 LFSR:LFSR1 result_r[0]	CLOCK_50	KEY[1]	0.000	6.663	6.265
4	-0.528	Top:top0 LFSR:LFSR1 processing[3]	Top:top0 LFSR:LFSR1 result_r[3]	CLOCK_50	KEY[1]	0.000	6.663	6.361

Slow 1200mV 85C Model Recovery: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.323	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	0.500	8.830	9.651
2	-0.323	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	0.500	8.830	9.651
3	-0.323	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	0.500	8.830	9.651
4	-0.323	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	0.500	8.830	9.651
5	-0.323	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	0.500	8.830	9.651
6	-0.323	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	0.500	8.830	9.651
7	-0.323	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	0.500	8.830	9.651
8	-0.323	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	0.500	8.830	9.651

Slow 1200mV 85C Model Removal: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.664	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	0.000	9.549	9.071
2	-0.664	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	0.000	9.549	9.071
3	-0.664	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	0.000	9.549	9.071
4	-0.664	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	0.000	9.549	9.071
5	-0.664	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	0.000	9.549	9.071
6	-0.664	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	0.000	9.549	9.071
7	-0.664	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	0.000	9.549	9.071
8	-0.664	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	0.000	9.549	9.071
9	-0.018	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	-0.500	9.549	9.237
10	-0.018	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	-0.500	9.549	9.237
11	-0.018	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	-0.500	9.549	9.237
12	-0.018	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	-0.500	9.549	9.237
13	-0.018	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	-0.500	9.549	9.237
14	-0.018	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	-0.500	9.549	9.237
15	-0.018	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	-0.500	9.549	9.237
16	-0.018	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	-0.500	9.549	9.237

Slow 1200mV 85C Model Removal: 'CLOCK_50'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.458	KEY[1]	Debounce:deb0 neg_r	KEY[1]	CLOCK_50	0.000	4.290	4.058

Slow 1200mV 85C Model Minimum Pulse Width: 'KEY[1]'							
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	KEY[1]	Rise	KEY[1]
2	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]
3	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]
4	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]
5	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]
6	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[0]
7	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[1]
8	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[2]
9	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[3]
10	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]
11	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]
12	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]
13	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]
14	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[0]
15	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[1]
16	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[2]
17	-0.093	0.095	0.188	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[3]
18	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]
19	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]
20	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]
21	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]
22	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[0]
23	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[1]
24	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[2]
25	-0.069	0.151	0.220	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[3]

Slow 1200mV 85C Model Recovery: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	3.691	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.IDLE~_emulated	CLOCK_50	CLOCK_50	1,000	-1.421	3.268
2	-3.073	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE0~_emulated	CLOCK_50	CLOCK_50	1,000	-0.161	3.910
3	-2.444	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 slower_dk_r	CLOCK_50	CLOCK_50	1,000	-0.279	3.163
4	-2.392	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE1	CLOCK_50	CLOCK_50	1,000	-0.227	3.163
5	-2.392	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE2	CLOCK_50	CLOCK_50	1,000	-0.227	3.163
6	-2.375	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE8	CLOCK_50	CLOCK_50	1,000	-0.240	3.133
7	-2.375	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE9	CLOCK_50	CLOCK_50	1,000	-0.240	3.133
8	-2.341	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE4	CLOCK_50	CLOCK_50	1,000	-0.166	3.173
9	-2.341	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE5	CLOCK_50	CLOCK_50	1,000	-0.166	3.173
10	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[18]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
11	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[22]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
12	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[14]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
13	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[15]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
14	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[16]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
15	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[17]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
16	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[19]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
17	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[20]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
18	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[21]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
19	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[23]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
20	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[24]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
21	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[26]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
22	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[25]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
23	-2.333	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[27]	CLOCK_50	CLOCK_50	1,000	-0.264	3.067
24	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE6	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
25	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE7	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
26	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE10	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
27	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE11	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
28	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE12	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
29	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE13	CLOCK_50	CLOCK_50	1,000	-0.196	3.133
30	-2.331	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 state_r.STATE14	CLOCK_50	CLOCK_50	1,000	-0.239	3.090
31	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[13]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
32	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[0]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
33	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[1]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
34	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[2]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
35	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[3]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
36	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[4]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
37	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[5]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
38	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[6]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074
39	-2.312	Debounce:deb0 neg_r	Top:top0 dk_counter:dk_counter1 count_r[7]	CLOCK_50	CLOCK_50	1,000	-0.236	3.074

Slow 1200mV 85C Model Minimum Pulse Width: 'CLOCK_50'							
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	CLOCK_50	Rise	CLOCK_50
2	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[0]
3	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[1]
4	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[2]
5	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 neg_r
6	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 o_debounced_r
7	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[0]
8	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[10]
9	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[11]
10	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[12]
11	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[13]
12	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[14]
13	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[15]
14	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[1]
15	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[2]
16	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[3]
17	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[4]
18	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[5]
19	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[6]
20	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[7]
21	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[8]
22	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[9]
23	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[0]
24	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[10]
25	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[11]
26	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[12]
27	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[13]
28	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[14]
29	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[15]
30	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[1]
31	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[2]
32	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[3]
33	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[4]
34	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[5]
35	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[6]
36	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[7]
37	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[8]
38	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[9]
39	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[0]
40	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[10]
41	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[11]
42	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[12]
43	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[13]
44	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[14]
45	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[15]
46	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[16]
47	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1 count_r[17]
48	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:dk_counter1

Timing Violation (Slow 1200mV 0C Model)

Slow 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-5.920	-288.961
2	KEY[1]	-0.124	-0.493

Slow 1200mV 0C Model Hold Summary

	Clock	Slack	End Point TNS
1	KEY[1]	-0.956	-3.275
2	CLOCK_50	0.342	0.000

Slow 1200mV 0C Model Recovery Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-3.346	-120.610
2	KEY[1]	0.068	0.000

Slow 1200mV 0C Model Removal Summary

	Clock	Slack	End Point TNS
1	KEY[1]	-0.632	-5.056
2	CLOCK_50	-0.451	-0.451

Slow 1200mV 0C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-3.000	-108.370
2	KEY[1]	-3.000	-16.336

[illegible]

Slow 1200mV 0C Model Setup: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.124	Top:top0 LFSR:LFSR1 result_r[0]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	1.000	-0.412	0.711
2	-0.123	Top:top0 LFSR:LFSR1 result_r[3]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	1.000	-0.412	0.710
3	-0.123	Top:top0 LFSR:LFSR1 result_r[2]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	1.000	-0.412	0.710
4	-0.123	Top:top0 LFSR:LFSR1 result_r[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	1.000	-0.412	0.710

Slow 1200mV 0C Model Hold: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.956	Top:top0 LFSR:LFSR1 processing[2]	Top:top0 LFSR:LFSR1 result_r[2]	CLOCK_50	KEY[1]	0.000	6.227	5.482
2	-0.808	Top:top0 LFSR:LFSR1 processing[0]	Top:top0 LFSR:LFSR1 result_r[0]	CLOCK_50	KEY[1]	0.000	6.227	5.630
3	-0.803	Top:top0 LFSR:LFSR1 processing[1]	Top:top0 LFSR:LFSR1 result_r[1]	CLOCK_50	KEY[1]	0.000	6.227	5.635
4	-0.708	Top:top0 LFSR:LFSR1 processing[3]	Top:top0 LFSR:LFSR1 result_r[3]	CLOCK_50	KEY[1]	0.000	6.227	5.730

Slow 1200mV 0C Model Removal: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.632	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	0.000	8.841	8.380
2	-0.632	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	0.000	8.841	8.380
3	-0.632	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	0.000	8.841	8.380
4	-0.632	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	0.000	8.841	8.380
5	-0.632	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	0.000	8.841	8.380
6	-0.632	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	0.000	8.841	8.380
7	-0.632	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	0.000	8.841	8.380
8	-0.632	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	0.000	8.841	8.380
9	-0.288	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	-0.500	8.841	8.244
10	-0.288	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	-0.500	8.841	8.244
11	-0.288	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	-0.500	8.841	8.244
12	-0.288	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	-0.500	8.841	8.244
13	-0.288	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	-0.500	8.841	8.244
14	-0.288	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	-0.500	8.841	8.244
15	-0.288	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	-0.500	8.841	8.244
16	-0.288	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	-0.500	8.841	8.244

Slow 1200mV 0C Model Removal: 'CLOCK_50'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.451	KEY[1]	Debounce:deb0 neg_r	KEY[1]	CLOCK_50	0.000	3.908	3.668

Slow 1200mV 0C Model Minimum Pulse Width: 'KEY[1]'								
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target	
1	-3.000	1.000	4.000	Port Rate	KEY[1]	Rise	KEY[1]	
2	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]	
3	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]	
4	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]	
5	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]	
6	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[0]	
7	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[1]	
8	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[2]	
9	-1.285	1.000	2.285	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[3]	
10	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]	
11	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]	
12	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]	
13	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]	
14	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[0]	
15	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[1]	
16	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[2]	
17	-0.313	-0.095	0.218	High Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[3]	
18	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[0] clk	
19	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[1] clk	
20	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[2] clk	
21	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[3] clk	
22	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 o_random_out_r[0] clk	
23	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 o_random_out_r[1] clk	
24	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 o_random_out_r[2] clk	
25	-0.057	-0.057	0.000	High Pulse Width	KEY[1]	Rise	top0 o_random_out_r[3] clk	
26	-0.048	-0.048	0.000	High Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~clkctrl indk[0]	
27	-0.048	-0.048	0.000	High Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~clkctrl outclk	

Stow 1200mV 0C Model Recovery: 'CLOCK_50'									
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay	
1	-3.346	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.IDLE~_emulated	CLOCK_50	CLOCK_50	1.000	-1.312	3.033	
2	-2.775	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE0~_emulated	CLOCK_50	CLOCK_50	1.000	-0.142	3.632	
3	-2.125	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 slower_clk_r	CLOCK_50	CLOCK_50	1.000	-0.247	2.877	
4	-2.080	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE1	CLOCK_50	CLOCK_50	1.000	-0.202	2.877	
5	-2.080	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE2	CLOCK_50	CLOCK_50	1.000	-0.202	2.877	
6	-2.057	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE8	CLOCK_50	CLOCK_50	1.000	-0.204	2.852	
7	-2.057	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE9	CLOCK_50	CLOCK_50	1.000	-0.204	2.852	
8	-2.057	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE14	CLOCK_50	CLOCK_50	1.000	-0.214	2.842	
9	-2.035	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[11]	CLOCK_50	CLOCK_50	1.000	-0.184	2.850	
10	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE6	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
11	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE7	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
12	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE10	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
13	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE11	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
14	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE12	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
15	-2.021	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE13	CLOCK_50	CLOCK_50	1.000	-0.168	2.852	
16	-2.002	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE4	CLOCK_50	CLOCK_50	1.000	-0.146	2.855	
17	-2.002	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE5	CLOCK_50	CLOCK_50	1.000	-0.146	2.855	
18	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[18]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
19	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[22]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
20	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[14]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
21	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[15]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
22	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[16]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
23	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[17]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
24	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[19]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
25	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[20]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
26	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[21]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
27	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[24]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
28	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[23]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
29	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[26]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
30	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[25]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
31	-1.990	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[27]	CLOCK_50	CLOCK_50	1.000	-0.236	2.753	
32	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[13]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
33	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[0]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
34	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[11]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
35	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[2]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
36	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[3]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
37	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[4]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
38	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[5]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
39	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[6]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
40	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[7]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
41	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[8]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
42	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[9]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
43	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[10]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
44	-1.979	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 count_r[12]	CLOCK_50	CLOCK_50	1.000	-0.213	2.765	
45	-1.957	Debounce:deb0 neg_r	Top:top0 clk_counter:dk_counter1 state_r.STATE3	CLOCK_50	CLOCK_50	1.000	-0.101	2.855	
46	-1.062	KEY[1]	Top:top0 lfsr:lfsr1 state_r.IDLE~_emulated	KEY[1]	CLOCK_50	0.500	2.596	4.137	
47	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[14]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
48	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[13]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
49	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[12]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
50	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[11]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
51	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[10]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
52	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[9]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
53	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[8]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
54	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[7]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
55	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[6]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
56	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[5]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
57	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[4]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
58	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[3]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
59	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[2]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
60	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[1]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
61	-0.827	KEY[1]	Top:top0 lfsr:lfsr1 processing[0]	KEY[1]	CLOCK_50	0.500	2.614	3.920	
62	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[0]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
63	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[1]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
64	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[2]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
65	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[3]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
66	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[4]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
67	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[5]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
68	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[6]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
69	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[7]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
70	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[8]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
71	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[9]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
72	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[10]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
73	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[11]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
74	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[12]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
75	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[13]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
76	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[14]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
77	-0.815	KEY[1]	Top:top0 lfsr:lfsr1 seed_r[15]	KEY[1]	CLOCK_50	0.500	2.614	3.908	
78	-0.662	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.IDLE~_emulated	KEY[1]	CLOCK_50	1.000	2.596	4.237	
79	-0.655	KEY[1]	Top:top0 lfsr:lfsr1 processing[15]	KEY[1]	CLOCK_50	0.500	2.613	3.747	
80	-0.556	KEY[1]	Debounce:deb0 counter_r[2]	KEY[1]	CLOCK_50	0.500	2.949	3.984	
81	-0.556	KEY[1]	Debounce:deb0 o_debounced_r	KEY[1]	CLOCK_50	0.500	2.949	3.984	
82	-0.556	KEY[1]	Debounce:deb0 counter_r[0]	KEY[1]	CLOCK_50	0.500	2.949	3.984	
83	-0.556	KEY[1]	Debounce:deb0 counter_r[1]	KEY[1]	CLOCK_50	0.500	2.949	3.984	
84	-0.426	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE0~_emulated	KEY[1]	CLOCK_50	0.500	3.764	4.669	
85	-0.416	KEY[1]	Top:top0 clk_counter:dk_counter1 slower_clk_r	KEY[1]	CLOCK_50	0.500	3.659	4.554	
86	-0.371	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE1	KEY[1]	CLOCK_50	0.500	3.704	4.554	
87	-0.371	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE2	KEY[1]	CLOCK_50	0.500	3.704	4.554	
88	-0.348	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE8	KEY[1]	CLOCK_50	0.500	3.702	4.529	
89	-0.348	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE9	KEY[1]	CLOCK_50	0.500	3.702	4.529	
90	-0.348	KEY[1]	Top:top0 clk_counter:dk_counter1 state_r.STATE14	KEY[1]	CLOCK_50	0.500	3.692	4.519	
91	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[14]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
92	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[13]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
93	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[12]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
94	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[11]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
95	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[10]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
96	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[9]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
97	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[8]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
98	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[7]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
99	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[6]	KEY[1]	CLOCK_50	1.000	2.614	3.927	
100	-0.334	KEY[1]	Top:top0 lfsr:lfsr1 processing[5]	KEY[1]	CLOCK_50	1.000	2.614	3.927	

Slow 1200mV 0C Model Minimum Pulse Width: 'CLOCK_50'							
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	CLOCK_50	Rise	CLOCK_50
2	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[0]
3	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[1]
4	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[2]
5	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 neg_r
6	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Debounce:deb0 o_debounced_r
7	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[0]
8	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[10]
9	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[11]
10	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[12]
11	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[13]
12	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[14]
13	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[15]
14	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[1]
15	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[2]
16	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[3]
17	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[4]
18	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[5]
19	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[6]
20	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[7]
21	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[8]
22	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[9]
23	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[0]
24	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[10]
25	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[11]
26	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[12]
27	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[13]
28	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[14]
29	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[15]
30	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[1]
31	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[2]
32	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[3]
33	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[4]
34	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[5]
35	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[6]
36	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[7]
37	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[8]
38	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[9]
39	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[0]
40	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[10]
41	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[11]
42	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[12]
43	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[13]
44	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[14]
45	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[15]
46	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[16]
47	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1 count_r[17]
48	-1.285	1.000	2.285	Min Period	CLOCK_50	Rise	Top:top0 dk_counter:dk_counter1

Timing Violation (Fast 1200mV 0C Model)

Fast 1200mV 0C Model Setup Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-2.610	-117.682
2	KEY[1]	-0.013	-0.013

Fast 1200mV 0C Model Hold Summary

	Clock	Slack	End Point TNS
1	KEY[1]	-0.241	-0.620
2	CLOCK_50	-0.168	-3.917

Fast 1200mV 0C Model Recovery Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-1.480	-57.479
2	KEY[1]	-0.876	-7.008

Fast 1200mV 0C Model Removal Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-0.388	-3.272
2	KEY[1]	-0.158	-1.264

Fast 1200mV 0C Model Minimum Pulse Width Summary

	Clock	Slack	End Point TNS
1	CLOCK_50	-3.000	-96.266
2	KEY[1]	-3.000	-21.478

Fast 1200mV 0C Model Hold: 'CLOCK_50'									
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay	
1	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[14]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
2	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[15]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
3	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[16]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
4	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[17]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
5	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[19]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
6	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[20]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
7	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[21]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
8	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[22]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
9	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[23]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
10	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[24]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
11	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[25]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
12	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[26]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
13	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[27]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
14	-0.168	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[18]	KEY[1]	CLOCK_50	0.000	2.203	2.159	
15	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[0]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
16	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[1]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
17	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[2]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
18	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[3]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
19	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[4]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
20	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[5]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
21	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[6]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
22	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[7]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
23	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[8]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
24	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[9]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
25	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[10]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
26	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[12]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
27	-0.100	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[13]	KEY[1]	CLOCK_50	0.000	2.222	2.246	
28	-0.098	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[11]	KEY[1]	CLOCK_50	0.000	2.231	2.257	
29	-0.089	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE1	KEY[1]	CLOCK_50	0.000	2.223	2.258	
30	-0.078	KEY[1]	Top:top0 clk_counter:clk_counter1 slower_clk_r	KEY[1]	CLOCK_50	0.000	2.194	2.240	

[illegible]

Fast 1200mV 0C Model Setup: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.013	Top:top0 LFSR:LFSR1 processing[3]	Top:top0 LFSR:LFSR1 result_r[3]	CLOCK_50	KEY[1]	1.000	2.713	3.693

Fast 1200mV 0C Model Hold: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.241	Top:top0 LFSR:LFSR1 processing[2]	Top:top0 LFSR:LFSR1 result_r[2]	CLOCK_50	KEY[1]	0.000	3.109	2.992
2	-0.142	Top:top0 LFSR:LFSR1 processing[0]	Top:top0 LFSR:LFSR1 result_r[0]	CLOCK_50	KEY[1]	0.000	3.109	3.091
3	-0.141	Top:top0 LFSR:LFSR1 processing[1]	Top:top0 LFSR:LFSR1 result_r[1]	CLOCK_50	KEY[1]	0.000	3.109	3.092
4	-0.096	Top:top0 LFSR:LFSR1 processing[3]	Top:top0 LFSR:LFSR1 result_r[3]	CLOCK_50	KEY[1]	0.000	3.109	3.137

Fast 1200mV 0C Model Recovery: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.876	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	0.500	4.222	5.585
2	-0.876	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	0.500	4.222	5.585
3	-0.876	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	0.500	4.222	5.585
4	-0.876	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	0.500	4.222	5.585
5	-0.876	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	0.500	4.222	5.585
6	-0.876	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	0.500	4.222	5.585
7	-0.876	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	0.500	4.222	5.585
8	-0.876	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	0.500	4.222	5.585

Fast 1200mV 0C Model Removal: 'KEY[1]'								
	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.158	KEY[1]	Top:top0 LFSR:LFSR1 result_r[0]	KEY[1]	KEY[1]	0.000	4.558	4.484
2	-0.158	KEY[1]	Top:top0 o_random_out_r[0]	KEY[1]	KEY[1]	0.000	4.558	4.484
3	-0.158	KEY[1]	Top:top0 LFSR:LFSR1 result_r[1]	KEY[1]	KEY[1]	0.000	4.558	4.484
4	-0.158	KEY[1]	Top:top0 o_random_out_r[1]	KEY[1]	KEY[1]	0.000	4.558	4.484
5	-0.158	KEY[1]	Top:top0 LFSR:LFSR1 result_r[2]	KEY[1]	KEY[1]	0.000	4.558	4.484
6	-0.158	KEY[1]	Top:top0 o_random_out_r[2]	KEY[1]	KEY[1]	0.000	4.558	4.484
7	-0.158	KEY[1]	Top:top0 LFSR:LFSR1 result_r[3]	KEY[1]	KEY[1]	0.000	4.558	4.484
8	-0.158	KEY[1]	Top:top0 o_random_out_r[3]	KEY[1]	KEY[1]	0.000	4.558	4.484

Fast 1200mV 0C Model Minimum Pulse Width: 'KEY[1]'								
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target	
1	-3.000	1.000	4.000	Port Rate	KEY[1]	Rise	KEY[1]	
2	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]	
3	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]	
4	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]	
5	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]	
6	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[0]	
7	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[1]	
8	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[2]	
9	-1.000	1.000	2.000	Min Period	KEY[1]	Rise	Top:top0 o_random_out_r[3]	
10	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[0]	
11	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[1]	
12	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[2]	
13	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 LFSR:LFSR1 result_r[3]	
14	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[0]	
15	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[1]	
16	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[2]	
17	-0.559	-0.375	0.184	Low Pulse Width	KEY[1]	Rise	Top:top0 o_random_out_r[3]	
18	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[0] clk	
19	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[1] clk	
20	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[2] clk	
21	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 LFSR1 result_r[3] clk	
22	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 o_random_out_r[0] clk	
23	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 o_random_out_r[1] clk	
24	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 o_random_out_r[2] clk	
25	-0.379	-0.379	0.000	Low Pulse Width	KEY[1]	Rise	top0 o_random_out_r[3] clk	
26	-0.367	-0.367	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~clkctrl indk[0]	
27	-0.367	-0.367	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~clkctrl outclk	
28	-0.258	-0.258	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0 combout	
29	-0.255	-0.255	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0 datac	
30	-0.238	-0.238	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~8 datad	
31	-0.233	-0.233	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~8 combout	
32	-0.220	-0.220	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~3 combout	
33	-0.209	-0.209	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~3 datac	
34	-0.186	-0.186	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~0 datad	
35	-0.181	-0.181	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 Selector0~0 combout	
36	-0.172	-0.172	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 count_r[12]~28 datad	
37	-0.167	-0.167	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 count_r[12]~28 combout	
38	-0.121	-0.121	0.000	Low Pulse Width	KEY[1]	Rise	top0 clk_counter1 state_r.STATE0~2 combout	

Fast 1200mV 0C Model Recovery: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-1.480	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.IDLE~_emulated	CLOCK_50	CLOCK_50	1.000	-0.837	1.630
2	-1.058	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE0~_emulated	CLOCK_50	CLOCK_50	1.000	-0.091	1.954
3	-0.796	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 slower_clk_r	CLOCK_50	CLOCK_50	1.000	-0.161	1.622
4	-0.769	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE1	CLOCK_50	CLOCK_50	1.000	-0.134	1.622
5	-0.769	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE2	CLOCK_50	CLOCK_50	1.000	-0.134	1.622
6	-0.739	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE8	CLOCK_50	CLOCK_50	1.000	-0.126	1.600
7	-0.739	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE9	CLOCK_50	CLOCK_50	1.000	-0.126	1.600
8	-0.732	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.IDLE~_emulated	KEY[1]	CLOCK_50	0.500	1.432	2.631
9	-0.724	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE4	CLOCK_50	CLOCK_50	1.000	-0.093	1.618
10	-0.724	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE5	CLOCK_50	CLOCK_50	1.000	-0.093	1.618
11	-0.722	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE14	CLOCK_50	CLOCK_50	1.000	-0.141	1.568
12	-0.717	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[11]	CLOCK_50	CLOCK_50	1.000	-0.126	1.578
13	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE6	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
14	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE7	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
15	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE10	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
16	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE11	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
17	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE12	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
18	-0.715	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 state_r.STATE13	CLOCK_50	CLOCK_50	1.000	-0.102	1.600
19	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[18]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
20	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[22]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
21	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[14]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
22	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[15]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
23	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[16]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
24	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[17]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
25	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[19]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
26	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[20]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
27	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[21]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
28	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[24]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
29	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[23]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
30	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[26]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
31	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[25]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
32	-0.714	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[27]	CLOCK_50	CLOCK_50	1.000	-0.152	1.549
33	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[13]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
34	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[0]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
35	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[1]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
36	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[2]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
37	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[3]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
38	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[4]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565
39	-0.713	Debounce:deb0 neg_r	Top:top0 clk_counter:clk_counter1 count_r[5]	CLOCK_50	CLOCK_50	1.000	-0.135	1.565

Fast 1200mV 0C Model Removal: 'CLOCK_50'

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	-0.388	KEY[1]	Debounce:deb0 neg_r	KEY[1]	CLOCK_50	0.000	2.269	2.005
2	-0.112	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE0~_emulated	KEY[1]	CLOCK_50	0.000	2.267	2.279
3	-0.092	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE3	KEY[1]	CLOCK_50	0.000	2.294	2.326
4	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[0]	KEY[1]	CLOCK_50	0.000	2.222	2.275
5	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[1]	KEY[1]	CLOCK_50	0.000	2.222	2.275
6	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[2]	KEY[1]	CLOCK_50	0.000	2.222	2.275
7	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[3]	KEY[1]	CLOCK_50	0.000	2.222	2.275
8	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[4]	KEY[1]	CLOCK_50	0.000	2.222	2.275
9	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[5]	KEY[1]	CLOCK_50	0.000	2.222	2.275
10	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[6]	KEY[1]	CLOCK_50	0.000	2.222	2.275
11	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[7]	KEY[1]	CLOCK_50	0.000	2.222	2.275
12	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[8]	KEY[1]	CLOCK_50	0.000	2.222	2.275
13	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[9]	KEY[1]	CLOCK_50	0.000	2.222	2.275
14	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[10]	KEY[1]	CLOCK_50	0.000	2.222	2.275
15	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[12]	KEY[1]	CLOCK_50	0.000	2.222	2.275
16	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[13]	KEY[1]	CLOCK_50	0.000	2.222	2.275
17	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE6	KEY[1]	CLOCK_50	0.000	2.256	2.309
18	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE7	KEY[1]	CLOCK_50	0.000	2.256	2.309
19	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE10	KEY[1]	CLOCK_50	0.000	2.256	2.309
20	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE11	KEY[1]	CLOCK_50	0.000	2.256	2.309
21	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE12	KEY[1]	CLOCK_50	0.000	2.256	2.309
22	-0.071	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE13	KEY[1]	CLOCK_50	0.000	2.256	2.309
23	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[11]	KEY[1]	CLOCK_50	0.000	2.231	2.287
24	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[14]	KEY[1]	CLOCK_50	0.000	2.203	2.259
25	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[15]	KEY[1]	CLOCK_50	0.000	2.203	2.259
26	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[16]	KEY[1]	CLOCK_50	0.000	2.203	2.259
27	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[17]	KEY[1]	CLOCK_50	0.000	2.203	2.259
28	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[19]	KEY[1]	CLOCK_50	0.000	2.203	2.259
29	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[20]	KEY[1]	CLOCK_50	0.000	2.203	2.259
30	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[21]	KEY[1]	CLOCK_50	0.000	2.203	2.259
31	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[22]	KEY[1]	CLOCK_50	0.000	2.203	2.259
32	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[23]	KEY[1]	CLOCK_50	0.000	2.203	2.259
33	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[24]	KEY[1]	CLOCK_50	0.000	2.203	2.259
34	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[25]	KEY[1]	CLOCK_50	0.000	2.203	2.259
35	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[26]	KEY[1]	CLOCK_50	0.000	2.203	2.259
36	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[27]	KEY[1]	CLOCK_50	0.000	2.203	2.259
37	-0.068	KEY[1]	Top:top0 clk_counter:clk_counter1 count_r[18]	KEY[1]	CLOCK_50	0.000	2.203	2.259
38	-0.063	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE4	KEY[1]	CLOCK_50	0.000	2.265	2.326
39	-0.063	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE5	KEY[1]	CLOCK_50	0.000	2.265	2.326
40	-0.061	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE14	KEY[1]	CLOCK_50	0.000	2.215	2.278
41	-0.045	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE8	KEY[1]	CLOCK_50	0.000	2.230	2.309
42	-0.045	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE9	KEY[1]	CLOCK_50	0.000	2.230	2.309
43	-0.017	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE1	KEY[1]	CLOCK_50	0.000	2.223	2.330
44	-0.017	KEY[1]	Top:top0 clk_counter:clk_counter1 state_r.STATE2	KEY[1]	CLOCK_50	0.000	2.223	2.330

Fast 1200mV 0C Model Minimum Pulse Width: 'CLOCK_50'							
	Slack	Actual Width	Required Width	Type	Clock	Clock Edge	Target
1	-3.000	1.000	4.000	Port Rate	CLOCK_50	Rise	CLOCK_50
2	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[0]
3	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[1]
4	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Debounce:deb0 counter_r[2]
5	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Debounce:deb0 neg_r
6	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Debounce:deb0 o_debounced_r
7	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[0]
8	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[10]
9	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[11]
10	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[12]
11	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[13]
12	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[14]
13	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[15]
14	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[1]
15	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[2]
16	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[3]
17	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[4]
18	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[5]
19	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[6]
20	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[7]
21	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[8]
22	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[9]
23	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[0]
24	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[10]
25	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[11]
26	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[12]
27	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[13]
28	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[14]
29	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[15]
30	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[1]
31	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[2]
32	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[3]
33	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[4]
34	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[5]
35	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[6]
36	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[7]
37	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[8]
38	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 seed_r[9]
39	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[0]
40	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[10]
41	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[11]
42	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[12]
43	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[13]
44	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[14]
45	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[15]
46	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[16]
47	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 count_r[17]
48	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1

Fast 1200mV 0C Model Minimum Pulse Width: 'CLOCK_50'							
81	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 state_r.STATE7
82	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 state_r.STATE8
83	-1.000	1.000	2.000	Min Period	CLOCK_50	Rise	Top:top0 clk_counter:clk_counter1 state_r.STATE9
84	-0.249	-0.065	0.184	Low Pulse Width	CLOCK_50	Rise	Debounce:deb0 counter_r[0]
85	-0.249	-0.065	0.184	Low Pulse Width	CLOCK_50	Rise	Debounce:deb0 counter_r[1]
86	-0.249	-0.065	0.184	Low Pulse Width	CLOCK_50	Rise	Debounce:deb0 counter_r[2]
87	-0.249	-0.065	0.184	Low Pulse Width	CLOCK_50	Rise	Debounce:deb0 o_debounced_r
88	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[0]
89	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[10]
90	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[11]
91	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[12]
92	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[13]
93	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[14]
94	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[15]
95	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[1]
96	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[2]
97	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[3]
98	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[4]
99	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[5]
100	-0.234	-0.050	0.184	Low Pulse Width	CLOCK_50	Rise	Top:top0 LFSR:LFSR1 processing[6]

Part 6: Thoughts

這次 Lab 由於我們部分組員對 Verilog 還在熟悉階段，因此對於許多的硬體設計還沒有很深刻的了解（看看我們 timing violation 有多少便知），再加上光舞的忙碌情形，使得這次 Lab 仍有許多改進的地方。我們遇到的最大問題應當是一個值不能同時在兩個不同的 always 被賦值，以及在一個 always 當中必須要保證每個 state 賦值的對稱性。總而言之，這次的 Lab 讓我們對於硬體的 verilog 設計有了基本概念，能夠讓下一次的實驗更加順手。