# RENESAS
# RISC-V MPU - RZ/Five -
# INTRODUCTION

MPU BUSINESS DEVELOPMENT
ENTERPRISE INFRASTRUCTURE BUSINESS DIVISION
IOT & INFRASTRUCTURE BUSINESS UNIT
RENESAS ELECTRONICS CORPORATION

# RENESAS' RZ MPU FAMILY

| | HMI | | Networking | Control | AI |
|---|---|---|---|---|---|
| | **RZ/A** | **RZ/G** | **RZ/N** | **RZ/T** | **RZ/V** |
| | 2D Graphics + RTOS | Multimedia /3D Graphics + Linux | Multi-protocol Industrial Ethernet + 5ports switch w/ GMAC & redundancy | Real-time control+ Multi-protocol Industrial Ethernet, FuSa | AI accelerator + Linux |
| **IoT Edge** | | ✔ Linux + RTOS<br>• Wider portfolio from High to Entry class<br>• Super long-term support Linux(CIP) | ✔ Linux + RTOS<br>• Up to 5 ports TSN switch with GMAC<br>• Redundancy network support | | ✔ Linux + RTOS<br>• DRP enabling good power efficiency (performance / watt)<br>• CIP Linux & Flexible AI Tool support |
| **Endpoint** | ✔ RTOS<br>• Integrated Large RAM (w/o DRAM)<br>• Easy to use GHz CPU like MCU | ✔ Linux + RTOS<br>• Wider portfolio from High to Entry class<br>• CIP Linux & GUI Framework support | ✔ Linux + RTOS<br>• Up to 5 ports TSN switch w/ GMAC<br>• Multi-protocol IA network support | ✔ RTOS<br>• Realtime CPU & large size TCM<br>• Multi-protocol IA network & FuSa | ✔ Linux + RTOS<br>• DRP enabling good power efficiency (performance / watt)<br>• CIP Linux & Flexible AI Tool support |

# RZ FAMILY FEATURES FOR IOT EDGE

| 8 to 2 cores | | | 2 cores | | 1 core | |
|---|---|---|---|---|---|---|
| Pin Compatible | | | | | Pin Compatible with Type1 | |
| G2H | G2M | G2N | G2E | G2L | G2UL Type1 Type2 | Five (RISC-V) New Product |
| | | | | Pin Compatible with Type2 | | |
| 4xCortex-A57<br>4xCortex-A53 | 2xCortex-A57<br>4xCortex-A53 | 2xCortex-A57<br>- | -<br>2xCortex-A53 | -<br>2xCortex-A55 | -<br>1xCortex-A55 | -<br>1xAX45MP (RISC-V) |
| 1xCortex-R7 | 1xCortex-R7 | 1xCortex-R7 | 1xCortex-R7 | 1xCortex-M33 | 1xCortex-M33 | - |
| LPDDR4x64 | LPDDR4x64 | LPDDR4x32 | DDR3Lx32 | DDR3L/4x16 | DDR3L/4x16 | DDR3L/4x16 |
| PCIe<br>Gbit Ether<br>USB3, USB2<br>CAN | PCIe<br>Gbit Ether<br>USB3, USB2<br>CAN | PCIe<br>Gbit Ether<br>USB3, USB2<br>CAN | PCIe<br>Gbit Ether<br>USB3, USB2<br>CAN | -<br>Gbit Ether<br>USB2<br>CAN | -<br>Gbit Ether<br>USB2<br>CAN | -<br>Gbit Ether<br>USB2<br>CAN |
| Security | Security | Security | Security | Security | Security | Security |

**CIP Linux**

# RZ/Five Product Concept

- Risks and challenges of CPU IP technology supported by one specific IP vendor

**Geopolitics Risk**

e.g. One Regional technology may have the barrier to use in another region.

**Monopoly Risk**

e.g. No alternative IP technology

**Non-neutral Risk**

e.g. IP technology cannot be used due to hostile takeovers

## RZ/Five(RISC-V) Product Concept

- Adopts Open-source Architecture RISC-V
- Providing a mutual migration solution between Arm and RISC-V
- General-purpose MPU specialized for IoT edge
- High reliability and long-term maintenance Linux support

**RZ/Five (RISC-V) contributes to solving these risks and issues**

# RZ/Five (RISC-V) Features

“RZ/Five” is an entry-class general-purpose Linux MPU with a 64-bit RISC-V architecture.(**Press Release**)

## ☐Feature#1：Adopt an Open Instruction Set Architecture CPU (RISC-V ISA*)

- Adopting RISC-V ISA, which can be used by anyone and is supported by multiple IP vendors, reduces the risk of long-term use of MPU.

## ☐Feature#2： Flexible Arm and RISC-V mutual migration solution

- Providing "Package Pin Compatibility Solution" and "SMARC Module Development Environment" for Mutual Migration

## ☐Feature#3：General-purpose MPU specialized for IoT Edge

- 1GHz 64bit CPU, Gigabit Ethernet 2ch, CAN-FD 2ch, USB2.0 2ch、ADC 2ch

## ☐Feature#4：High reliability and long-term maintenance Linux support

- Supports the ECC function, the Security function and the long-term maintenance Linux(CIP)

*ISA: Instruction Set Architecture

# Feature #1: Adopt an Open Instruction Set Architecture CPU (RISC-V ISA)

## USES RISC-V ARCHITECTURE (ISA) COMPLIANT ANDES CORE

- **By adopting Andes*1 AX45MP, we can quickly provide customers with a general-purpose MPU that complies with RISC-V ISA.**
- **CPUs with high processing performance per frequency are ideal for many applications.**

### RZ/Five(RISC-V CPU) Overview

- AndesCore™ AX45MP Single core 1.0 GHz
- 64-bit in-order dual-issue 8-stage pipeline CPU architecture
- L1 I-cache 32 Kbytes (Parity) / D-cache 32 Kbytes (ECC)
- L2 cache 256 KBytes (ECC)
- Floating point extension DSP/SIMD ISA
- Andes Star™ V5 Instruction Set Architecture (ISA). Compliant to RISC-V ISA IMACFDN*2, with Andes performance/functionality extensions

RISC-V: AX45MP - Andes Technology

| Key feature | Benefit |
|---|---|
| 8-stage in-order superscalar pipeline | Superior performance-efficiency, while allowing for high speeds |

Information source: Andes Technology

***1: Andes Technogym is a founding premium member of the RISC-V International Association.**

***2: IMACFDN**

- **I: Integer instruction**
- **M: Integer Multiplication and Division**
- **A: Extension for Atomic instructions**
- **C: Extension for Compressed Instructions**
- **F: Single precision floating point instruction**
- **D: Double precision floating point instruction**
- **N: User-level interrupts and Memory Management Unit**

# RZ/Five Product Feature Overview

## System

- Debugger
- 16ch DMAC
- Interrupt Controller
- PLL/SSCG

## CPU

**AX45MP Single (1GHz)**
**With SIMD / FPU**
**I-L1$ : 32KB(Parity) , D-L1$ : 32KB(ECC)**

- TCM (ILM/DLM) : Total 128KB (1GHz) w/ECC
- L2$ : 256KB w/ECC

## Peripheral I/F

- 1 x USB2.0 (Host)
  1 x USB2.0
  (Host / Function)
- 2 x 100/1000Mbps
  Ether MAC *
- 4 x I2C
- 2 x SCI 8/9bit (incl. IrDA)
- 5 x SCIF (UART)
- GPIO
- 3 x RSPI
- 2 x CAN-FD

## Timers

- 1 x 32bit MTU3
- 8 x 16bit MTU3
- 1 x WDT

## Internal Memory

- RAM 128KB w/ECC

## Analog

- 2 input 12bit ADC (1 unit)
- Thermal Sensor

## Security(Option)

- Secure Boot
- Crypto Engine
- Secure JTAG
- TRNG
- OTP 1Kbit

## External memory I/F

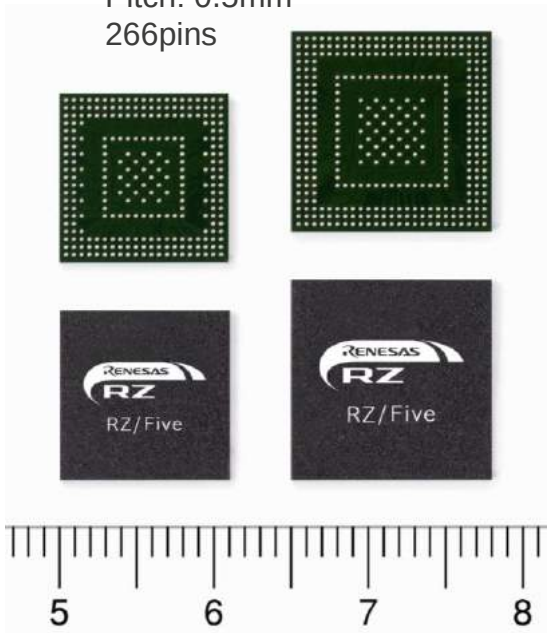
- 1 x DDR3L/DDR4-1600 16bit
  (In line ECC)
- 1 x SPI Multi I/O
  (4bit DDR)
- 1 x SDHI(UHS-I)/MMC
  1 x SDHI(UHS-I)

[More information]
Press Release Link [Here]
Product link [Here]

## Package

✓ PBGA 13mm x 13mm
Pitch: 0.5mm
361pins

✓ PBGA 11mm x 11mm
Pitch: 0.5mm
266pins




*: The 266pin package has one channel of Gigabit Ethernet.

# Feature #2: Flexible Arm and RISC-V mutual migration solution(1/3)

## Mutual migration of CPU architecture is possible with the same PCB design

✓ **Pin compatibility with RZ/G2UL and adoption of a common peripheral IP enable product development of two architectures (RISC-V or Arm) with one PCB.**

### RISC-V CPU Product

RZ/Five

- AX45MP Single Core
- USB2.0
- Gbit Ether
- SDHI
- CAN

361pin,13mm□LFBGA

361pin LFBGA

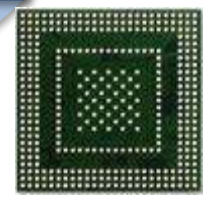
Package Compatibles Products

### Arm CPU Product

RZ/G2UL

- Cortex-A55
- Cortex-M33
- USB2.0
- Gbit Ether
- SDHI
- CAN
- Video in MIPI
- Video out Parallel

361pin,13mm□LFBGA



361pin LFBGA (Type-1)

# Feature #2:Flexible Arm and RISC-V mutual migration solution(2/3)

## Easy evaluation by replacing the SMARC compliant module board

- ✓ Evaluation board Kit consists of Module Board(SOM) + Carrier Board
- ✓ SOM created by SMARC V2.1 standard
- ✓ Renesas prepares SOM for each product, And carrier board is the same and RZ/Five and RZ/G2UL products can be evaluated
- ✓ Board design reference data will be provided to customers

### RISC-V CPU Product

RZ/Five SOM
SMARC V2.1


Carrier Board

### Arm CPU Product

RZ/G2UL SOM
SMARC V2.1

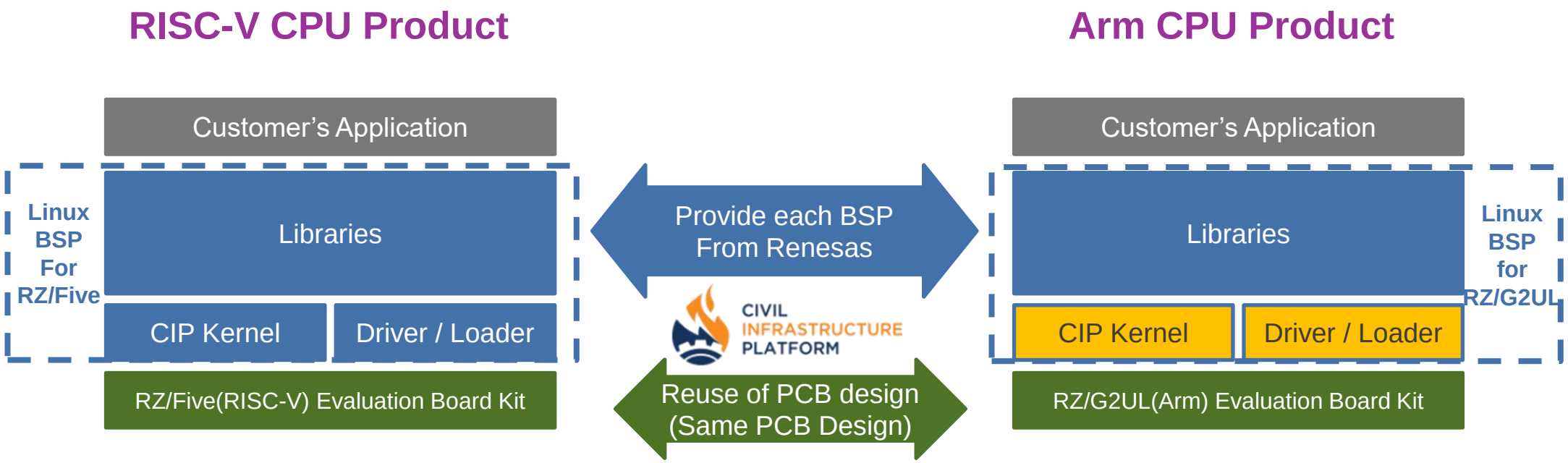

Carrier Board

SOM：System on Module

# Feature #2:Flexible Arm and RISC-V mutual migration solution(3/3)

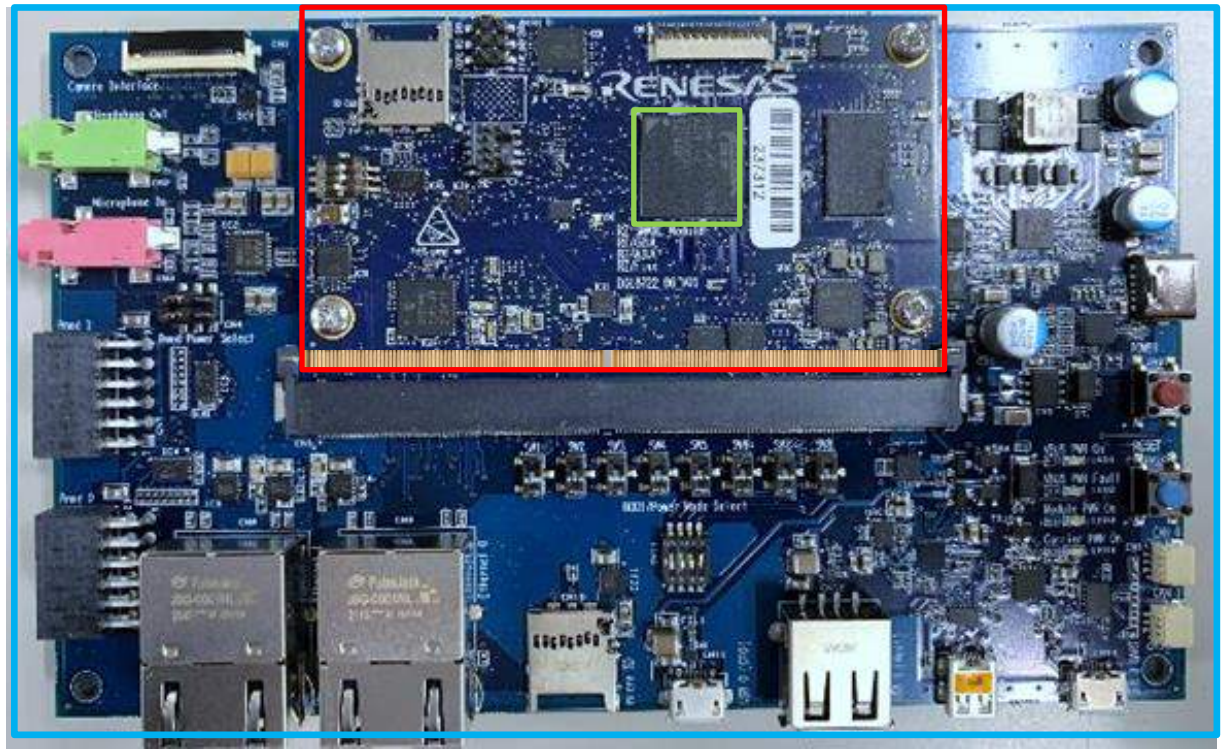
## RZ/Five and RZ/G2UL have the same build machine development environment and development procedure

- ✓ Renesas provides each BSP (Board Support Package)
- ✓ RZ/Five and RZ/G2UL have the same build machine development environment and development procedure.



# RZ/Five EVALUATION BOARD KIT (EVK)

## RZ/Five SMARC v2.1 Module board + Carrier Board




**Module board (Dimension: 82 mm x 50mm )**

- Processor: RZ/Five
- Main Memory: 1GB DDR4 (1GB x1)
- QSPI NOR FLASH: 16MB
- eMMC Memory: 64GB
- External Storage: micro SD x1
- A/D Converter Interface x2
- JTAG connector

**Carrier board (Dimension: 160mm x 100mm )**

- Gigabit Ethernet x2
- USB2.0x 2ch (OTG x1ch, Host x1ch)
- CAN-FD x2
- External Storage : micro SD x1
- Audio Line in x1
- Audio Line out x1
- PMOD x2
- USB-Type C for Power Input

# COMPARISON BETWEEN RZ/G2UL AND RZ/Five SPEC

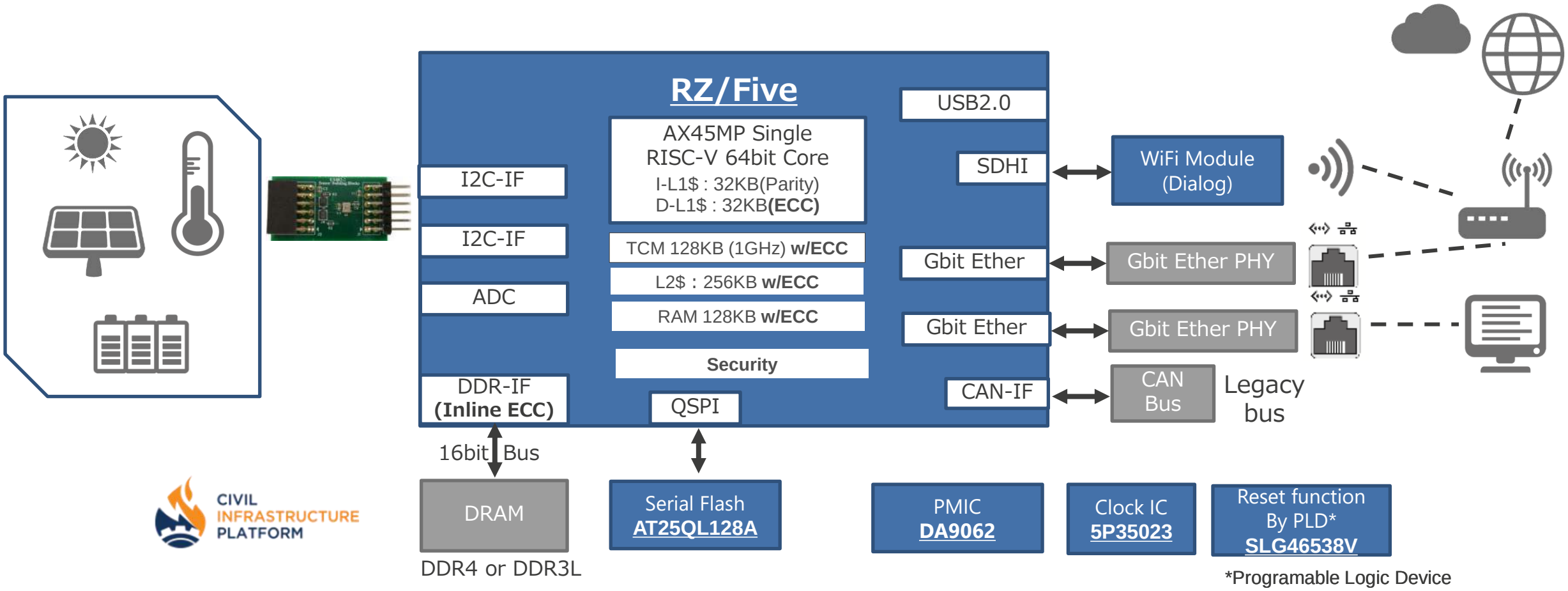
- RISC-V MPU focus on IoT gateway, so no Camera and Display.
- For keep the pin compatibility, use the same function peripheral modules other than the CPU Core

| IP Spec | RZ/Five | RZ/G2UL (Type1) |
|---|---|---|
| CPU | AX45MP Single Core<br>RISC-V 64bit @1.0GHz | 1x Cortex-A55@1.0GHz<br>+Cortex-M33 |
| Internal RAM | 128KB w/ECC | 128KB w/ECC |
| DRAM I/F | 16bit x1ch DDR3L/DDR4 w/ECC | 16bit x1ch DDR3L/DDR4 w/ECC |
| Camera in | — | MIPI CSI-2 |
| Display out | — | Digital RGB |
| USB | USB2.0 Host 1ch, USB2.0 Host/Function 1ch | USB2.0 Host 1ch, USB2.0 Host/Function 1ch |
| Ether | Gbit 2ch(361pin package), Gbit 1ch(266pin package) | Gbit 2ch |
| SDHI | 2 x SDHI(UHS-I)/MMC | 2 x SDHI(UHS-I)/MMC |
| SPI | 1 x SPI Multi I/O (4bit DDR) | 1 x SPI Multi I/O (4bit DDR) |
| CAN | 2x CAN | 2x CAN |
| Serial | 4x I2C, 2x SCI, 5x UART, 3x RSPI | 4x I2C, 2x SCI, 5x UART, 3x RSPI |
| Timer | 8x 16bit MTU, 1x WDT | 8x 16bit MTU, 2x WDT |
| ADC | 2x 12bit ADC | 2x 12bit ADC |
| Package | 361pin, 13x13mm PBGA (0.5mmPitch)<br>266pin, 11x11mm PBGA (0.5mmPitch) | 361pin 13x13mm PBGA(0.5mmPitch) |

# Feature #3: General-purpose MPU specialized for IoT Edge

## Supports 64-bit CPU, peripherals, ECC, security, and industrial grade CIP Linux

- Functions of RZ/Five are ideal for IoT edge devices such as solar inverters that collect data from various sensors and communicate with servers and clouds via networks, and gateways for home security.



# Feature#4 High Reliability, Long-Term Maintenance Linux Support

## Supports ECC Features, Security, and Industrial Grade CIP Linux

- ECC(Error Correction Code) Function
  - Built-in memory
    - L1 I-cache 32 Kbytes (Parity)
    - D-cache 32 Kbytes (ECC)
    - L2 cache 256 KBytes (ECC)
    - ILM 64 Kbytes (ECC)
    - DLM 64 Kbytes (ECC), Total 128 KBytes
  - External memory
    - In line ECC supported (Support error detection interrupt)
- Security
  - Boot protection、Secure Debug、Secure Update
- Industrial grade Linux (CIP Linux)
  - Civil Infrastructure Platform project
  - CIP SLTS Kernel: 10+ years Super Long-Term Support
  - (cf. LTS kernel: 2-6years support)
  - Reliability/Security/Real-time




# WINNING COMBINATIONS (WC)

- Winning combinations(WC) shorten your product development time
  - WC provide a set of scalable power control ICs and clock control ICs required for MPU products.
  - WC provide a reference design that implemented these ICs.

- Some of the winning combinations available in RZ/Five are introduced on the next page
  - US244 SMARC system for Single-core RISC-V MPU
  - 5P35023 – VersaClock® Programmable Clock Generator
  - DA9061/62 – Flexible, Scalable PMIC

# US244 SMARC SYSTEM FOR SINGLE-CORE RISC-V MPU

### System Overview

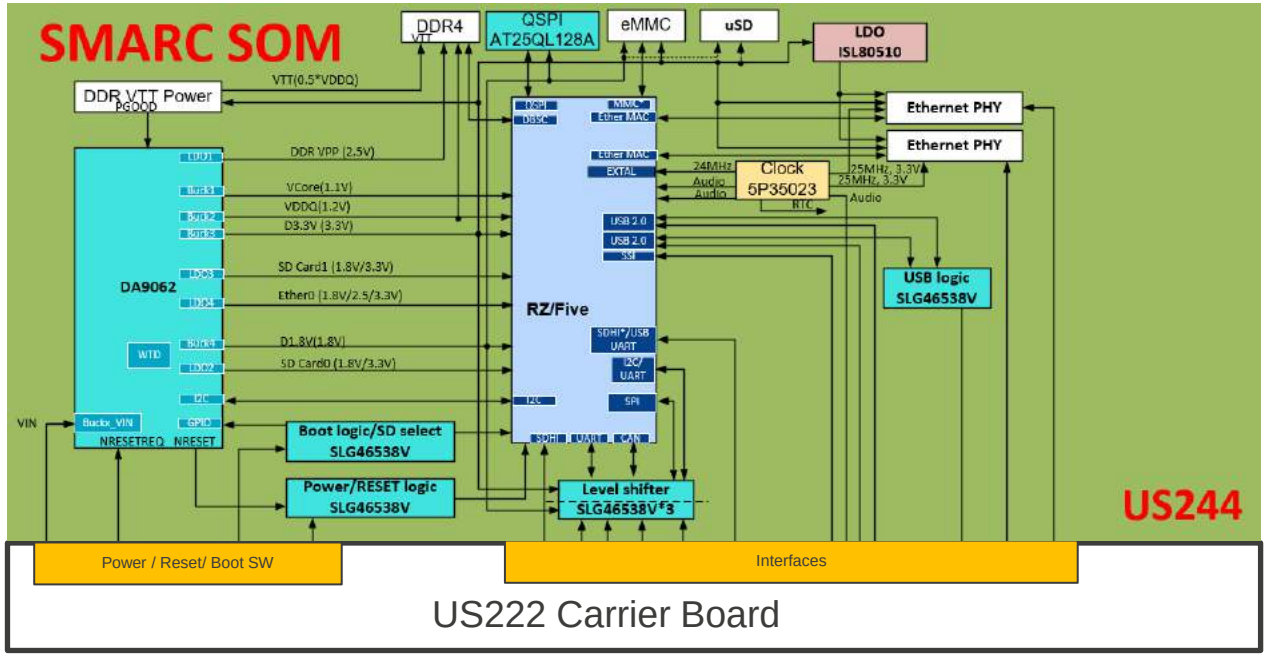
This scalable SMARC 2.1 System on Module (SoM) solution is based on the powerful Renesas RZ/Five microprocessor and a full power and timing tree. It demonstrates a turn-key architecture for Gateway applications, such as sensor IOT gateways

### System Benefits

- Linux operating system
- Single-core configurations for low power consumption
- Single programmable clock generator on board
- Extensive communications interface support
- Single power supply for MPU processing
- Low-cost logic ICs covers the SMARC standard requirement with minimum space

### Target Application

- IIOT Gateway




| Device Category | Orderable P/N | Key Features |
|---|---|---|
| MPU | RZ/Five | Single-core RISC-V CPU with 2ch Giga bit Ethernet |
| Analog | 5P35023 | Programmable VersaClock® Clock |
| Dialog | DA9062 | PMIC for Applications Requiring up to 8.5 A |
| | SLG46538V | GreenPAK Programmable Mixed-signal Matrix |
| | SLG46535 | GreenPAK Programmable Mixed-signal Matrix |
| Power | ISL80510 | High Performance 1A LDO |

# 5P35023 – VERSACLOCK® PROGRAMMABLE CLOCK GENERATOR

## FOR LOW POWER, CONSUMER AND COMPUTING PCI EXPRESS APPLICATIONS

### Key Features

- PCIe clocks phase jitter: PCIe Gen1-3
- Differential clocks < 1.5 ps rms jitter integer range: 12kHz–20MHz
- 3 LVCMOS outputs: 1MHz–160MHz
- Maximum 8 LVCMOS outputs as REF + 3 × SE + 2 × DIFF_T as LVCMOS
- < 2µA current consumption for system RTC reference clock
- Integrated crystal

### Configurability Built-in

- Configurable OE pin function as OE, PD#, PPS or DFC control function
- Configurable PLL bandwidth; minimizes jitter peaking
- PPS: Proactive Power Saving features save power during the end device power down mode
- PPB: Performance Power Balancing feature allows minimum power consumption based on required performance
- DFC: Dynamic Frequency Control feature allows up to 4 different frequencies to switch dynamically

| Part # | Carrier Type | Temp. | Package |
|---|---|---|---|
| 5P35023B-000NXGI | Tray | -40 to +85°C | 24Ld 4x4mm VFQFPN |
| 5P35023B-000NXGI8 | Reel | -40 to +85°C | 24Ld 4x4mm VFQFPN |

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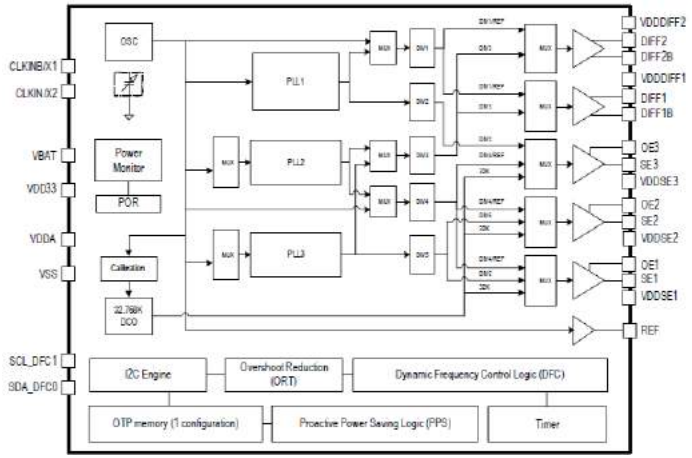
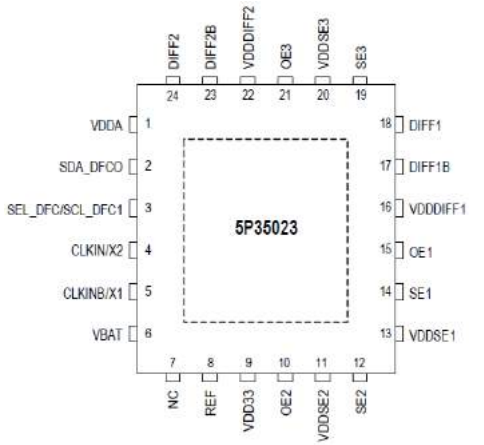



**Block Diagram**




**Pin Configuration**

# DA9061/62 – FLEXIBLE, SCALABLE PMIC

## FLEXIBLE, SCALABLE, RELIABLE AUTOMOTIVE GRADE POWER MANAGEMENT IC (PMIC) SOLUTION

### Highly Integrated Capabilities

- Input voltage 2.8 V to 5.5 V
- 3x Buck converters with 0.3 V to 3.34 V output
  - Buck1: 0.3 V to 1.57 V, 2.5 A
  - Buck2: 0.8 V to 3.34 V, 2 A
  - Buck3: 0.53 V to 1.8 V, 1.5 A
- 3 MHz switching frequency allows use of low-profile inductors
- Dynamic Voltage Scaling (DVS) support
- 4x LDO regulators, 0.9 V to 3.6 V up to 300 mA
  - LDO1: 0.9 V to 3.6 V, 100 mA
  - LDO2 - 4: 0.9 V to 3.6 V, 300 mA
- 5x GPIOs
- Programmable power mode sequencer

### Enhanced Security

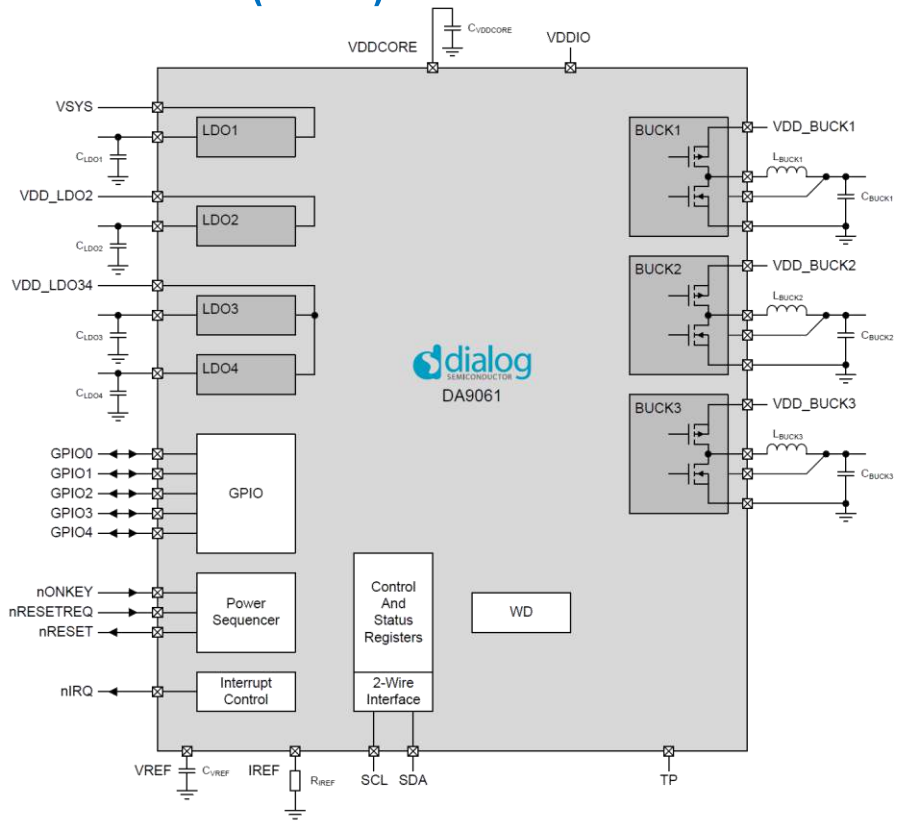
- System supply monitoring
- Junction temperature monitoring
- Watchdog timer

### Additional Features

- Automotive AEC-Q100 Grade 2 version available

| Part # | Description | Package |
|---|---|---|
| DA9061-xxAM1-A | 3x Buck up to 2.5A, 4x LDO PMIC | QFN-40, (6.0 × 6.0 mm, 0.5 mm pitch) |
| DA9061-xxAM1-AT | Automotive AEC-Q100 Grade 2 version | |
| DA9062-xxAM1-A | 4x Buck up to 5A in dual-phase, DDR VTT supply mode, 4x LDO, RTC, coin-cell charger | |
| DA9062-xxAM1-AT | Automotive AEC-Q100 Grade 2 version | |

'xx' = OTP variant

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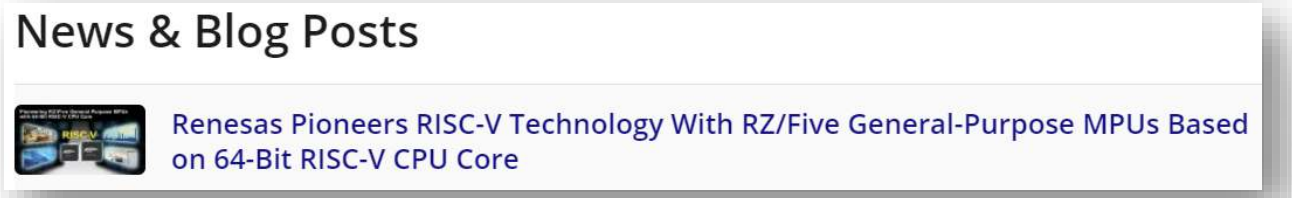
# RZ/FIVE : SOLUTION

| Information | Category | Link |
|---|---|---|
| News Release | Web Page | Renesas Pioneers RISC-V Technology With RZ/Five General-Purpose MPUs Based on 64-Bit RISC-V CPU Core |
| Product Web Page | Web Page | RZ/Five-RISC-V(https://reurl.cc/rDMaOx) |
| User's Manual: Hardware | Document | RZ/Five Group User's Manual: Hardware |
| SMARC Module User's Manual | Document | RZ/Five SMARC Module User's Manual: Hardware |
| Carrier Board User's Manual | Document | RZ SMARC Series Carrier Board User's Manual: Hardware |
| Board Start-up Guide | Document | Board Start-up Guide for RZ/Five EVK |
| Release Note | Document | Release Note for RZ/Five Board Support Package V1.0 |
| Board Support Package | Software | RZ/Five Board Support Package V1.0 [5.10-CIP] |
| SMARC Module Board | Data | RZ/Five SMARC Module Board Design Data V1.00 |

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