University of California, Davis
Department of Computer Science

ECS-154A Computer Architecture

Professor Farrens

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Assessment 1

Cheating on exams is prohibited by the Academic Code of Conduct. I understand that if I am caught cheating on this exam my scores will be negated and I will receive no credit on the exam. Persons caught cheating will also face University disciplinary actions.

Name: _____

Signature: _____

Student ID number: _____

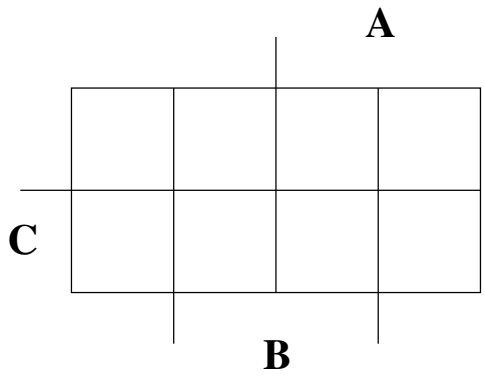
Given the following truth table:

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

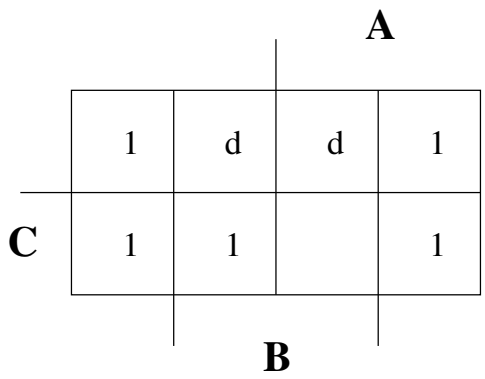
1] (4) On the truth table above, identify which entries are minterms and which are maxterms.

2] (4) Write down the Canonical SOP expression for F

3] (6) Write down the minimum SOP expression for F. Here is a K-map for you to use.

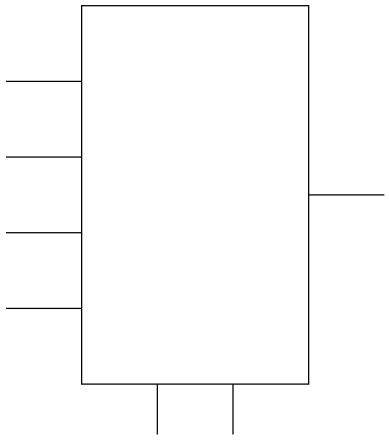


Given the following K-map:



4] (6) What is the minimum SOP expression for F? (d stands for don't care)

5] (6) Use a 4-1 mux to implement the above function. You must use B and C as the control inputs to the mux. (You do not have to draw the inner workings of the MUX).



6] (2) Given the bit pattern 1100101, if you want to add a parity bit and use odd parity, what should the bit be set to?

7] (2) A * 1 = _____

8] (2) A + 1 = _____

9] (8) Draw the gate-level diagram (this means draw the gates) of a 4-1 multiplexor

Given

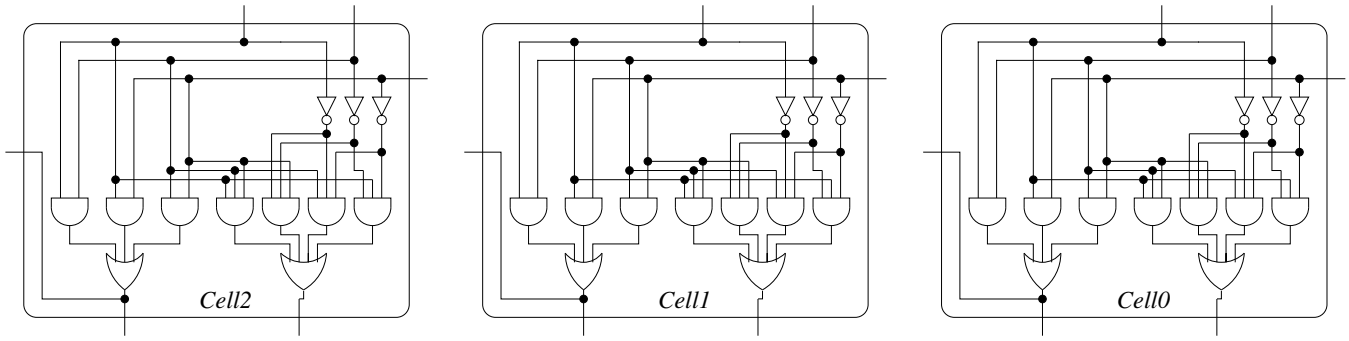
f = $A\bar{B}\bar{C} + \bar{A}\bar{C} + BC$

g = $\bar{A}B + ABC + \bar{B}\bar{C}$

10] (8) Does f = g? (you must show why or why not to get credit)

11] (8) Show how you can build a functionally complete set of gates using only NOR gates.

12] (8) In the diagram below, draw lines to show how you would connect this up to provide a 3-bit adder. Label all the inputs and outputs accordingly.



Assuming all input signals arrive at time zero, and

NOT gate takes 1 time units

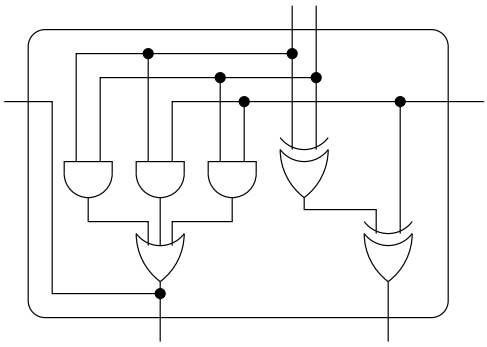
AND gate takes 3 time units

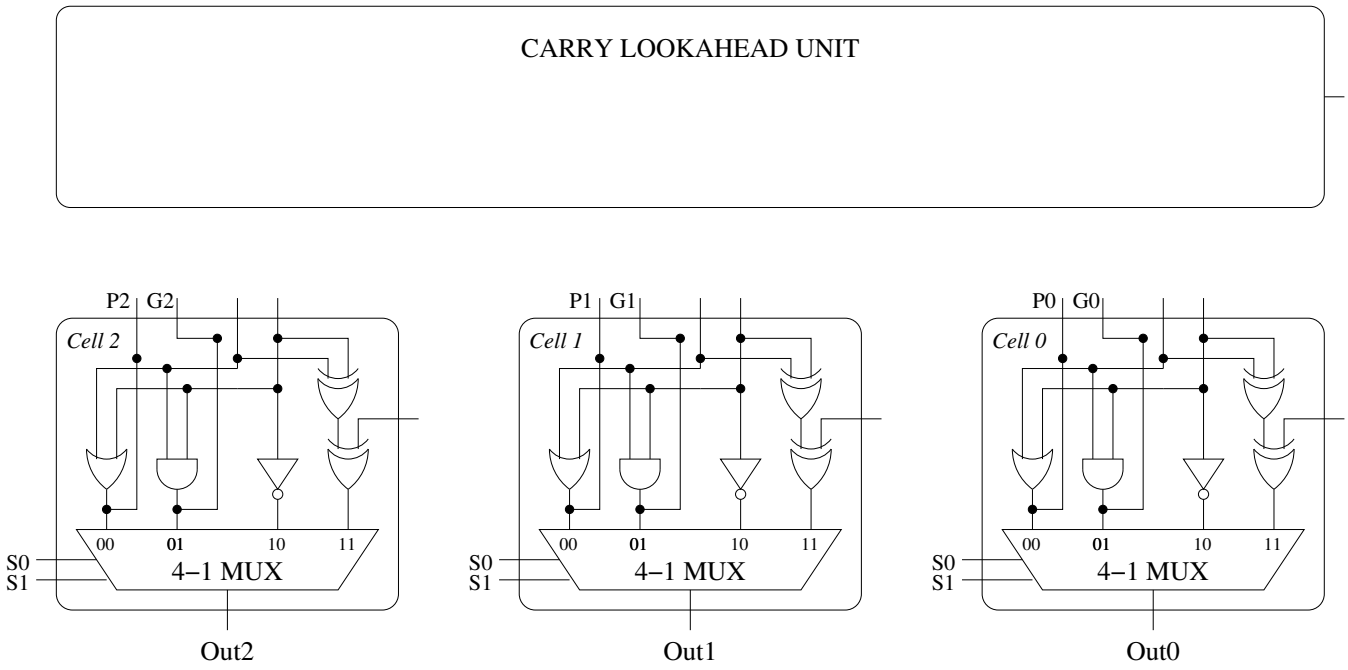
OR gate takes 2 time units

XOR gate takes 4

13] (8) In the above 3-bit adder, what signal takes the **second** longest to become valid, and how long does it take?

14] (6) Here is a Full Adder cell. Label the inputs and outputs and add the circuitry to this necessary to allow it to support subtraction.





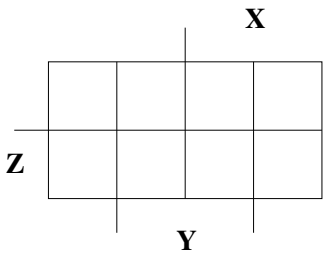
15] (10) The diagram above shows 3 ALU cells and a Carry Lookahead Unit. In the above diagram, draw lines to show how you would connect this up to provide a 3-bit ALU which uses Carry Lookahead. Label all the (unlabled) inputs and outputs accordingly. (You do not have to draw what is inside the Carry Lookahead Unit, and you do not need to worry about subtraction for this problem.)

16] (4) Write the equation for the carry into Cell2 in this ALU, in terms of P's and G's. The equation must not have any parenthesis in it.

Assuming all input signals arrive at time zero, and

NOT gate takes 2 time units
OR gate takes 4 time units
AND gate takes 6 time units
XOR gate takes 8 time units
CL unit takes 10 time units
MUX takes 12 time units

17] (8) What is the worst case time to create Out0? Out2?


X
Z
Y