For the following written/short answer questions with a point value of 3 or less, the correct answer requires fewer than 6 words. So I will only read the first 5 words of your answer. If the point value of the question is 4 or more, you can use up to 12 words.

1] [2] Advances in technology allow us to make both transistors and wires smaller and smaller. If everything else is held constant, what happens to the power density as things shrink?

2] [2] Caches, and in fact the entire memory hierarchy is possible because programs exhibit what principle?

3] [3] When dealing with writes to a cache that hit, what are the two possible approaches? Which approach requires a dirty bit?

4] [2] When dealing with a write that misses in the cache, what are the two possible approaches?

5] [2] What are the two main ways to define performance?

6] [4] Which one is used more now when reporting the performance of a modern chip? Why?

7] [4] Is a Dynamic RAM cell hotter or cooler than a Static RAM cell? Why?

8] [4] What is a benchmark program?

9] [4] Do benchmark programs remain valid indefinitely? Why or why not?

10] [3] Given the following 15-bit address and a 128-byte Direct Mapped cache with a linesize=16, show how an address is partitioned/interpreted by the cache.

0 1 1 1 0 0 0 1 0 1 0 0 1 1 0

11] [4] Assuming a 15-bit address and a 128-byte 4-way Set Associative cache with a linesize=8, show how an address is partitioned/interpreted by the cache.

0 1 1 1 0 0 0 1 0 1 0 0 1 1 0

12] [2] Assuming a 15-bit address and a 160-byte Fully Associative cache with a linesize=4, show how an address is partitioned/interpreted by the cache.

0 1 1 1 0 0 0 1 0 1 0 0 1 1 0

13] [6] Processor A requires 50 instructions to execute a given program, uses 4 cycles per instruction, and has a cycle time of 2 ns. If Processor B takes 5 cycles per instruction, and executes the same program using 20 instructions, what must the cycle time be for Processor B in order to give the same CPU time as Processor A? (Show your work)

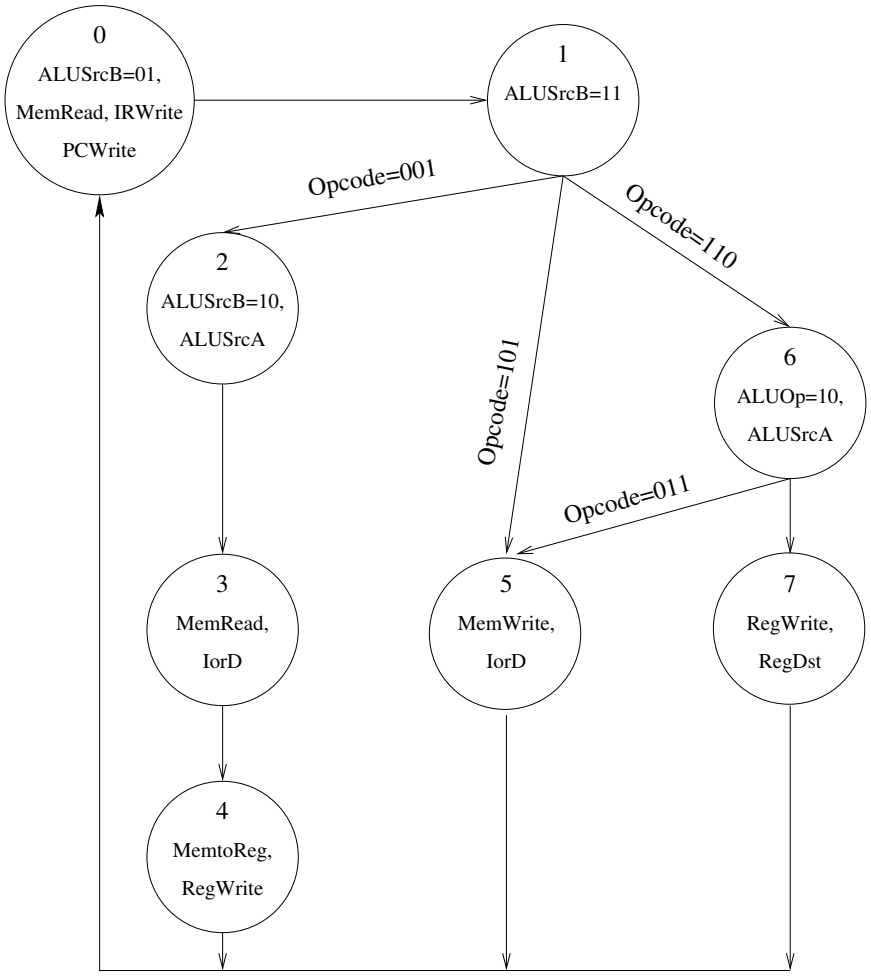
14] [6] An important program spends 80% of its time doing Integer operations, and 20% of its time doing floating point arithmetic. By redesigning the hardware you can make the Integer unit 20% faster (take 80% as long), or you can make the Floating Point unit 90% faster (take 10% as long). Which should you do, and why? (Show your work).

You are working with a processor which has a 1 ns clock cycle time, a cache access time (including hit detection) of 1 clock cycle, a cache miss rate of 0.10 misses per instruction, and a miss penalty of 30 clock cycles. Assuming that the read and write miss penalties are the same and ignoring other stalls,

15] [4] What is the Average Memory Access Time (AMAT)?

16] [2] What is the AMAT if a different cache is used and the miss rate is .01 misses per instruction?

Here is the state diagram for a "random" machine:



17] [4] Assuming there are 3 state variables (Y2-Y0), that State0 = $\overline{Y2}$*$\overline{Y1}$*$\overline{Y0}$ (000) and State7 = Y2*Y1*Y0 (111), and that the 3 opcode bits are in I7-I5, write down the exact boolean equation for the **ALUSrcA** signal.

18] [4] Assuming the same situation as in the previous question, write down the exact boolean equation for **NextState6**.

19] [2] How many total cycles does the shortest instruction take to execute, start to finish? How many does the longest instruction take?

In this question, we are going to wire up an 8-bit machine. This machine will use a 1-operand format, meaning that instructions are of the type ACC=ACC+R. So, for example, "Add R" is ACC=ACC+R.

The machine is byte-addressable. Immediates are sign-extended, and jumps are done by adding the sign-extended Immediate field to the PC.

The machine has 2 different instruction formats: A and B.

A-type:	Opcode	extra
	7-4	3-0

B-type:	Opcode	Immediate
	7-4	3-0

The ALU can perform 7 functions, written this way: OP [ALU2 ALU1 ALU0]

Operation	**ALU2**	**ALU1**	**ALU0**
Add	0	0	1
Sub	0	1	0
Increment B	0	1	1
AND	1	0	0
OR	1	0	1
NOT A	1	1	0
XOR	1	1	1

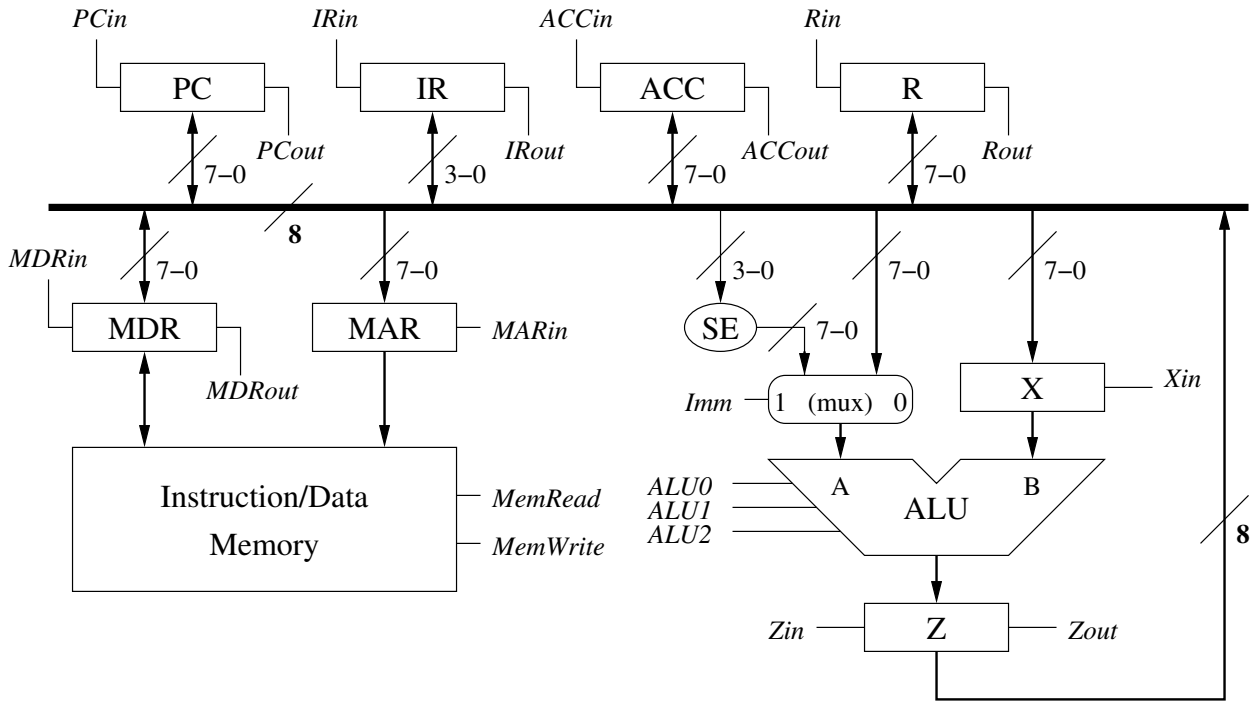
Here are a few of the instructions that have been defined:

Name	**Opcode**	**Operation**
ADD	0001	ACC=ACC+R
ADDM	0010	ACC=ACC+MEM[R]
DDI	0011	ACC=ACC+Imm
COPYA2R	0100	R=ACC
COPYR2A	0101	ACC=R
LOADACC	0110	ACC=MEM[R]
JMP	1111	PC=PC+Imm

On the following page is a diagram of the machine. The control signals are in italics. The sign extend logic creates a 5-bit value which matches the contents of bit 3, so that the 8-bit value generated looks like 33333210 (instead of 76543210).

Here are the 20 control signals.

PCin	PCout	IRin	IRout	Rin	Rout	MARin
ACCin	ACCout	MDRin	MDRout	Zin	Zout	Xin
ALU0	ALU1	ALU2	MemRead	MemWrite	Imm	



20] [10] Fill in the steps necessary to perform an instruction fetch (incrementing the PC is considered part of the instruction fetch process). Assume memory can respond in a single cycle.

Step	PCin	IRin	Rin	ACCin	MARin	MDRin	Zin	Xin	PCout	IRout	Rout	ACCout	MDRout	Zout	ALU2	ALU1	ALU0	Mread	Mwrite	Imm
0																				
1																				
2																				
3																				
4																				
5																				

21] [8] Now that you have done the instruction fetch, fill in the microcode steps necessary to perform the following instruction: **JMP -3**

Step	PCin	IRin	Rin	ACCin	MARin	MDRin	Zin	Xin	PCout	IRout	Rout	ACCout	MDRout	Zout	ALU2	ALU1	ALU0	Mread	Mwrite	Imm
0																				
1																				
2																				
3																				
4																				

22] [6] Assume a 10-bit processor, with a 64-byte 2-way set associative cache and a linesize of 8. This is the contents of the cache (as always, there may be more information than you need):

Set 0								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
10101	3B	C1	43	86	3B	C1	43	86
11001	9D	90	B3	65	F4	EB	7A	BC

Set 1								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	72	9A	49	6F	84	CC	62	8D
11011	C4	25	C8	2E	75	E0	5A	F5

Set 2								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	E9	BA	C6	03	B8	AB	14	2B
11011	17	09	5A	8B	8F	0D	25	CD

Set 3								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	F8	E5	B4	AB	F4	50	6B	07
11011	EF	8C	99	9E	71	46	BF	0F

Set 7								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
00010	03	47	05	45	E8	39	39	9D
10101	51	FE	CF	B5	5D	2A	DE	D8

Set 6								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11111	5A	70	5C	18	15	52	ED	1C
01011	CF	7E	2E	F9	25	8C	9C	38

Set 5								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	E0	C4	2C	B4	5D	AE	66	6E
11011	FF	D0	81	2E	4E	94	E5	20

Set 4								
Tag	D(0)	D(1)	D(2)	D(3)	D(4)	D(5)	D(6)	D(7)
11110	F7	8B	4E	E6	E7	94	B9	2D
11011	F9	09	23	A1	7A	C5	65	35

a) If the processor issues the address

1 0 1 0 1 1 0 1 1 0

Is this a hit in the cache? (YES NO) If YES, circle the entry and the data value that is returned.

b) If the processor issues the address

1 1 0 1 1 1 1 1 1 0

Is this a hit in the cache? (YES NO) If YES, circle the entry and the data value that is returned.

In this question we are dealing with a Direct Mapped cache. Assume 8-bit addresses are partitioned in the following manner:

Tag	Entry	Offset
TTTT	EEE	L

(Tag is left most 4 bits, entry is middle 3, offset into line is right most bit)

You are given the following address reference sequence (in Hex):

0x47,0x46,0x44,0x93,0x45

23] [10] In the table below, fill in the Cache's Tag values after each memory reference has been processed. If it is a miss, you should enter what the new tag should be in the appropriate slot. (X indicates the entry is invalid). If it is a hit, you should place an H in the correct location. There may be more Tag Array entries than you need. *Only write down things that change - do not fill in all the entries that remain the same.*

Tag Array	Contents of Tag Array after processing address (Time ->)					
Entry Number	Initial Contents	0x47 (0 1 0 0 0 1 1 1)	0x46 (0 1 0 0 0 1 1 0)	0x44 (0 1 0 0 0 1 0 0)	0x93 (1 0 0 1 0 0 1 1)	0x45 (0 1 0 0 0 1 0 1)
0	X					
1	X					
2	X					
3	X					
4	X					
5	X					
6	X					
7	X					
8	X					
9	X					
10	X					
11	X					
12	X					
13	X					
14	X					
15	X					

24] [2] What set of memory addresses are sent to memory on the first miss?