University of California, Davis
Department of Computer Science

ECS-154A Computer Architecture

Professor Farrens

Fall 2024

Assessment 2

Cheating on exams is prohibited by the Academic Code of Conduct. I understand that if I am caught cheating on this exam my scores will be negated and I will receive no credit on the exam. Persons caught cheating will also face University disciplinary actions.

Name: _____

Signature: _____

Student ID number: _____

1] (3) Explain what the hold time is for a flip-flop.

2] (3) Explain what the setup time is for a flip-flop.

3] (3) Explain what the propagation time is for a latch.

4] (4) What is the difference between the Mealy and Moore models of sequential design? Give one disadvantage for the Mealy approach.

5] (3) Draw a gate-level diagram of an SR latch. Label the inputs and outputs

6] (3) Are these K-maps for Y1', Y2', or Y3'? How can you tell?

J'

Y2 \ X				
		d	d	
	d	d	d	d
Y3	d	d	d	d
	1	d	d	1

Y1

K'

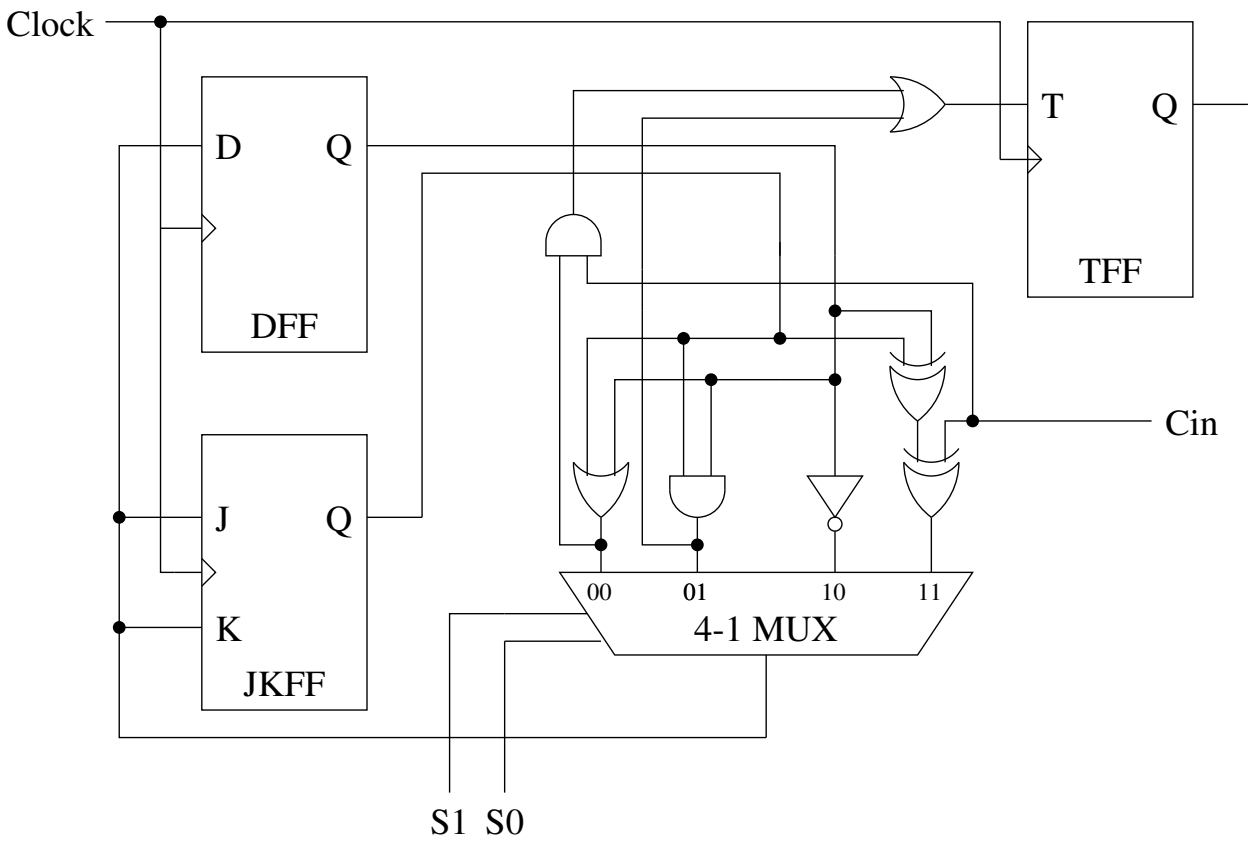
Y2 \ X				
	d	d	d	d
	d	1	1	d
Y3	d			d
	d	d		d

Y1

7] (10) Assuming rising edge-triggered flipflops, what is the minimum cycle time (the minimum time between rising clock edges) that will still guarantee correct behavior for the following circuit? Use the following delay values, and assume all input signals become valid at time 0.

AND: 5ns | OR: 4ns | NOT: 2ns | XOR: 6ns | NAND: 3ns | NOR: 5ns | MUX: 7ns
Tprop (DFF): 7ns | Tsetup (DFF): 3ns | Thold (DFF): 1ns
Tprop (TFF): 8ns | Tsetup (TFF): 4ns | Thold (TFF): 1ns
Tprop (SRFF): 9ns | Tsetup (SRFF): 4ns | Thold (SRFF): 1ns
Tprop (JKFF): 10ns | Tsetup (JKFF): 5ns | Thold (JKFF): 1ns

Note: You must show the path in order to get credit.

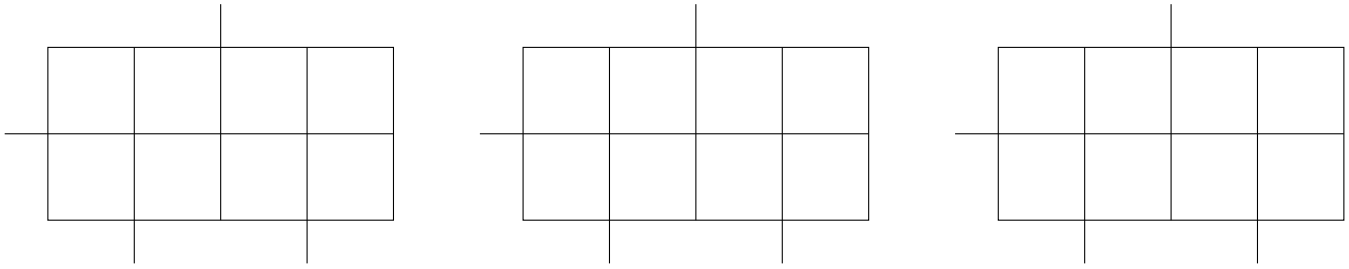


8] (2) Suppose the OR gate takes 8ns instead of 4ns - would your answer change? If so, how?

9] (8) You have been asked to create a new flipflop, which has two inputs - the "D" and the "E". All you have to work with is an SRFF. The DEFF is to exhibit the following behavior:

Present State		Next State
D	E	Z'
0	0	0
0	1	Z
1	0	1
1	1	Zbar

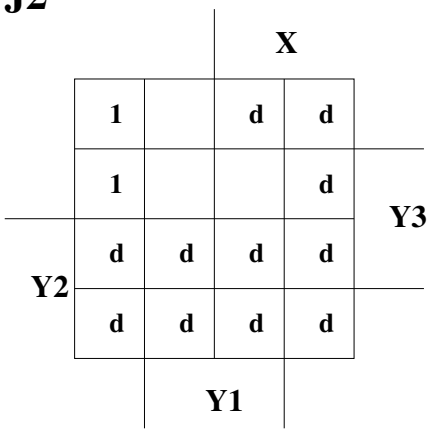
Write down what the S and R inputs must be (in terms of D, E, and Z) in order to provide the desired functionality. Be sure to minimize the equations.



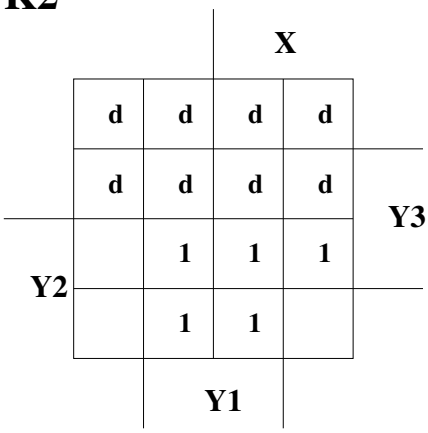
Desired Transition	SR FF	JK FF	T FF	D FF
Y -> Y'	S R	J K	T	D
0 -> 0	0 d	0 d	0	0
0 -> 1	1 0	1 d	1	1
1 -> 0	0 1	d 1	1	0
1 -> 1	d 0	d 0	0	1

10] (4) You have derived the following karnaugh maps for the inputs to a JK flip-flop. Unfortunately, all you have available to use are T flip-flops, which you will have to use instead. Show the resulting karnaugh map for the modified version of the circuit (the one that uses the T instead of the JK flip-flop), and minimize the equations.

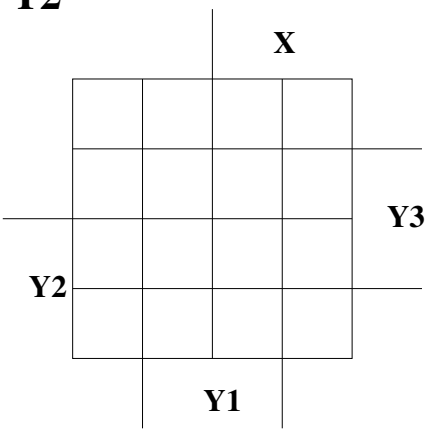
J2'



K2'



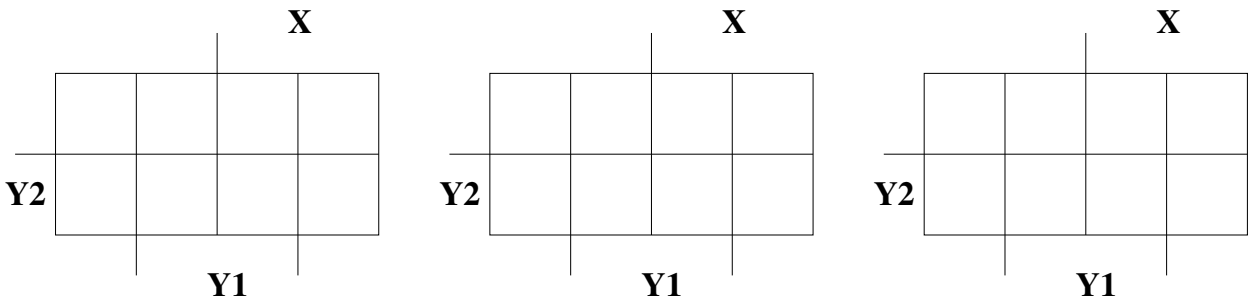
T2'



Desired Transition Y -> Y'	SR FF S R	JK FF J K	T FF T	D FF D
0 -> 0	0 d	0 d	0	0
0 -> 1	1 0	1 d	1	1
1 -> 0	0 1	d 1	1	0
1 -> 1	d 0	d 0	0	1

11] (12) Given the following table, draw the Karnaugh maps for Y1', Y2' and Z in terms of X, Y1 and Y2, and then write **minimum** boolean equations for each. Do not worry about the fact that the machine might get stuck in a particular state and be unable to get out - just solve the problem as presented.

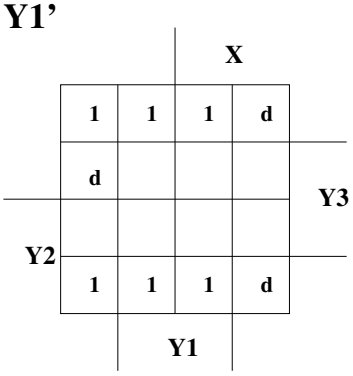
Present State (Y1 Y2)	Next State X=0 (Y1' Y2')	Next State X=1 (Y1' Y2')	Output X=0	Output X=1
01	10	00	1	0
10	10	11	1	0
11	10	01	1	0



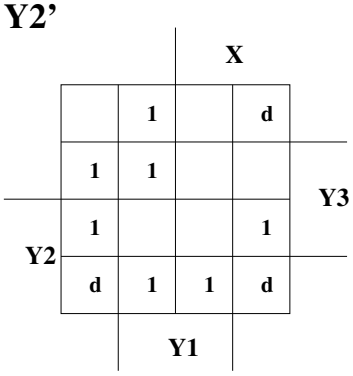
Desired Transition Y -> Y'	SR FF S R	JK FF J K	T FF T	D FF D
0 -> 0	0 d	0 d	0	0
0 -> 1	1 0	1 d	1	1
1 -> 0	0 1	d 1	1	0
1 -> 1	d 0	d 0	0	1

12] (15) Given the following Karnaugh maps, implement the sequential machine using an SR FF for Y1, a JK FF for Y2, and a T FF for Y3. You do not need to draw the gates, but you do need to write down the **minimized** input equations for each of the inputs of each of the Flip Flops in the circuit.

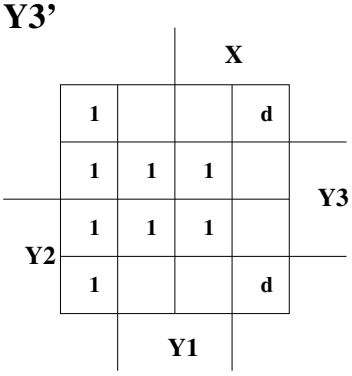
Y1'



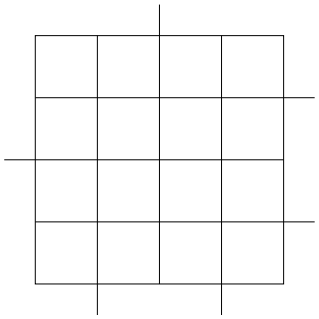
Y2'



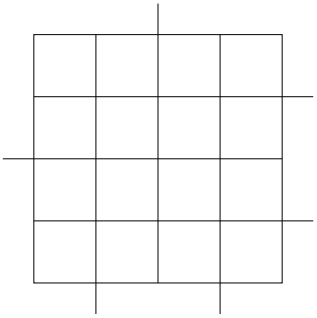
Y3'



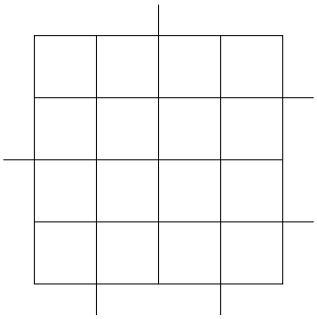
S1



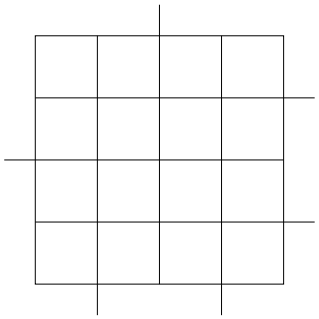
J2



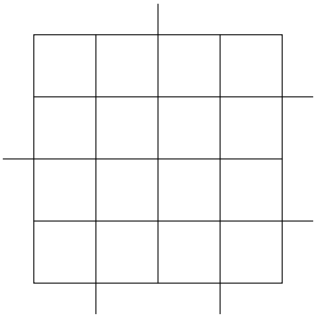
T3

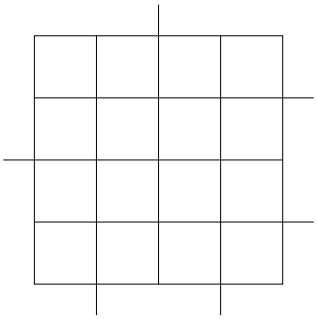


R1



K2





Desired Transition Y -> Y'	SR FF S R	JK FF J K	T FF T	D FF D
0 -> 0	0 d	0 d	0	0
0 -> 1	1 0	1 d	1	1
1 -> 0	0 1	d 1	1	0
1 -> 1	d 0	d 0	0	1

13] (12) On a planet far, far away you have been hired to create a vending machine which accepts two coins, the 1 Quatloo piece and the 3 Quatloo piece. Merchandise costs 4 Quatloos, and the machine must give exact change. Let X1=3 Quatloo coin and X2=1 Quatloo coin, and assume both coins cannot be inserted simultaneously.

Using a Mealy model, draw the State Transistion Diagram (the circles and the arcs) for this finite state machine. Label the transitions on the diagram using the format we used in class (inputs over outputs). You must clearly show what each output bit represents. Let state S0=no money input (the Start state). Input 00 sends you to the same state you are currently in.

14] (10) Draw the state transition diagram for a 2-bit shifter that always shifts the input variable into the least significant bit and discards the most significant bit (it shifts left, in other words). X=1 indicates a 1 should be shifted in, X=0 indicates a 0 should be shifted in. Use a Moore model.

15] (8) Here is a state transition table. Minimize this if possible, and then assign bit patterns to each state.

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A	B	C	0	0
B	E	D	0	1
C	A	D	1	0
D	B	C	0	0
E	B	C	1	0