UNIVERSIDAD FRANCISCO DE VITORIA
Computación de Alto Rendimiento

COMPUTACIÓN DE ALTO RENDIMIENTO

Tema 1: Introducción

Grado en Ingeniería Informática ***Curso 2022/2023***

Objetivos

- Introducción al paralelismo
- Grandes retos de la humanidad – oportunidades de uso de HPC
- Pasado, presente y futuro de la supercomputación

Introducción

- ¿Qué es el paralelismo? : Combinar la potencia de cálculo de varios procesadores para aumentar el rendimiento.
  - Distintas formas de interconexión.
  - Información compartida.
  - Datos compartidos
  - Paralelización del código.
  - Reparto de la carga de trabajo.

Introducción

- Ingeniería y diseño:
  - Solución a problemas de optimización. Simulación.
    - (p.e., High-speed circuits, Simplex, Branch-and-bound, Genetic programming…)
  - Aplicaciones científicas: Solución a problemas científicos con alta carga computacional
    - (p.e., bioinformática, proyecto Genoma Humano, modelado de la climatología).
  - Aplicaciones comerciales: Sistemas distribuidos en Internet altamente escalables.
    - (p.e., Wall Street plataformas IBMs SP supercomputers y Sun Ultra HPC servers)

Introducción

Tipos de paralelismo

- **Implícito: transparente al usuario**
  - Hardware: 1 Procesador, 1 Sistema de Memoria, 1 Red de interconexión (datapath)
  - Uso de técnicas que permiten ejecutar más de una instrucción por ciclo de reloj: **segmentación (pipelining)**, **superescalar, multithreading**…

- **Explícito**
  - Hardware:
    - Múltiples procesadores
    - Múltiples memorias: low-latency high-bandwidth storage
    - Redes de interconexión (datapaths)
  - Software:
    - Sistemas Operativos paralelos
    - Programas orientados a concurrencia

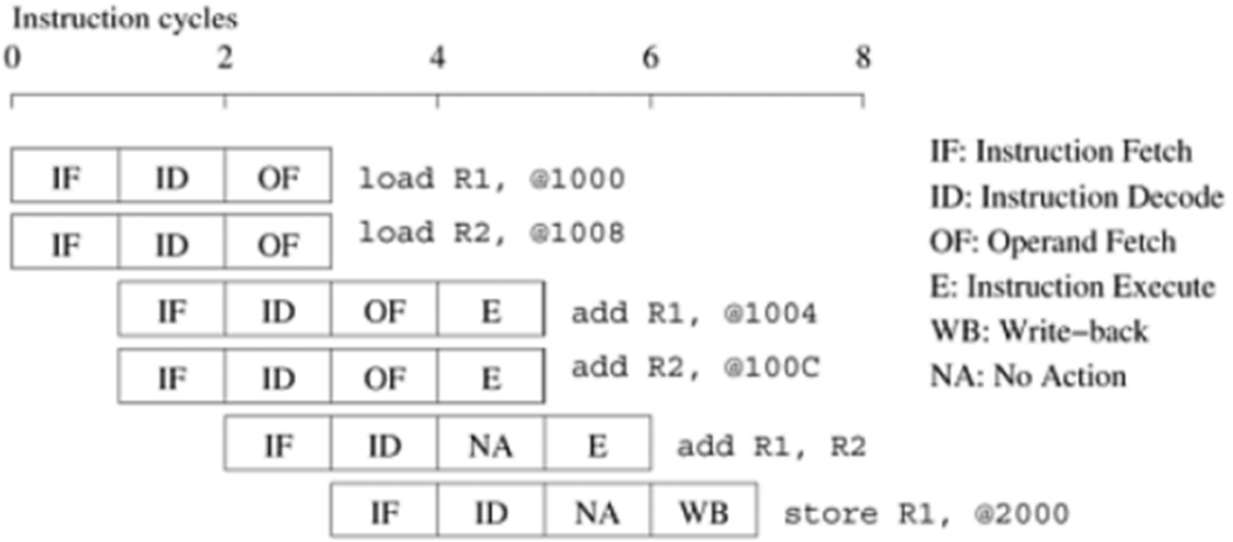
Objetivo: Utilizar estos elementos para
Mejorar el Speed-up: $S = T_s / T_p$
Abordar problemas con alta demanda de memoria

Ejecución: Pipelining & Superescalar

```
1. load R1, @1000        1. load R1, @1000        1. load R1, @1000
2. load R2, @1008        2. add R1, @1004         2. add R1, @1004
3. add R1, @1004         3. add R1, @1008         3. load R2, @1008
4. add R2, @100C         4. add R1, @100C         4. add R2, @100C
5. add R1, R2            5. store R1, @2000       5. add R1, R2
6. store R1, @2000                                6. store R1, @2000
```

(i) (ii) (iii)

(a) Three different code fragments for adding a list of four numbers.



Introducción

Elementos de un computador paralelo

- Hardware:
  - Múltiples procesadores
  - Múltiples memorias
  - Redes de interconexión (datapaths)
- Software:
  - Sistemas Operativos paralelos
  - Programas orientados a concurrencia

Introducción

Plataformas para procesamiento paralelo

- Organización lógica: Visión que tiene el programador de la máquina, desde el punto de vista del software del sistema.
  - Cómo expresar tareas paralelas: Modelo de Control.
  - Cómo expresar la interacción entre estas tareas: Modelo de Comunicación.
- Organización física: La arquitectura hardware real.
- La Arquitectura física es, hasta cierto punto, independiente de la arquitectura lógica.

Introducción

Organización lógica - Modelo de control

Taxonomía de Flynn:

Es una clasificación para las computadoras con arquitectura paralela, propuesta por el profesor emérito de la Universidad de Stanford Michael J. Flynn, la cual clasifica a las mismas atendiendo a la cantidad de instrucciones y flujo de datos concurrentes en un instante de procesamiento

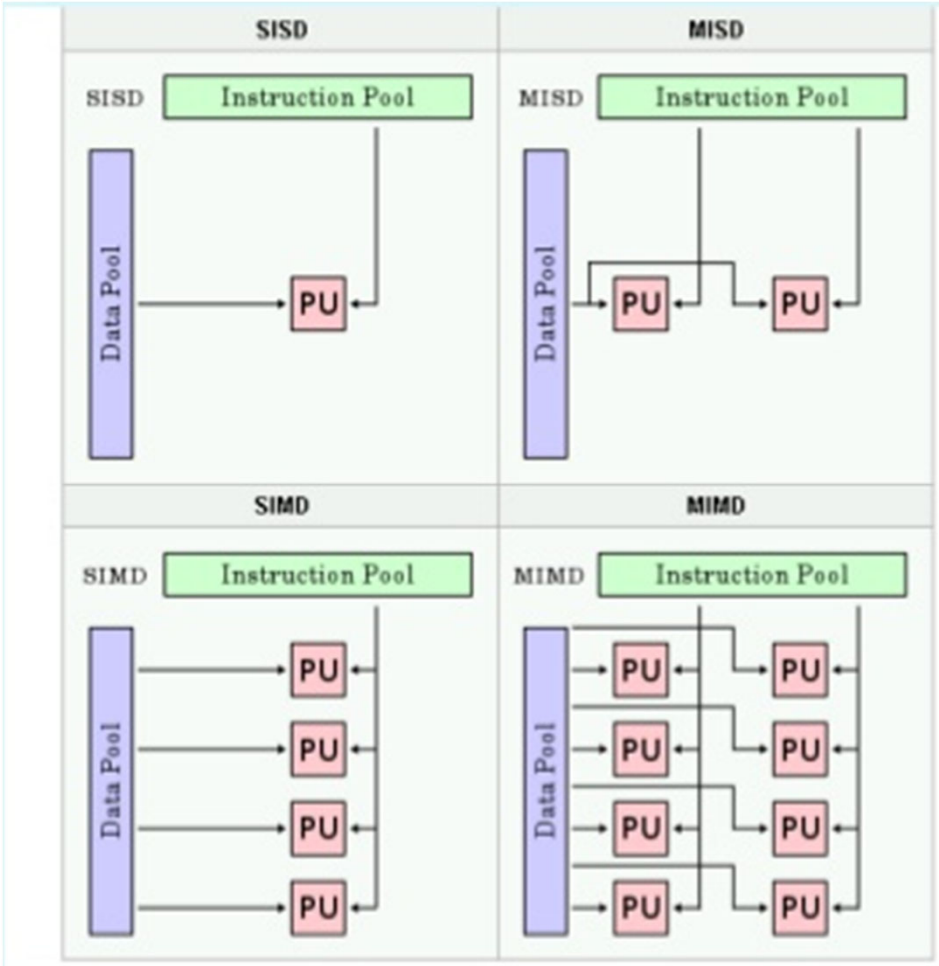
Esta taxonomía enuncia 4 clasificaciones las cuales son:

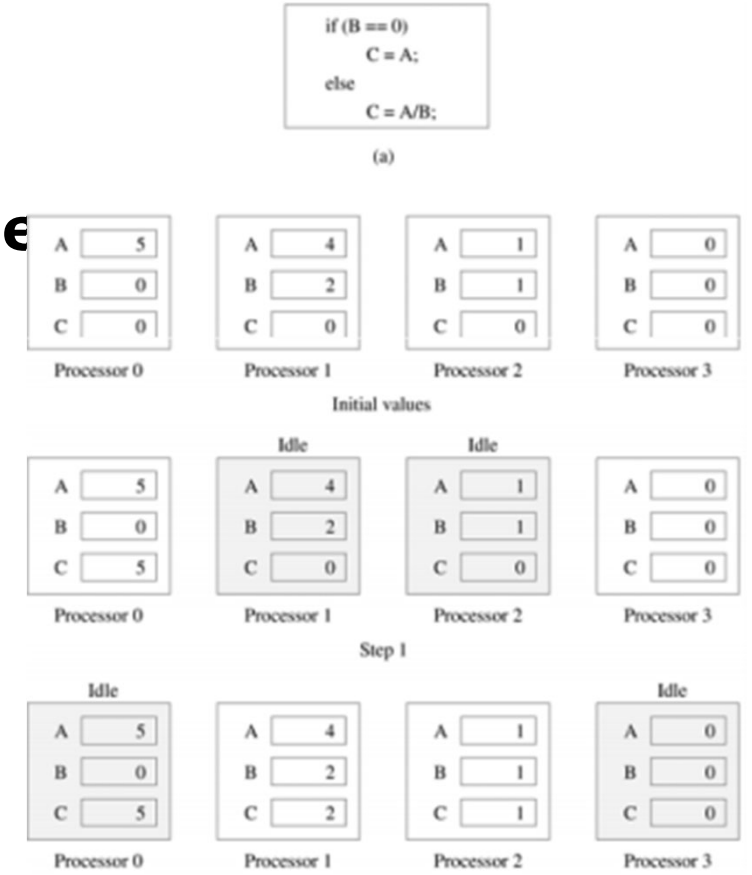
- **SISD:***(Single Instruction Single Data)*
- **MISD:***(Multiple Instruction Single Data)*
- **SIMD:***(Single Instruction Multiple Data)*
- **MIMD:***(Multiple Instruction Multiple Data)*

Introducción

Organización lógica - Modelo de

Taxonomía de Flynn:





Falta de eficiencia en SIMD

Introducción

Organización Lógica - Modelo de comunicación:

Dos maneras distintas de intercambiar información entre tareas paralelas:

- Paso de mensajes (estándar MPI).
- Espacio de memoria compartida (estándar OpenMP).

Introducción

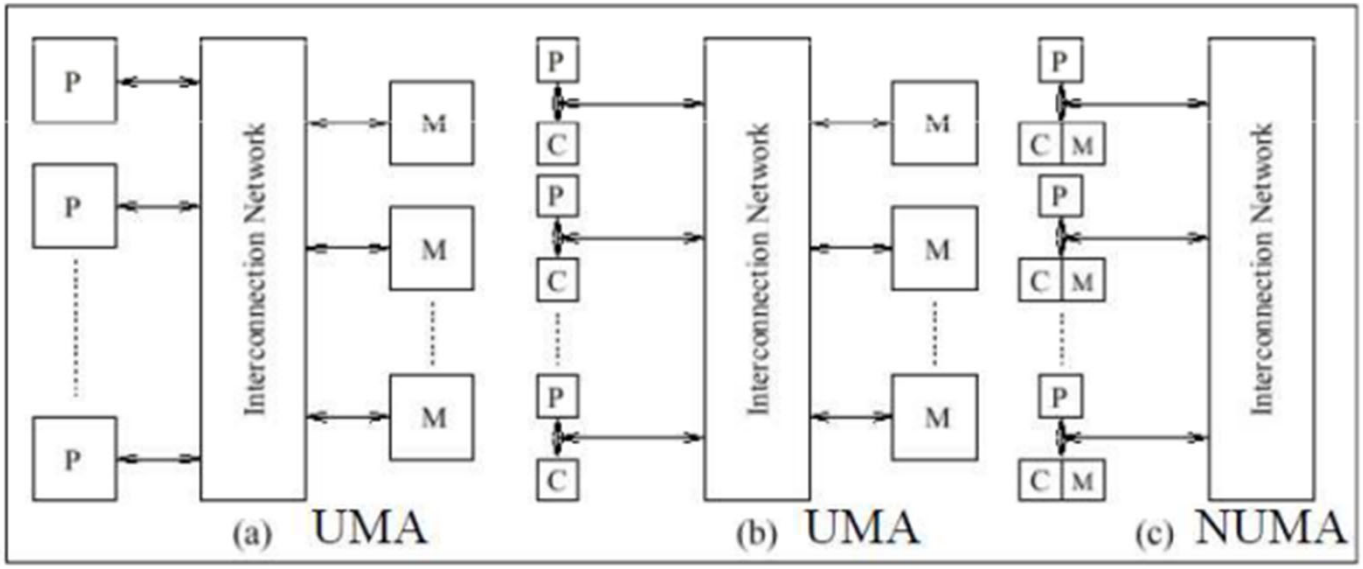
Organización Lógica: Paso de mensajes
(Multicomputadores)

- Cada procesador tiene un espacio de memoria propio e independiente.
  - No existen problemas en el acceso a memoria.
- La comunicación se produce a través de mensajes entre el procesador emisor y el receptor.
  - Las dificultades se presentan en la red de conexión.
- Operaciones básicas: send, receive, numprocs y whoami.
- Estándares: MPI (Message Passing Interface), PVM (Parallel Virtual Machine).
- Ejemplos: IBM SP, SGI Origin 2000, workstation clusters.

Introducción

Organización Lógica: Espacio de memoria compartida (Multiprocesadores)

- UMA: Acceso a memoria uniforme.
- NUMA: Acceso a memoria no uniforme.



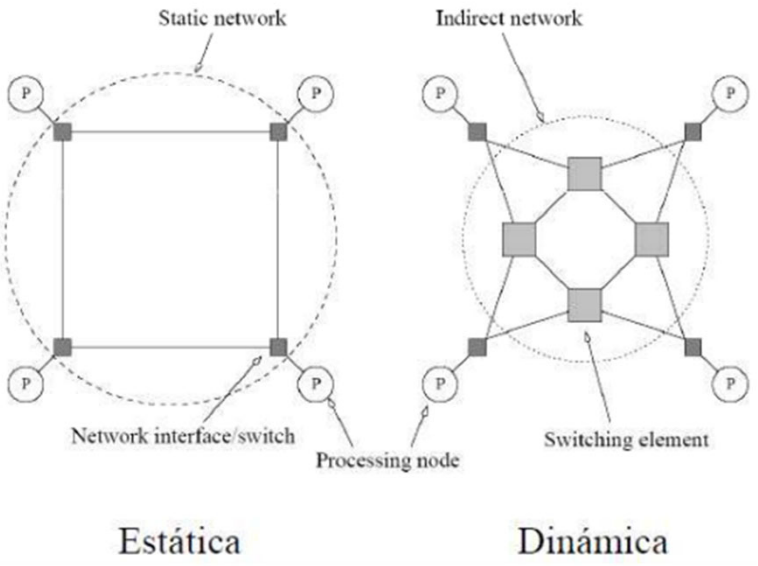
- Estándares: Posix, OpenMP.

Introducción

Organización Física:

- Redes de interconexión (RICs):
  - Proporcionar conexión entre los distintos procesadores y memorias del sistemas

  - Tipo de redes
    - Estática:
      - Enlaces punto a punto: conectan nodos
    - Dinámica:
      - Formada por elementos de conmutación: conectan nodos o bancos de memoria.



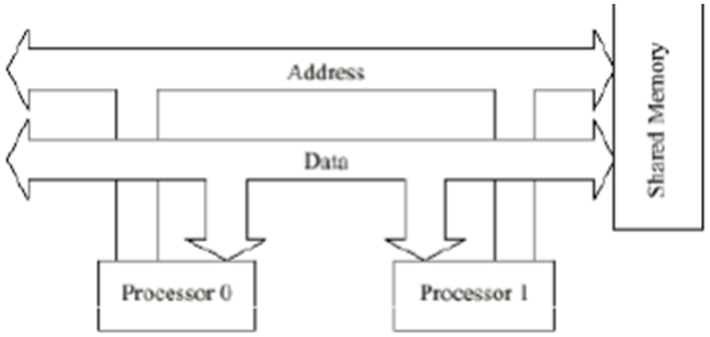
Introducción

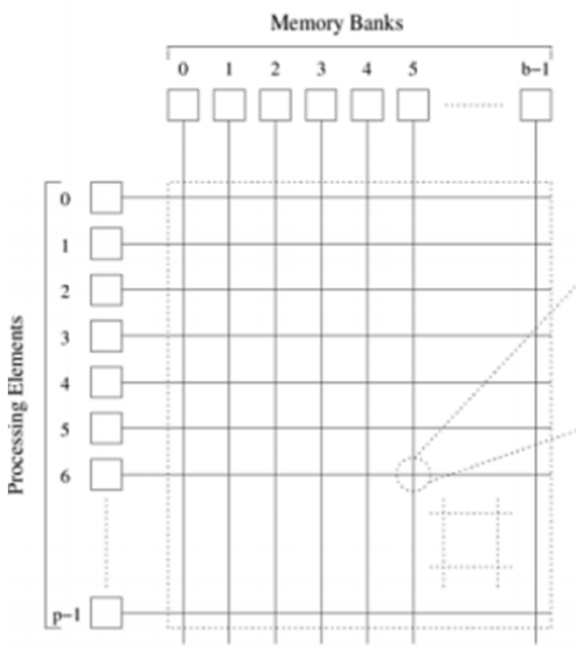
Organización Física - Métricas de evaluación para RICs

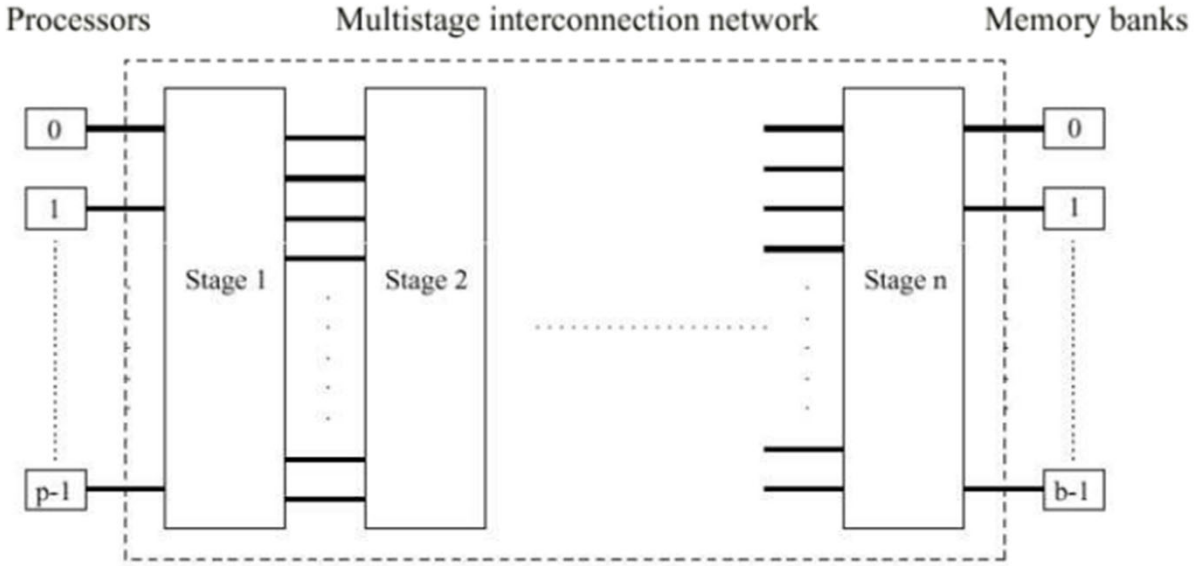
- **Diámetro**: Distancia máxima entre cualquier par de nodos. (Cuanto más pequeño mejor).
- **Conectividad**: Mínimo número de arcos que hay que eliminar para convertir la red en dos subredes desconectadas. (Cuanto más grande mejor).
- **Ancho de Bisección**: Mínimo número de arcos que hay que eliminar para dividir la red en dos mitades iguales. (Cuanto más grande mejor).
- **Ancho de Banda de Bisección**: Mínimo volumen de comunicación permitido entre dos mitades cualesquiera de la red. (Cuanto más grande mejor).
- **Coste**: Número de enlaces en la red. (Cuanto más pequeño mejor).

Introducción

Organización Física - Métricas de evaluación para RICs







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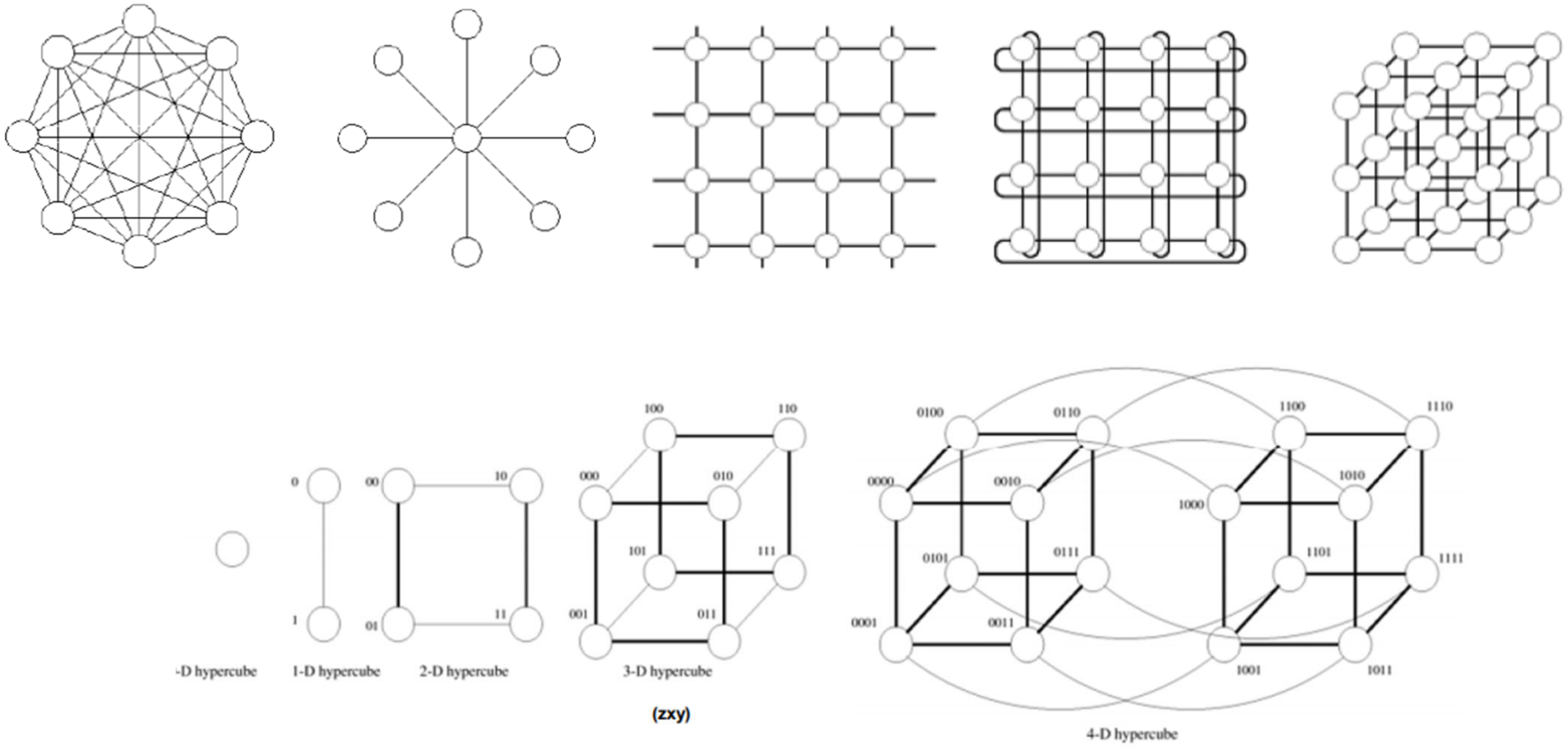
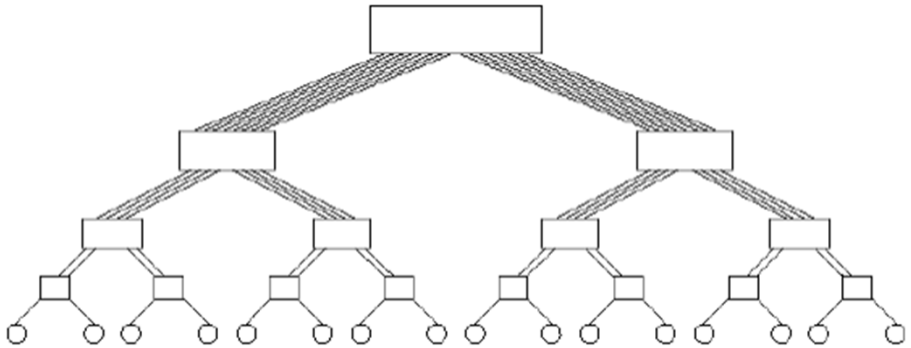
Organización Física - Métricas de evaluación para RICs



Introducción

Organización Física - Métricas de evaluación para RICs



Network	Diameter	Bisection Width	Arc Connectivity	Cost (No. of links)
Completely-connected	1	$p^2/4$	$p-1$	$p(p-1)/2$
Star	2	1	1	$p-1$
Complete binary tree	$2\log((p+1)/2)$	1	1	$p-1$
Linear array	$p-1$	1	1	$p-1$
2-D mesh, no wraparound	$2(\sqrt{p}-1)$	$\sqrt{p}$	2	$2(p-\sqrt{p})$
2-D wraparound mesh	$2\lfloor\sqrt{p}/2\rfloor$	$2\sqrt{p}$	4	$2p$
Hypercube	$\log p$	$p/2$	$\log p$	$(p\log p)/2$
Wraparound k-ary d-cube	$d\lfloor k/2\rfloor$	$2k^{d-1}$	$2d$	dp

Grandes retos de la humanidad – oportunidad uso HPC

https://en.unesco.org/news/top-challenges-future-humanity-and-planet-include-sustaining-ocean-health-reversing

Nxdod#Dxp sxu/#P dod|vld/#rq#58059#P d|#5348

The Board's list of main concerns includes:

- One Ocean, Many Countries: Building a "Blue Economy" Sustainably
- Addressing threats to biodiversity and establishing a new paradigm for the global tropics
- Developing a Comprehensive Strategy Against Infectious Agents, Including a Global System for Immediate Response
- Investing a Fraction of GDP in Research and Education in Basic Science
- Averting Enormous Human Disasters Through Prediction
- Emissions Free Technology: Changing the Fossil Fuel Paradigm
- Providing Drinkable Water for All
- Finding Solutions for a World Overwhelmed by Unequal Resource-use and Continued Population Growth

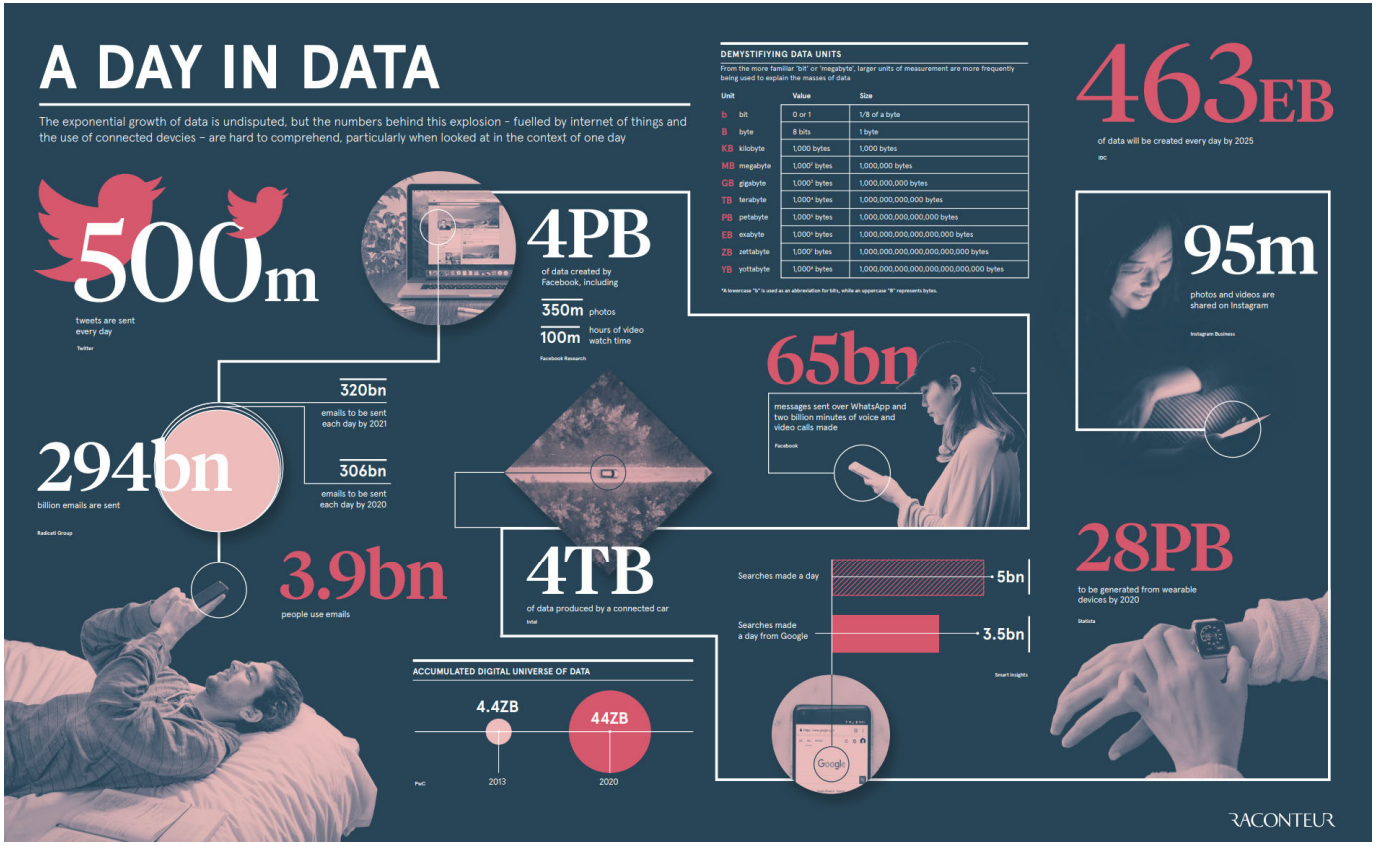
Grandes retos de la humanidad – oportunidad uso HPC

- https://digital-strategy.ec.europa.eu/en/policies/destination-earth
- https://top500.org
- https://www.r-ccs.riken.jp/en/fugaku/
- https://schmidtocean.org/technology/high-performance-computing/

Grandes retos de la humanidad – Uso clave HPC

- “Data has become the driving force behind business, academic, and social progress, forcing significant advancements in computer processing. By **2025, an estimated 463 exabytes of data will be created each day globally**.1 As institutions embrace a “data everywhere” mentality, high-performance computing (HPC) presents new opportunities to take on emerging challenges in these fields.”

Desjardins, jeff. “How much data is generated each day?” World Economic Forum. April 17, 2019. https://www.weforum.org/agenda/2019/04/how-much-data-is-generated-each-day-cf4bddf29f/



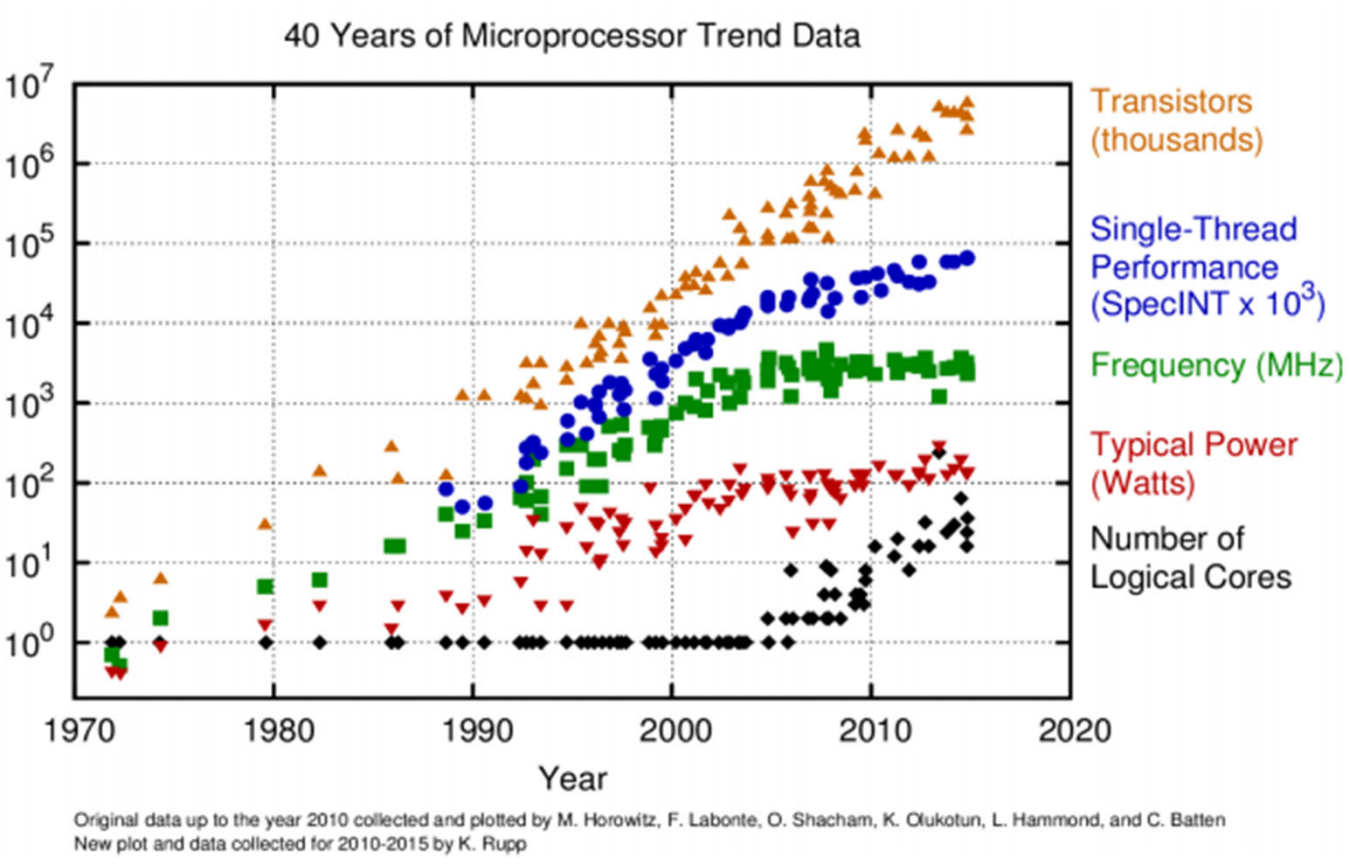
Pasado, presente y futuro de la supercomputación

Motivaciones del paralelismo

- Moore's Law – "number of transistors (components) in an integrated circuit would double approximately every two years" . Maintained this exponential growth for over five decades.
- Dennard Scaling - "as transistors become smaller, their power density remains constant". the clock frequencies flattened in the 1 GHz (= 103 MHz) range since around 2005 (limit of Dennard Scaling)
- → 2005 marked the start of the "multicore era" in which the additional transistors predicted by Moore's Law are being used to increase the number of processor cores in a single integrated circuit.

Pasado, presente y futuro de la supercomputación

Motivaciones del paralelismo



Pasado, presente y futuro de la supercomputación

Past and present

- Vector-MPP (Massively Parallel Processing) Transition
  - *There was no incremental transition path from a shared memory vector design to a distributed memory MPP design*

- Terascaled – Petascaled transition
  - *For most applications, this transition was incremental in the sense that the MPP framework continued to be applicable*
  - *introduction of intra-process parallelism, e.g., use of OpenMP threading, use of GPU accelerators*

- **Petascaled – Exascaled transition**.
  - *exascale transition is currently under way.*
  - *Investing in new control layers and system software support is helpful for addressing the disruption of large on-node heterogenous parallelism*

Pasado, presente y futuro de la supercomputación

petascaled, exascaled supercomputers

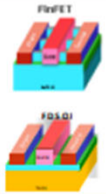
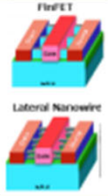
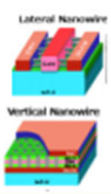
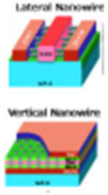
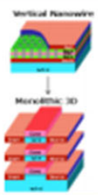
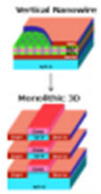
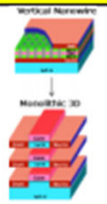
- Exascale computing refers to computing systems capable of **calculating at least 10^{18} floating point operations** per second (1 exaFLOPS). The terminology generally refers to the performance of supercomputer systems and although no single machine has reached this goal as of January 2021, there are systems being designed to reach this milestone. In April 2020, the distributed computing Folding@home network attained one exaFLOPS of computing performance.

Fugaku (supercomputer)

Pasado, presente y futuro de la supercomputación

will exascale and Moore's eras ever end?

Table MM01 - More Moore - Logic Core Device Technology Roadmap

YEAR OF PRODUCTION	2017	2019	2021	2024	2027	2030	2033
	P54M36	P48M28	P42M24	P36M21	P28M14G1	P26M14G2	P24M14G3
Logic industry "Node Range" Labeling (nm)	"10"	"7"	"5"	"3"	"2.1"	"1.5"	"1.0"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5-f1.0	i1.0-f0.7
Logic device structure options	finFET FDSOI	finFET LGAA	LGAA VGAA	LGAA VGAA	VGAA M3D	VGAA M3D	VGAA M3D
Logic device mainstream device	finFET	finFET	LGAA	LGAA	VGAA	VGAA	VGAA
Logic device technology naming							
Patterning technology inflection for Mx interconnect	193i	193i, EUV	193i, EUV	193i, EUV	193i, EUV	193i, EUV	193i, EUV
Channel material technology inflection	Si	SiGe25%	SiGe50%	Ge, IIIV (TFET)	Ge, IIIV (TFET)	Ge, IIIV (TFET)	Ge, IIIV (TFET)
Process technogy inflection	Conformal deposition	Conformal Doping, Contact	Channel, RMG	CFET	Seq. 3D	Seq. 3D	Seq. 3D
Stacking generation	2D	2D	2D 3D: W2W or D2W	3D: P-over-N	3D: SRAM-on-Logic	3D: Logic-on-Logic, Hetero	3D: Logic-on-Logic, Hetero
Design-technology scaling factor for standard cell	-	1.11	2.00	1.13	0.53	1.00	1.00
Design-technology scaling factor for SRAM (111) bitcell	1.00	1.00	1.00	1.00	1.25	1.00	1.00
Number of stacked devices in one tier	1	1	3	4	1	1	1
Tier stacking scaling factor for SoC	1.00	1.00	1.00	1.00	1.80	1.80	1.80
Vdd (V)	0.75	0.70	0.65	0.60	0.50	0.45	0.40
Physical gate length for HP Logic (nm)	20.00	18.00	14.00	12.00	10.00	10.00	10.00
SoC footprint scaling node-to-node - 50% digital, 35% SRAM, 15% analog+IO	-	64.9%	51.3%	64.3%	64.2%	50.9%	50.7%

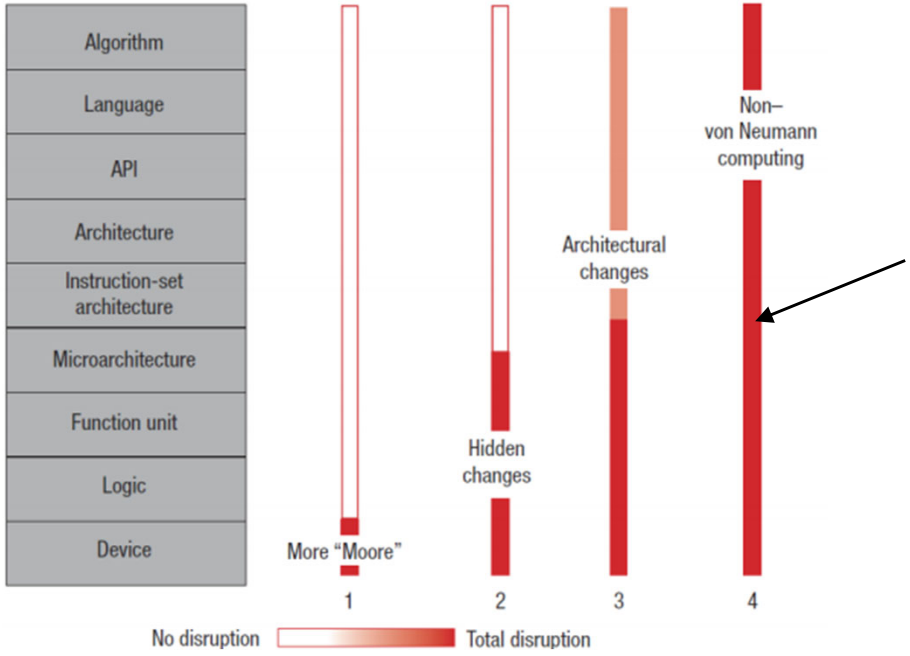
Yes!

Moore's Law must come to an end due to basic physical limitations, including the fact that the size of the atoms used in silicon chip fabrication is around 0.2nm. Table shows the projected transistor size ("node range") decreasing from 10nm in 2017 to 1.0nm in 2033

Pasado, presente y futuro de la supercomputación

Future – still in CMOS

Levels of Disruption in Post-Moore era:



The most radical (Level 4) approaches rethink computing paradigms from the ground up, and will require new algorithms, programming systems, system software, and hardware. Examples of this include Neuromorphic Computing, Quantum Computing and Analog/Thermodynamic Computing.

Pasado, presente y futuro de la supercomputación

Future – Finding and risks:

- *Need for clarity in future HPC roadmap for science applications.*
- *Extreme heterogeneity with new computing paradigms will be a common theme in future HPC technologies*
- *Need to prepare applications and system software for extreme heterogeneity*
- Need for early testbeds for future HPC technologies
- Open hardware is a growing trend in future platforms

Pasado, presente y futuro de la supercomputación

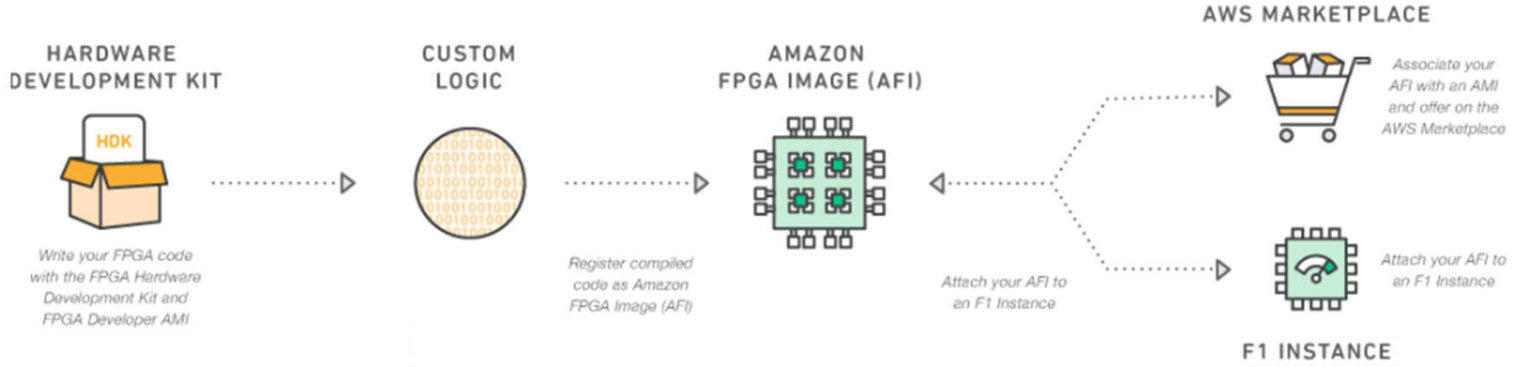
Future trends

- 6 most representative of the trends expected in future HPC systems:
  - Reconfigurable Logic
  - Memory-Centric Processing
  - Silicon Photonics
  - Neuromorphic Computing
  - Quantum Computing
  - Analog Computing

Pasado, presente y futuro de la supercomputación

Future - Reconfigurable Logic

Field Programmable Gate Arrays (FPGAs) offers a low-power, high performance option for exascale and post-exascale computing



DEVELOP

Develop custom Amazon FPGA Images (AFI) using the Hardware Development Kit (HDK) and full set of design tools and simulators.

DEPLOY

Deploy your AFI directly on F1 instances and take advantage of all the scalability, agility, and security benefits of EC2.

OFFER

Offer AFIs you design on the AWS Marketplace for other customers.

PURCHASE

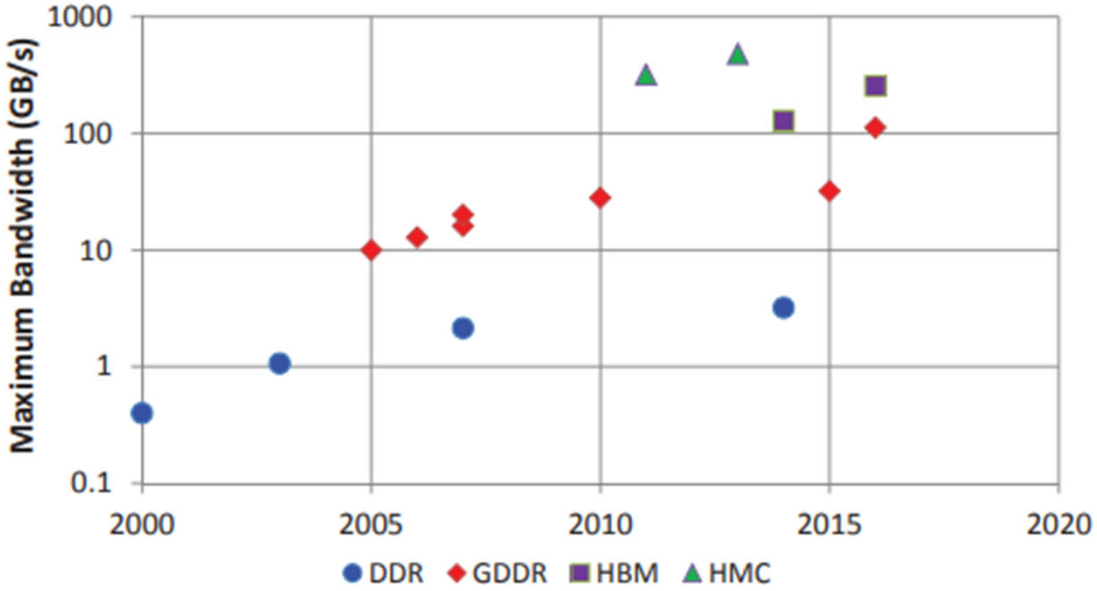
Purchase AFIs built and listed on AWS Marketplace to quickly implement common hardware accelerations.

Figure 4.1: Growing an ecosystem for Amazon EC2 F1 FPGA instances (image source: `https://aws.amazon.com/ec2/instance-types/f1`)

Pasado, presente y futuro de la supercomputación

Future - Memory-Centric Processing

When we think of the effects of Moore's Law, we think of a continued increase in the compute performance of conventional processor chips. While true, this ignores what is needed from memory chips to balance this performance increase



Pasado, presente y futuro de la supercomputación

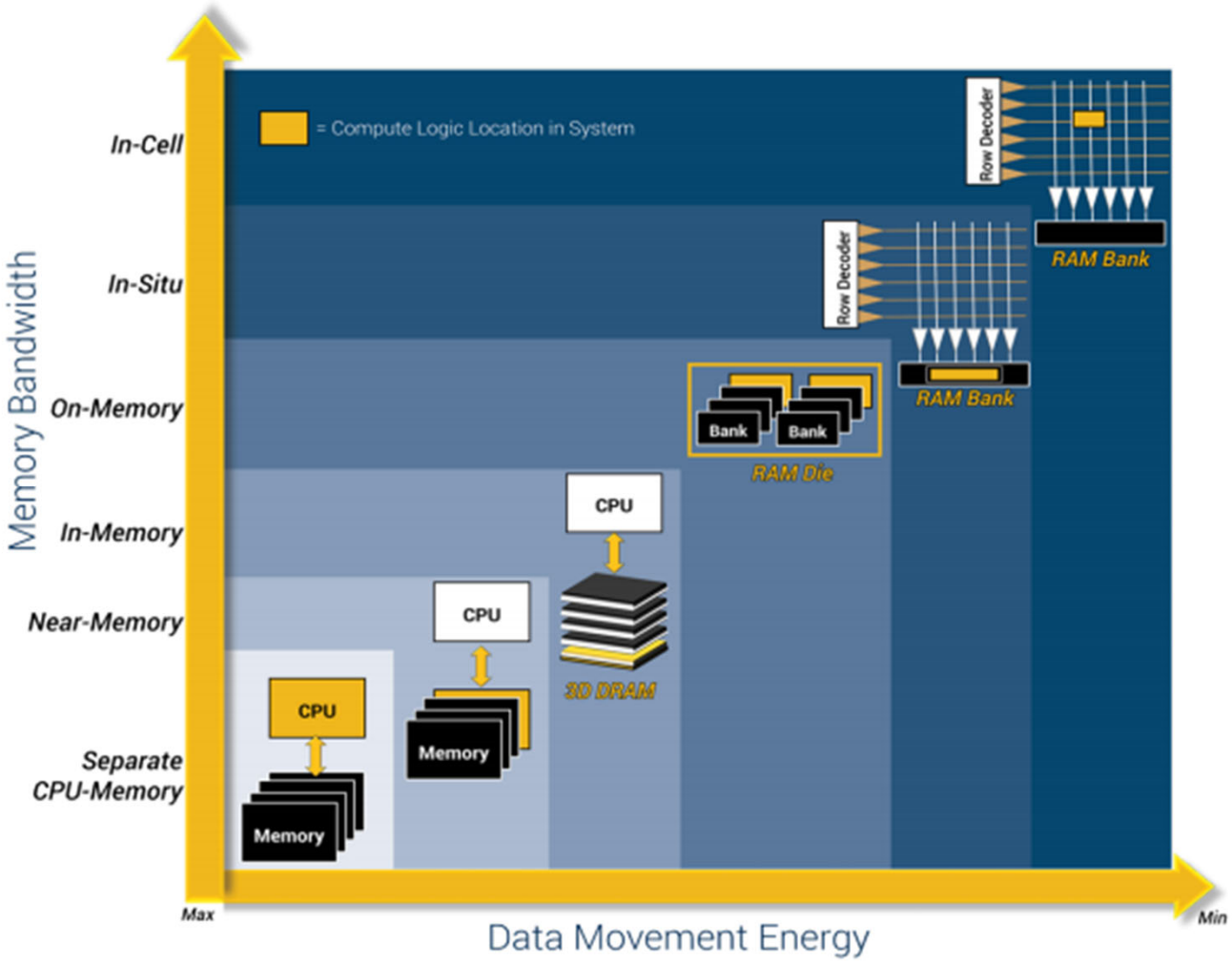
Future - Memory-Centric Processing

Memory-centric processing is a technique that attempts to break this interface problem by moving processing much closer to memory than a conventional core.

- **In Cell**: within the bit cell storing the data.
- **At the Sense Amps**: at the bottom of the block of memory cells, at the first point where the data is converted to a digital level, and where it has access to literally hundreds to thousands of bits from a complete "row".
- **In-Situ**: a bit further down the digital chain but still within a memory bank, typically just after a "column" multiplexer that is driven from the output of the sense amps.
- **On Memory**: on the memory die itself, typically with access to all the independent memory banks on the die.
- **In Memory**: on a die between a memory, or stack of memory die, and the processor.
- **Near memory**: near the memory controller that may be on the memory die, but typically on a processor die.

Pasado, presente y futuro de la supercomputación

Future - Memory-Centric Processing



Pasado, presente y futuro de la supercomputación

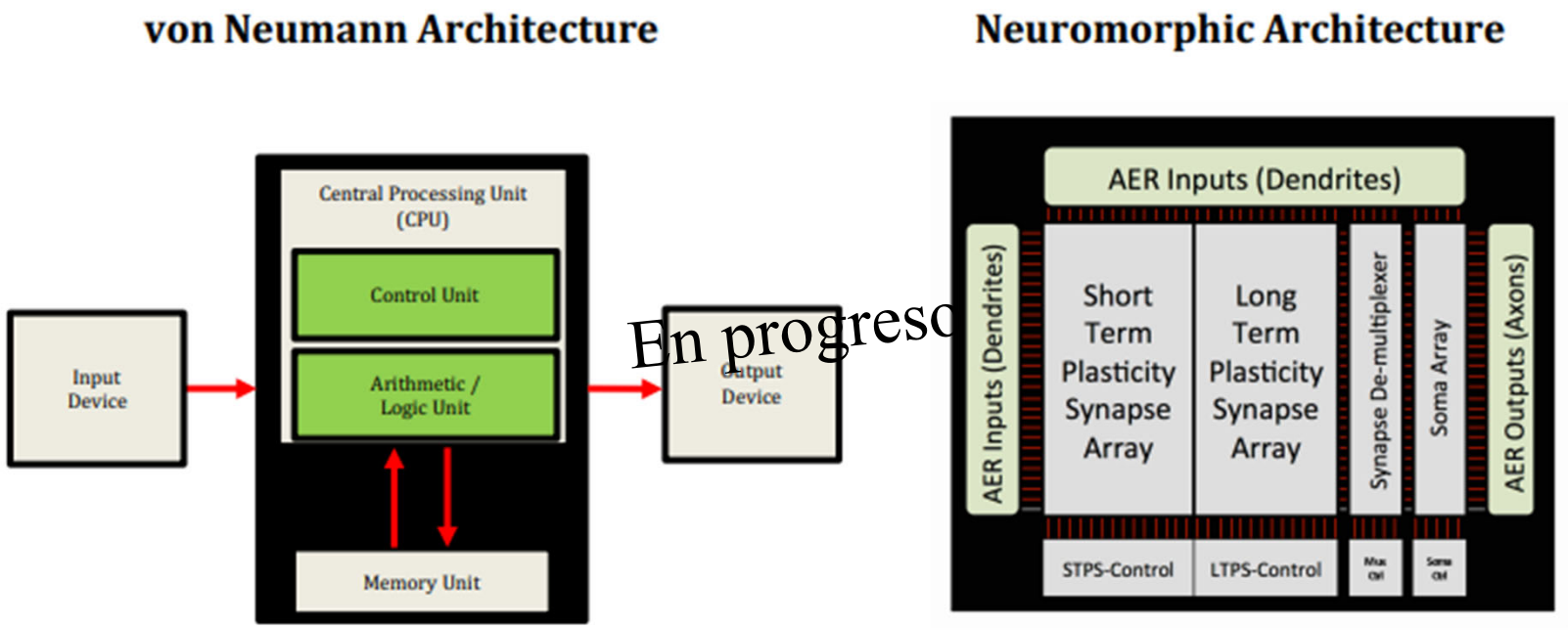
Future - Silicon Photonics

Among the technologies emerging toward creating a fundamentally energy efficient interconnect, photonics is perhaps the most promising to enable a transition to a new generation of scaled extreme

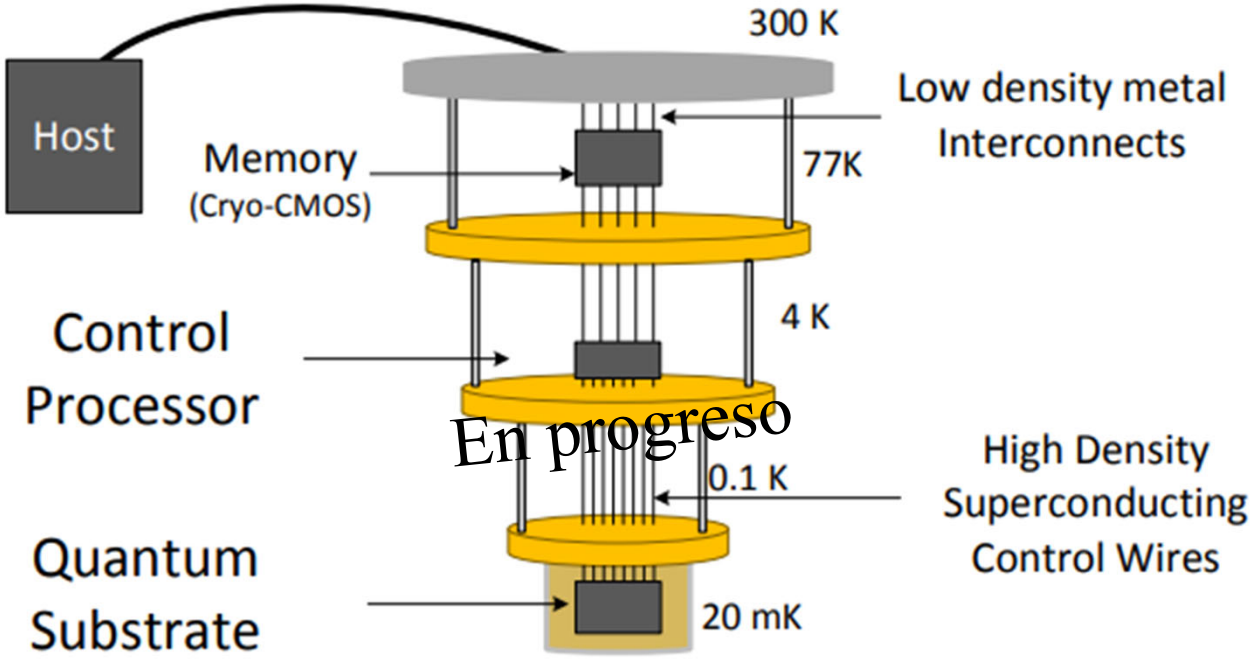
Optical technologies can directly impact the critical communications challenges within computing systems through their remarkable capabilities to generate, transmit, and receive ultra-high bandwidth densities with fundamentally superior power efficiencies and with inherent immunity to noise and degradation.

Pasado, presente y futuro de la supercomputación

Future - Neuromorphic Computing



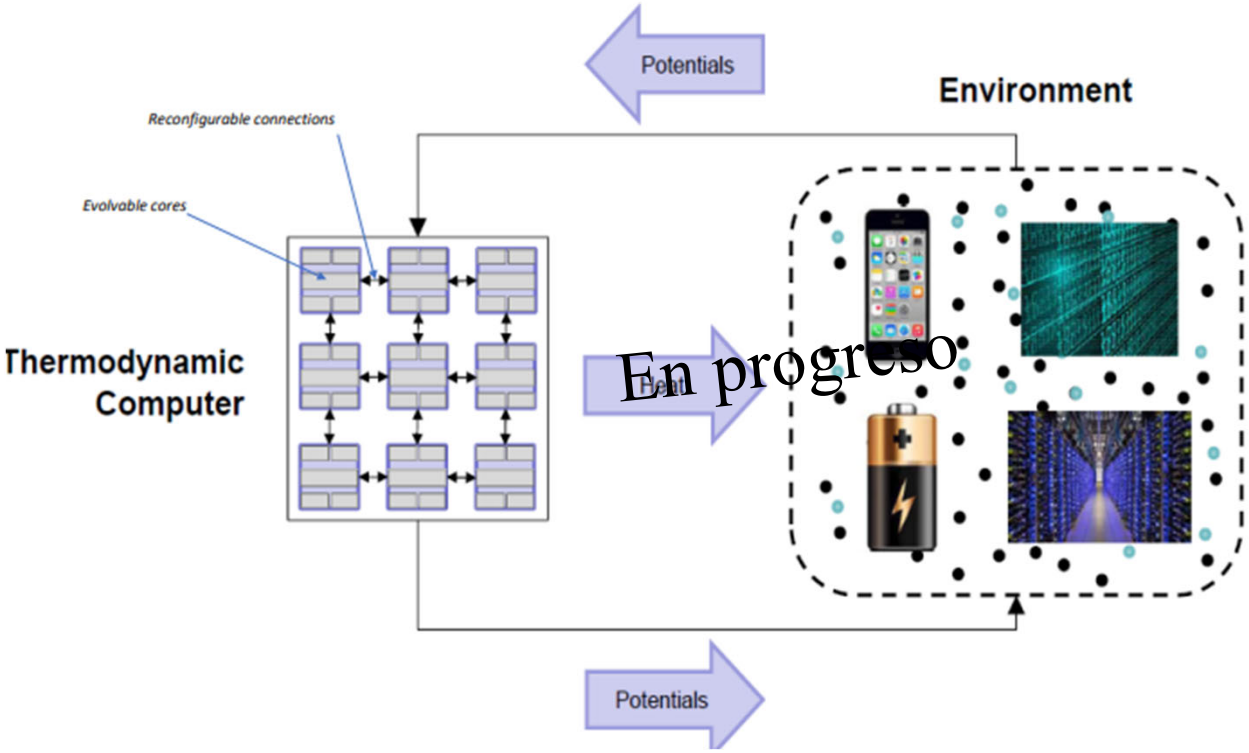
Pasado, presente y futuro de la supercomputación



Whereas N digital bits contain one N-bit state, N entangled quantum bits (qubits) contain 2N states upon which operations can be simultaneously applied.

Quantum computing today is a promising technological direction, but one which will still require significant research and development effort

Pasado, presente y futuro de la supercomputación



Pasado, presente y futuro de la supercomputación

En progreso