Homework 5

Diego Rodrigues

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1 Problem 1

a. **How many 32-bit integers can be stored in a 16-byte cache block?** Each 32-bit integer occupies 4 bytes:

$$\frac{16 \text{ bytes}}{4 \text{ bytes/integer}} = 4 \text{ integers.}$$

b. **References to which variables exhibit temporal locality?** Temporal locality is exhibited by the loop variables `I`, `J` and addresses of `A` and `B` since they are accessed repeatedly in every iteration of the loop. Also `B(I, 0)` is accessed multiple times in the inner loop and therefore exhibits temporal locality, only in the inner loop as `I` changes in the outer loop and breaks temporal locality.

c. **References to which variables exhibit spatial locality?** Spatial locality is exhibited by the variables `A(J, I)` it is accessed contiguously in memory because arrays are stored in row-major order. Notice that `A(J, I)` is accessed in column-major which doesnt exhibit spatial locality in C. And `B(I, 0)` is not accessed contiguously as it is jumping row by row in the outer loop.

d. **How many 16-byte cache blocks are needed to store all 32-bit matrix elements being referenced?** Given that the matrix has 8 rows and 8000 columns, and each element is a 32-bit integer (4 bytes), the total number of cache blocks required is:

$$\frac{8 \times 8000 \times 4 \text{ bytes}}{16 \text{ bytes/block}} = 16000 \text{ blocks.}$$

e. **References to which variables exhibit temporal locality?** Temporal locality is exhibited by the variables `I`, `J` and addresses of `A` and `B`. Also `B(I, 0)` is accessed multiple times in the inner loop and therefore exhibits temporal locality, only in the inner loop as `I` changes in the outer loop and breaks temporal locality.

f. **References to which variables exhibit spatial locality?** This time `A(J, I)` and `B(I, 0)` exhibits spatial locality, as it is accessed contiguously through the outer loop. In this case `A(I, J)` is not accessed contiguously as it will jump in memory because of the column-major order.

2 Problem 2

Binary Address	Tag	Index	Hit/Miss
00000011	0000	0011	miss
10110100	1011	0100	miss
00101011	0010	1011	miss
00000010	0000	0010	miss
10111111	1011	1111	miss
01011000	0101	1000	miss
10111110	1011	1110	miss
00001110	0000	1110	miss
10110101	1011	0101	miss
10110101	1011	0101	miss
00101100	0010	1100	miss
10111010	1011	1010	miss
11111101	1111	1101	miss

Table 1: Cache A: Direct-mapped cache with 16 one-word blocks

a.

Binary Address	Tag	Index	Hit/Miss
00000011	-	0001	miss
10110100	101	1010	miss
00101011	1	0101	miss
00000010	-	0001	hit
10111111	101	1111	miss
01011000	10	1100	miss
10001110	100	0111	miss
00001110	-	0111	miss
00001110	-	0111	hit
10110101	101	1010	hit
00101100	1	0110	miss
10111010	101	1101	miss
11111101	111	1110	miss

Table 2: Cache B: Direct-mapped cache with two-word blocks and a total of 8 blocks

b.

3 Problem 3

a. The cache block size is **4 words**.

b. The cache has **32 entries**.

c. The ratio between total bits required for such a cache implementation over the data storage bits is approximately **1.1796875**.

1. d.

Hex Address	Tag	Index	Offset	Hit/Miss	Replaced Tag
00	00000000000000000000	00000	0000	miss	-
04	00000000000000000000	00000	0100	hit	-
10	00000000000000000000	00000	0000	hit	-
84	00000000000000000000	00100	0100	miss	-
E8	00000000000000000000	00111	1000	miss	-
A0	00000000000000000000	00101	0000	miss	-
400	00000000000000000001	00000	0000	miss	00000000000000000000
1E	00000000000000000000	00000	1110	miss	00000000000000000001
8C	00000000000000000000	00100	1100	hit	-
C1C	00000000000000000011	00000	1100	miss	00000000000000000000
B4	00000000000000000000	00101	0100	hit	-
884	00000000000000000010	00100	0100	miss	00000000000000000000

Table 3: Cache actions for each address reference.

e. The hit ratio for the given cache references is **0.3333** (or **33.33%**).

f.
- <00000, 00000000000000000011>
- <00100, 00000000000000000010>
- <00101, 00000000000000000000>
- <00111, 00000000000000000000>

Question 4 Answers

a.

Word Address	Hit/Miss
2	miss
3	miss
11	miss
16	miss
21	miss
13	miss
64	miss
48	miss
19	miss
11	hit
3	miss
22	miss
4	miss
27	miss
6	miss
11	miss

Final cache contents:

Set Index	Words
0	64, 48
1	-
2	2
3	27, 11
4	4
5	21, 13
6	22, 6
7	-

b.

Word Address	Hit/Miss
2	miss
3	miss
11	miss
16	miss
21	miss
13	miss
64	miss
48	miss
19	miss
11	hit
3	hit
22	miss
4	miss
27	miss
6	miss
11	hit

Final cache contents:

Words
2, 3, 11, 16, 21, 13, 64, 48, 19, 22, 4, 27, 6