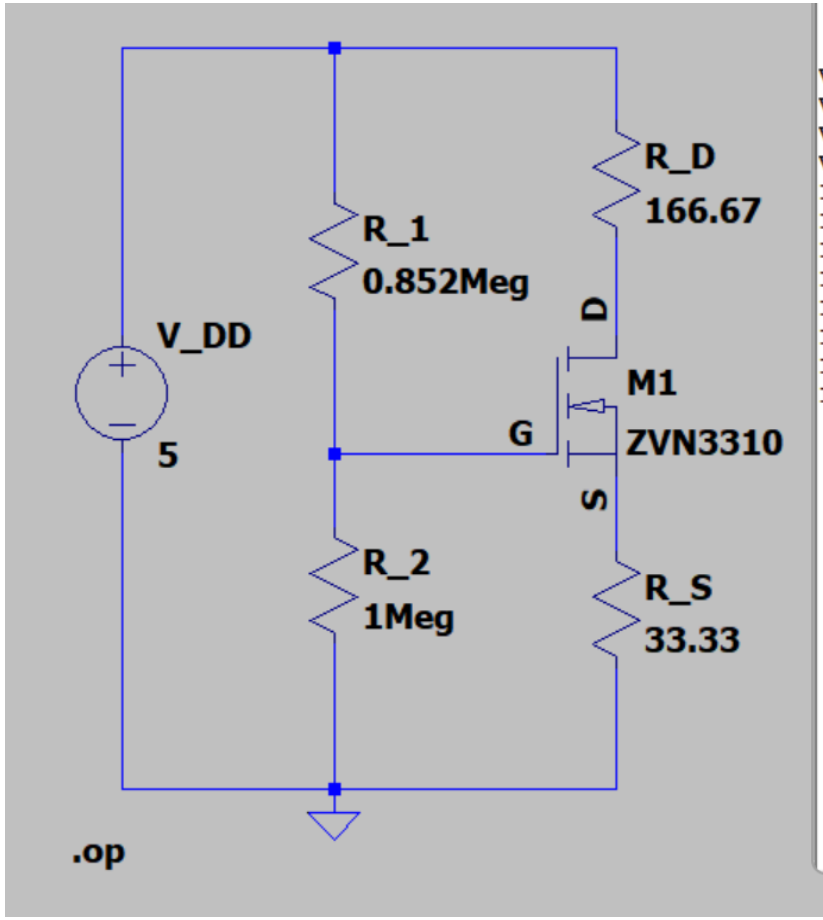
Exercise E12




```
        --- Operating Point ---

V(d):           2.51826         voltage
V(s):           0.496289        voltage
V(g):           2.69978         voltage
V(n001):        5               voltage
I(R_s):         0.0148901       device_current
I(R_d):         0.0148901       device_current
I(R_1):         2.69978e-06     device_current
I(R_2):         2.69978e-06     device_current
I(V_dd):        -0.0148928      device_current
Ix(m1:3):       0.0148901       subckt_current
Ix(m1:4):       0               subckt_current
Ix(m1:5):       -0.0148901      subckt_current
```

Exercise E12

V_S and V_D are mixed up in the initial LTSpice model, so these two values are wrong as well. The errors are left here, serving as a reminder.

LTSpice Simulation Results:

- $V_S = 2.52V; V_D = 0.50V; V_G = 2.70V; V_{DD} = 5.00V$
- $I_D = 14.9mA$, and the current floating through R_S, R_D, Source-to-Drain, are all the exact same. (Probably the LTSpice model is just configured to do this?)
- $I_{R1} = I_{R2} = 2.70\mu A$
- No current between Gate and Drain

- Comments: From the values above (after the orange corrections): $V_{DS} = 2.02V$, $V_{GS} = 2.20V$, $I_D = 14.9mA$. All these values match very well with the givens, especially considering I only kept four sig figs in the resistances in the simulation. (i.e., 33.33Ohms)