IEP-E

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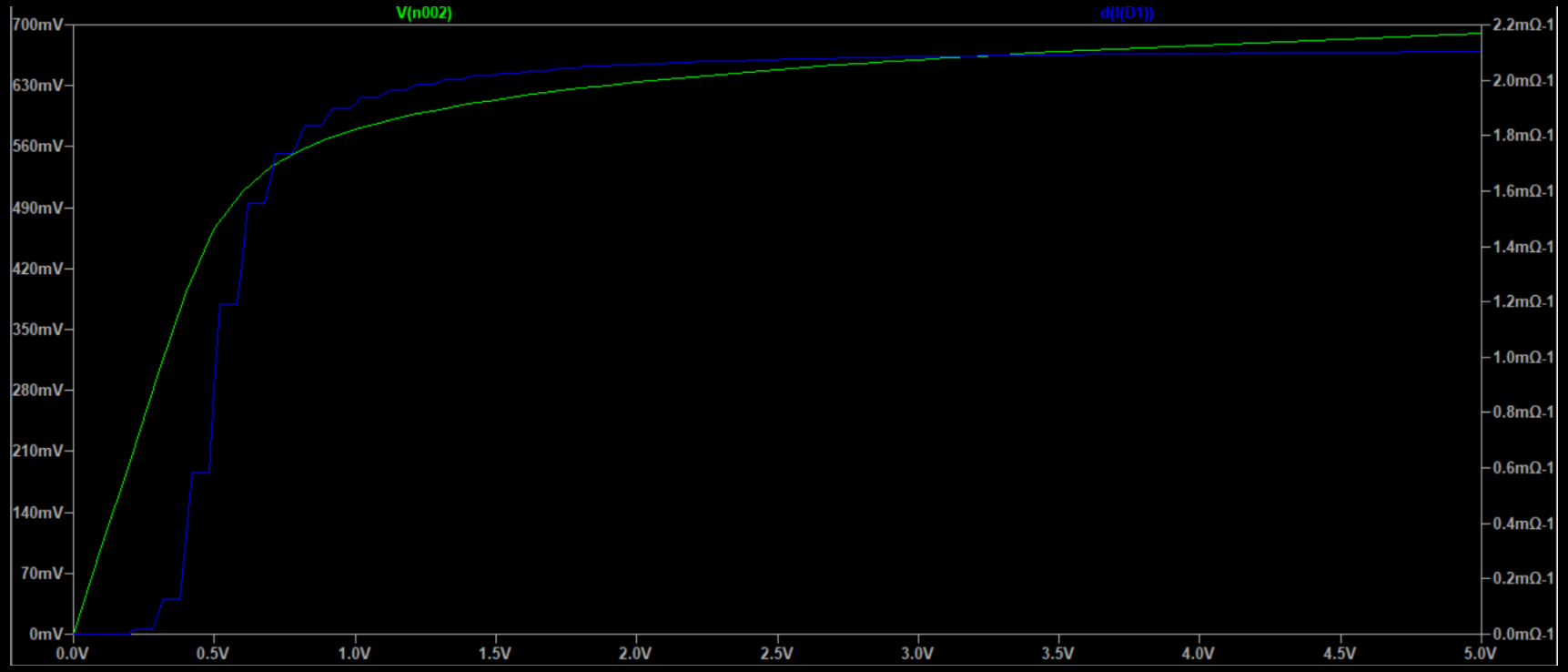
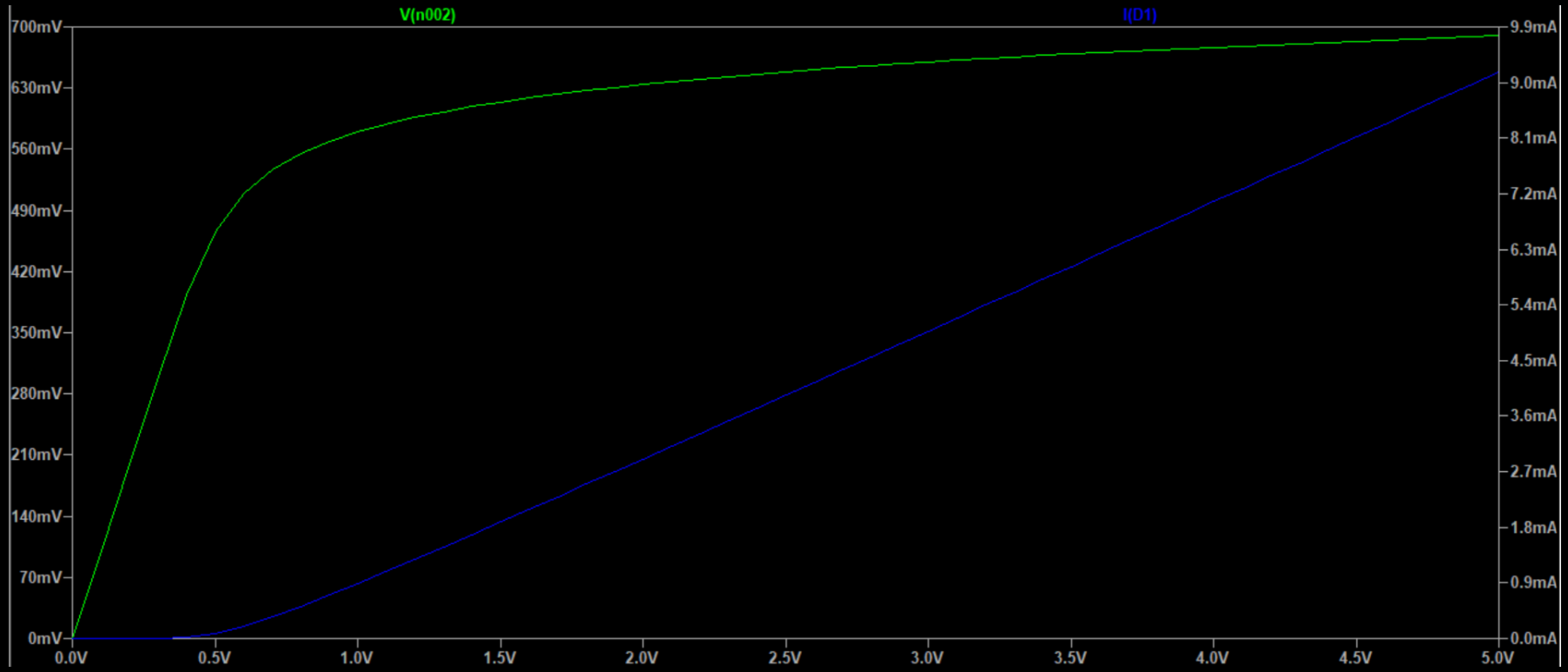
Christmas Vacation, 12/2023-01/2024

Exercise E1



$\frac{1}{R} = 2.1028 m\Omega^{-1}, R = 475.56\Omega$

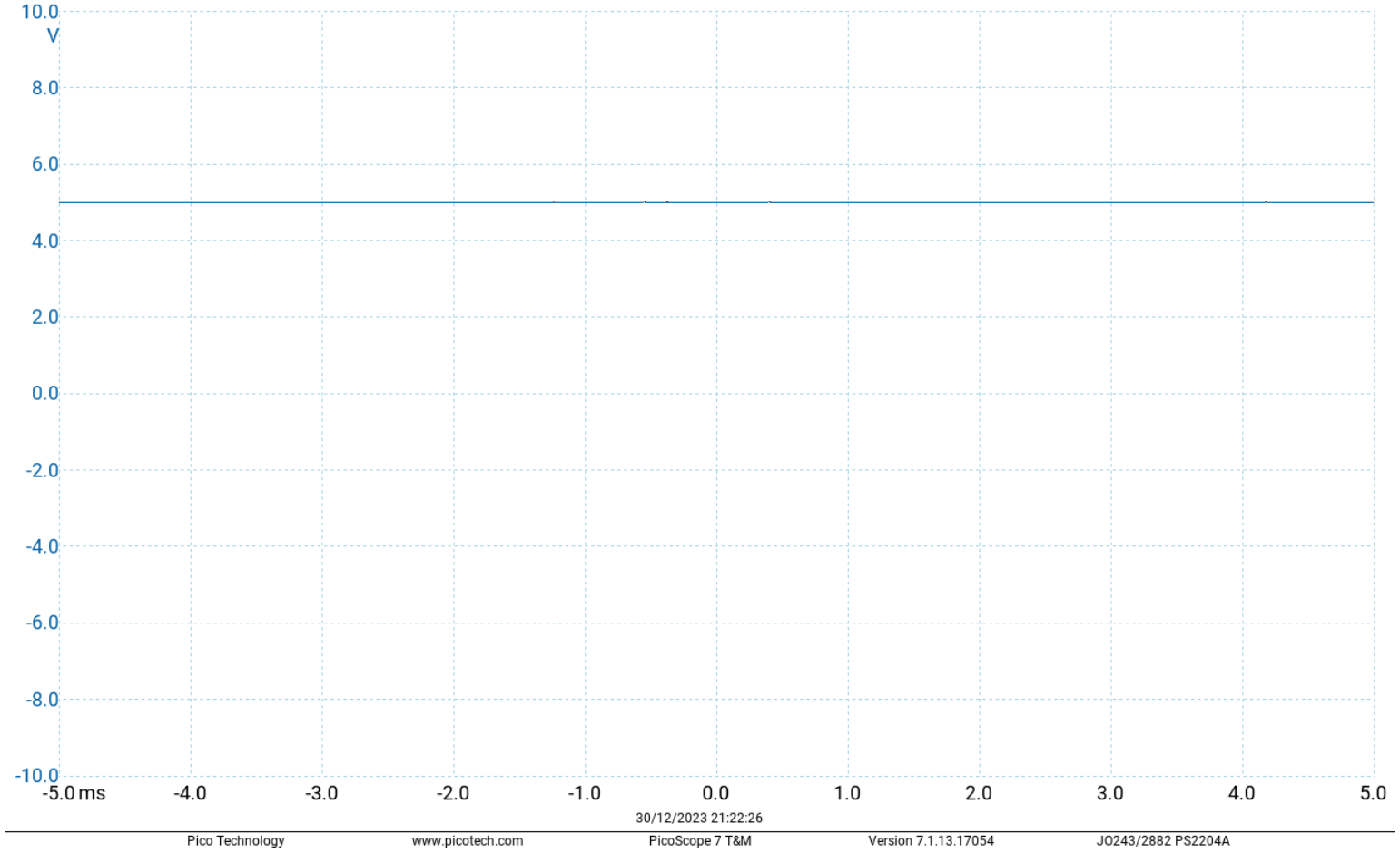
Exercise E1



$I = 9.171mA$ when $V = 5.0V$

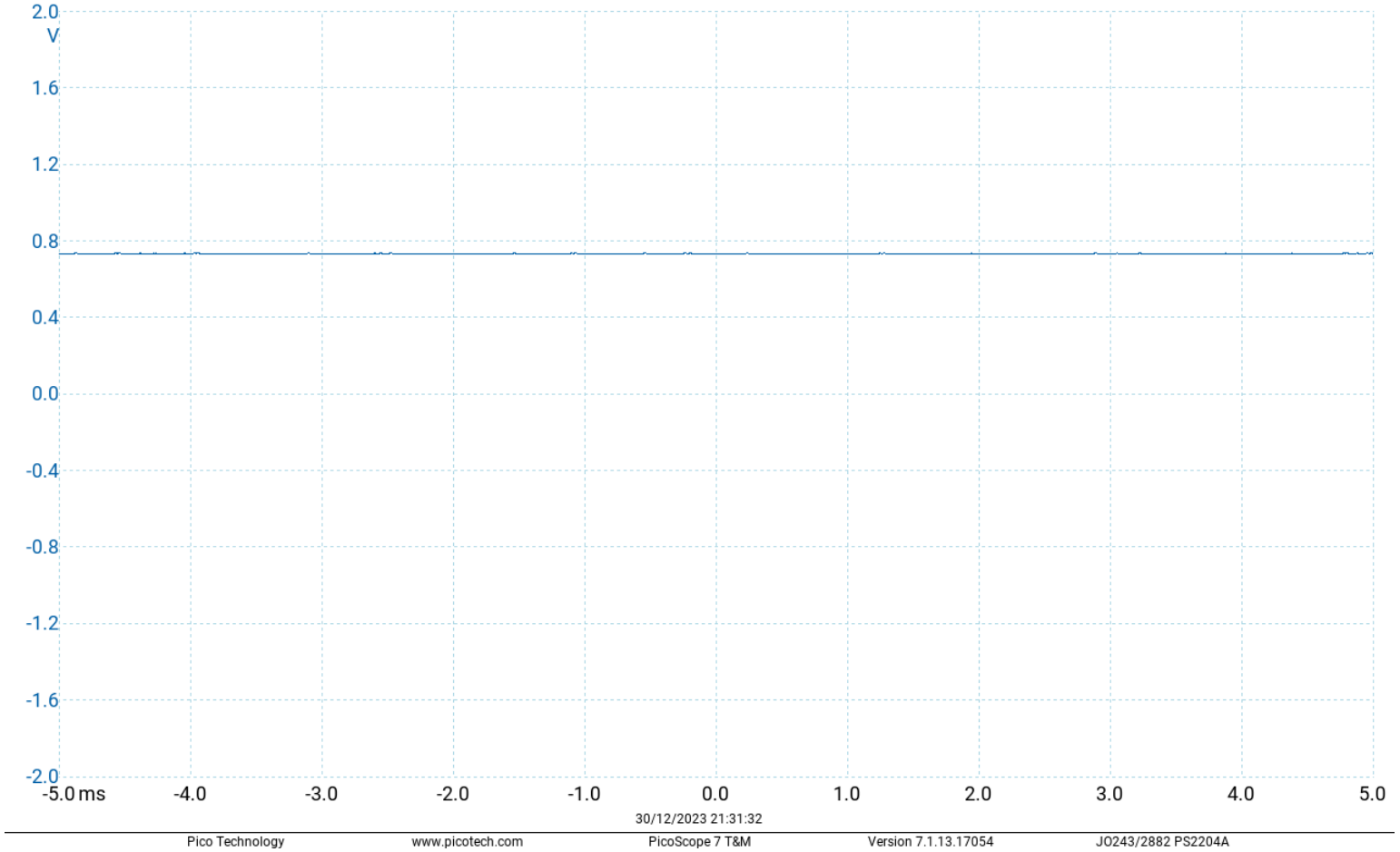
$V_f = V - IR = 0.639V$

Exercise E2



$$V_{USB} = 5.012V$$

Exercise E2

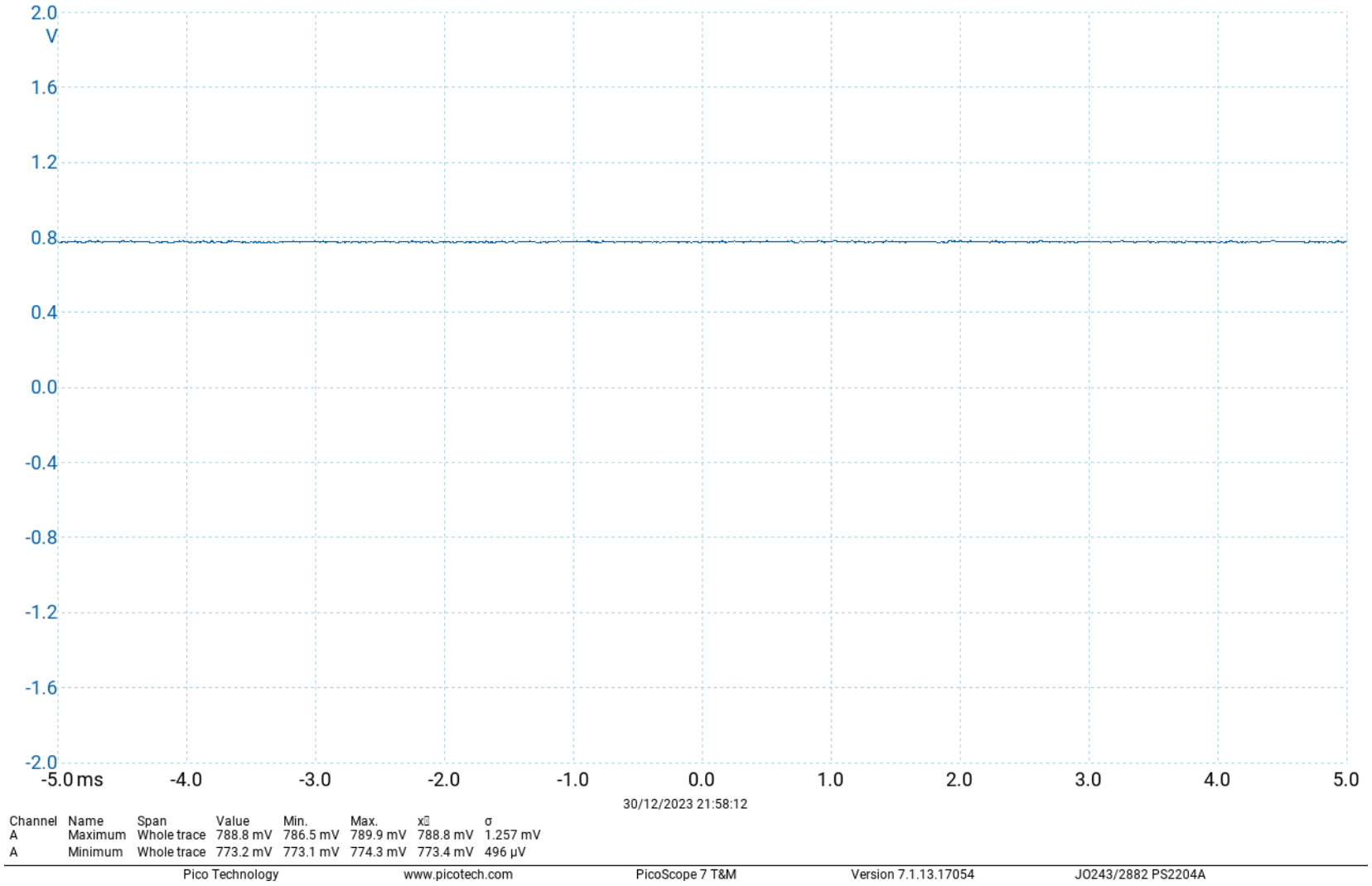


$V_{fd} = 0.729V$ (Note: V_{fd} is forward biased voltage drop across diode)

Exercise E2

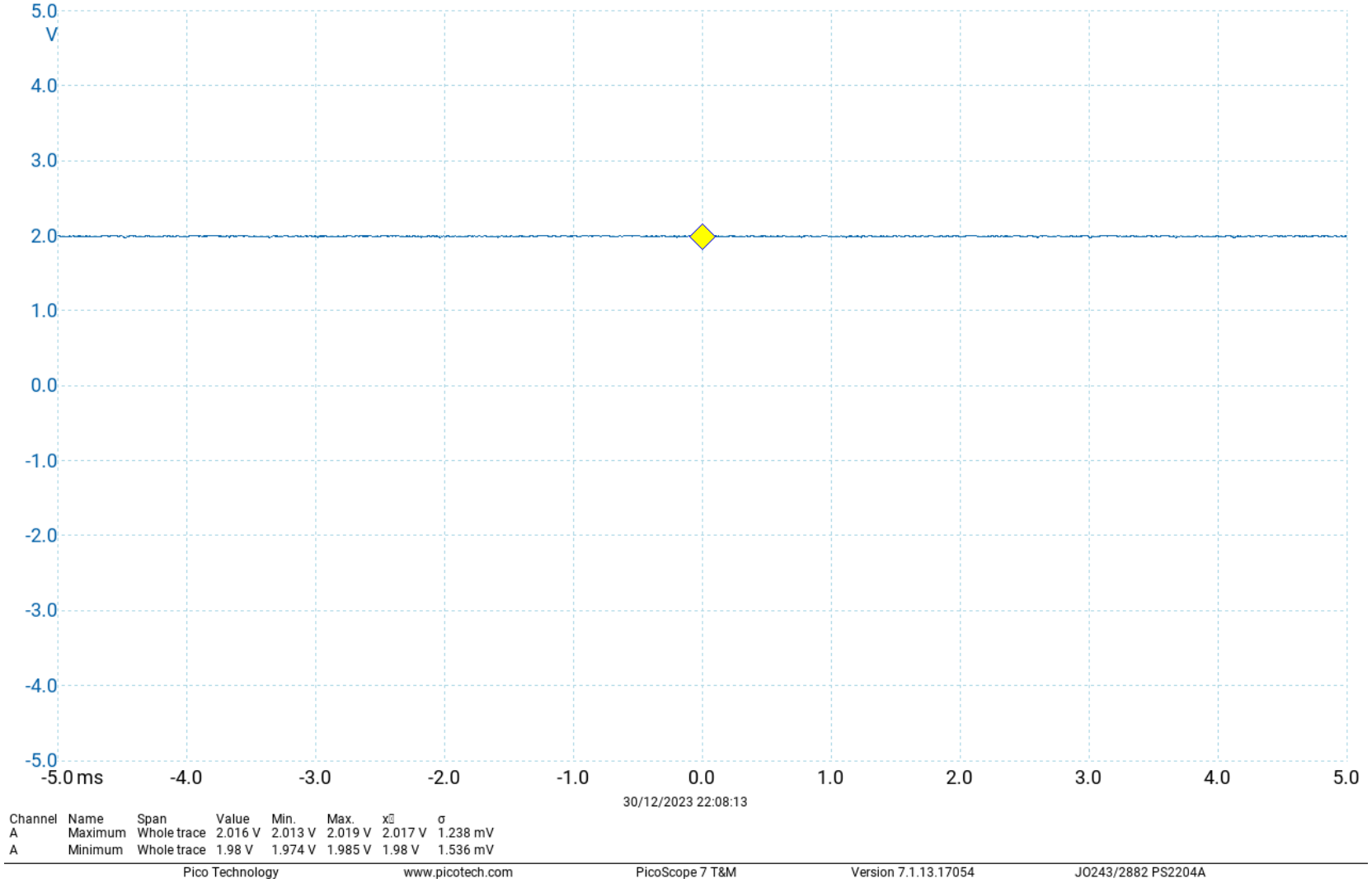
- Experimental values:
  - $V_{fd} = 0.729V$
  - $I = \frac{V_{USB} - V_{fd}}{R_0} = 9.113mA$
- Theoretical values from LTSpice in E1:
  - $I = 9.17mA$
  - $V_{fd} = 0.690V$
- The two results are closely matched.

Exercise E2



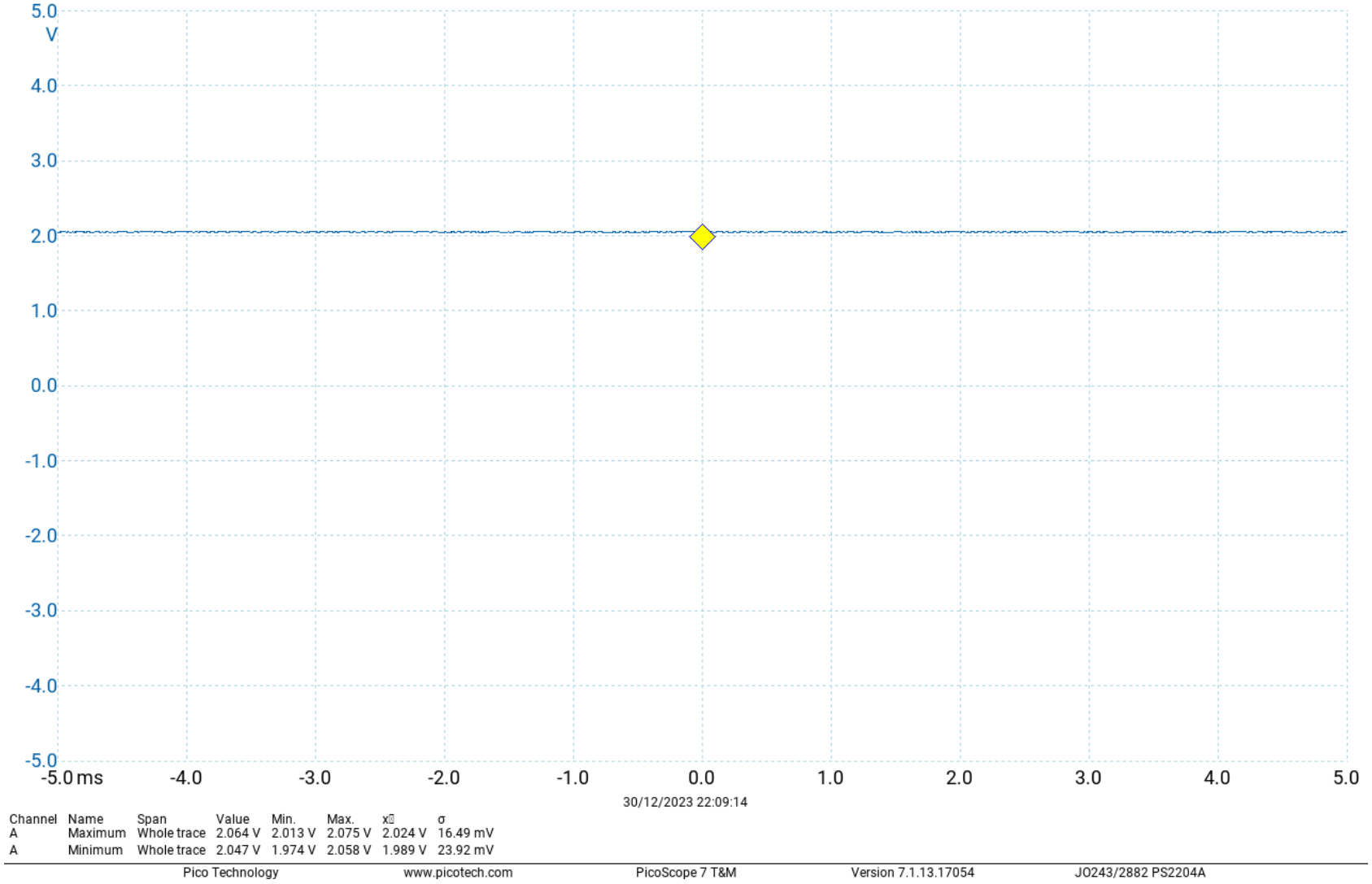
- 1N4001:
- $V_{fd} = 0.700V$

Exercise E2



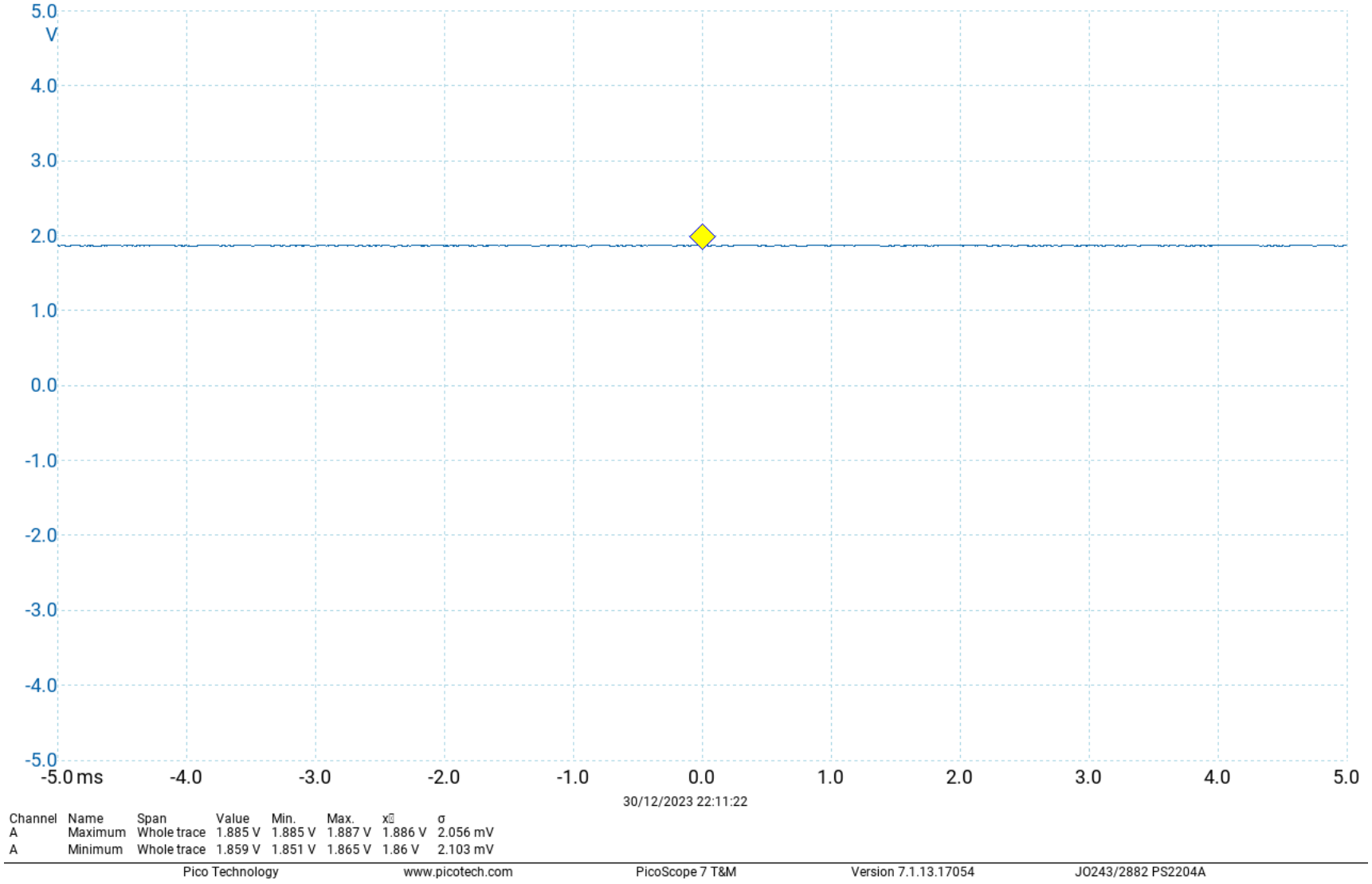
- Yellow LED:
- $V_{fd} = 2.000V$

Exercise E2



- Green LED:
- $V_{fd} = 2.057V$

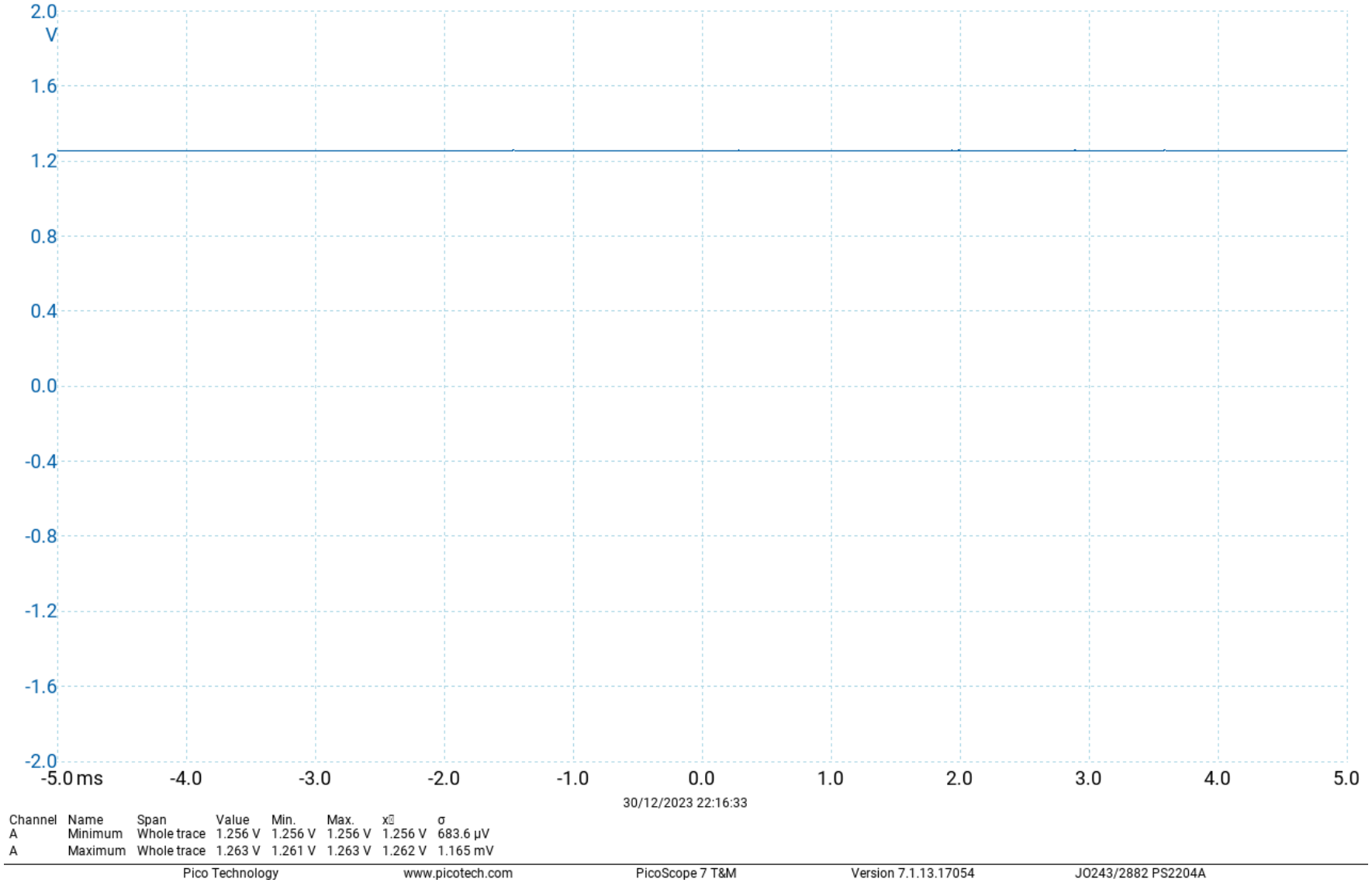
Exercise E2



- Red LED:
- $V_{fd} = 1.875V$

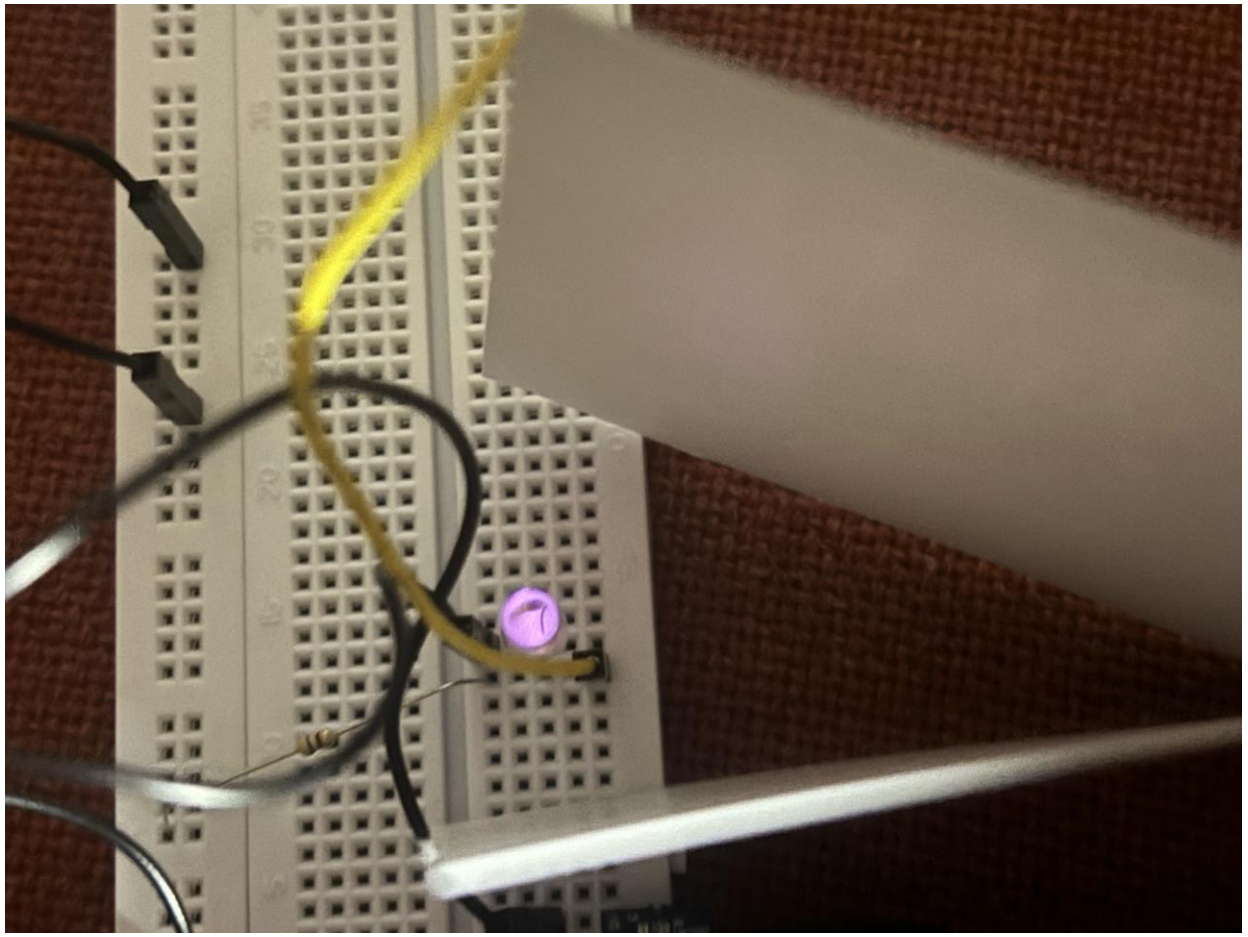
- Presumably the forward voltages are different due to the materials of different diodes being different, especially between the light emitting ones and the none-light-emitting ones.

Exercise E2



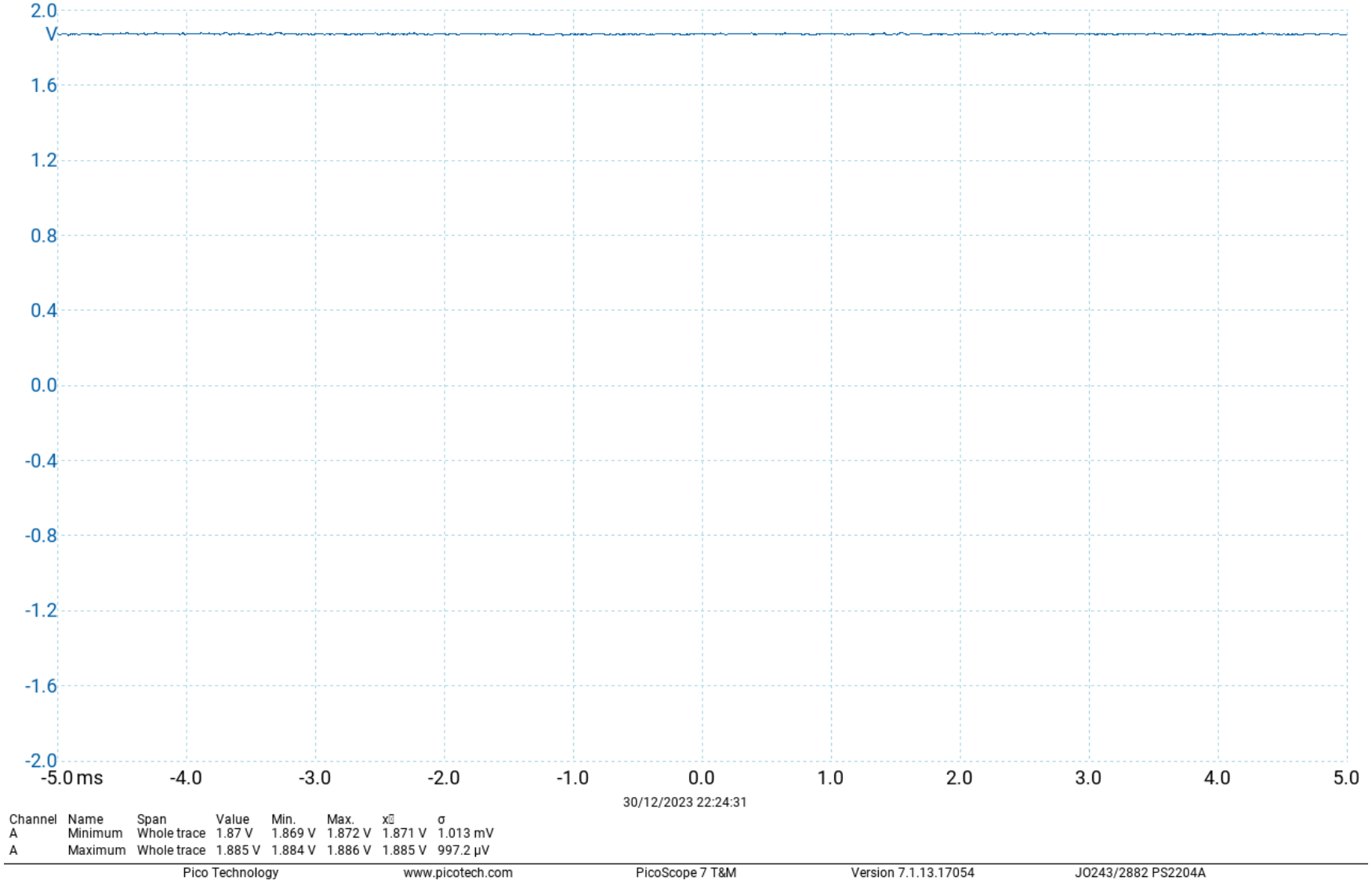
- Infrared Red LED:
- $V_{fd} = 1.260V$

Exercise E2



- Infrared light can be seen with phone cameras
- The photo in the left is taken with most light sources turned off and the only light source blocked by a Christmas card – It seems like removing all light sources will make the photo blurry

Exercise E2

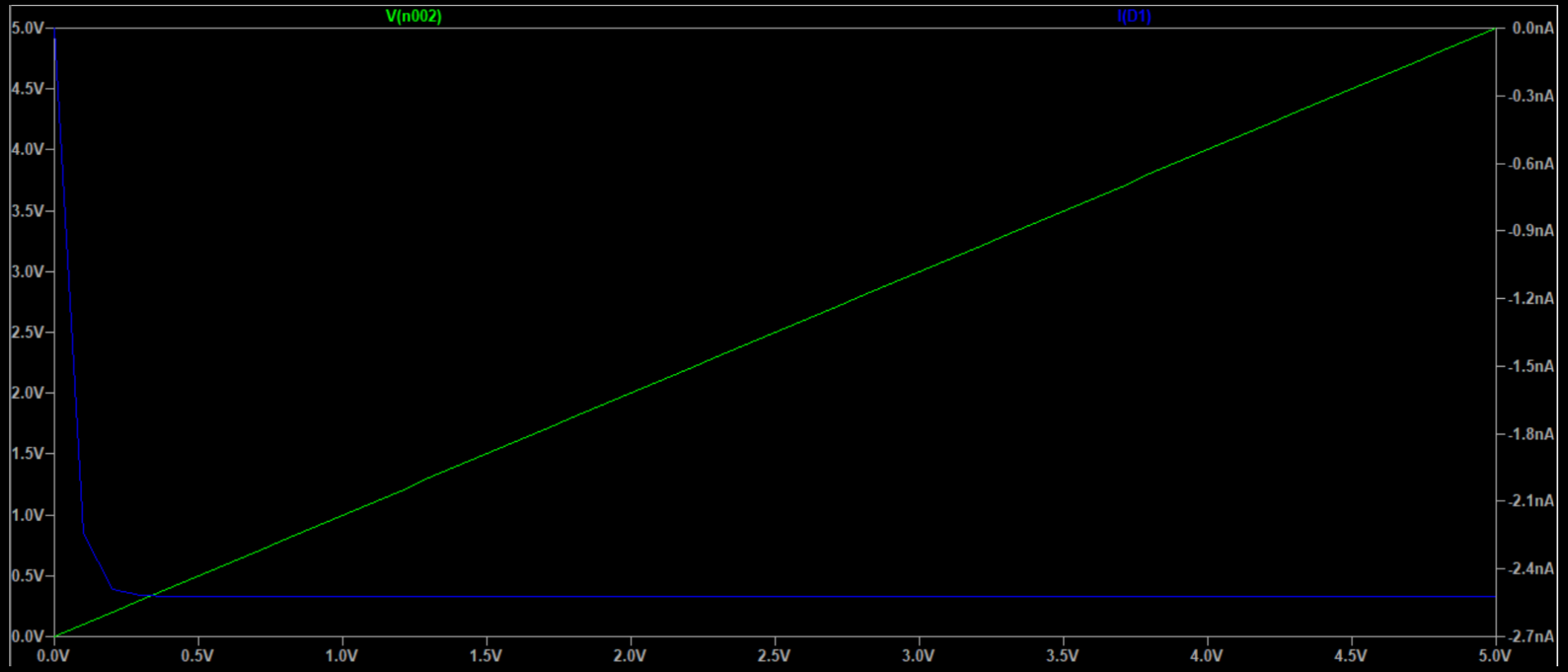


- $V_{fd} = 1.877V$
- $I_{tot} = 6.645mA$
- Both diodes are darker than being alone, which is expected, since the voltages across them decreases from the nearly halved resistance caused by parallel.
- Nothing else seem to change significantly.

Exercise E3

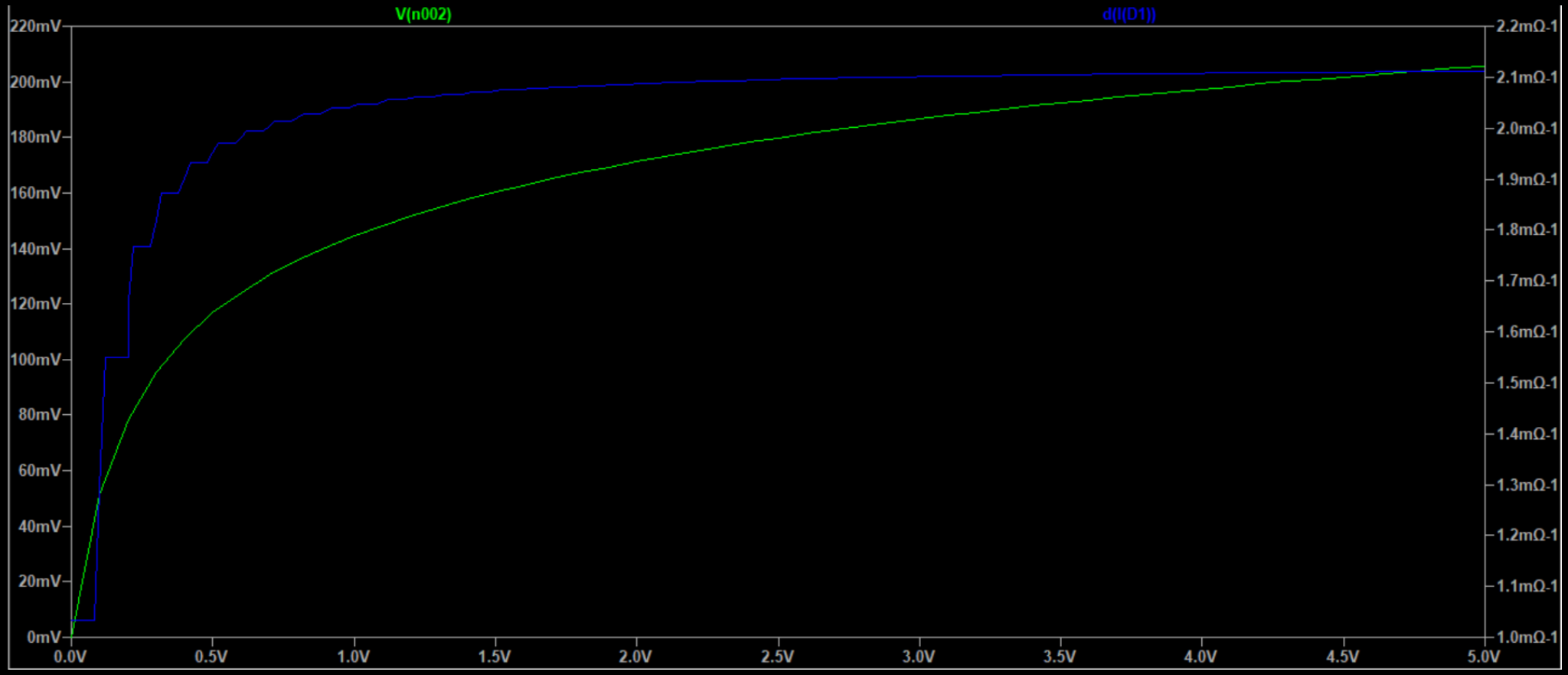
When $V > 0.7V$, $\frac{1}{R} = -1.039p\ \Omega^{-1}$, $R = 9.62 \times 10^{11}\Omega$

Exercise E3



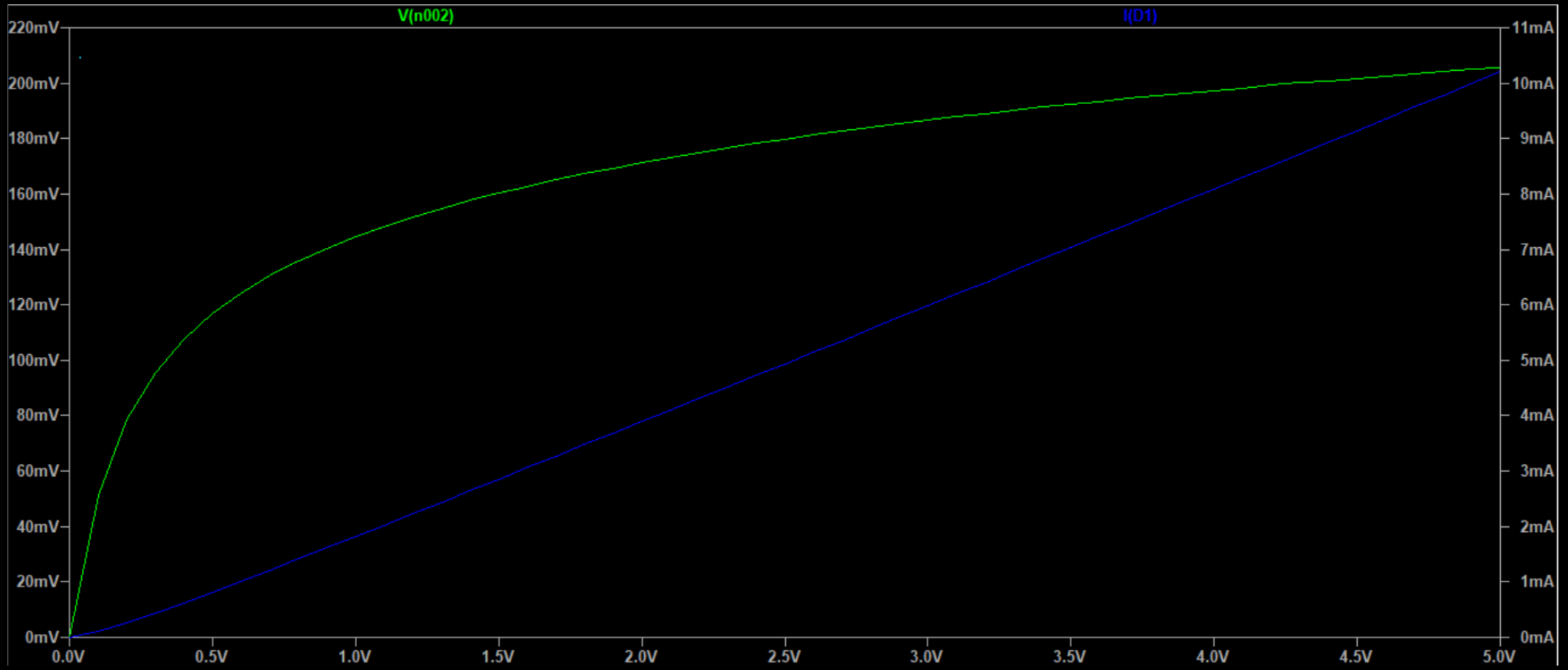
Leakage current: when $V = 5.0V$, $I = -2.525nA$. Negligible.

Exercise E4



For the 1N5817, the main difference lies in that it seems to have a way smaller forward voltage than 1N914.

Exercise E4


V(n002)
I(D1)
220mV
200mV
180mV
160mV
140mV
120mV
100mV
80mV
60mV
40mV
20mV
0mV
11mA
10mA
9mA
8mA
7mA
6mA
5mA
4mA
3mA
2mA
1mA
0mA
0.0V
0.5V
1.0V
1.5V
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V

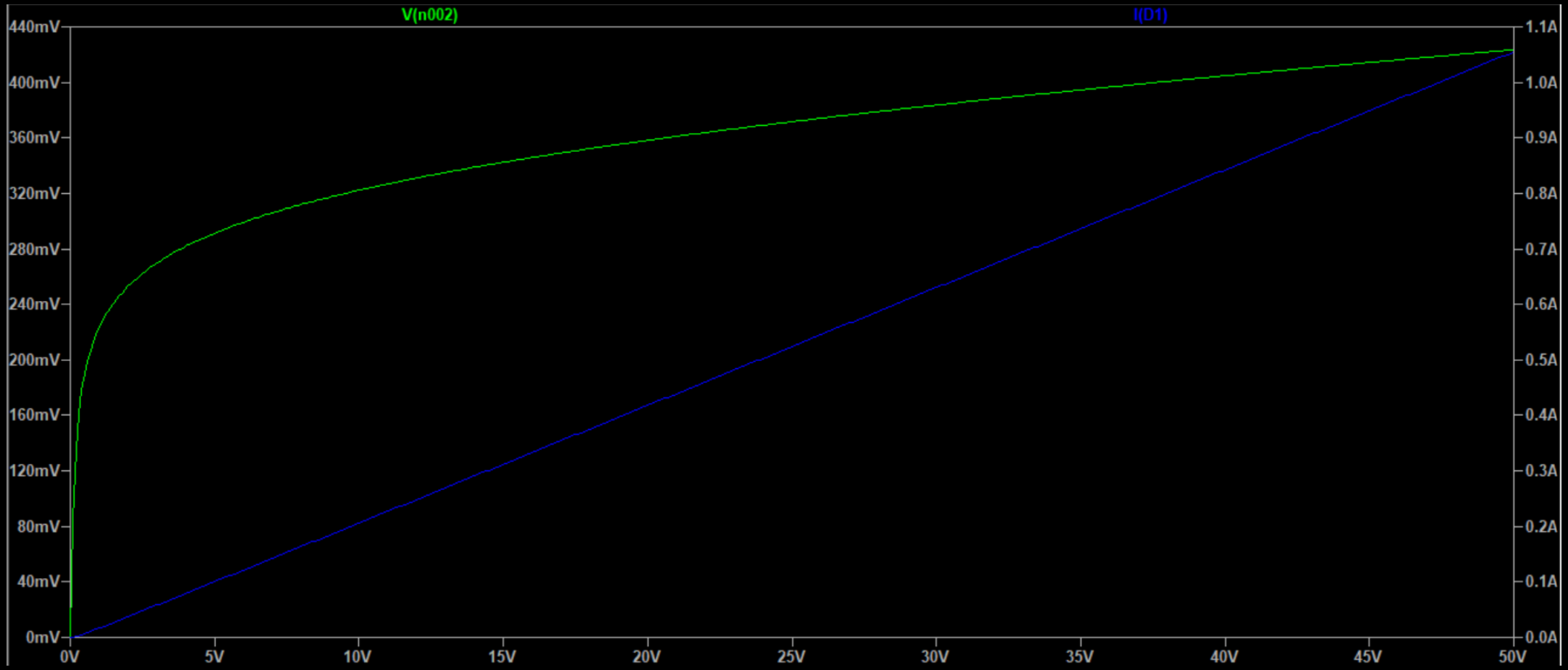
Exercise E4

- https://www.diodes.com/assets/Datasheets/1N5817-1N5819.pdf

Forward Voltage (Note 5)	@ I_F = 1.0A @ I_F = 3.0A	V_{FM}	0.450 0.750

- At 5V, with around 10mA max current, we cannot reproduce the results listed in the specification. However, given that the forward voltage seems to rise with the current, and that it's 0.450V at I=1.0A, our prediction that the forward voltage is very small is correct.
- However if the model is changed to having a 0-50V voltage swipe and a 47 Ohms resistor, we can indeed reach I=1.0A.

Exercise E4


V(n002)
I(D1)
440mV
400mV
360mV
320mV
280mV
240mV
200mV
160mV
120mV
80mV
40mV
0mV
1.1A
1.0A
0.9A
0.8A
0.7A
0.6A
0.5A
0.4A
0.3A
0.2A
0.1A
0.0A
0V
5V
10V
15V
20V
25V
30V
35V
40V
45V
50V

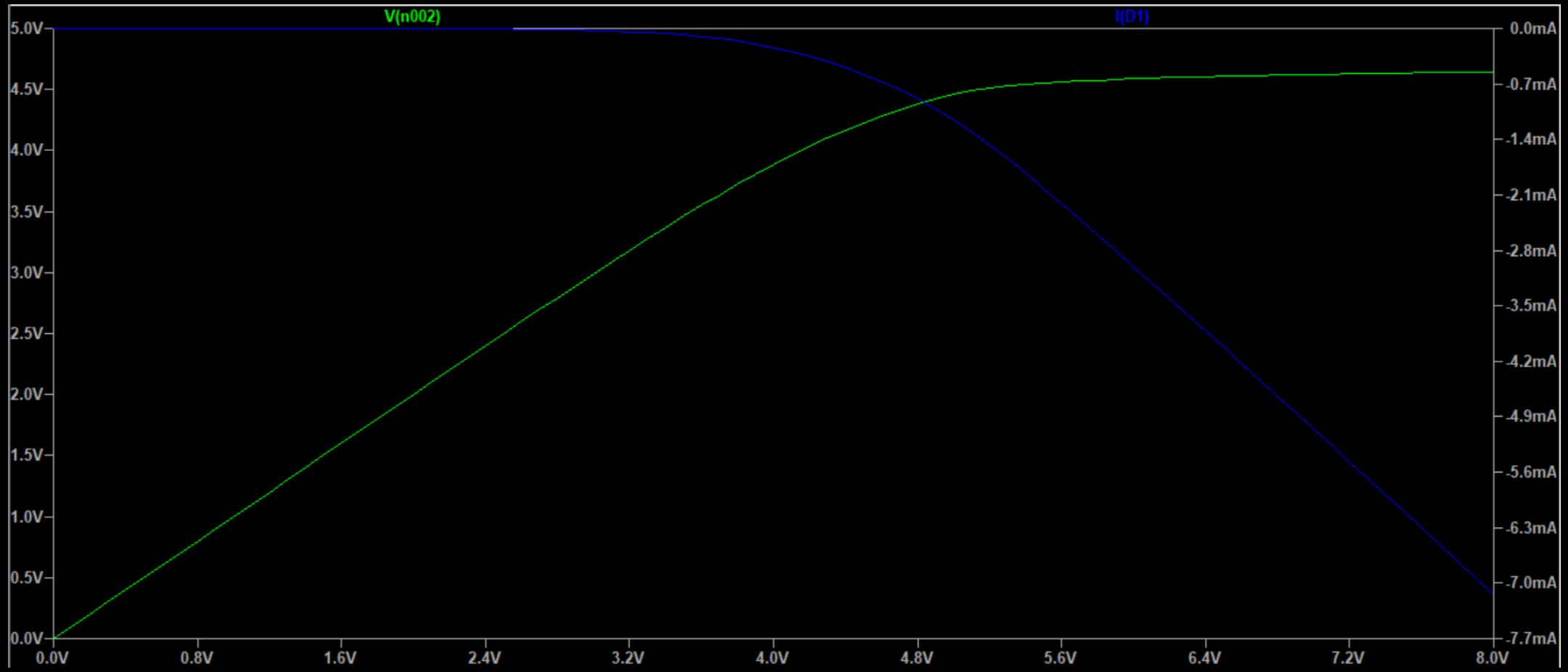
Exercise E4


V(n002)
d(I(D1))
440mV
400mV
360mV
320mV
280mV
240mV
200mV
160mV
120mV
80mV
40mV
0mV
22mΩ-1
20mΩ-1
18mΩ-1
16mΩ-1
14mΩ-1
12mΩ-1
10mΩ-1
8mΩ-1
6mΩ-1
4mΩ-1
2mΩ-1
0V
5V
10V
15V
20V
25V
30V
35V
40V
45V
50V

Exercise E4

- $\frac{1}{R} = 21.237m\Omega$, $R = 47.09\Omega$
- When $I = 0.999A$, $V = 47.36V$
- Thus $V_f = V - IR = 270mV$
- It's quite far from the published values (450mV). I am not sure about the cause of the issue.

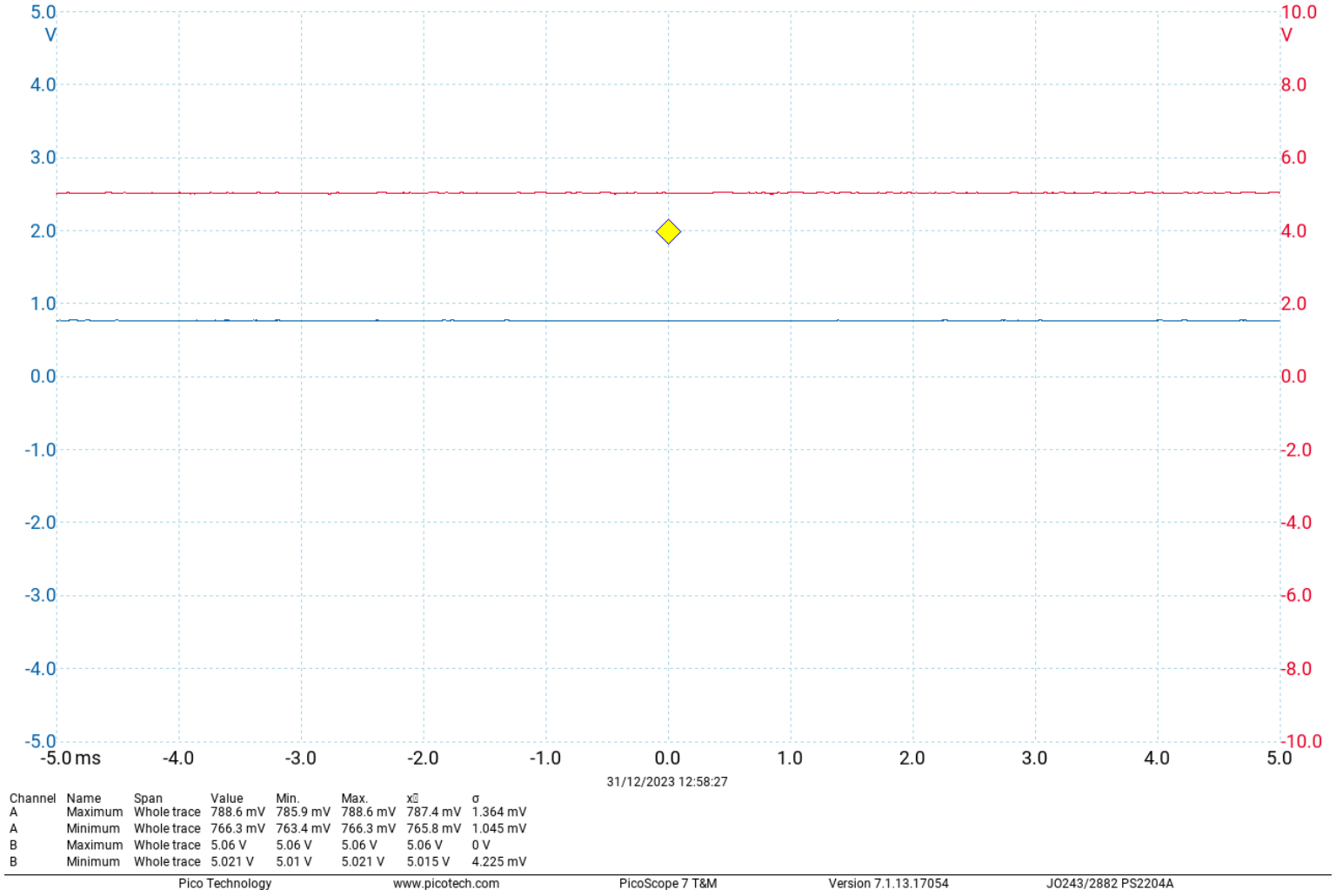
Exercise E5


V(n002)
I(D1)
5.0V
4.5V
4.0V
3.5V
3.0V
2.5V
2.0V
1.5V
1.0V
0.5V
0.0V
0.0mA
-0.7mA
-1.4mA
-2.1mA
-2.8mA
-3.5mA
-4.2mA
-4.9mA
-5.6mA
-6.3mA
-7.0mA
-7.7mA
0.0V
0.8V
1.6V
2.4V
3.2V
4.0V
4.8V
5.6V
6.4V
7.2V
8.0V

Exercise E5

- From the LTSpice graph, the breakdown voltage is approximately 2.264 V.
- The current on the graph is negative, because (presumably) the positive direction for a diode is defined as anode – cathode in LTSpice.
- Real life usages of the Zener diode should include ensuring the minimum voltage of a circuit. By connecting in series the Zener diode with the original circuit, the circuit will only be powered if the voltages are higher than a specific value.

Exercise E6



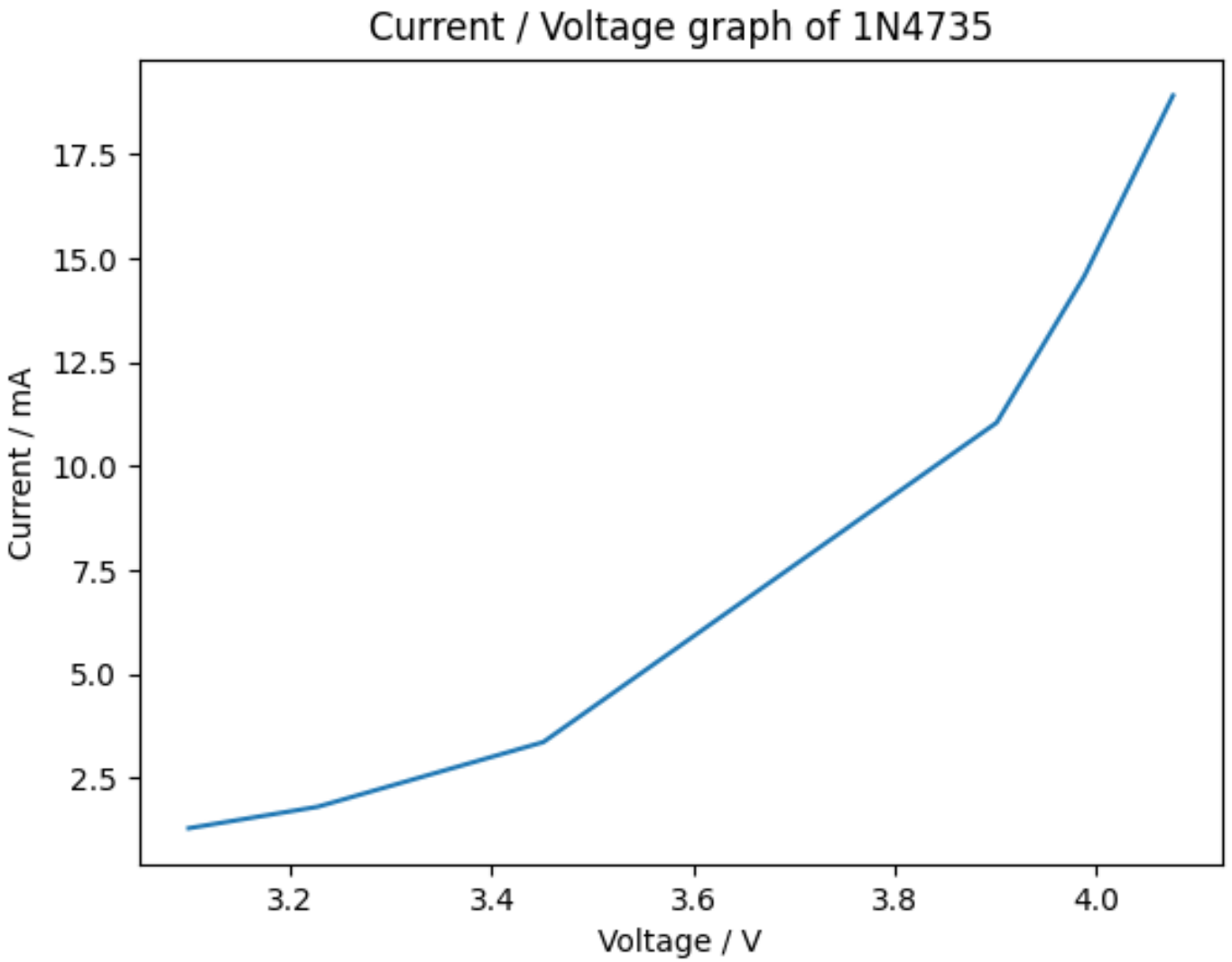
- Datasheets: breakdown voltage is 6.2V

- A: $V_{fd} = 777mV$
- B: $V_{USB} = 5.037V$
- $I = \frac{V_{USB} - V_{fd}}{R_0} = 9.064mA$
- These values are within expectations.

Exercise E6

R_0/Ω	V_{USB}/V	V_{fd}/V	I/mA
1500	5.045	3.099	1.297
1000	5.040	3.227	1.813
470	5.034	3.451	3.368
100	5.006	3.901	11.050
68	4.979	3.988	14.574
47	4.965	4.076	18.915

Exercise E6

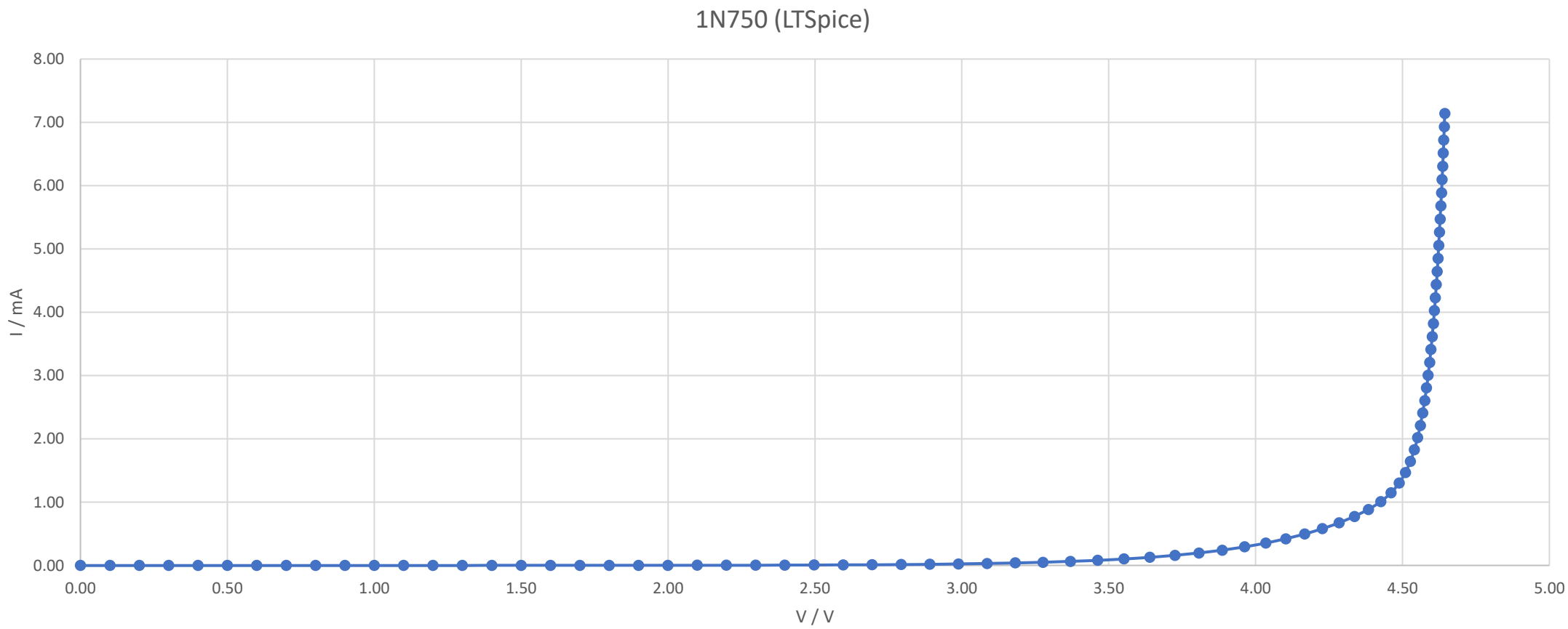

Current / Voltage graph of 1N4735
Current / mA
17.5
15.0
12.5
10.0
7.5
5.0
2.5
3.2
3.4
3.6
3.8
4.0
Voltage / V

Exercise E6

- There doesn't seem to be a way to compare the experimental results with the specifications, which claims that when $I_{ZT} = 41mA$, $V_Z = 6.2V$. (See: https://www.futurlec.com/Diodes/1N4735.shtml)

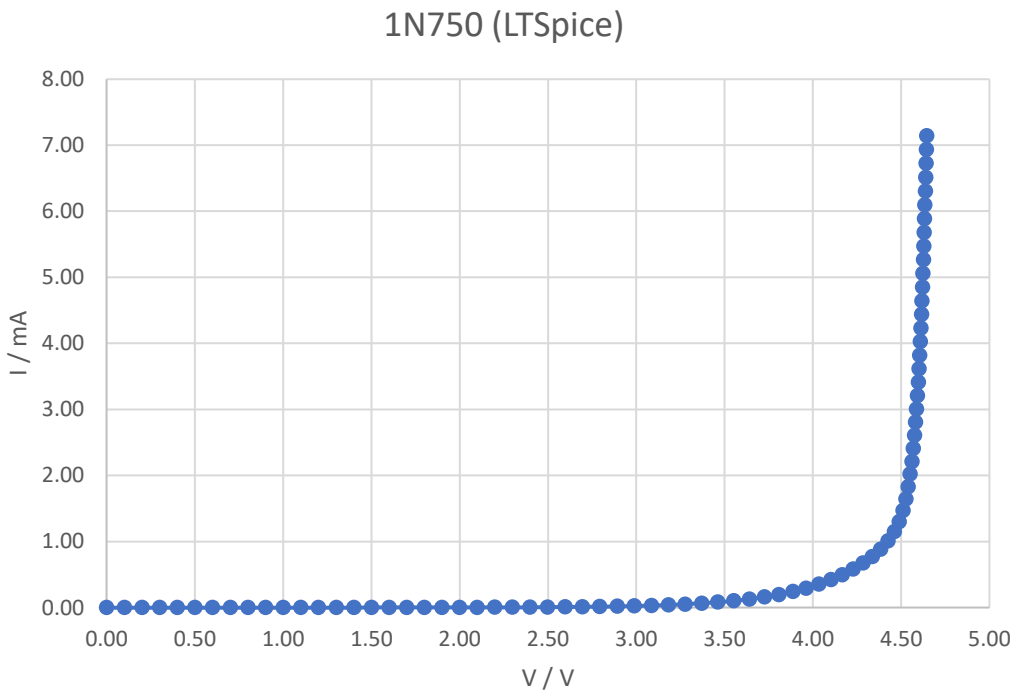
- There are also no models of 1N4735 available in LTSpice. Comparations with the 1N750 model cannot be directly made, but the simulation of 1N750 in LTSpice can be plotted as follows:

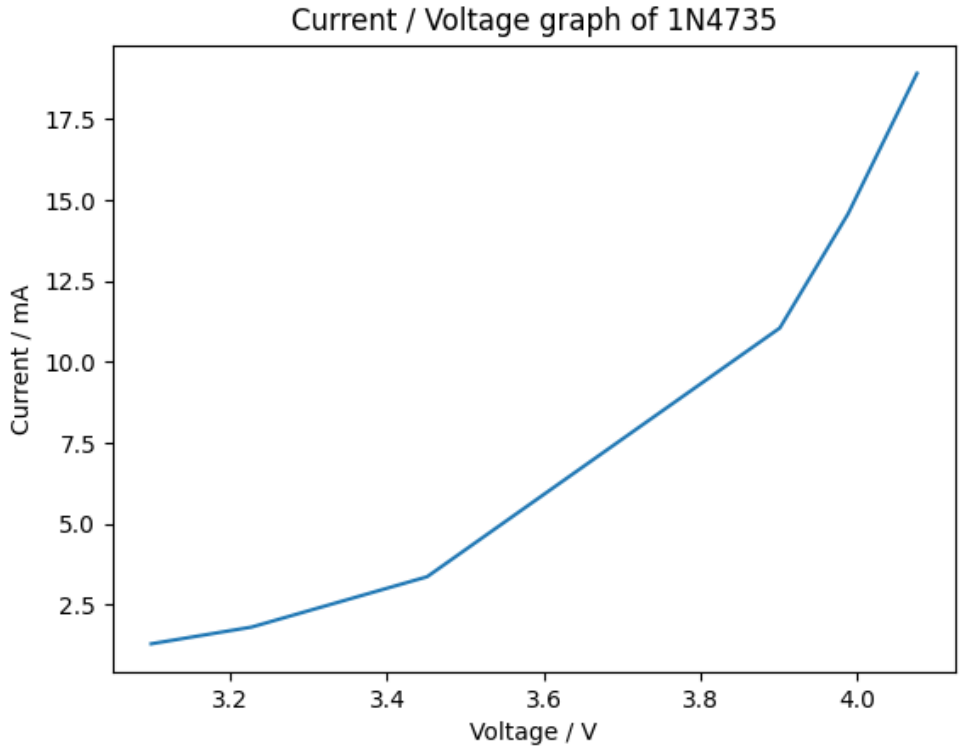
Exercise E6


1N750 (LTSpice)
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
I / mA
0.00
0.50
1.00
1.50
2.00
2.50
3.00
3.50
4.00
4.50
5.00
V / V

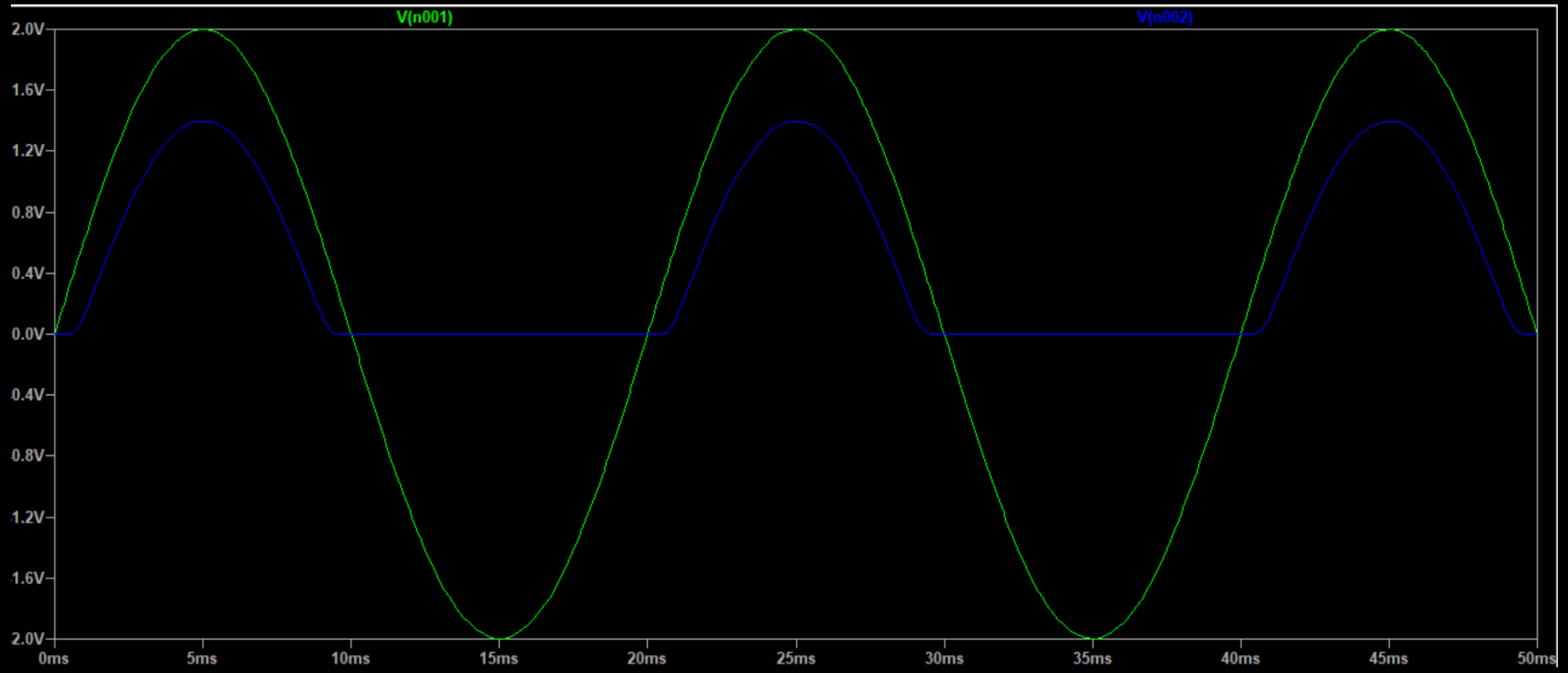
Exercise E6

- Although not very obvious, we may notice a similar trend of increasing slope in both plots.





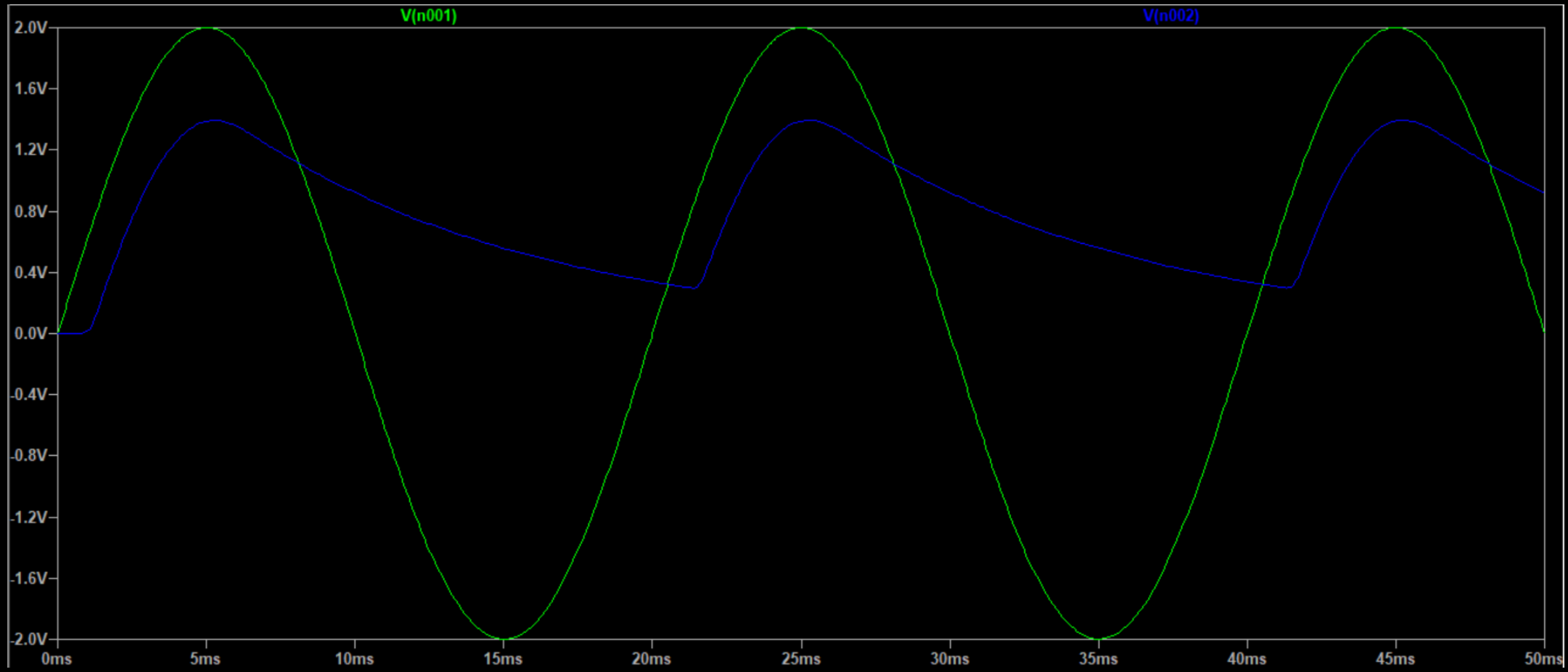
Exercise E7


V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
0.4V
0.8V
1.2V
1.6V
2.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms

Exercise E7

- From the graph above:
  - Width of Pulse: 9.756 – 0.384 = 9.372ms
  - Peak Voltage: 1.398V
- The peak voltage and width are both a bit less than what I expected – I didn’t expect such a voltage decrease since the resistance of the diode is quite low compared with the 1kΩ resistor – but they are within reasonable range.

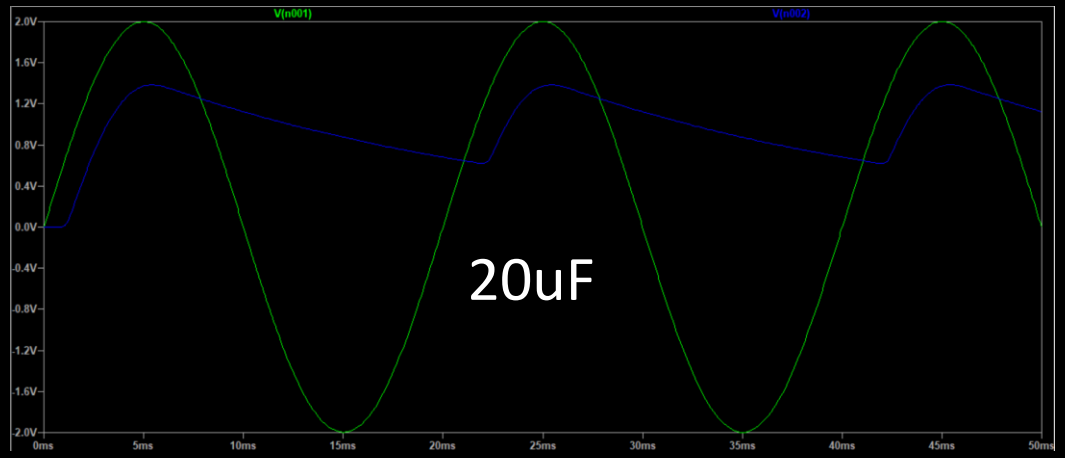
Exercise E8

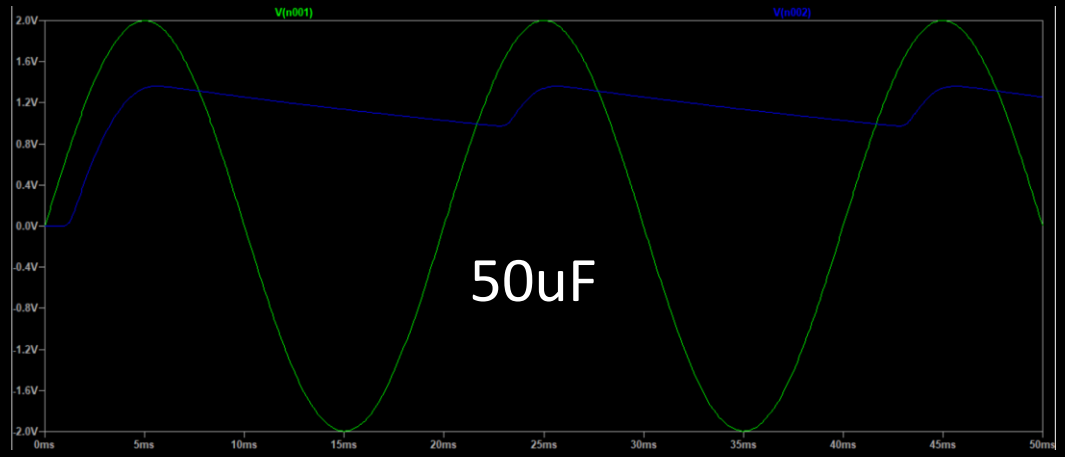

V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms

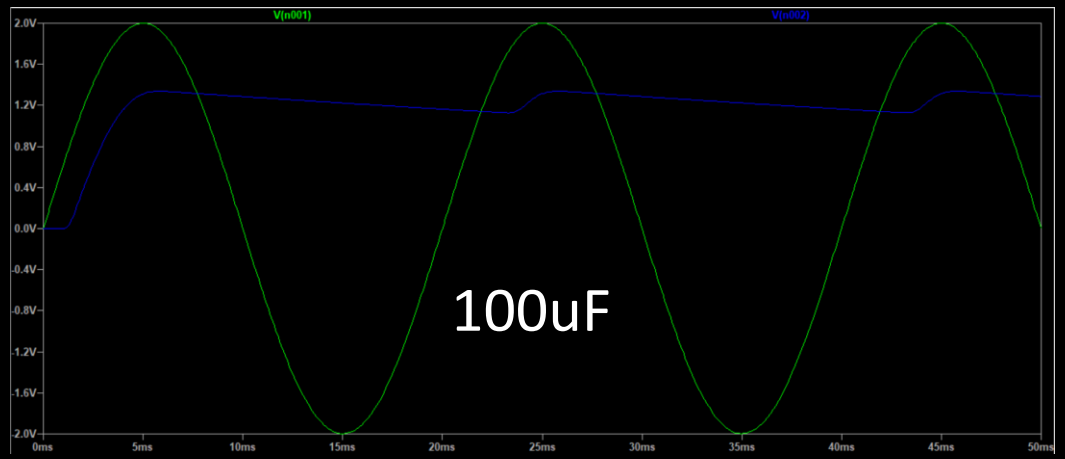
Exercise E8

- As can be seen in the image above, the capacitor slows down the voltage decrease across the parallel resistor&capacitor (and make it a shape similar to a e^x curve). This also results in the minimum voltage being 297mV instead of 0 after the initial charging.

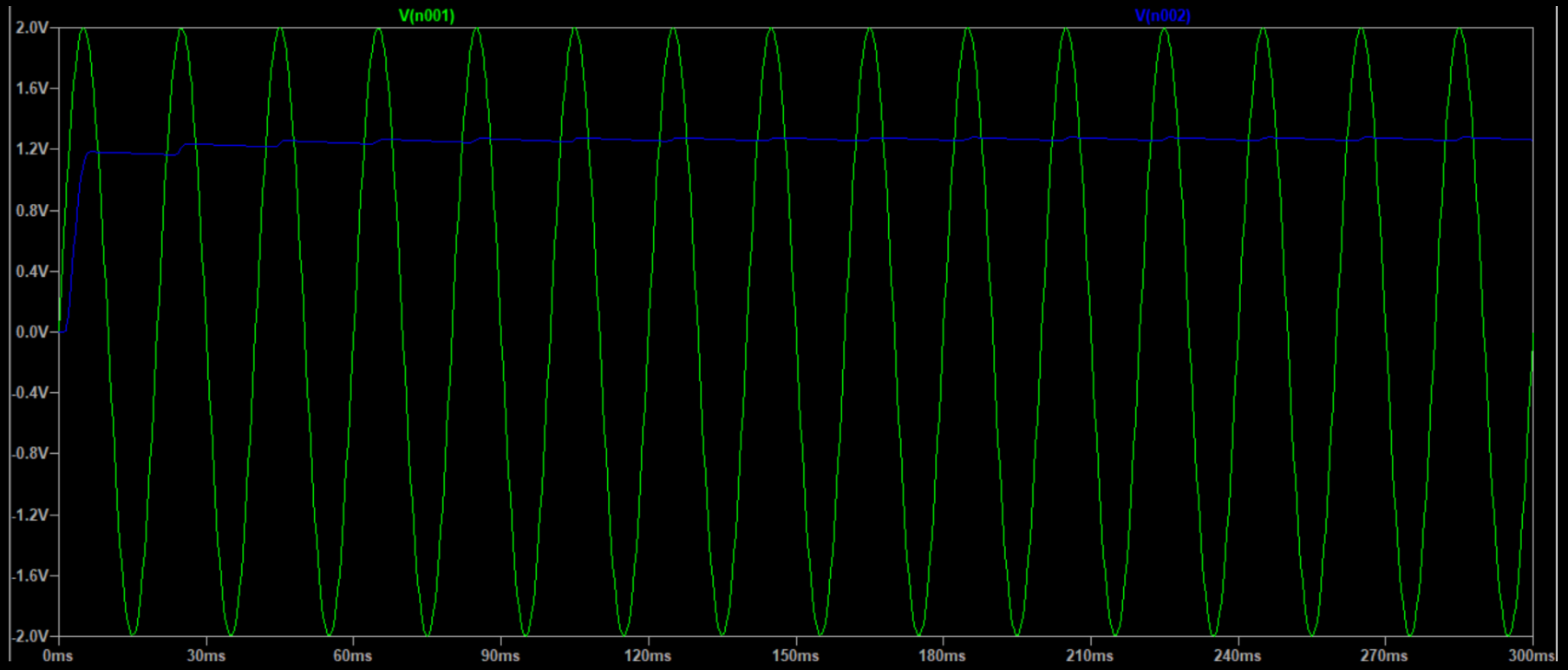
Exercise E8


V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
20uF


V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
50uF


V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
50ms
100uF

Exercise E8



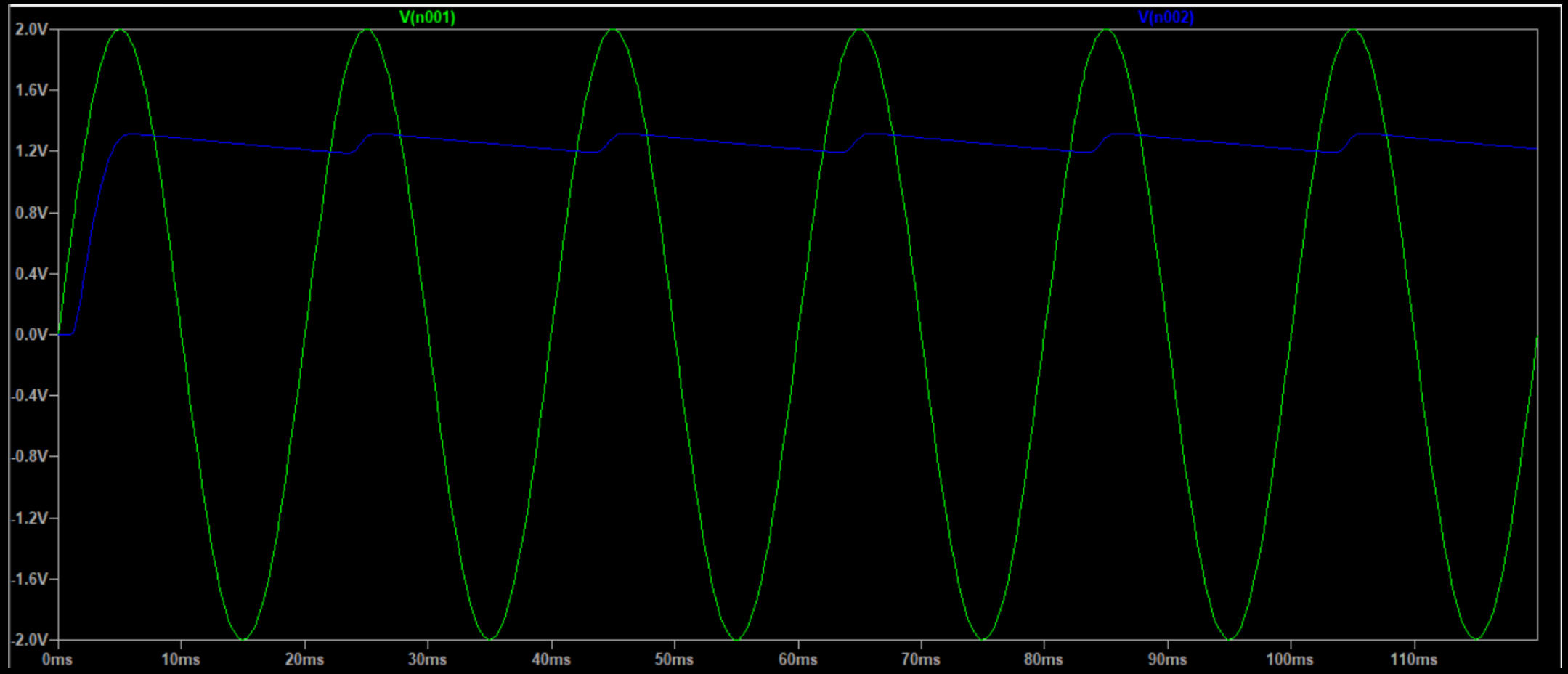
When C = 1mF, the “delay” of increase of voltage caused by the capacitor becomes so significant that it takes several times for the voltage to reach its peak. Due to the capacitor also countering voltage decrease, the voltage changes are nearly negligible.

Exercise E8

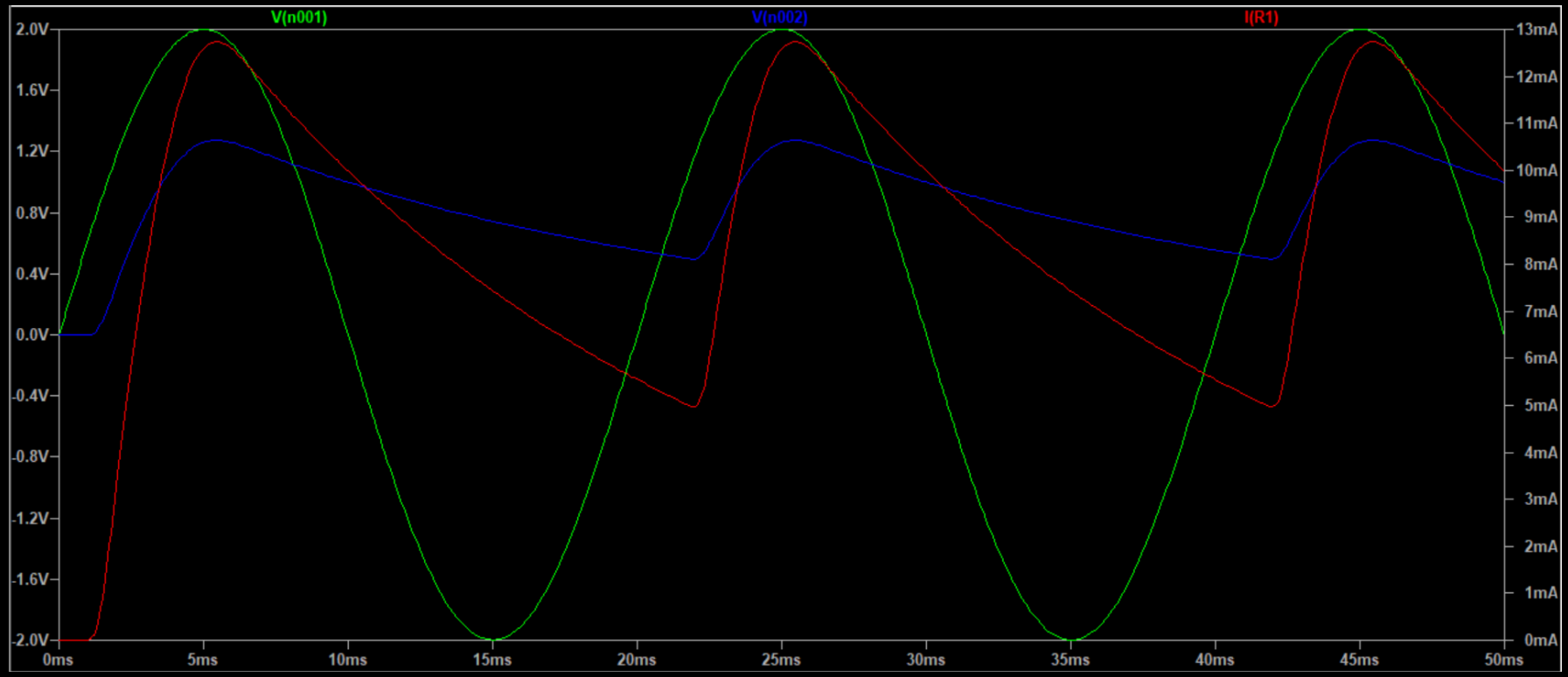
- From the previous images, we can see that between 50-100 uF * is a decent range where the AC ripple should be around 1/10 of their DC offset.
- [*] Data manipulation using an Excel spreadsheet shows that it should be 100uF-500uF. Mistake caused by intuition.
- The final result would be around 170uF.

500u	3.45%
300u	5.73%
200u	8.58%
170u	10.08%
160u	10.71%
150u	11.41%
100u	16.94%
50u	33.15%

Exercise E8


V(n001)
V(n002)
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
-0.4V
-0.8V
-1.2V
-1.6V
-2.0V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
90ms
100ms
110ms

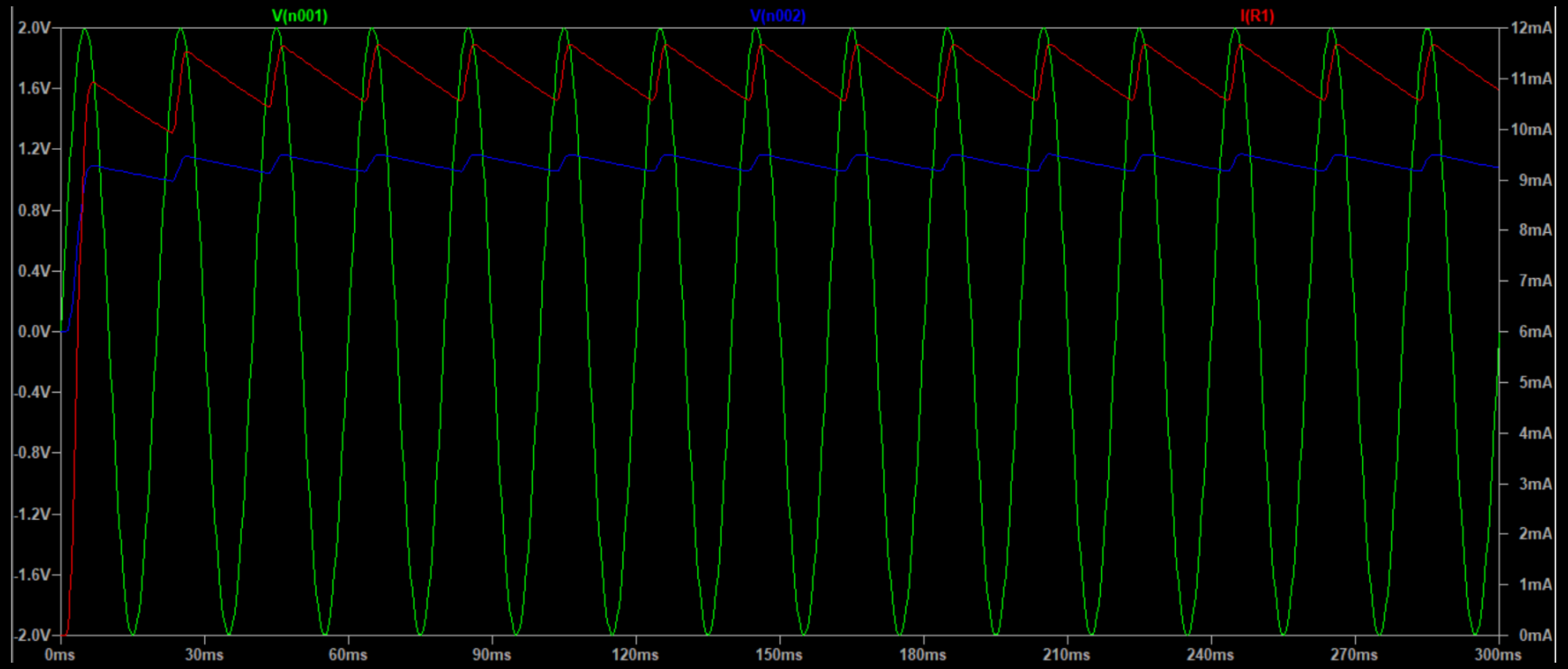
Exercise E8



(When R=100Ω)

Exercise E8

Note: The red plot here is current through the resistor.



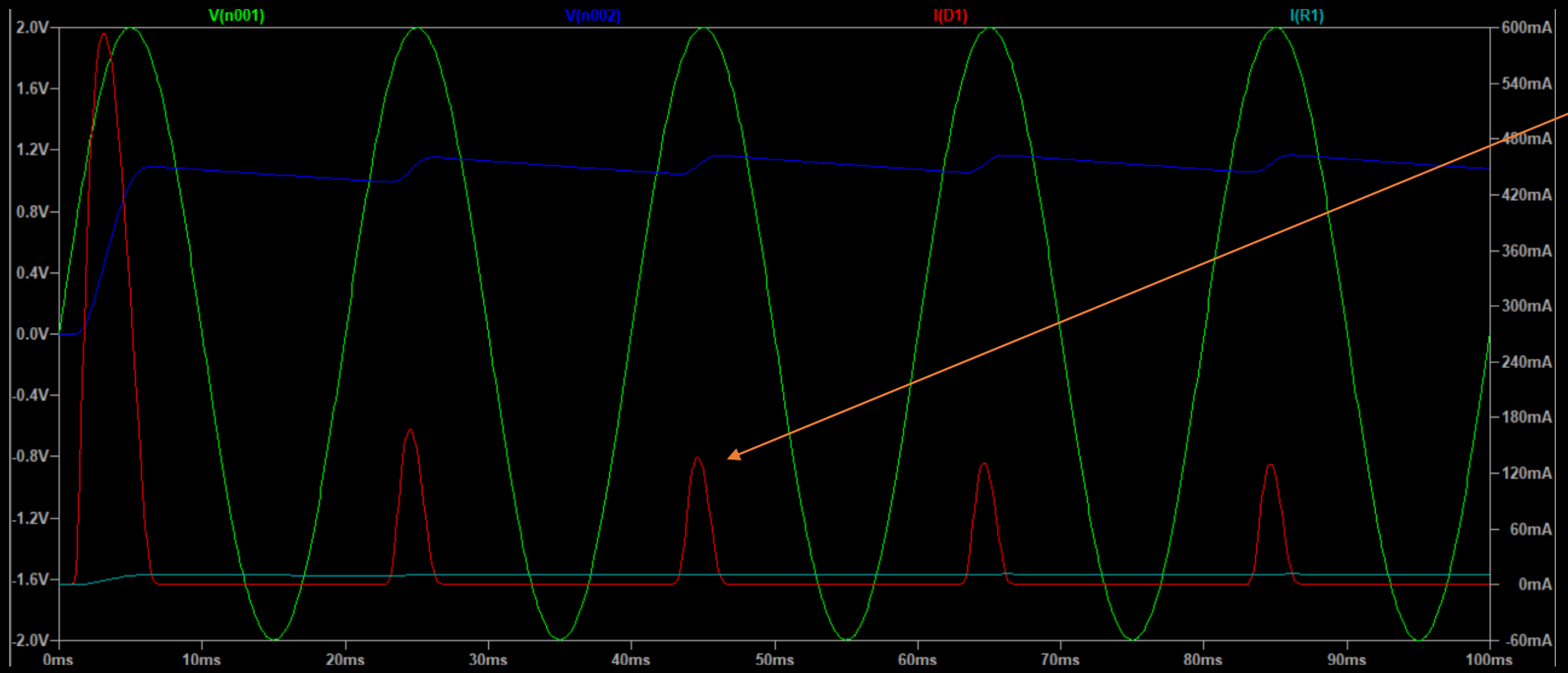
2m	8.42%
1.7m	9.90%
1.68m	10.01%
1.65m	10.20%
1.6m	10.51%
1.5m	11.21%
1m	16.76%
500u	32.93%
170u	87.46%

When R=100Ω, C=1.68mF makes it (almost) exactly 10%. This is an extremely significant and roughly 10 times difference.

Considering that the difference between 100Ω and 1kΩ is also 10 times, these two data might have something to do with each other. My guess would be that the voltage through the parallel part of the circuit has little to do with its overall impedance, but as long as the resistor and capacitor increase/decrease in the same ratio, the “current divider” circuit will work as normal.

Exercise E8

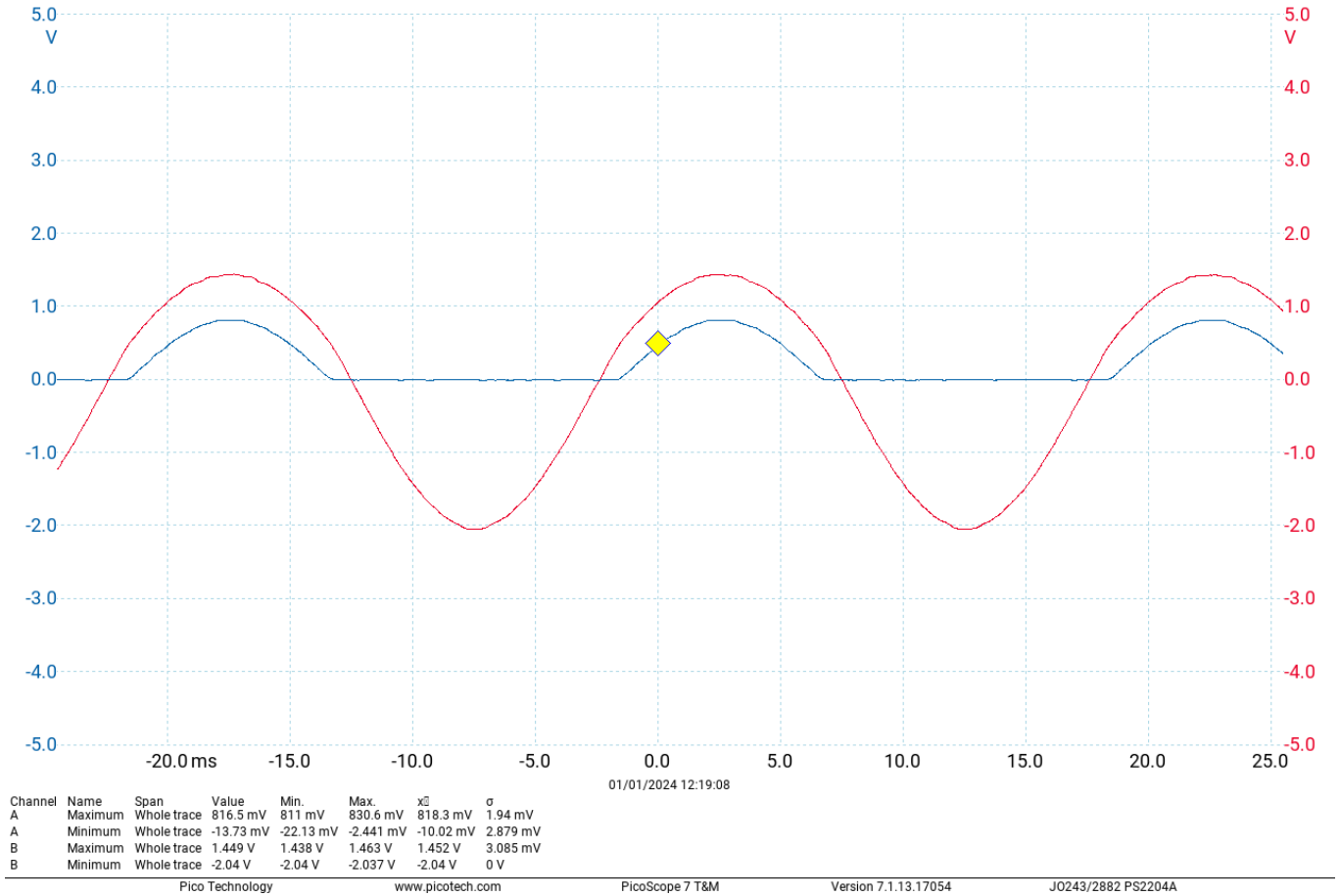
Note: The red plot here is the total current (i.e. current through diode), and the cyan plot is the current through the resistor.



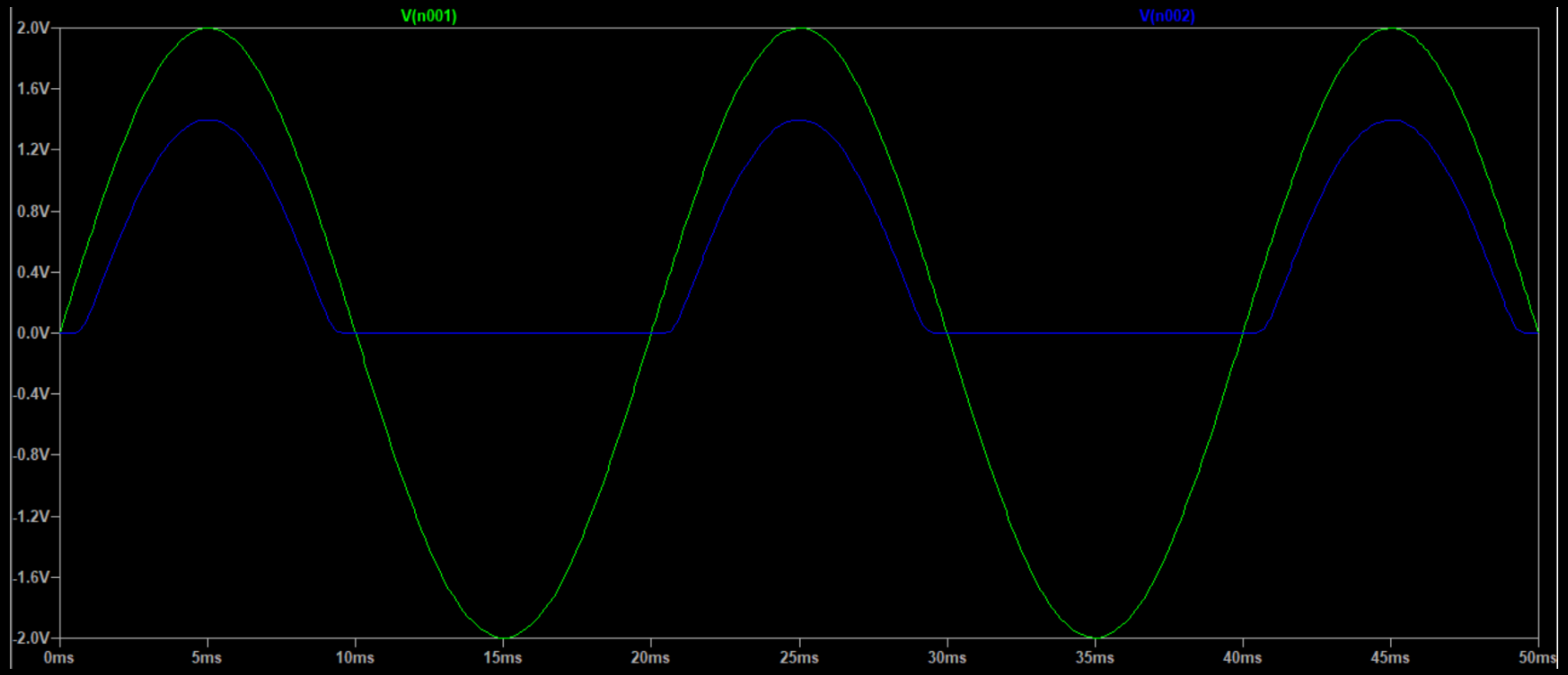
A mistake I made is comparing this with the voltage around diodes in previous exercises. This is the current.

The initial current through the diode is weirdly large, but the peak keep decreasing until it remains stable, presumably when the capacitor enters its fully charged cycle.

Exercise E9


5.0
V
4.0
3.0
2.0
1.0
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
-20.0 ms
-15.0
-10.0
-5.0
0.0
5.0
10.0
15.0
20.0
25.0
01/01/2024 12:19:08
Channel Name Span Value Min. Max. x̄ σ
A Maximum Whole trace 816.5 mV 811 mV 830.6 mV 818.3 mV 1.94 mV
A Minimum Whole trace -13.73 mV -22.13 mV -2.441 mV -10.02 mV 2.879 mV
B Maximum Whole trace 1.449 V 1.438 V 1.463 V 1.452 V 3.085 mV
B Minimum Whole trace -2.04 V -2.04 V -2.037 V -2.04 V 0 V
Pico Technology
www.picotech.com
PicoScope 7 T&M
Version 7.1.13.17054
JO243/2882 PS2204A

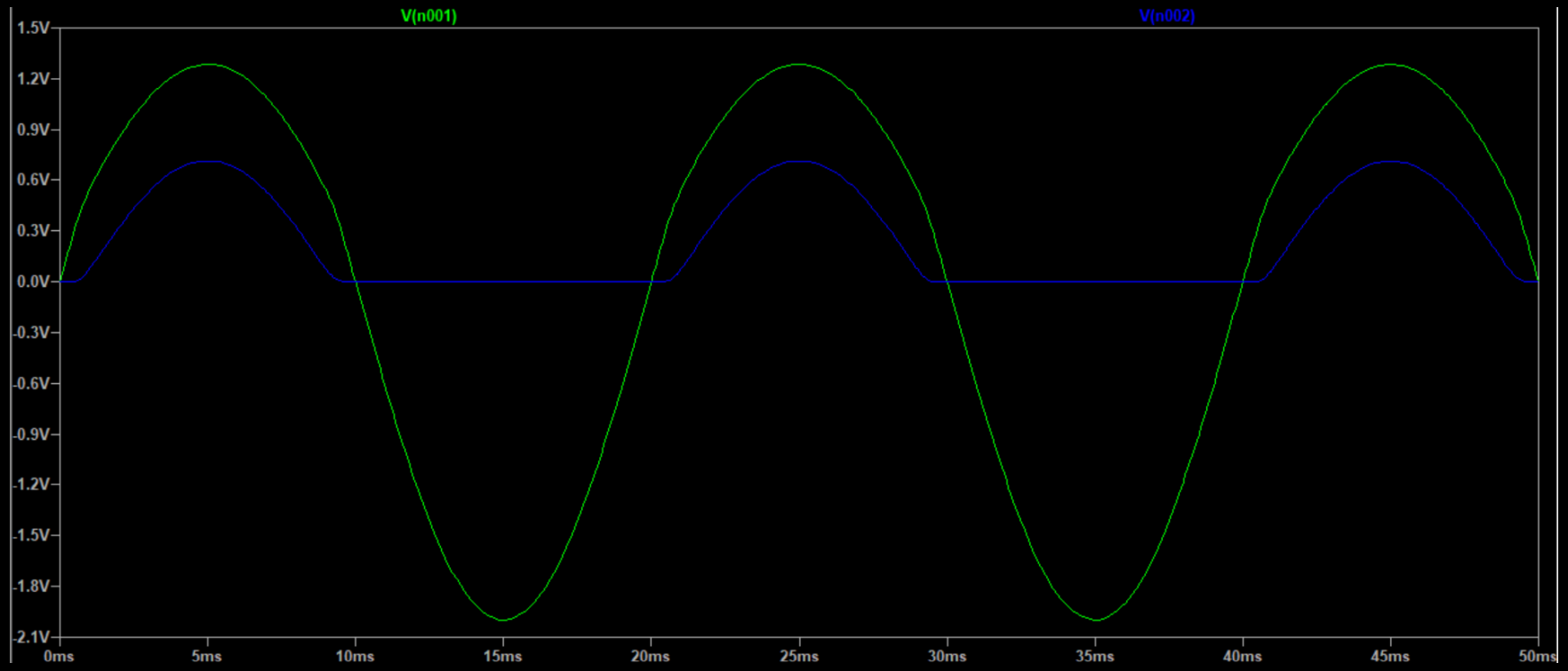
Exercise E9



- LTSpice V_R:
  - Max 1.398V
  - Min 0
- Experiment V_R:
  - Max 819.1mV
  - Min -9.603mV
- LTSpice V_All:
  - Max 2V
  - Min -2V
- Experiment V_All:
  - Max 1.450V
  - Min -2.040V

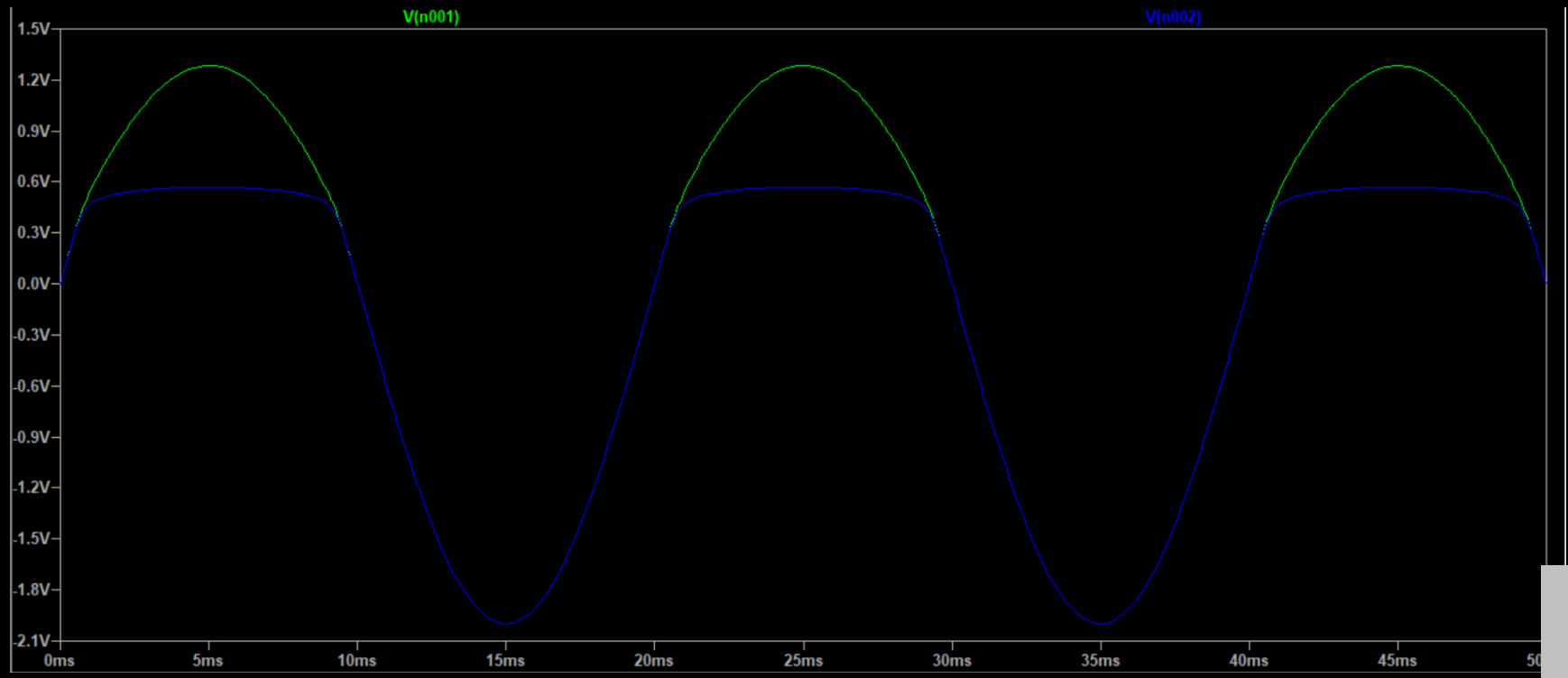
The experiment voltages are significantly lower than the simulation ones. This is presumably due to source impedance or some other impedance.

Exercise E9

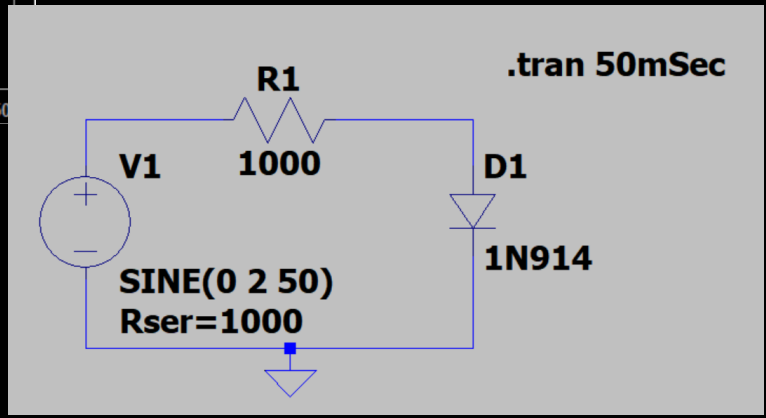


- When the series resistance of the source is set to 1kΩ, the results are quite similar to what we saw from the experiment results.

Exercise E9

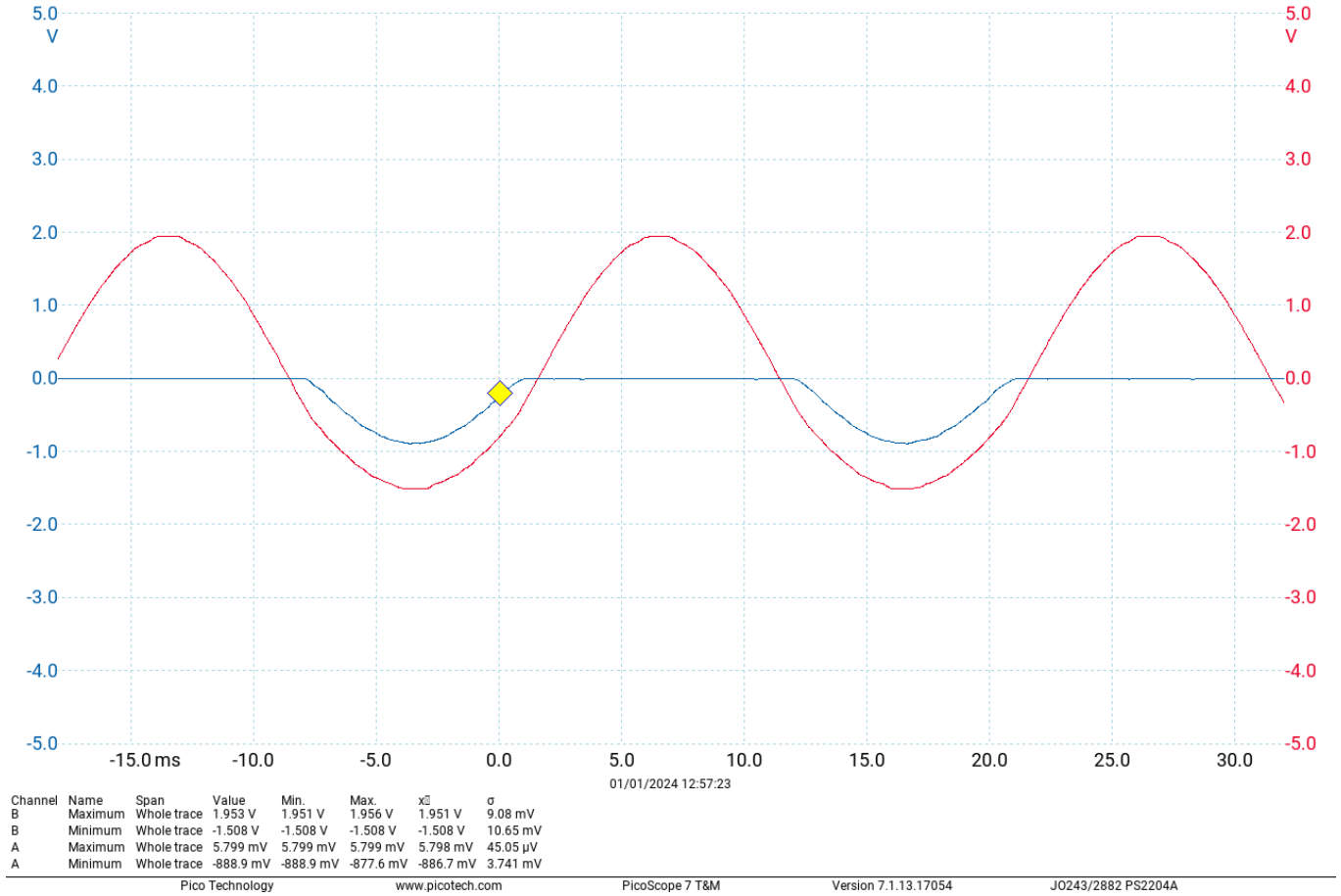


- The blue trace in this graph is the voltage across the diode.
- The schematic can be found below, but this graph can also be achieved by using V(n001) – V(n002) in the original circuit.



Exercise E9

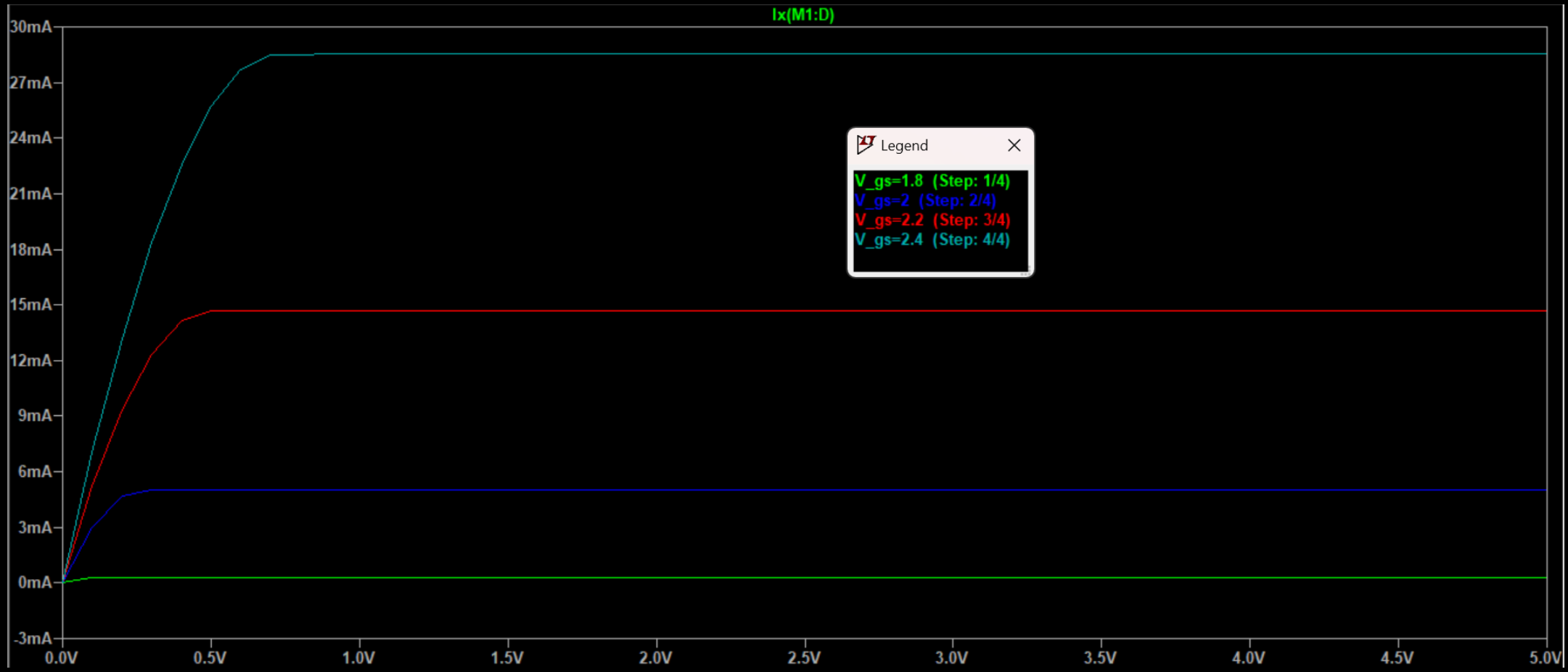
As expected, reversing the diode has little effect on the voltages besides reversing them.



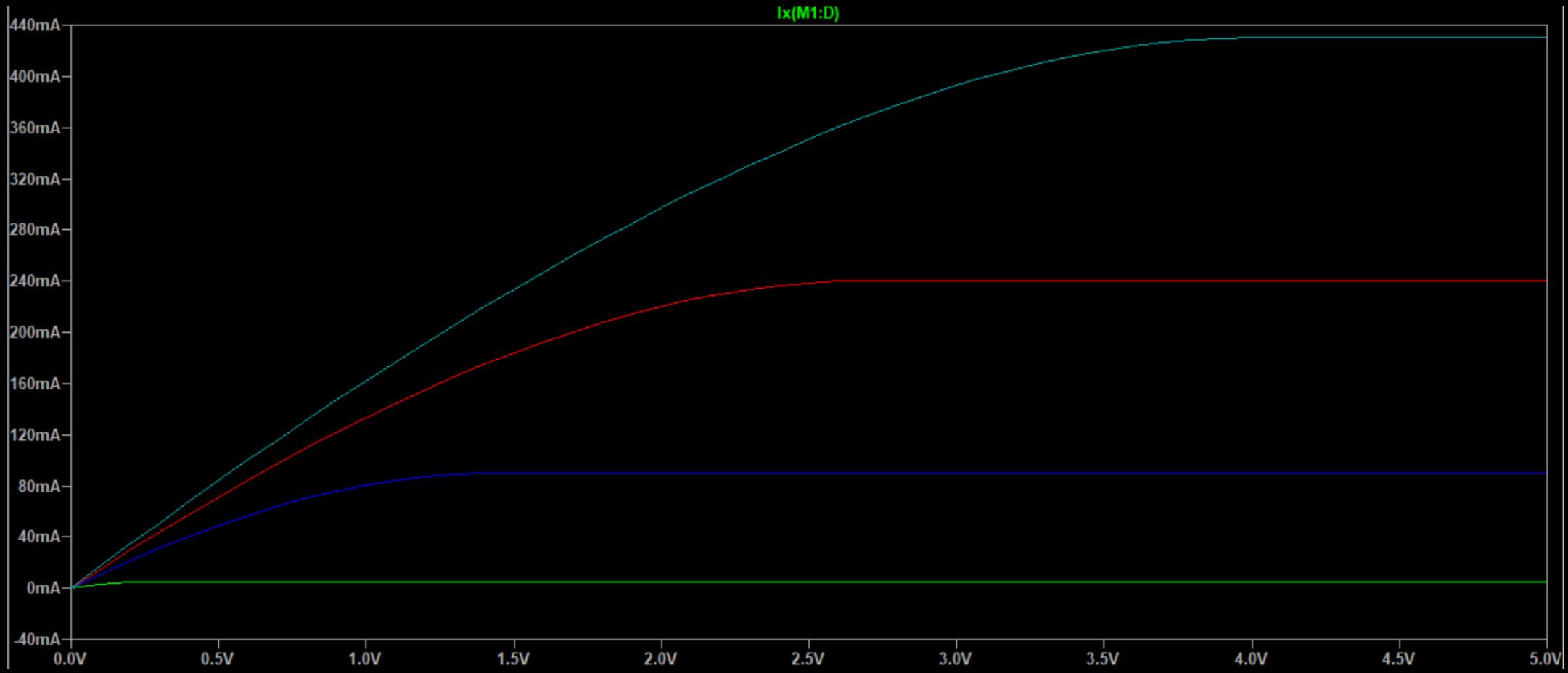
Exercise E9a

- Placeholder for now
- Left for finish after revision.

Exercise E10



Exercise E10



Exercise E10

- When gate-source voltage (V_GS) is quite large, it takes a significantly larger drain-source voltage (V_DS) to reach the max current (I_DS).
- Beside this, there are no significant differences between the two sweeps.

Exercise E11

(Does the load line always intercept the X axis at V_DD?)

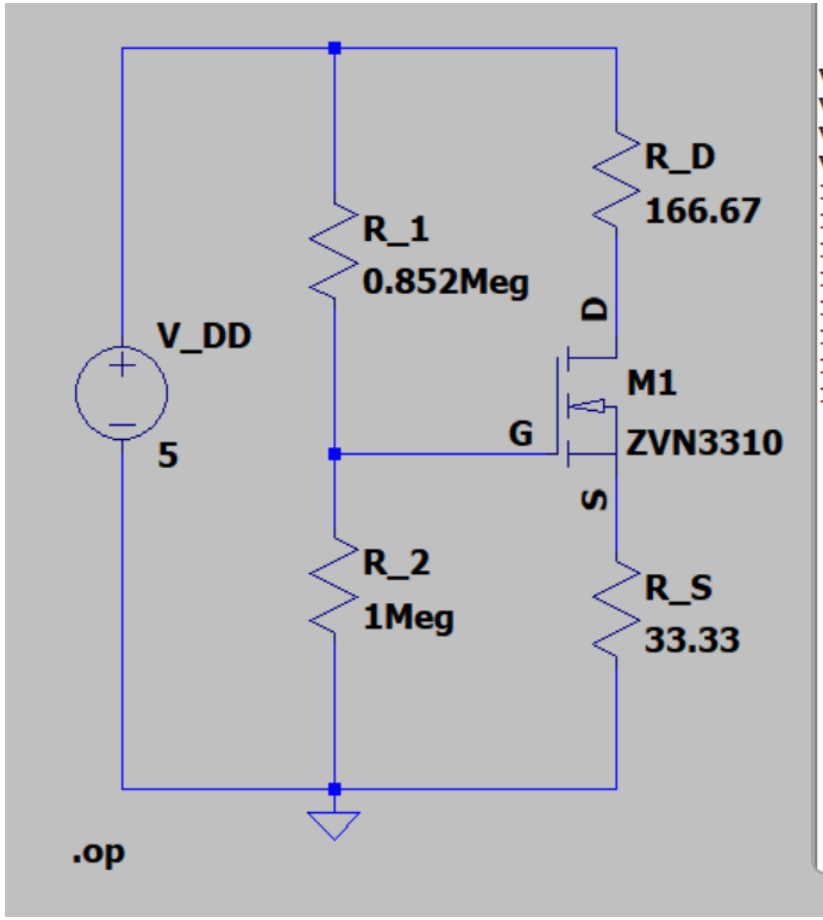
Exercise E11

- Max voltage swing at drain: $V_D = 0.5V_{DD} = 2.5V$
- Thus $R_S = \frac{V_D - V_{DS}}{I_D} = 33.33\Omega$, and $R_D = \frac{V_{DD} - V_D}{I_D} = 166.67\Omega$

- $V_G = V_{GS} + V_S = V_{GS} + I_D R_S = 2.7V$
- Since also $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$, given $R_2 = 1M\Omega$, we have $R_1 = 0.852M\Omega$

- Presumably 1MΩ is just chosen because it has a large resistance, and thus eliminating any current at gate.

Exercise E12




```
        --- Operating Point ---

V(d):           2.51826         voltage
V(s):           0.496289        voltage
V(g):           2.69978         voltage
V(n001):        5               voltage
I(R_s):         0.0148901       device_current
I(R_d):         0.0148901       device_current
I(R_1):         2.69978e-06     device_current
I(R_2):         2.69978e-06     device_current
I(V_dd):        -0.0148928      device_current
Ix(m1:3):       0.0148901       subckt_current
Ix(m1:4):       0               subckt_current
Ix(m1:5):       -0.0148901      subckt_current
```

Exercise E12

V_S and V_D are mixed up in the initial LTSpice model, so these two values are wrong as well. The errors are left here, serving as a reminder.

LTSpice Simulation Results:

- $V_S = 2.52V; V_D = 0.50V; V_G = 2.70V; V_{DD} = 5.00V$
- $I_D = 14.9mA$, and the current floating through R_S, R_D, Source-to-Drain, are all the exact same. (Probably the LTSpice model is just configured to do this?)
- $I_{R1} = I_{R2} = 2.70\mu A$
- No current between Gate and Drain

- Comments: From the values above (after the orange corrections): $V_{DS} = 2.02V$, $V_{GS} = 2.20V$, $I_D = 14.9mA$. All these values match very well with the givens, especially considering I only kept four sig figs in the resistances in the simulation. (i.e., 33.33Ohms)

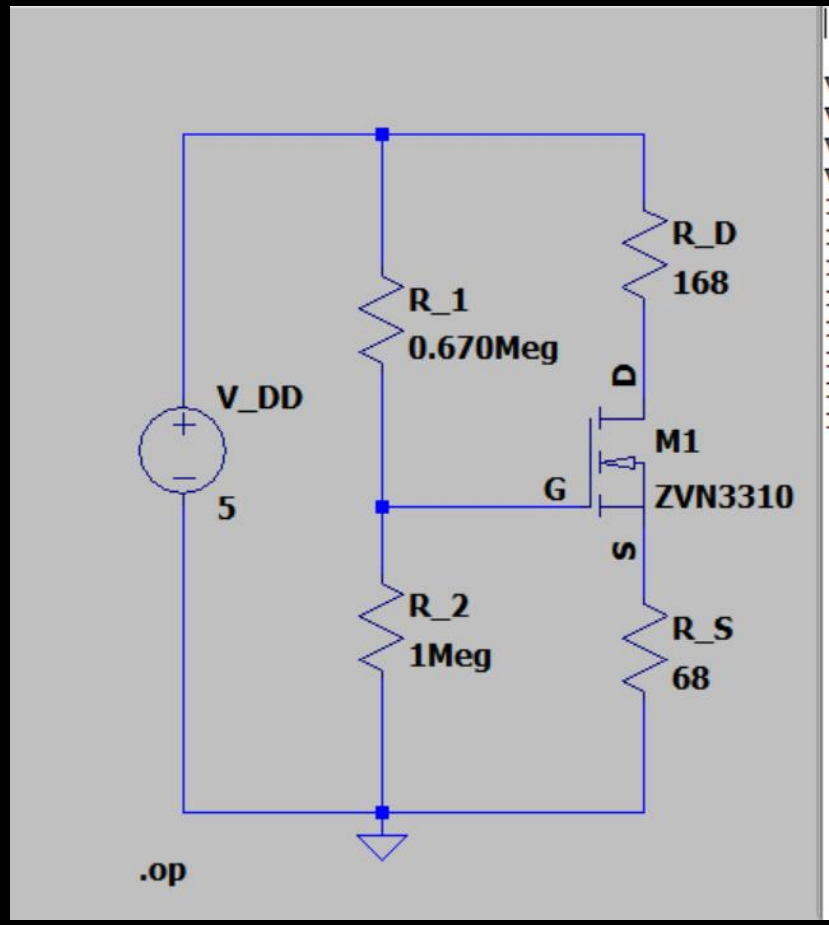
Exercise E13

- Two equations always apply to this circuit:
  - $I_D(R_D + R_S) = V_{DD} - V_{DS}$
  - $\frac{R_2}{R_1+R_2} V_{DD} = V_{GS} + I_D R_S$
- While changing the resistors, V_{GS} should stay from 1.8 to 2.4; $V_{DD} = 5V$. Also, according to the available resistors, we have $R_1 = 0.67M\Omega$, $R_2 = 1M\Omega$ and $R_D = 168\Omega$.
- Ideally, V_{DS} should be larger than $1V$ so it's guaranteed to stay in the "safe zone".

Exercise E13

- After simplifying things further, we have:
  - $2 + I_D R_S = 2.994$
  - $I_D(168 + R_S) = 5 - V_{DS}$
- One solution would be letting $R_S = 68\Omega$. Then we have
  - $I_D = 14.62mA$
  - $V_{DS} = 1.550V$

Exercise E13



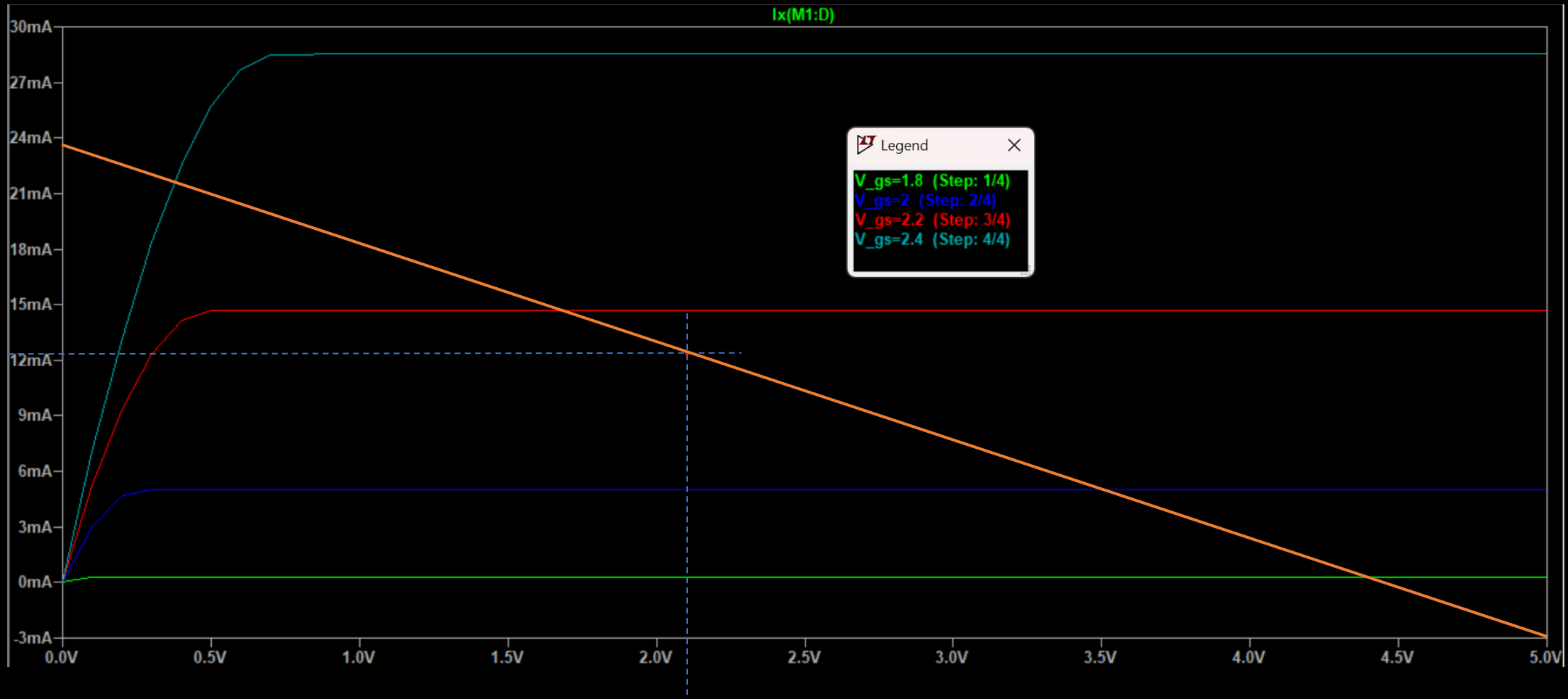

```
        --- Operating Point ---

V(d):           2.93484         voltage
V(s):           0.8359          voltage
V(g):           2.99401         voltage
V(n001):        5               voltage
I(R_s):         0.0122926       device_current
I(R_d):         0.0122926       device_current
I(R_1):         2.99401e-06     device_current
I(R_2):         2.99401e-06     device_current
I(V_dd):        -0.0122956      device_current
Ix(m1:3):       0.0122926       subckt_current
Ix(m1:4):       0               subckt_current
Ix(m1:5):       -0.0122926      subckt_current
```

Exercise E13

- Operating Point:
  - $V_{DS} = 2.09894V$
  - $I_D = 12.2926mA$

Exercise E13: Revision Acceptable



Exercise E13

- At time of submission, the circuit was unable to be built due to lack of equipment (ZVN3310 MOS FET)