Examen de mostra/pràctica, preguntes i respostes

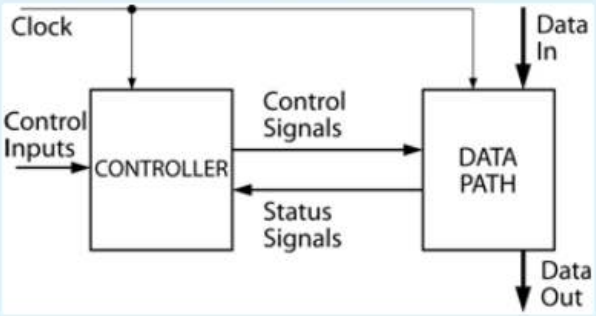
Circuits i Sistemes Digitals (Universitat Politècnica de Catalunya)

CSD.

Example questions for the P7-P8 questionnaire

In datapath there are registers to save operants and results, an arithmetic and logic unit (ALU) and other combinational circuits.

The function of the status signals from the datapath to the controller FSM is to inform about the result of the operations (flags), for instance zero, carry out, negative, overflow, division by zero, etc.

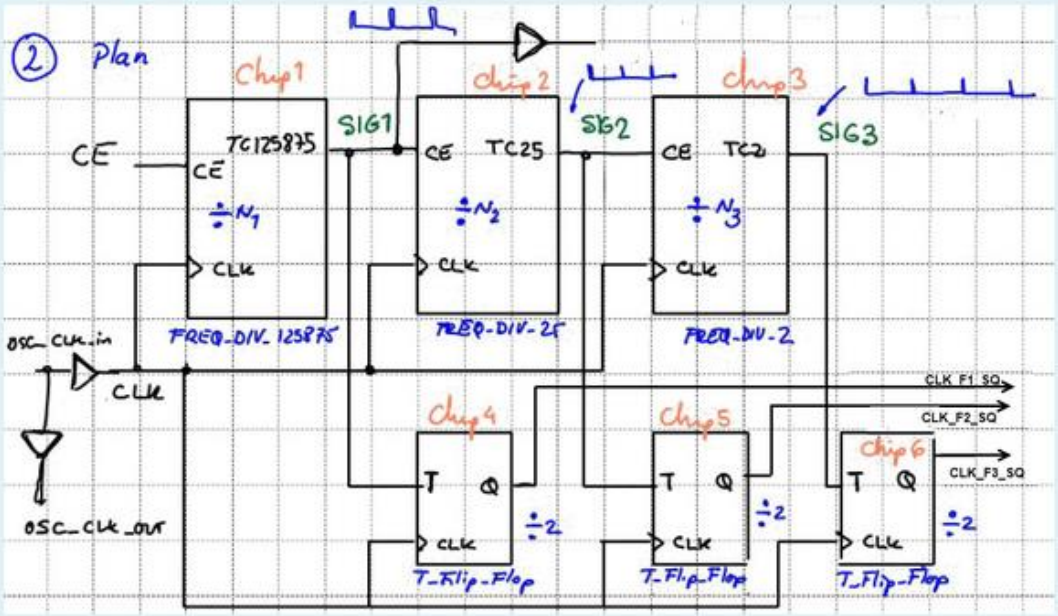


Select one:

Answers

- (●) True
- ( ) False

A *CLK_generator* circuit sketch is presented below. Which is the frequency of the output **CLK_F1_SQ** when applying an oscillator input of 100.7 MHz ?

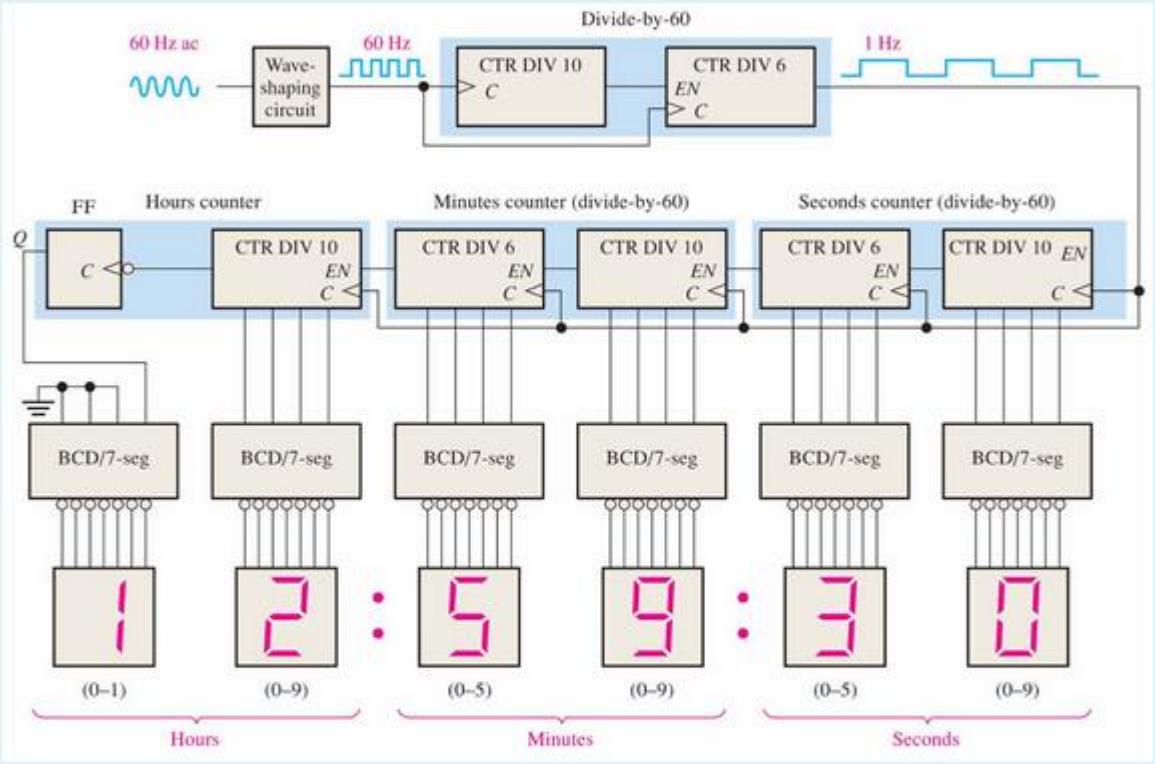


Select one:

- ( ) a. 1 Hz
- ( ) b. 25 Hz
- ( ) c. 800 Hz
- (●) d. 400 Hz

This is a schematic copied from the book T. L. Floyd, Digital Fundamentals, 9th ed., Prentice Hall, 2006. It is a design of a real-time clock that has HH:MM:SS BCD outputs. The names of the components and signals has not been adapted to our CSD naming style, but they are very similar. The wave-shaping circuit is analogue.

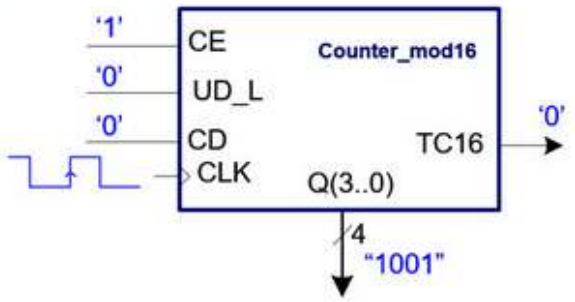
The question, after inspecting the circuit, is: how many D-FF it contains?



Select one:

- a. The circuit contains **59** data registers D-FF
- b. The circuit contains **14** data registers D-FF
- c. The circuit contains **26** data registers D-FF
- d. The circuit contains **192** data registers D-FF

With respect to the *Counter_mod16* in the picture below, which is the next state after the CLK's rising edge?



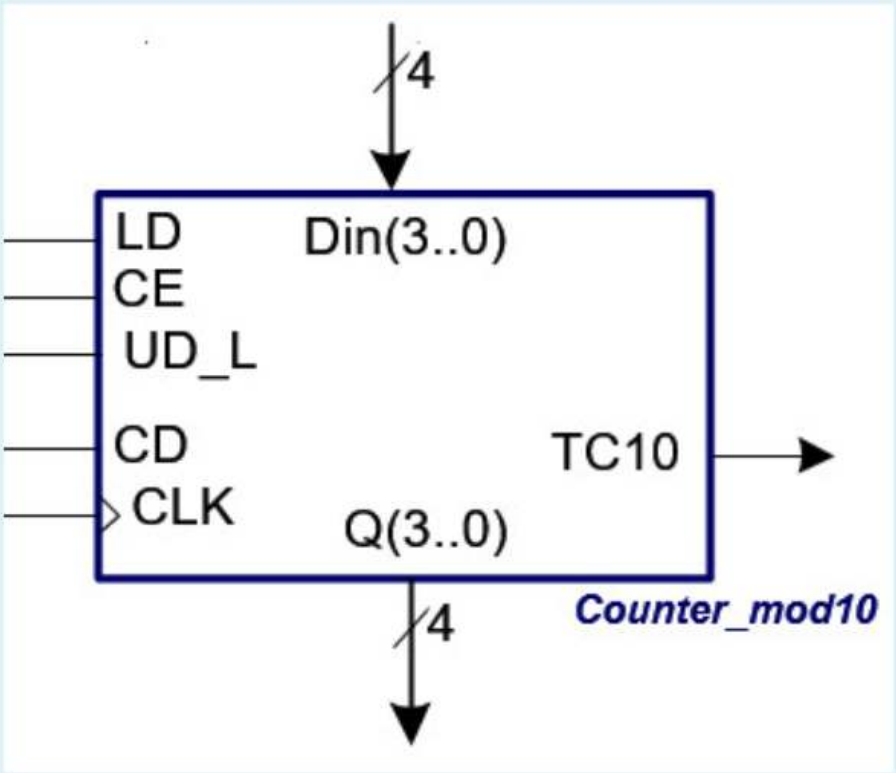
CE	UD_L	Q*	Synchronous operation after the CLK's rising edge
0	x	Q	Do nothing (inhibit)
1	1	$(Q+1)_{mod16}$	Up counting in binary
1	0	$(Q-1)_{mod16}$	Down counting in binary

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Select one:

- (●) a. "1000"
- ( ) b. "1011"
- ( ) c. "1001", because the system is disabled or inhibited
- ( ) d. "1100"

Using and interconnecting 3 universal counters modulo 10 (*Counter_mod10*) like the one depicted below and other components like logic gates, we can design many different counters. Which is the maximum modulo that can be attained when connected in cascade?



Select one:

- ( ) a. *Counter_mod100*
- (●) b. *Counter_mod1000*
- ( ) c. *Counter_mod30*
- ( ) d. *Counter_mod300*