# TEST Abril 2018, preguntas

Circuits i Sistemes Digitals (Universitat Politècnica de Catalunya)

# CSD TEST 5-6 Q2 2018

Question **1**

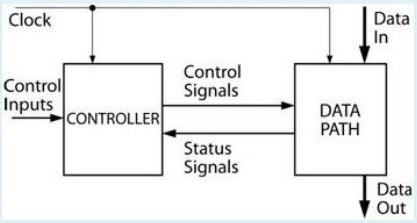
Not yet answered

Marked out of 1.00

Flag question

In datapath there are registers to save operants and results, an arithmetic and logic unit (ALU) and other combinational circuits.

The function of the status signals from the datapath to the controller FSM is to inform about the result of the operations (flags), for instance zero, carry out, negative, overflow, division by zero, etc.




Select one:

Answers

- True
- False

Question **2**

Not yet answered

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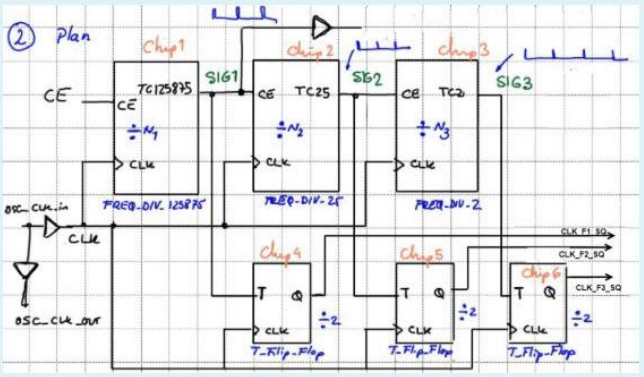
Flag question

A *CLK_generator* circuit sketch is presented below. How many D_FF are required to solve it?




Select one:

- a. 17
- b. 26
- c. 30

Question **3**

Not yet answered

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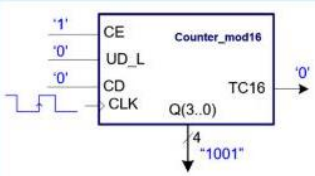
Flag question

With respect to the *Counter_mod16* in the picture below, which is the next state after the CLK's rising edge?




| CE | UD_L | Q* | Synchronous operation after the CLK's rising edge |
|---|---|---|---|
| 0 | x | Q | Do nothing (inhibit) |
| 1 | 1 | $(Q+1)_{mod16}$ | Up counting in binary |
| 1 | 0 | $(Q-1)_{mod16}$ | Down counting in binary |

TC16 = '1' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Select one:

a. "1100"

b. "1000"

c. "1001", because the system is disabled or inhibited

d. "1011"

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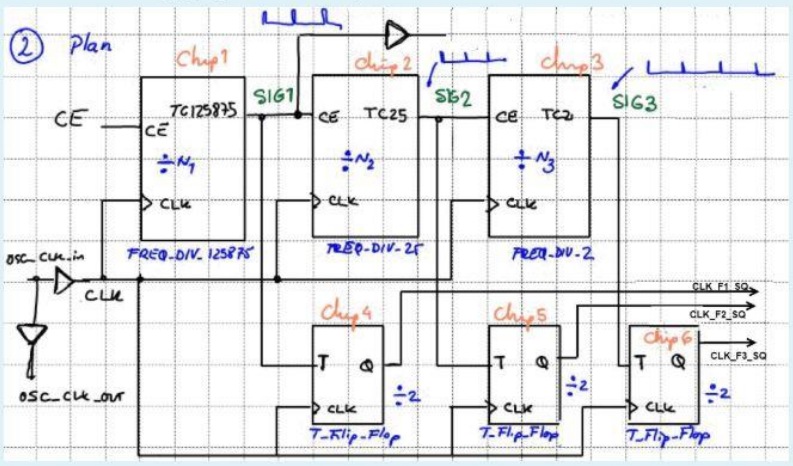
A *CLK_generator* circuit sketch is presented below. Which is the frequency of the output **CLK_F1_SQ** when applying an oscillator input of 100.7 MHz ?




Select one:

a. 25 Hz

b. 800 Hz

c. 400 Hz

d. 1 Hz

Question 5

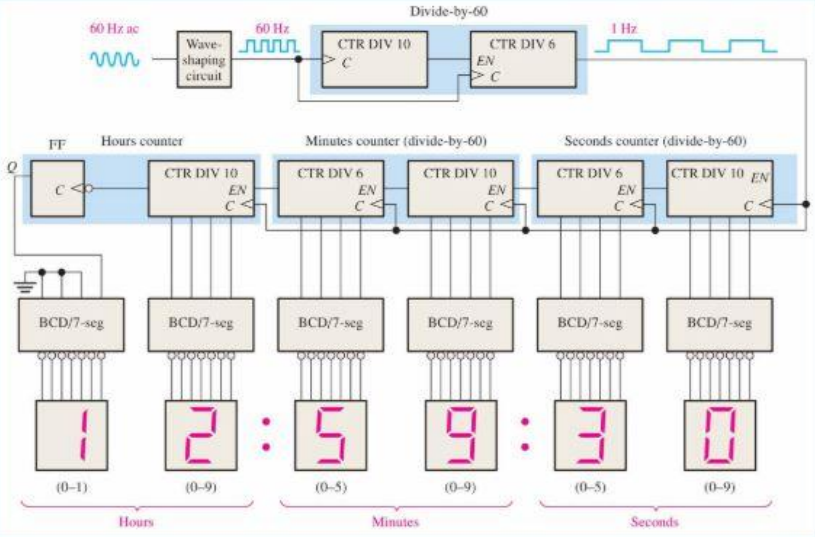
Not yet answered

Marked out of 1.00

Flag question

This is a schematic copied from the book T. L. Floyd, Digital Fundamentals, 9th ed., Prentice Hall, 2006. It is a design of a real-time clock that has HH:MM:SS BCD outputs. The names of the components and signals has not been adapted to our CSD naming style, but they are very similar. The wave-shaping circuit is analogue.

The question, after inspecting the circuit, is: how many D-FF it contains?




Select one:

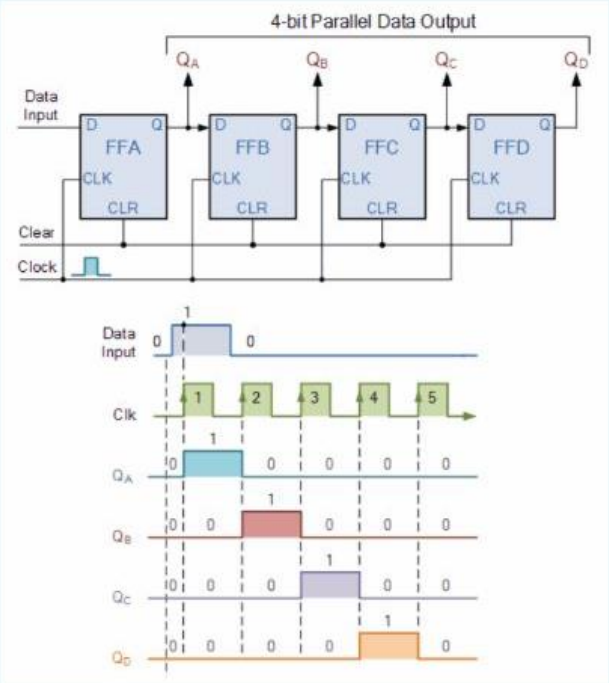
a. The circuit contains **192** data registers D-FF

b. The circuit contains **26** data registers D-FF

c. The circuit contains **14** data registers D-FF

d. The circuit contains **59** data registers D-FF

This schematic is taken from the internet. It looks like some kind of synchronous sequential circuit because it is based on data flip-flops (D_FF). Which statement below is correct attending to the Data input?




Select one:

- a. After 4 CLK periods the outputs will be zeroed (reset) and the only way to reload the system will be sampling another pulse at Data Input.
- b. The output $Q_D$ will have the same information currently in Data Input after 2 CLK periods.
- c. The sequence generated in the outputs $Q_A, Q_B, Q_C, Q_D$ is a Johnson code.

Question **7**

Not yet answered

Marked out of 1.00

Flag question

Which is the maximum module of a binary counter of 3 bits? How many flip flops it has?

Select one:

- a. 16 and 4
- b. 8 and 2
- c. 4 and 3
- d. 8 and 3

Question **8**

Answer saved

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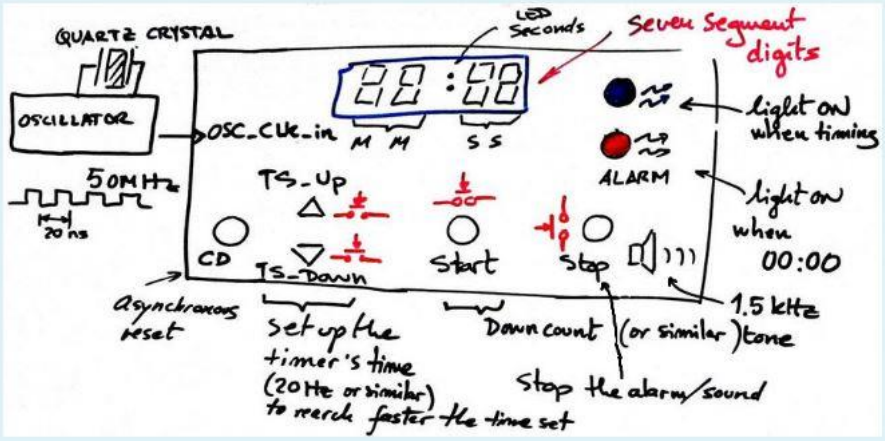
Flag question

The sketch below belongs to a Timer that can be planned as a dedicated processor with a datapath, a CLK_Generator and a control FSM. The timer has a 1 hour capacity represented in MM:SS, being able to countdown from 59:59 to 00:00. Which is the modulo of this counter in the datapath, and how many D_FF are required to build it?




Select one:

- a. The counter in the datapath has a modulo of 65536 and contain 12 D_FF.
- b. The counter in the datapath has a modulo of 9999 and contain 16 D_FF.
- c. The counter in the datapath has a modulo of 60 and contain 8 D_FF.
- d. The counter in the datapath has a modulo of 3600 and contain 16 D_FF.

Question **9**

Not yet answered

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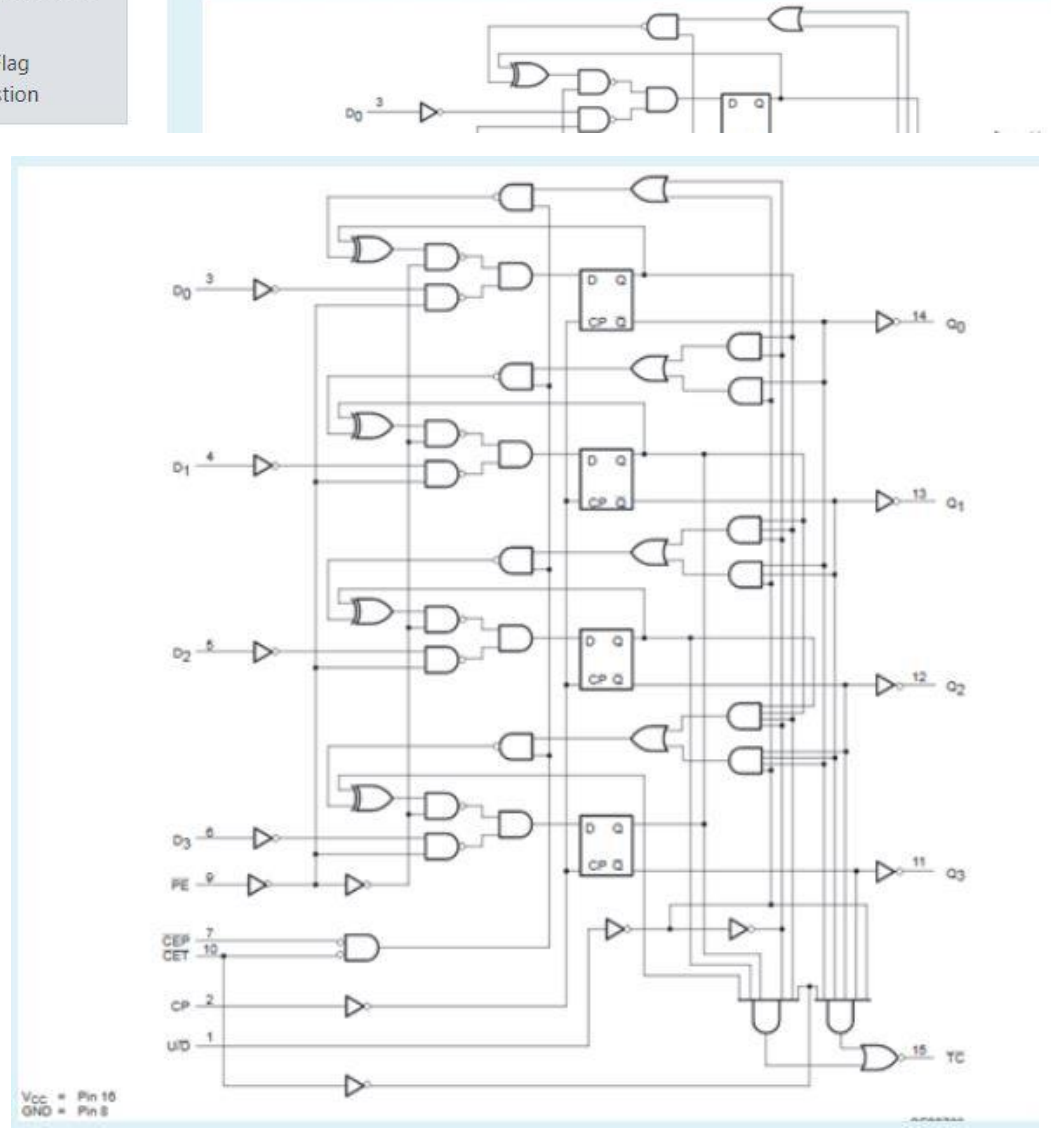
Flag question

The following figure shows the logic diagram of a presettable synchronous up/down binary counter. Indicate the number of states of the counter and justify your response.




Select one:

- a. 2
- b. 16
- c. 8
- d. 4

Question **10**

Not yet answered

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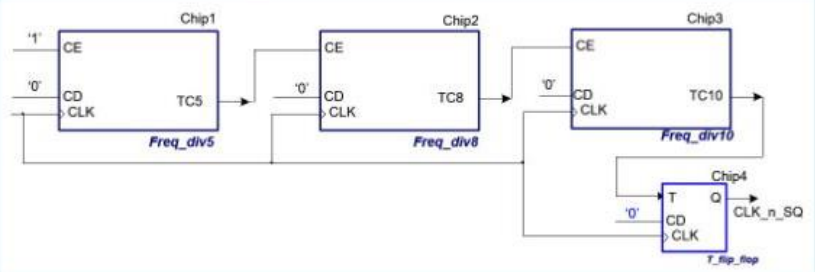
Flag question

A *CLK_generator* circuit is designed cascading frequency dividers and a T_FF as shown in the picture. Which is the frequency of the output port ***CLK_n_SQ*** if the input CLK frequency is 10 MHz?




Select one:

a. 12.5 kHz

b. 25 kHz

c. 250 kHz

d. 250 Hz