Dhruv Dighrasker

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Education

University of Michigan - College of Engineering **Ann Arbor, MI**

M.S.E in Electrical + Computer Engineering (Integrated Circuits & VLSI) *Apr. 2027*

- **GPA:** 4.0/4.0
- **Coursework:** Parallel Computer Architecture, VLSI, Quantum Hardware

B.S.E in Computer Engineering *Dec. 2025*

- **GPA/Awards:** 3.64/4.0 — Stellantis Student Award (2023), Engineering Dean's List Honor Roll
- **Coursework:** Advanced Computer Architecture, Operating Systems, Applied GPU Programming, Digital Integrated Circuits, Digital Signal Processing, Data Structures + Algorithms, Digital Logic Design, Electrical Circuits

Technical Skills

Languages: C/C++, SystemVerilog/Verilog, ARM Assembly, Python, Matlab, Tcl
Software: Synopsys VCS, ModelSim, Quartus, Cadence Virtuoso, STM32CubeIDE, Verdi, SolidWorks
Hardware + Tools: FPGA, Arduino, STM32 (NUCLEO), Git, Linux, perf, UVM

Work Experience

University of Michigan - CSE Department **Ann Arbor, MI**

Graduate Student Instructor (former TA), Digital Logic Design *Apr. 2024 – Present*

- Led weekly labs & office hours for a 220+ student course, teaching complex topics such as FSM design, sequential multiplication, logic minimization, & timing analysis using Quartus & Verilog on DE2-115 FPGA Development Boards
- Maintained the course autograder infrastructure that validates student FPGA designs for 8+ projects using automated Verilog testbenches & utilizes mutation testing techniques to ensure robustness of student-written tests

Computer Engineering Laboratory **Ann Arbor, MI**

Research Assistant *Feb. 2025 - Present*

- Evaluated correlation between accuracy and SRAM area consumption for state-of-the-art TAGE & perceptron branch predictors using gem5 simulator & Synopsys Design Compiler to determine baseline for memory under-utilization
- Trained a Transformer-based oracle branch predictor on over 100 CBP2025 traces & conducted comprehensive ablation studies to quantify the accuracy contribution of each input feature, laying the groundwork for hardware synthesis

Openstream.ai **Bridgewater, NJ**

Software Engineering Intern *May 2025 - Aug. 2025*

- Integrated Whisper.cpp Speech Recognition engine into Android app, implementing a Kotlin-JNI-C++ pipeline to enable real-time transcription, achieving word-error-rate of less than 8% & complete on-device recognition for 75+ languages
- Fine-tuned Gemma 3n, an 8B-parameter multi-modal model, for on-device image inference by analyzing the impact of prompt complexity, image resolution, & token limits; successfully quantized model from 10GB to 4GB, reducing memory usage by 60% while limiting accuracy loss to just 18% through targeted fine-tuning with client-relevant datasets

Projects

127 MHz RISC-V CPU

- Designed & verified a 32-bit, N-way superscalar, MIPS R10K-style RISC-V out-of-order processor in SystemVerilog
- Integrated nonblocking caches, tournament branch predictor, & load-store queue with byte-level forwarding
- Developed custom testbenches to validate functionality & achieved performance of 1.13 IPC for clock period of 7.8ns

UVM Testing Env for Write-Back L2 Cache

- Created modular UVM environment (10+ reusable components) to verify multi-core L2 cache, passing 90 + testcases
- Incorporated MESI coherence, MSHRs, AXI4-Lite DRAM interface & identified bugs through directed testing

FlashAttention-ASIC-Accelerator

- Designed fixed-point FlashAttention-2 ASIC accelerator with tiled, IO-aware dataflow and fully fused attention pipeline
- Implemented Expmul-based softmax and Q-format datapath achieving 385 MHz operation with minimal accuracy loss

8-Bit Ripple-Carry Adder

- Designed 8-bit ripple-carry adder in Cadence Virtuoso through 10+ components to perform addition & accumulation
- Optimized transistor sizing & logic families to achieve 1.5 GHz functionality with power consumption 28% below budget

RTL Four-Function Calculator on FPGA

- Engineered four-function calculator on DE2-115 FPGA using Verilog for RTL design & Modelsim for verification
- Implemented arithmetic operations on 11-bit two's complement inputs, featuring booth multiplication, & integer division