

SLS Lecture 10 : Assembly : Program Analysis

Contents

- [10.1. sumit.s and usesum.s](#)
- [10.2. This code has a problem that we will address in the next lecture](#)

**SO HOW DO WE MAKE
USE OF A COMPUTER?**

IDEA/TASK:
ADD NUMBERS

IDEA/TASK:
ADD NUMBERS

MY DATA NUMBERS AS
BYTE VALUES

ISA: SPEC

ADD, SUB, IMUL, MUL, IDIV,
DIV, INC, DEC, NEG, CMP

ALU

AND, OR, NOT, XOR, SHL, SHR
TEST

DATA TRANSFER

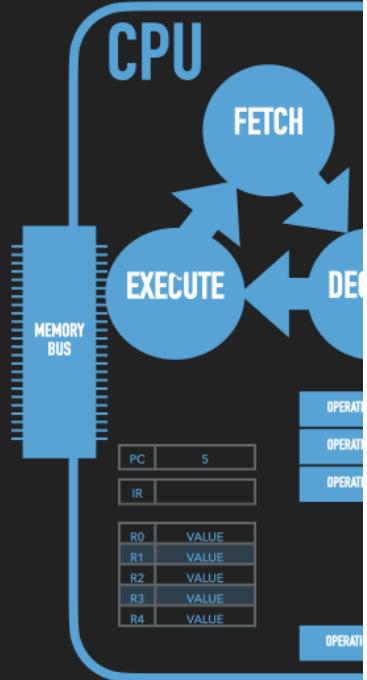
CONTROL FLOW

MY DATA NUMBERS AS
BYTE VALUES

VNA : COMPUTER

MEMORY

0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
⋮	
N-1	
N	



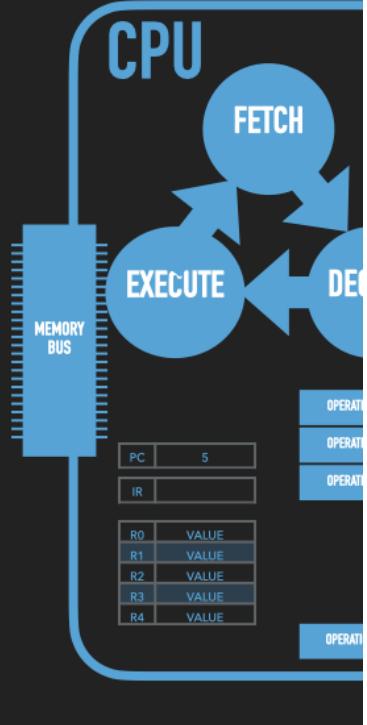
IDEA/TASK:
ADD NUMBERS

MY DATA NUMBERS AS
BYTE VALUES

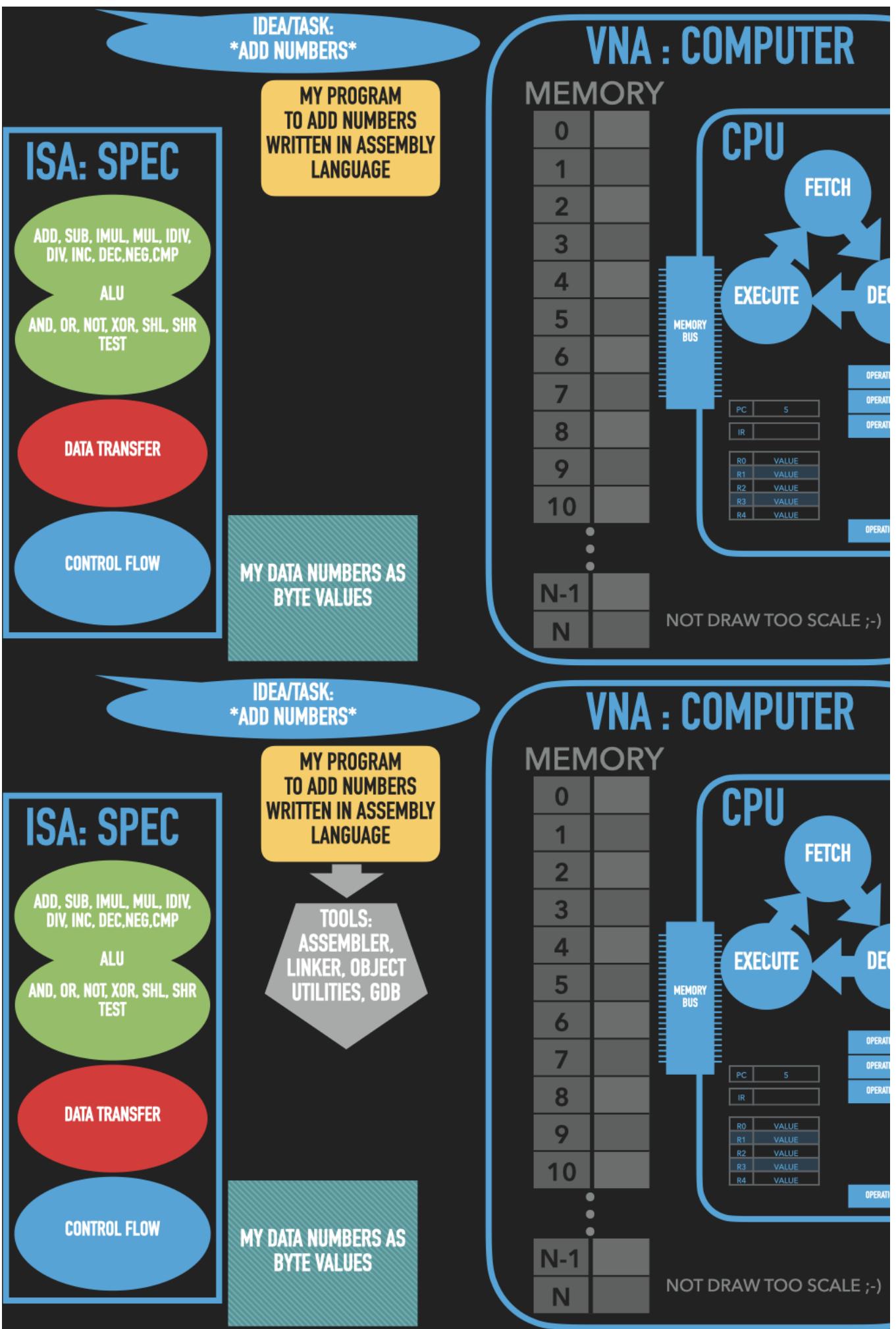
VNA : COMPUTER

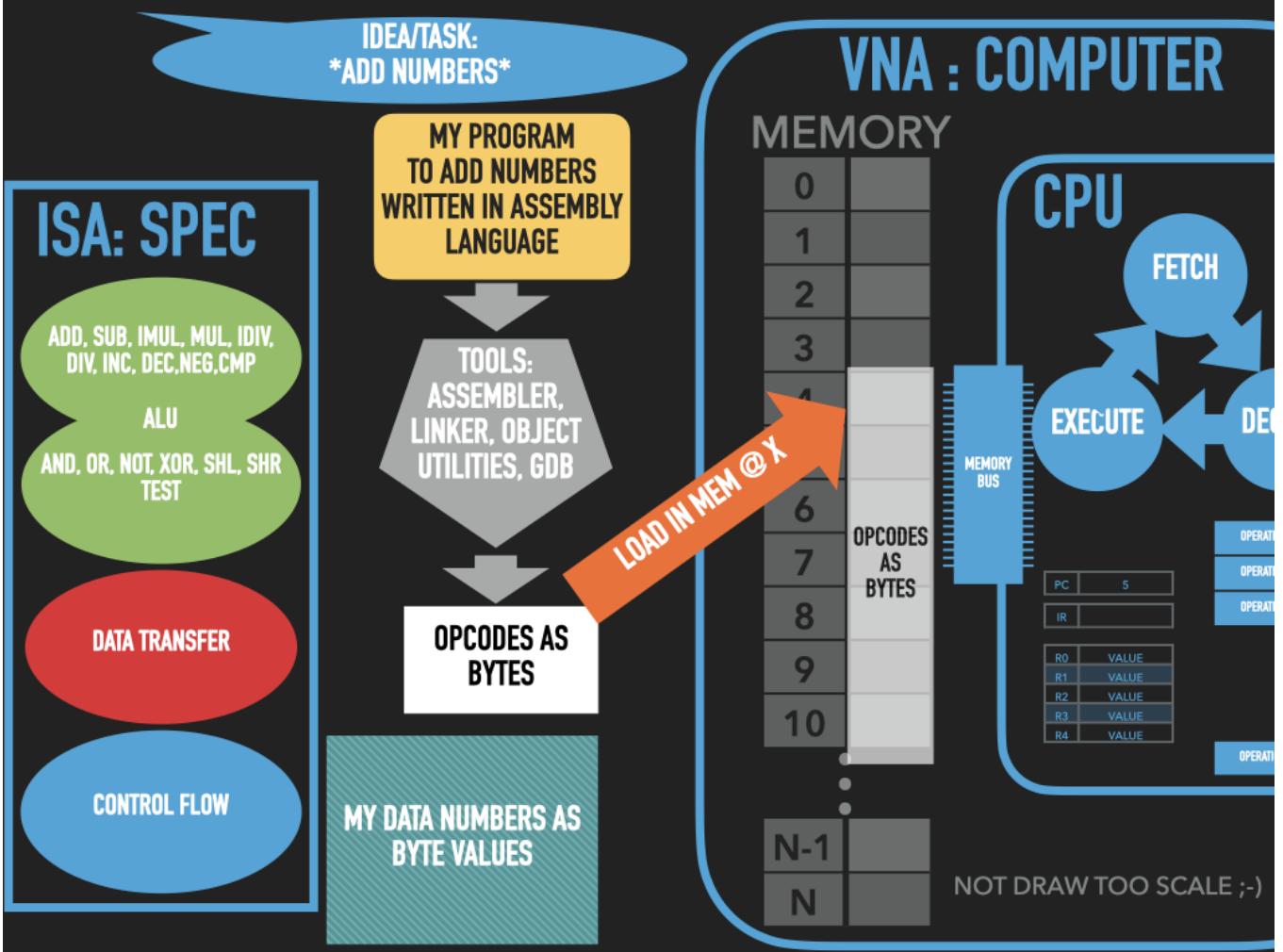
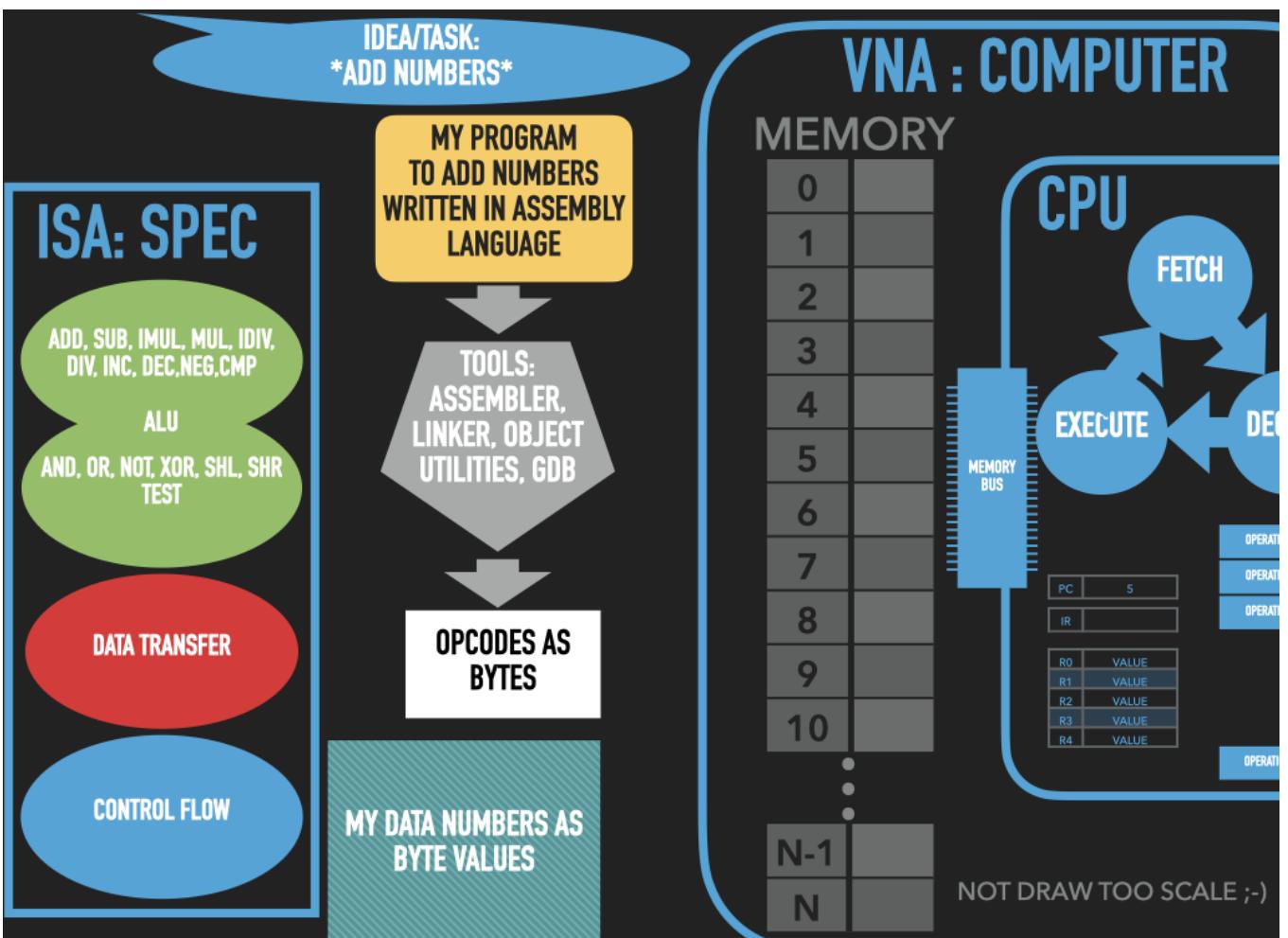
MEMORY

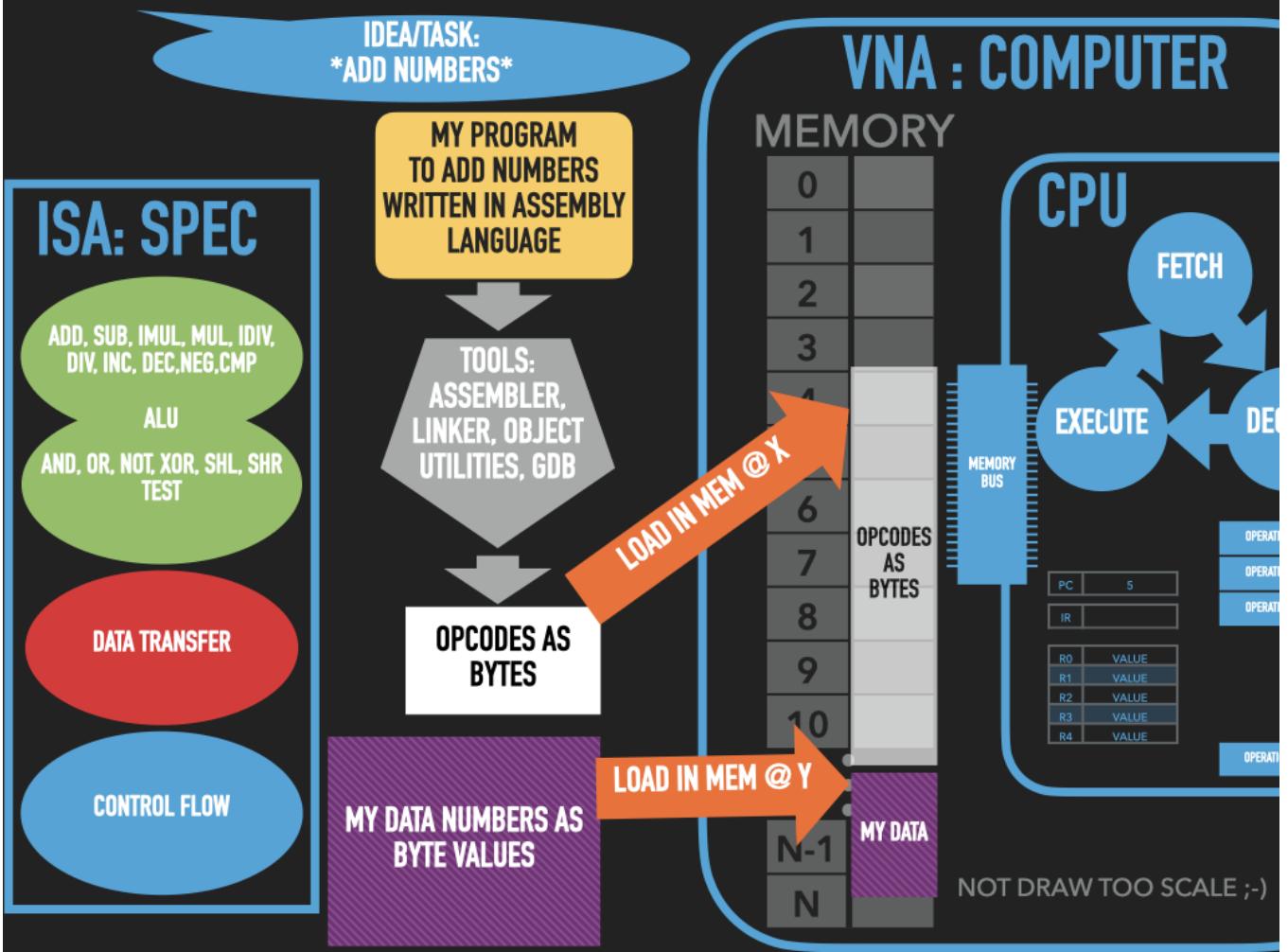
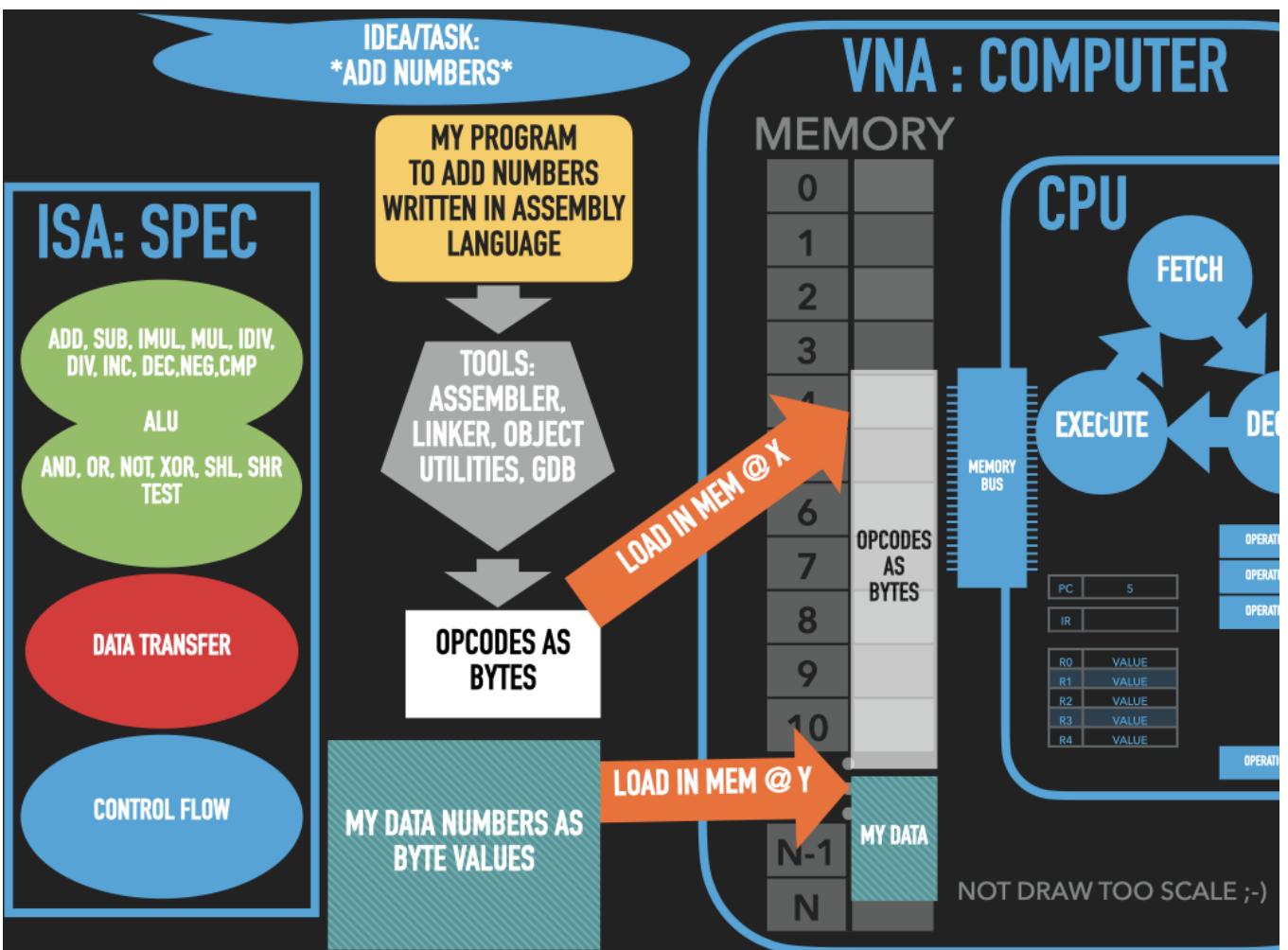
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
⋮	
N-1	
N	



NOT DRAW TOO SCALE ;-)







USING THE EXAMPLE WE ARE GOING TO WORK THROUGH

THE ANATOMY OF A PROGRAM

- ▶ Simple linear sequence of instructions
- ▶ Repeat sequence
 - ▶ Go back to a prior location in a sequence – special case of goto
 - ▶ Goto an arbitrary place
- ▶ Conditional
 - ▶ If goto
 - ▶ If mov
- ▶ Advanced :
 - ▶ Functions & recursion
 - ▶ Jump table

anatomy

Pronunciation /ə'naðəmē/ /ə'nædəmē/

NOUN (anatomies)

- 1 The branch of science concerned with the bodily structure of humans and other living organisms, especially as revealed by dissection and the study of disease: '*he studied physiology and anatomy*' '*human anatomy*'

[+ More example sentences](#)

- 1.1 The bodily structure of an organism.

'descriptions of the cat's anatomy and behavior'

[+ More example sentences](#) [+ Synonyms](#)

- 1.2 *informal* A person's body.

'every part of his anatomy hurt'

'people should never be reduced to their anatomies'

[+ More example sentences](#) [+ Synonyms](#)

- 2 A study of the structure or internal workings of something.

'Machiavelli's anatomy of the art of war'

[+ More example sentences](#) [+ Synonyms](#)

BEFORE WE GET GOING WHAT ARE WE MISSING?

$$S = \sum_{i=0}^n x_i$$

int i;

for (i=0; i<n; i++) {

$$S = S + x[i]$$

}

VARIABLES AND DATA STRUCTURES

SCALARS, ARRAYS,
LISTS, ETC ...

VARIABLES, DATA STRUCTURES AND INPUT DATA : ORGANIZED BYTES IN MEMORY

LOCATIONS AND VALUES

- ▶ We pick locations to hold our data:
- ▶ We pick the number of bytes we need to reserve based on what we want data we plan to store and work with
- ▶ Our job to stay organized and keep track of things
- ▶ Write code that moves data in and out of registers so that we can do operations on it

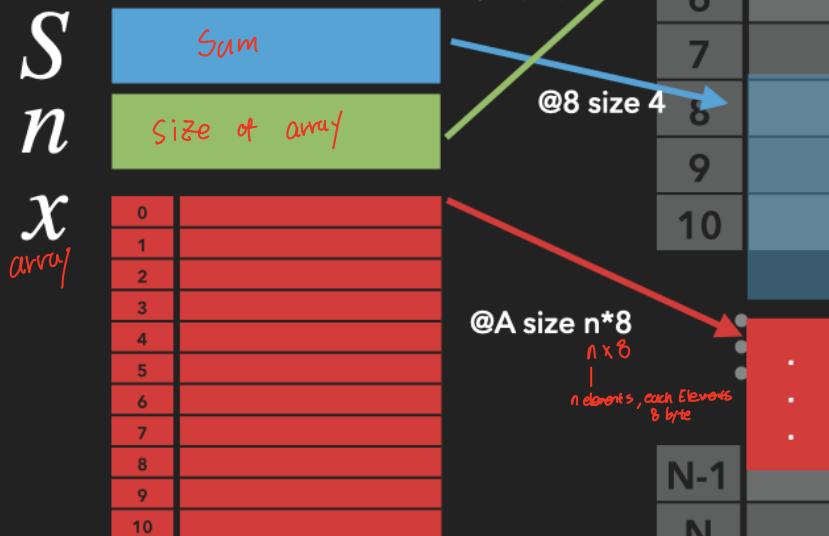
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
⋮	⋮
N-1	
N	

	byte 7	byte 6	byte	byte	byte 3	byte 2	byte
PC							
R0							
R2							
R3							
R4							

VARIABLES, DATA STRUCTURES AND INPUT DATA : ORGANIZED BYTES IN MEMORY

LOCATIONS AND VALUES

$$S = \sum_{i=0}^n x_i$$



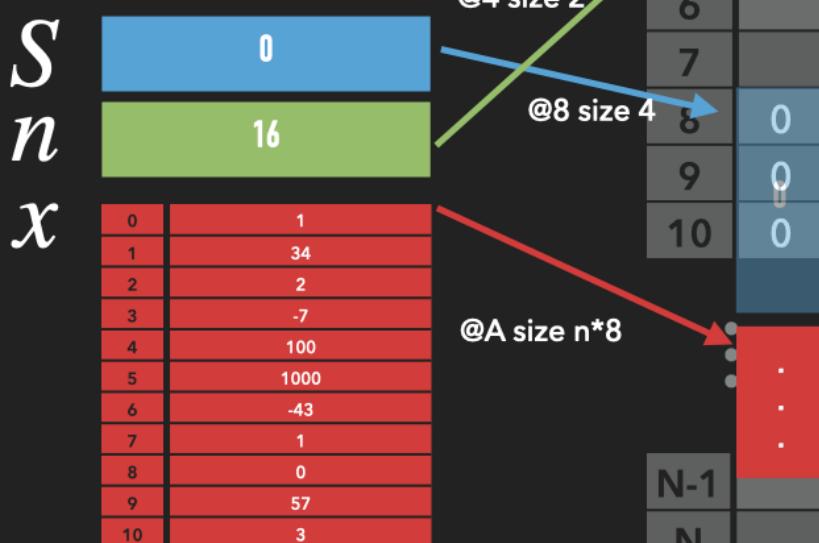
REGISTER FILE — THE ARRAY OF CPU REGISTER

	byte 7	byte 6	byte	byte	byte 3	byte 2	byte
PC							
R0							
R2							
R3							
R4							

VARIABLES, DATA STRUCTURES AND INPUT DATA : ORGANIZED BYTES IN MEMORY

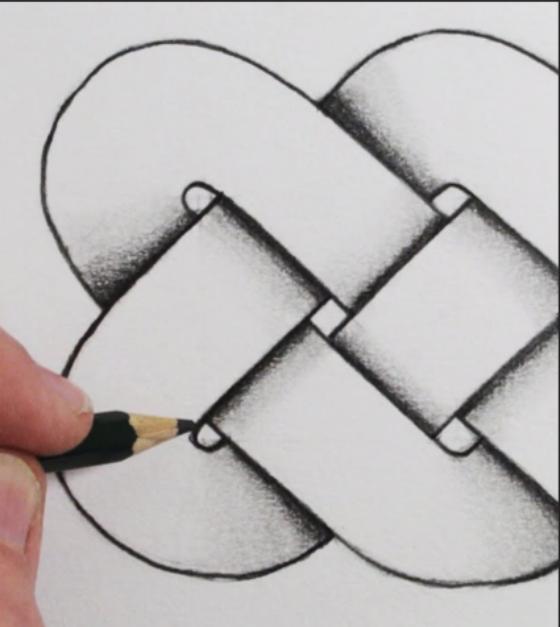
LOCATIONS AND VALUES

$$S = \sum_{i=0}^n x_i$$



REGISTER FILE — THE ARRAY OF CPU REGISTER

	byte 7	byte 6	byte	byte	byte 3	byte 2	byte
PC							
R0							
R2							
R3							
R4							

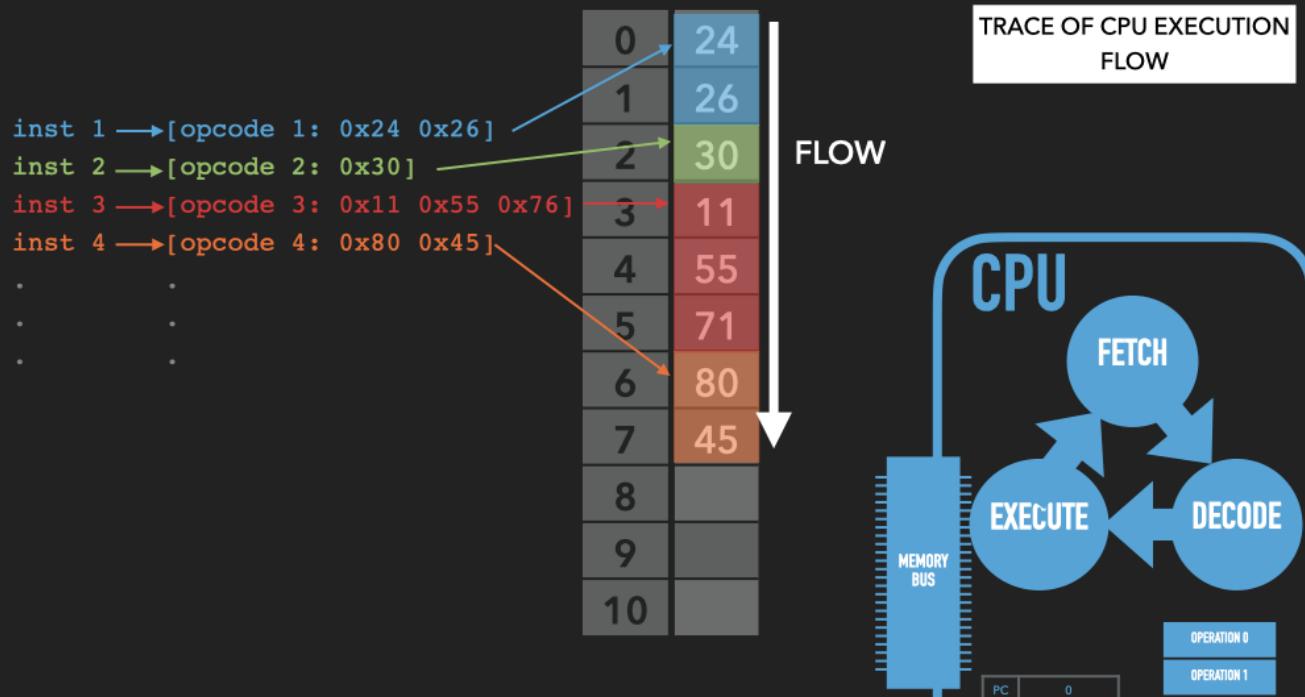


LEARN TO DRAW & VISUALIZE YOUR PROGRAMS

EVERYTHING MUST BE REPRESENTED IN MEMORY AND REGISTERS

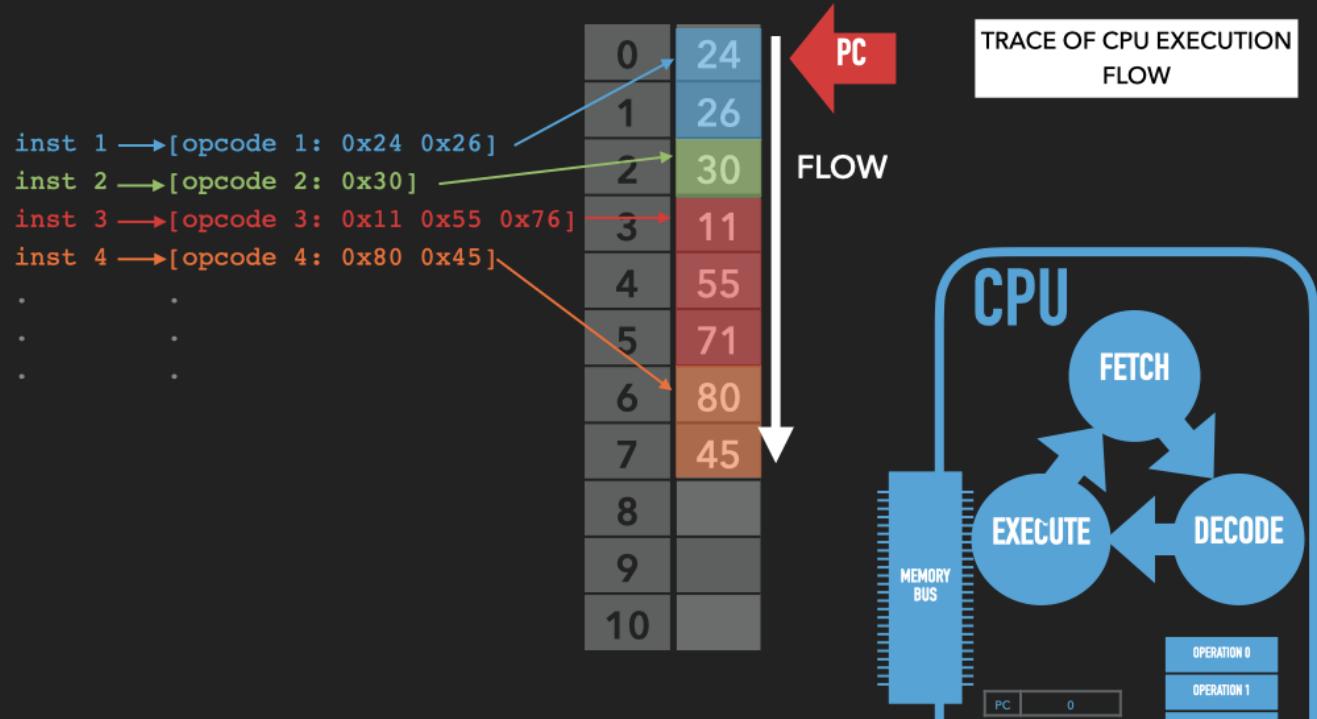
LOCATION AND SIZE: EVERYTHING HAS A SHAPE AND MOST OFTEN ARROWS CONNECTING THINGS

SIMPLE SEQUENCE: — LINEAR LAYOUT — LINEAR “FLOW” OF EXECUTION



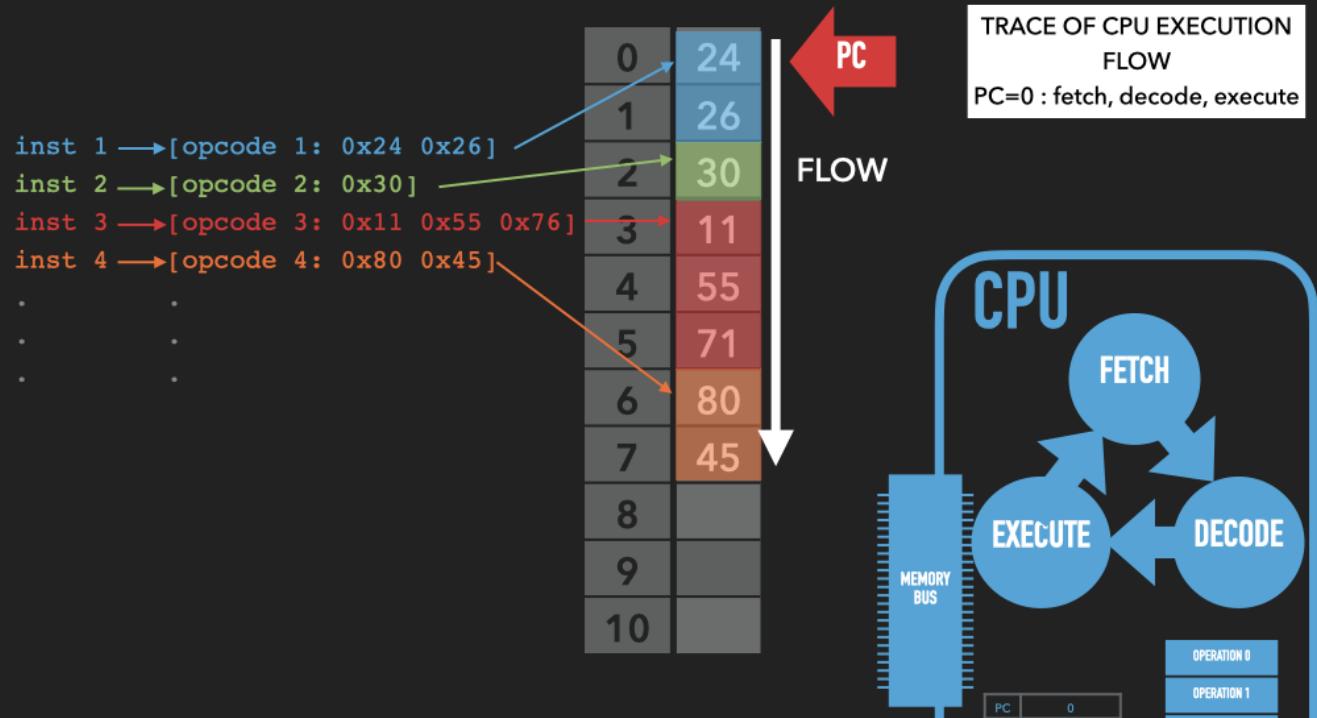
SIMPLE SEQUENCE:

- LINEAR LAYOUT
- LINEAR “FLOW” OF EXECUTION



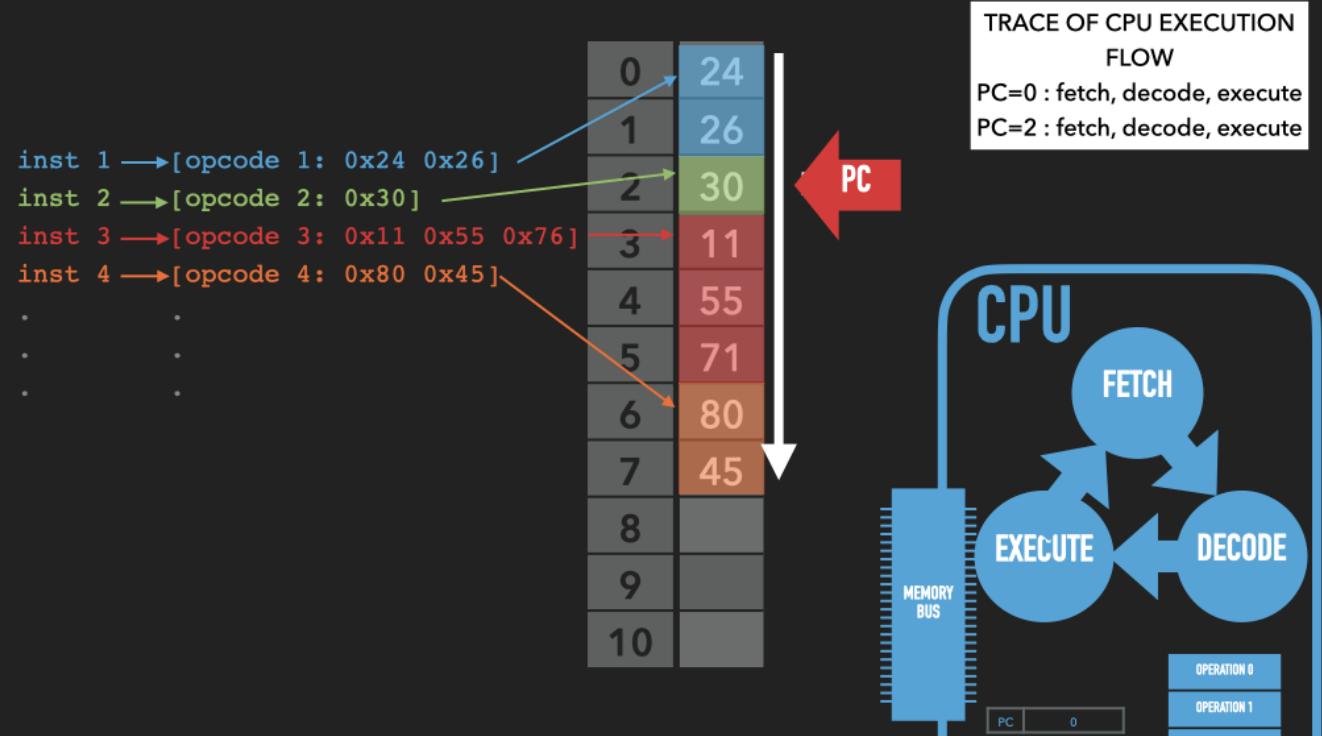
SIMPLE SEQUENCE:

- LINEAR LAYOUT
- LINEAR “FLOW” OF EXECUTION



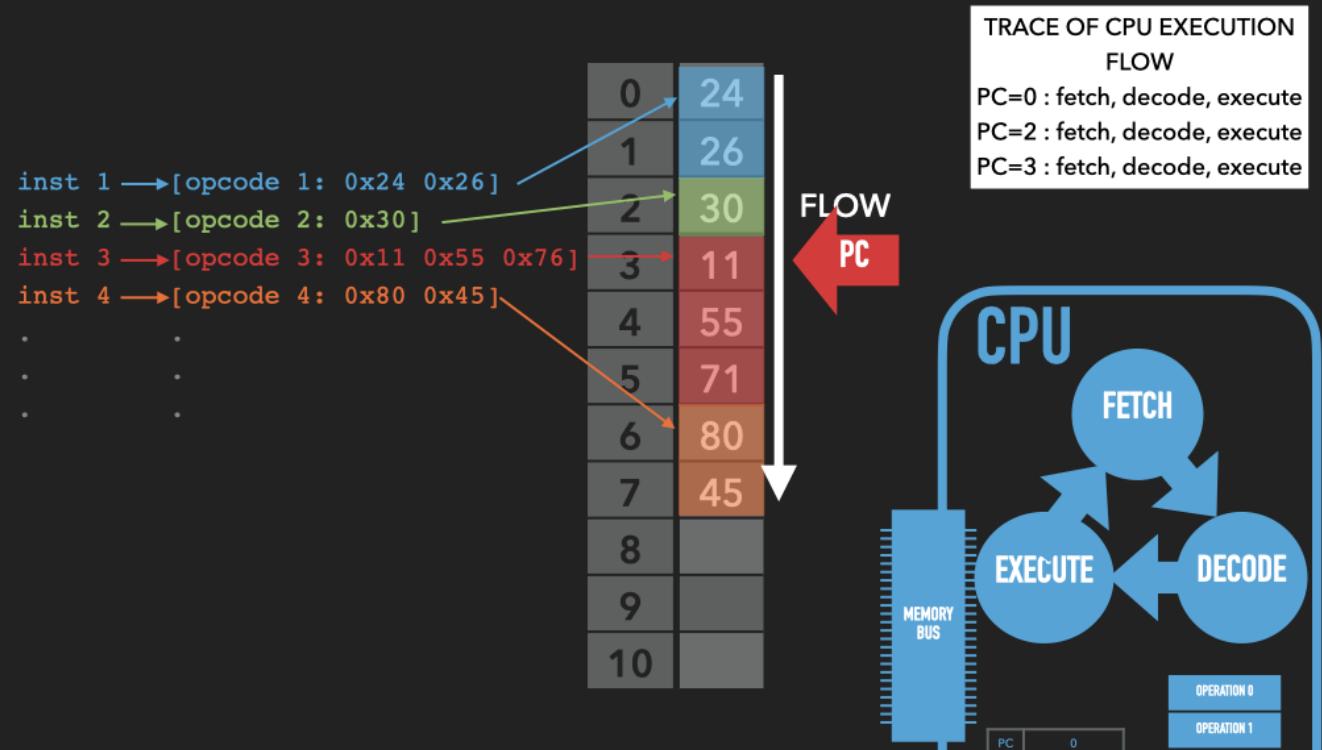
SIMPLE SEQUENCE:

- LINEAR LAYOUT
- LINEAR “FLOW” OF EXECUTION



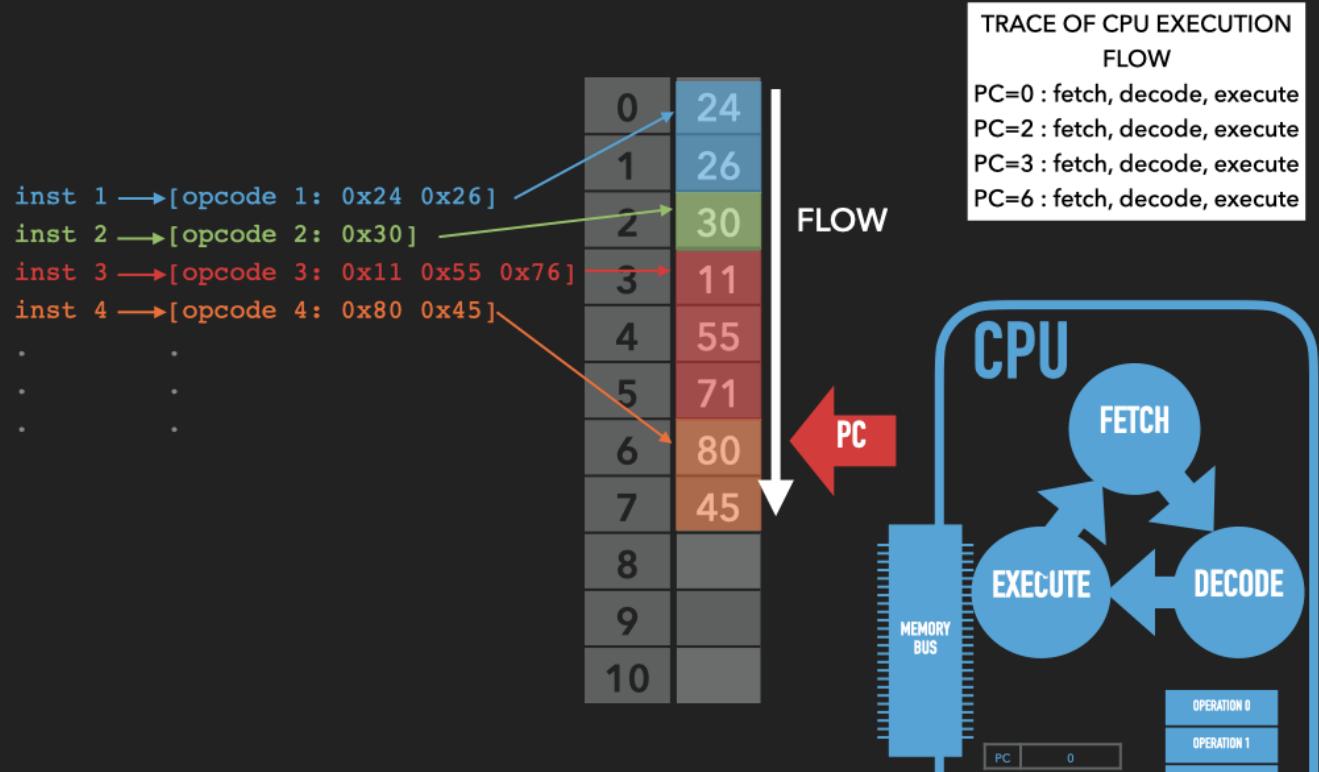
SIMPLE SEQUENCE:

- LINEAR LAYOUT
- LINEAR “FLOW” OF EXECUTION



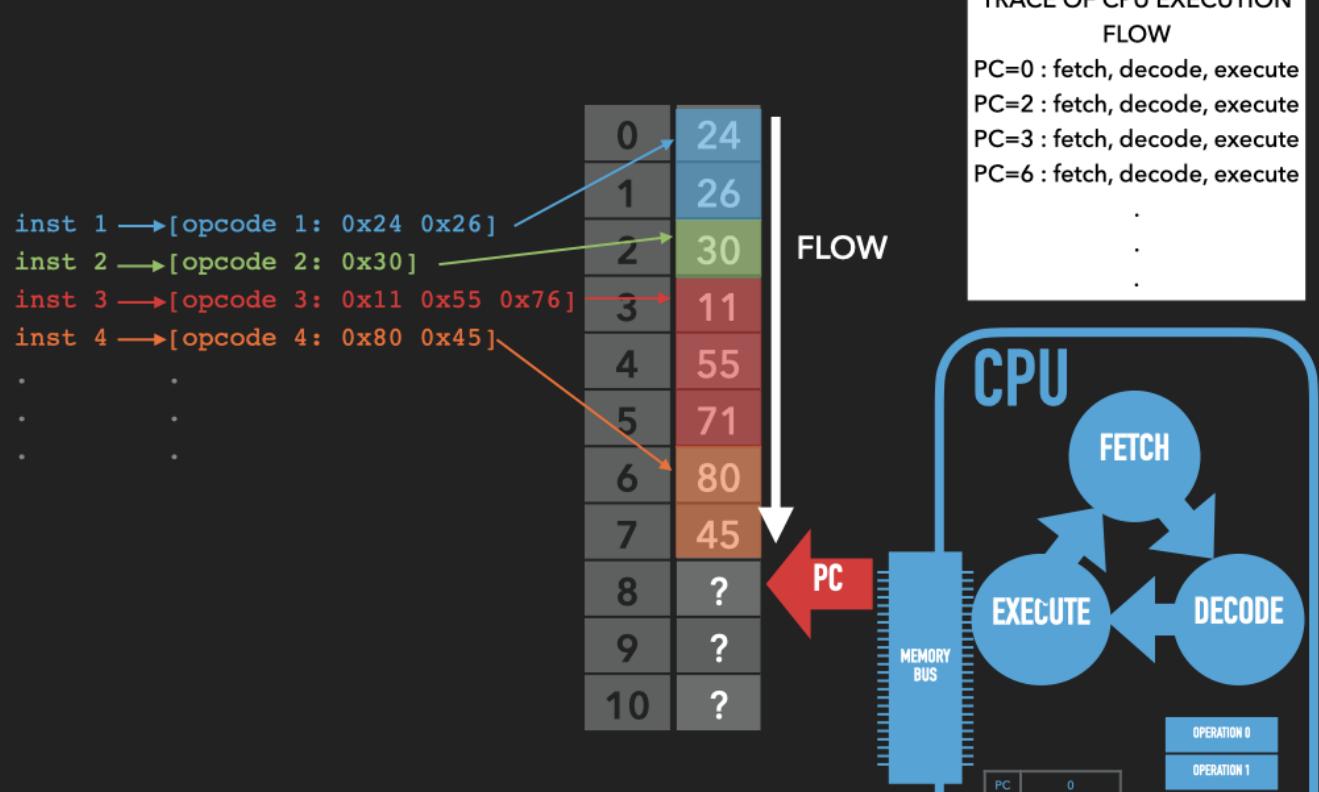
SIMPLE SEQUENCE:

- LINEAR LAYOUT
- LINEAR “FLOW” OF EXECUTION



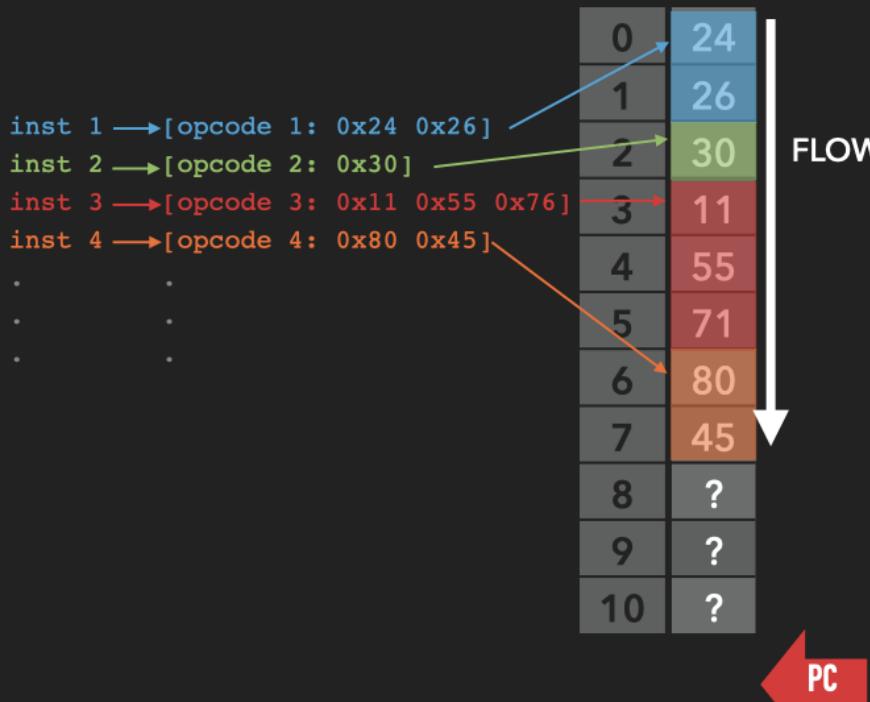
SIMPLE SEQUENCE:

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SIMPLE SEQUENCE:

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- LINEAR “FLOW” OF EXECUTION

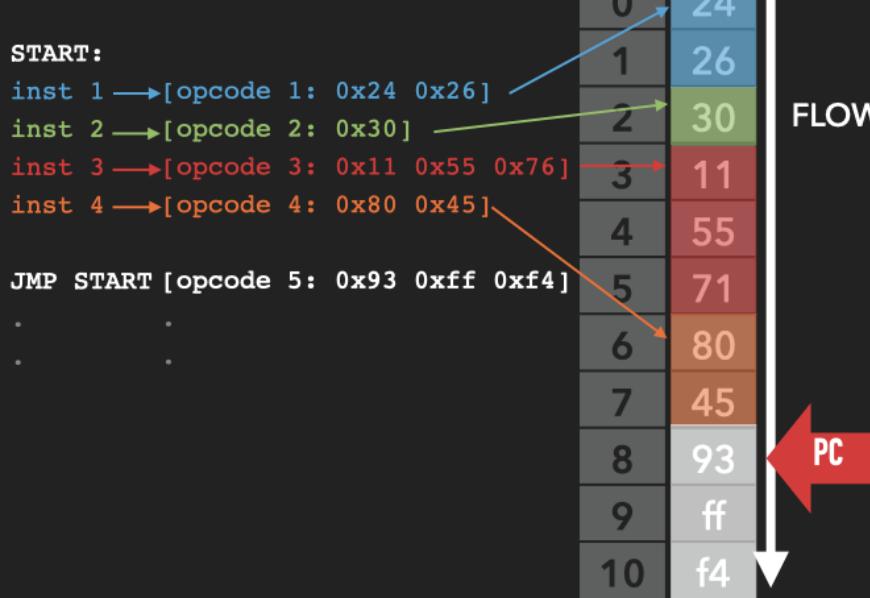


TRACE OF CPU EXECUTION FLOW

PC=0 : fetch, decode, execute
 PC=2 : fetch, decode, execute
 PC=3 : fetch, decode, execute
 PC=6 : fetch, decode, execute
 .
 .

REPEAT SEQUENCE:

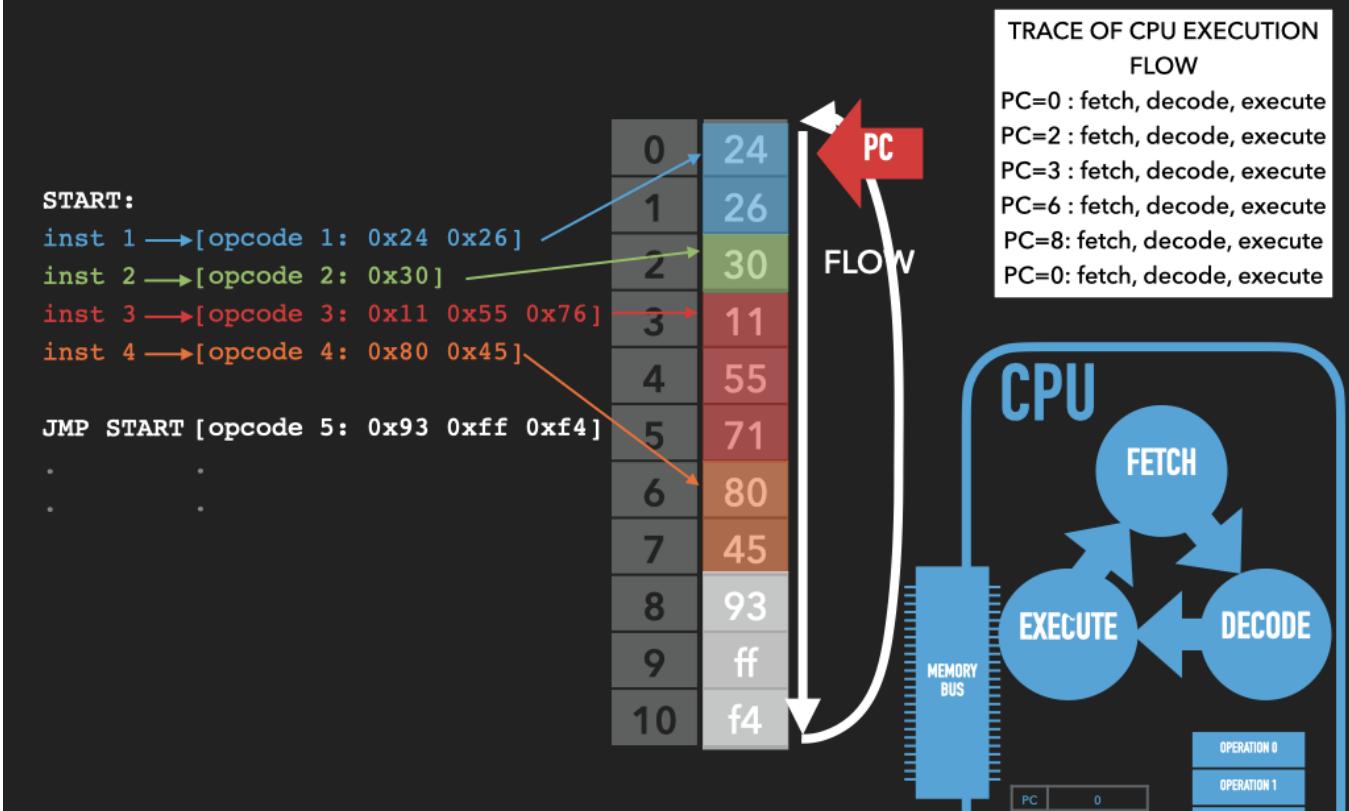
- JUMP BACKWARDS



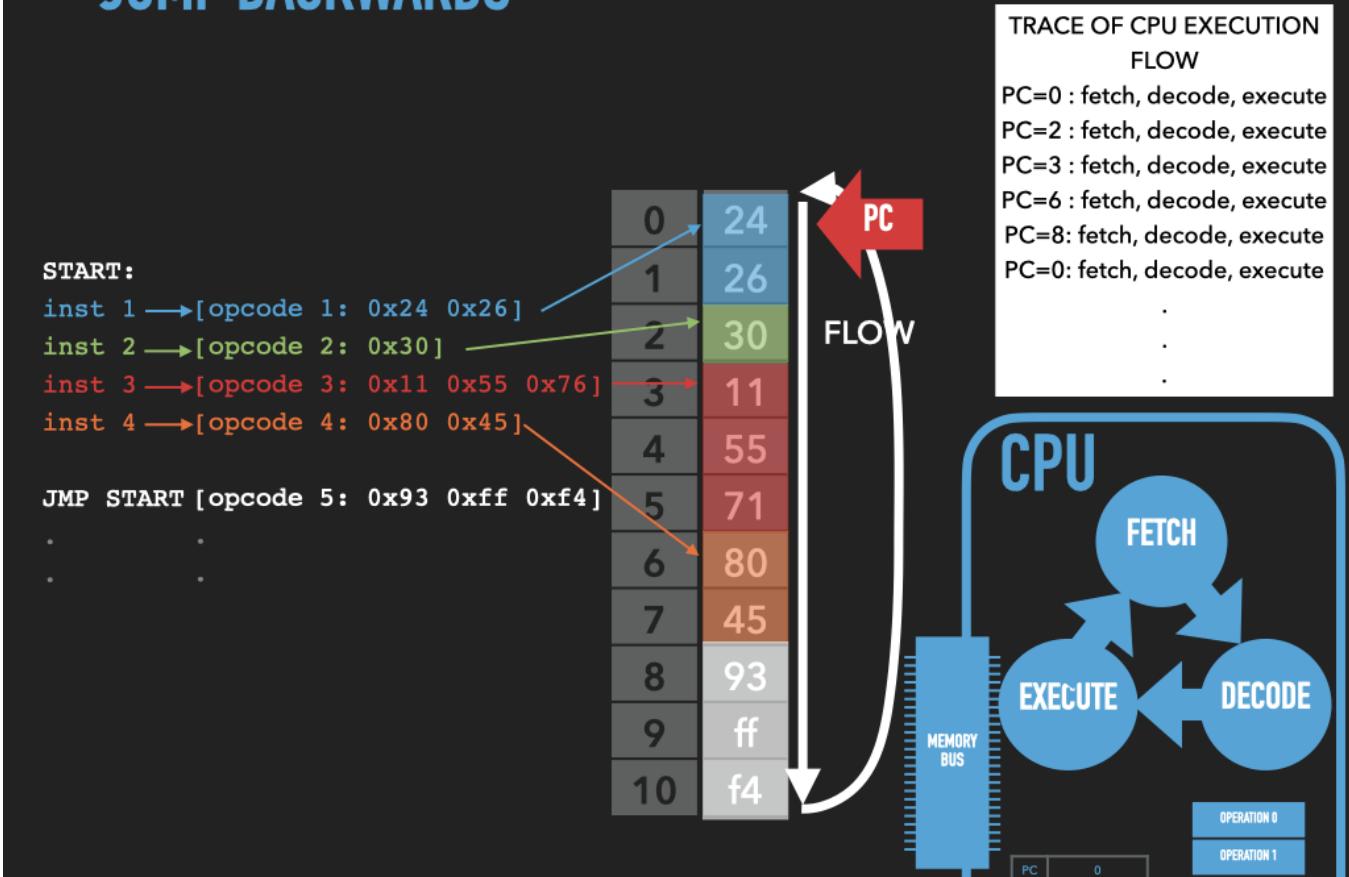
TRACE OF CPU EXECUTION FLOW

PC=0 : fetch, decode, execute
 PC=2 : fetch, decode, execute
 PC=3 : fetch, decode, execute
 PC=6 : fetch, decode, execute
 PC=8: fetch, decode, execute

REPEAT SEQUENCE: — JUMP BACKWARDS



REPEAT SEQUENCE: — JUMP BACKWARDS



CONDITIONS AND IF

— FORK FLOW : A VS B

— MOVE IF : CONDITIONAL MOVE

A

if ? then

B

else

C

D

CONDITIONS AND IF

— FORK FLOW : A VS B

A

if ? then

B

else

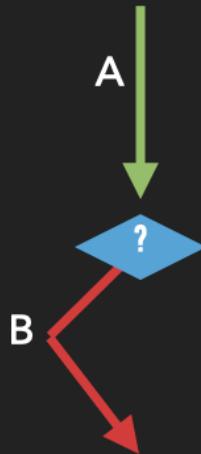
C

D



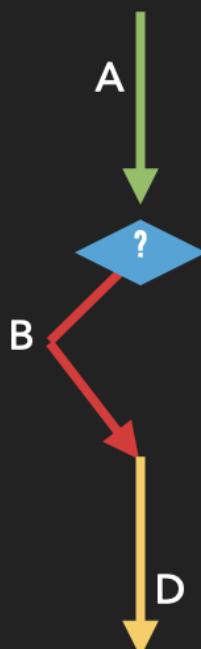
CONDITIONS AND IF — FORK FLOW : A VS B

A
if ? then
 B
else
 C
D



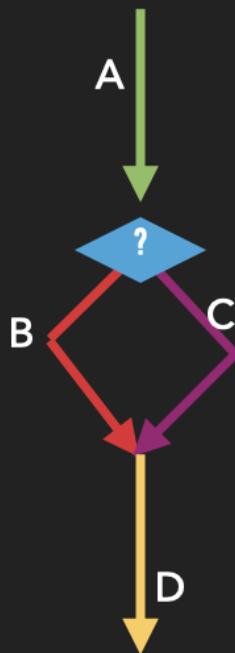
CONDITIONS AND IF — FORK FLOW : A VS B

A
if ? then
 B
else
 C
D



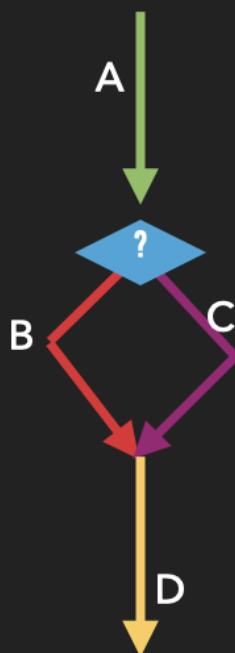
CONDITIONS AND IF — FORK FLOW : A VS B

A
if ? then
 B
else
 C
D



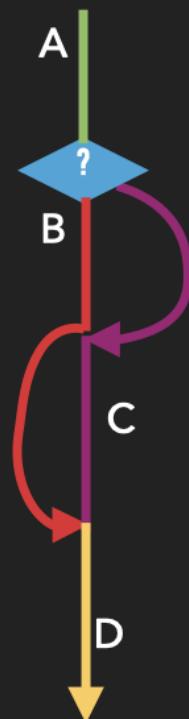
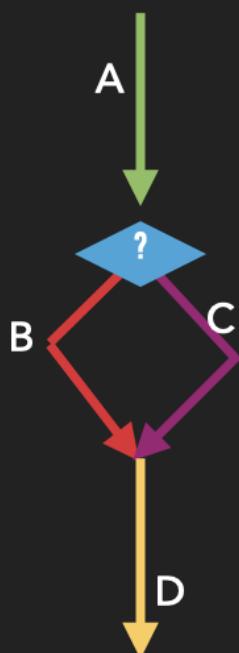
CONDITIONS AND IF — FORK FLOW : A VS B

A
if ? then
 B
else
 C
D



CONDITIONS AND IF — FORK FLOW : A VS B

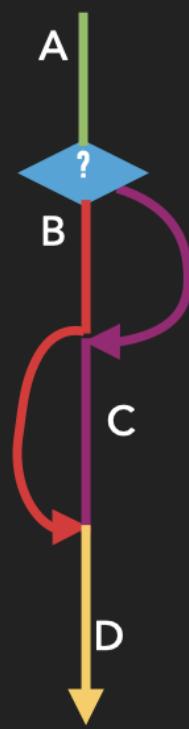
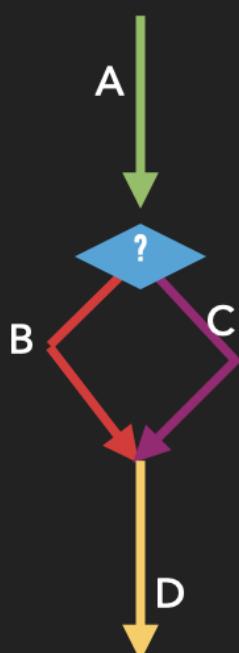
A
if ? then
 B
else
 C
D



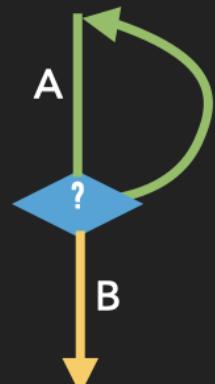
do
 A
while ?
 B

CONDITIONS AND IF — FORK FLOW : A VS B

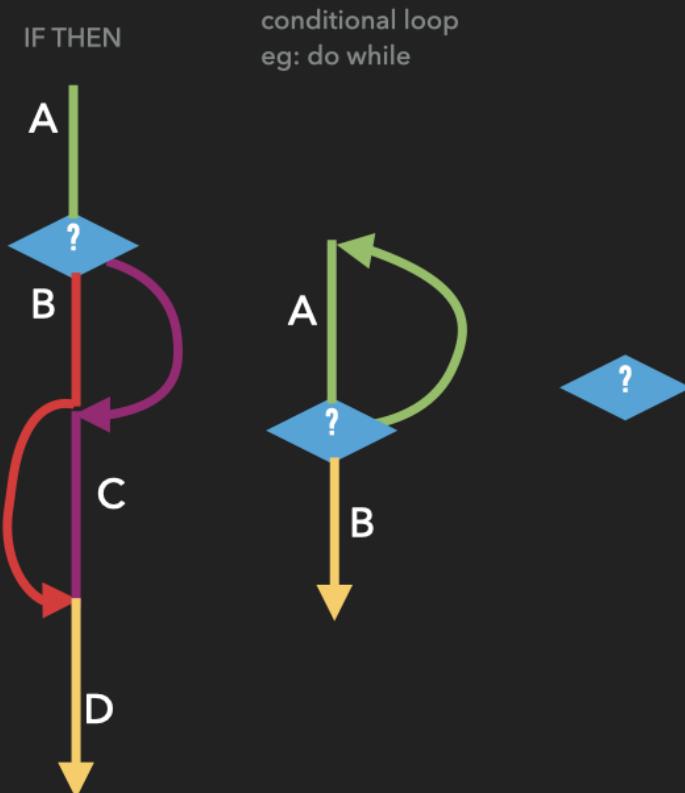
A
if ? then
 B
else
 C
D



do
 A
while ?
 B



IF CONDITION THEN-> 1) CONDITION 2) GOTO ELSE FALL THROUGH



- We implement with a pair of instructions that cooperate with a special set of single bit "condition" flags/registers

1. AN ALU INSTRUCTION
2. A CONDITIONAL JUMP INSTRUCTION

TEST, AND, CMP, SUB
J<CC>

IF CONDITION THEN-> 1) CONDITION 2) GOTO ELSE FALL THROUGH

- We implement with a pair of instructions that cooperate with a special set of single bit "condition" flags/registers

CONDITION FLAGS : BIT FIELDS OF EFLAGS

PC

1. AN ALU INSTRUCTION
2. A CONDITIONAL JUMP INSTRUCTION

CF overflow	OF Signed overflow	SF output is negative Sign flag	ZF output is zero
0	0	0	0

j|

- ALU : INSTRUCTIONS DO SOME EXTRA WORK: AFTER RESULT IS CALCULATE THEY WILL SET CONDITION
FLAGS: EG. SUB – RAX, RBX → RBX = RBX - RAX AND SET OF, SF, ZF, AF, PF, and :CF flags are set according to the result

IF CONDITION THEN-> 1) CONDITION 2) GOTO ELSE FALL THROUGH

- ▶ We implement with a pair of instructions that cooperate with a special set of single bit “condition” flags/registers

CONDITION FLAGS : BIT FIELDS OF EFLAGS

PC

1. SUB RBX, RAX
2. A CONDITIONAL JUMP INSTRUCTION

CF	OF	SF	ZF
0	0	0	1

RBX = RAX then 1

- ▶ ALU : INSTRUCTIONS DO SOME EXTRA WORK: AFTER RESULT IS CALCULATE THEY WILL SET CONDITION
FLAGS: EG. SUB RBX, RBA → RBX = RBX - RAX AND SET OF, SF, ZF, AF, PF, and CF flags are set according to the result

IF CONDITION THEN-> 1) CONDITION 2) GOTO ELSE FALL THROUGH

- ▶ We implement with a pair of instructions that cooperate with a special set of single bit “condition” flags/registers

CONDITION FLAGS : BIT FIELDS OF EFLAGS

PC

1. SUB RBX, RAX
2. A CONDITIONAL JUMP INSTRUCTION

check whichever flag

CF	OF	SF	ZF
0	0	0	1

- ▶ Conditional Jump instructions : $j<cc>$ jump (change the pc) if and only if a certain set of condition flags are set otherwise the pc is updated to the address of the opcode following the jump instruction in linear order eg we skip doing the jump
- ▶ see manual for the full list there are a lot of them!

IF CONDITION THEN-> 1) CONDITION 2) GOTO ELSE FALL THROUGH

- We implement with a pair of instructions that cooperate with a special set of single bit “condition” flags/registers

CONDITION FLAGS : BIT FIELDS OF EFLAGS

PC →
1. SUB RBX, RAX
2. JE <ADDR>

CF	OF	SF	ZF
0	0	0	1

- eg. JE – “Jump near if equal (ZF=1)” -- PC = <ADDR> else PC continues to address of next opcode as “usual”
- So that's it that's our “fork in execution flow”
- **JZ** is equivalent
- similarly JNE - “Jump near if not equal (ZF=0)” : JNZ equivalent

CONDITIONS AND IF — MOV IF

if ? {x=a} else no change to x

CONDITION FLAGS : BIT FIELDS OF EFLAGS

1. SUB RBX, RAX
2. CMOVEQ <ADDR>

CF	OF	SF	ZF
0	0	0	1

- “Move if equal (ZF=1)” else **DO NOTHING**. Similarly CMOVNE “Move if not equal (ZF=0). Remember Q just tells us the “size” of the mov

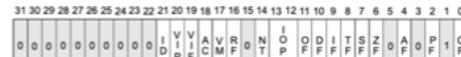
TEXT

ADD, SUB, IMUL, MUL, IDIV,
DIV, INC, DEC, NEG, CMP

ALU
AND, OR, NOT, XOR, SHL, SHR
TEST

CONTROL FLOW:

Many types of conditional jumps
predicated on eflag bits



X ID Flag (ID)
X Virtual Interrupt Pending (VIP)
X Virtual Interrupt Flag (VIF)
X Alignment Check / Access Control (AC)
X Virtual-8086 Mode (VM)
X Resume Flag (RF)
X Nested Task (NT)
X I/O Privilege Level (IOPL)

S Overflow Flag (OF)
C Direction Flag (DF)
X Interrupt Enable Flag (IF)

X Trap Flag (TF)
S Sign Flag (SF)
S Zero Flag (ZF)
S Auxiliary Carry Flag (AF)

S Parity Flag (PF)
S Carry Flag (CF)

S Indicates a Status Flag

C Indicates a Control Flag

X Indicates a System Flag

■ Reserved bit positions. DO NOT USE.
Always set to values previously read.

Figure 3-8. EFLAGS Register

As the IA-32 Architecture has evolved, flags have been added to the EFLAGS register, but the function and placement of existing flags have remained the same from one family of the IA-32 processors to the next. As a result, code that accesses or modifies these flags for one family of IA-32 processors works as expected when run on later families of processors.

3.4.3.1 Status Flags

The status flags (bits 0, 2, 4, 6, 7, and 11) of the EFLAGS register indicate the results of arithmetic instructions, such as the ADD, SUB, MUL, and DIV instructions. The status flag functions are:

CF (bit 0)

Carry flag — Set if an arithmetic operation generates a carry or a borrow out of the most-significant bit of the result; cleared otherwise. This flag indicates an overflow condition for unsigned-integer arithmetic. It is also used in multiple-precision arithmetic.

PF (bit 2)

Parity flag — Set if the least-significant byte of the result contains an even number of 1 bits; cleared otherwise.

AF (bit 4)

Auxiliary Carry flag — Set if an arithmetic operation generates a carry or a borrow out of bit 3 of the result; cleared otherwise. This flag is used in binary-coded decimal (BCD) arithmetic.

ZF (bit 6)

Zero flag — Set if the result is zero; cleared otherwise.

SF (bit 7)

Sign flag — Set equal to the most-significant bit of the result, which is the sign bit of a signed integer. (0 indicates a positive value and 1 indicates a negative value.)

OF (bit 11)

Overflow flag — Set if the integer result is too large a positive number or too small a negative number (excluding the sign-bit) to fit in the destination operand; cleared otherwise. This flag indicates an overflow condition for signed-integer (two's complement) arithmetic.

Of these status flags, only the CF flag can be modified directly, using the STC, CLC, and CMC instructions. Also the

Jcc—Jump if Condition Is Met

Opcode	Instruction	Opc/ En	64-Bit Mode	Compat/ Leg Mod	Description
77 cb	JNE rel8	D	Valid	Valid	jump short if above (CF=0 and ZF=0).
73 cb	JAE rel8	D	Valid	Valid	jump short if above or equal (CF=0).
72 cb	JBE rel8	D	Valid	Valid	jump short if below (CF=1).
76 cb	JBE rel8	D	Valid	Valid	jump short if below or equal (CF=1 or ZF=1).
72 cb	JC rel8	D	Valid	Valid	jump short if carry (F=1).
E3 cb	JCXZ rel8	D	N.E.	Valid	jump short if CX register is 0.
E3 cb	JECXZ rel8	D	Valid	Valid	jump short if ECX register is 0.
E3 cb	JRCXZ rel8	D	Valid	N.E.	jump short if RCX register is 0.
74 cb	JE rel8	D	Valid	Valid	jump short if equal (ZF=1).
7F cb	JGE rel8	D	Valid	Valid	jump short if greater (ZF=0 and SF=OF).
7D cb	JGE rel8	D	Valid	Valid	jump short if greater or equal (SF=OF).
7C cb	JL rel8	D	Valid	Valid	jump short if less (SF#OF).
7E cb	JLE rel8	D	Valid	Valid	jump short if less or equal (ZF=1 or SF#OF).
76 cb	JNA rel8	D	Valid	Valid	jump short if not above (CF=1 or ZF=1).
72 cb	JNAE rel8	D	Valid	Valid	jump short if not above or equal (CF=1).
73 cb	JNB rel8	D	Valid	Valid	jump short if not below (CF=0).
77 cb	JNBE rel8	D	Valid	Valid	jump short if not below or equal (CF=0 and ZF=0).
73 cb	JNC rel8	D	Valid	Valid	jump short if not carry (F=0).
75 cb	JNE rel8	D	Valid	Valid	jump short if not equal (ZF=0).
7E cb	JNG rel8	D	Valid	Valid	jump short if not greater (ZF=1 or SF#OF).
7C cb	JNGE rel8	D	Valid	Valid	jump short if not greater or equal (SF#OF).
7D cb	JNL rel8	D	Valid	Valid	jump short if not less (SF#OF).
7F cb	JNLE rel8	D	Valid	Valid	jump short if not less or equal (ZF=0 and SF#OF).
71 cb	JNO rel8	D	Valid	Valid	jump short if not overflow (OF=0).
7B cb	JNP rel8	D	Valid	Valid	jump short if not parity (PF=0).
79 cb	JNS rel8	D	Valid	Valid	jump short if not sign (SF=0).
75 cb	JNZ rel8	D	Valid	Valid	jump short if not zero (ZF=0).
70 cb	JO rel8	D	Valid	Valid	jump short if overflow (OF=1).
7A cb	JP rel8	D	Valid	Valid	jump short if parity (PF=1).
7A cb	JPE rel8	D	Valid	Valid	jump short if parity even (PF=1).
7B cb	JPO rel8	D	Valid	Valid	jump short if parity odd (PF=0).
78 cb	J5 rel8	D	Valid	Valid	jump short if sign (SF=1).
74 cb	JZ rel8	D	Valid	Valid	jump short if zero (ZF=1).
OF B7 cw	JAE rel16	D	N.S.	Valid	jump near if above (CF=0 and ZF=0). Not supported in 64-bit mode.
OF B7 cf	JAE rel32	D	Valid	Valid	jump near if above (CF=0 and ZF=0).
OF B3 cw	JAE rel16	D	N.S.	Valid	jump near if above or equal (CF=0). Not supported in 64-bit mode.

TEXT

DATA TRANSFER

cmov<cc> CONTROL FLOW: Many types of conditional jumps predicated on eflag bits

CMOVcc—Conditional Move

Opcode	Instruction	Op/En	64-Bit Mode	Compat/Leg Mode	Description
OF 47 //	CMOVE r16, r/m16	RM	Valid	Valid	Move if above (OF=0 and ZF=0).
OF 47 //	CMOVE r32, r/m32	RM	Valid	Valid	Move if above (OF=0 and ZF=0).
REXW + OF 47 //	CMOVE r64, r/m64	RM	Valid	N.E.	Move if above (CF=0 and ZF=0).
OF 43 //	CMOVEAE r16, r/m16	RM	Valid	Valid	Move if above or equal (OF=0).
OF 43 //	CMOVEAE r32, r/m32	RM	Valid	Valid	Move if above or equal (OF=0).
REXW + OF 43 //	CMOVEAE r64, r/m64	RM	Valid	N.E.	Move if above or equal (OF=0).
OF 42 //	CMOVEB r16, r/m16	RM	Valid	Valid	Move if below (CF=1).
OF 42 //	CMOVEB r32, r/m32	RM	Valid	Valid	Move if below (CF=1).
REXW + OF 42 //	CMOVEB r64, r/m64	RM	Valid	N.E.	Move if below (CF=1).
OF 46 //	CMOVEBE r16, r/m16	RM	Valid	Valid	Move if below or equal (OF=1 or ZF=1).
OF 46 //	CMOVEBE r32, r/m32	RM	Valid	Valid	Move if below or equal (OF=1 or ZF=1).
REXW + OF 46 //	CMOVEBE r64, r/m64	RM	Valid	N.E.	Move if below or equal (OF=1 or ZF=1).
OF 42 //	CMOVEC r16, r/m16	RM	Valid	Valid	Move if carry (CF=1).
OF 42 //	CMOVEC r32, r/m32	RM	Valid	Valid	Move if carry (CF=1).
REXW + OF 42 //	CMOVEC r64, r/m64	RM	Valid	N.E.	Move if carry (CF=1).
OF 44 //	CMOVE r16, r/m16	RM	Valid	Valid	Move if equal (ZF=1).
OF 44 //	CMOVE r32, r/m32	RM	Valid	Valid	Move if equal (ZF=1).
REXW + OF 44 //	CMOVE r64, r/m64	RM	Valid	N.E.	Move if equal (ZF=1).
OF 4F //	CMOVG r16, r/m16	RM	Valid	Valid	Move if greater (ZF=0 and SF=OF).
OF 4F //	CMOVG r32, r/m32	RM	Valid	Valid	Move if greater (ZF=0 and SF=OF).
REXW + OF 4F //	CMOVG r64, r/m64	RM	V/N.E.	NA	Move if greater (ZF=0 and SF=OF).
OF 4D //	CMOVGE r16, r/m16	RM	Valid	Valid	Move if greater or equal (SF=OF).
OF 4D //	CMOVGE r32, r/m32	RM	Valid	Valid	Move if greater or equal (SF=OF).
REXW + OF 4D //	CMOVGE r64, r/m64	RM	Valid	N.E.	Move if greater or equal (SF=OF).
OF 4C //	CMOVNL r16, r/m16	RM	Valid	Valid	Move if less (SF≠OF).
OF 4C //	CMOVNL r32, r/m32	RM	Valid	Valid	Move if less (SF≠OF).
REXW + OF 4C //	CMOVNL r64, r/m64	RM	Valid	N.E.	Move if less (SF≠OF).
OF 4E //	CMOVLE r16, r/m16	RM	Valid	Valid	Move if less or equal (ZF=1 or SF≠OF).
OF 4E //	CMOVLE r32, r/m32	RM	Valid	Valid	Move if less or equal (ZF=1 or SF≠OF).
REXW + OF 4E //	CMOVLE r64, r/m64	RM	Valid	N.E.	Move if less or equal (ZF=1 or SF≠OF).
OF 46 //	CMOVNA r16, r/m16	RM	Valid	Valid	Move if not above (CF=1 or ZF=1).
OF 46 //	CMOVNA r32, r/m32	RM	Valid	Valid	Move if not above (CF=1 or ZF=1).
REXW + OF 46 //	CMOVNA r64, r/m64	RM	Valid	N.E.	Move if not above (CF=1 or ZF=1).
OF 42 //	CMOVNAE r16, r/m16	RM	Valid	Valid	Move if not above or equal (CF=1).
OF 42 //	CMOVNAE r32, r/m32	RM	Valid	Valid	Move if not above or equal (CF=1).
REXW + OF 42 //	CMOVNAE r64, r/m64	RM	Valid	N.E.	Move if not above or equal (CF=1).
OF 43 //	CMOVNB r16, r/m16	RM	Valid	Valid	Move if not above or equal (CF=0).
OF 43 //	CMOVNB r32, r/m32	RM	Valid	Valid	Move if not above or equal (CF=0).
REXW + OF 43 //	CMOVNB r64, r/m64	RM	Valid	N.E.	Move if not below (CF=0).
OF 47 //	CMOVNBE r16, r/m16	RM	Valid	Valid	Move if not below or equal (CF=0 and ZF=0).

CMOVcc—Conditional Move

CMOVcc—Conditional Move

3-150 Vol. 2A

Vol. 2A 3-149

CMOVcc—Conditional Move

Vol. 2A 3-151

10.1. sumit.s and usesumit.s

10.1.1. Setup

- create a directory `mkdir sum; cd sum`
- create and write `sumit.s` and `usesumit.s` see below
- add a `Makefile` to automate assembling and linking
 - we are going run the commands by hand this time to highlight the details
- add our `setup.gdb` to make working in gdb easier
- normally you would want to track everything in git

10.1.2. Lets try and write a reusable routine

- lets assume that we have a symbol `XARRAY` that is the address of the data
- lets assume to use our routine you need to pass the length of the array
 - len in `rbx`
 - use `rdi` for loop index (`i`)
- let put the result in `rax`

Think about our objective in these terms

$$S = \sum_{i=0}^{n-1} x_i \rightarrow rax = \sum_{rdi=0}^{rbx-1} XARRAY[rdi]$$

right?

Ok remember the tricky part is realizing that it is up to us to implement the idea of an array.

- it is a data structure that we need to keep straight our head

10.1.2.1. To assemble `sumit.s` into `sumit.o`

```
as -g sumit.s -o sumit.o
```

10.1.3. So how might we use our “fragment”

Lets create a program that defines a `_start` routine and creates the memory locations that we can control.

Lets create `usesum.s`

Lets assume that

- will set aside enough memory for a maximum of 1000 values in where we set the `XARRAY` symbol
- we will allow the length actual length of data in `XARRAY` to be specified at a location marked by `XARRAY_LEN`.
- we will store the result in a location marked by the symbol `sum`

We will use our code by loading our data at `XARRAY`, updating `XARRAY_LEN`, executing the code and examining the result

1. The code should setup the memory we need
2. setup the registers as needed for `sumIt`
3. run `sumIt`
4. store the results at the location of `sum`

CODE: asm - usesum.s

```
.intel_syntax noprefix

.section .data
# a place for us to store how much data is in the XARRAY
# initialized it to 0
XARRAY_LEN:
.quad 0x0
# reserve enough space for 1024 8 byte values
# third argument is alignment.... turns out cpu
# cpu is more efficient if things are located at address
# of a particular 'alignment' (see intel manual)
.comm XARRAY, 8*1024, 8 - each Element
.comm sum, 8, 8 # space to store final sum
Element

.section .text
.global _start
_start:
    mov rbx, QWORD PTR [XARRAY_LEN]

    jmp sumIt
    mov QWORD PTR [sum], rax

    int3
```

10.1.3.1. To assemble `usesum.s` into `usesum.o`

```
as -g usesum.s -o usesum.o
```

10.1.3.2. To link `usesum.o` and `sumit.o` into an executable `usesum`

```
ld -g usesum.o sumit.o -o usesum
```

10.1.4. Lets make some data!

```
$ od -t d8 100randomnum.bin | head -10
00000000 6259685114560636175 -5631557134040358807
0000020 -4712855910177624953 -1255241704514375442
0000040 7845991343176347585 -329389044239553636
0000060 -2978603470776467133 -5260348793470561499
0000100 5985439629054967546 -2291256575101715932
0000120 5705005805913173539 -7574407545681432134
0000140 8170410682191702331 1406609228846829472
0000160 -96234991007374263 5830597432406181851
0000200 3243745949415779362 -3237505134039398800
0000220 -3990275624606574921 -2683132816410759618
```

10.1.5. How to run `usesum` and load data with gdb

```
gdb -x setup.gdb usesum
b _start
run
# restore lets us load memory from a file
restore 10num.bin binary &XARRAY
# set the number of elements
set {long long} & XARRAY_LEN = 10
# get address of XARRAY
p & XARRAY
# now use this address to display the element we are currently summing
# eg lets assume the prior command indicated that the address of XARRAY is 0x402010
display {long long}(0x402010 + ($rdi * 8))
# display the XARRAY_LEN and sum so we can see if and when they change
display {{long long} & XARRAY_LEN, {long long} & sum}
# now we can single step our way through or continue till we hit an int3
```

You can do the same now with the `100randomnum.bin` file. Eg. `restore 100randomnum.bin & XARRAY` and `set {long long} & XARRAY_LEN = 100`

10.2. This code has a problem that we will address in the next lecture *cannot go back*

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