DIGVIJAY BANSAL

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EDUCATION

BITS PILANI
B.E.(HONS.) Electrical & Electronics
Expected May 2019 | Pilani, India
Cum. GPA: 7.72/10

LAL BAHADUR SHASTRI SMARAK JAVM SR. SEC. SCHOOL
Class 12th
Graduated May 2014 | New Delhi, India
Grade: 95.2%

LINKS

Website:// **digvijay-bansal.github.io**
Github:// **bansaldigvijay**
LinkedIn:// **Digvijay Bansal**

COURSEWORK

COMPLETED
- Analog & Digital VLSI Design
- Microelectronic Circuits
- Electronic Devices
- Digital Design
- Signals and Systems
- Control Systems
- Microprocessors & Interfacing(x86)
- Fiber Optics & Optoelectronics
- Communications Systems

AUDITED
- Berkeleyx CS-191x Introduction to Quantum Mechanics and Quantum Computation
- PurdueX nano-535x Principles of Electronic Biosensors*
- MITx 3.15.1x Electronic Materials and Devices

*ongoing

SKILLS

TOOLS
- nanoMOS*
- Silvaco
- Cadence Virtuoso
- MATLAB
- LTSpice
- Microwind
- ModelSim
- Verilog

*nanoHUB.org

EXPERIENCE

ADANI POWER TRAINING AND RESEARCH INSTITUTE
Industrial Training
May 2017 – July 2017 | Gujarat, India
- Worked in Maintenance & Testing Division under the guidance of Mr. Ajit Kumar.
- Analyzed existing operation data for exploring possibilities of reducing losses during maintenance of Power Generators.
- Gained hands-on experience in Industrial Standard Testing procedures followed during overhauling of Power Generation Units.

MAJOR PROJECTS

SIMULATION OF ELECTROLYTES AND FDSOI ISFETS ON CONVENTIONAL TCAD SIMULATORS
Aug'2017–Present
- Working under the guidance of Dr. Soumendu Sinha and Prof. Dr. VK Chaubey.
- Developing techniques for modelling of electrolytes used in ISFETs as semiconductors to obtain I-V Characteristics.
- Performing Permittivity Variation Analysis at the sensing layer, Semiconductor - Electrolyte Interface of ISFETs.

[PROJECT REPORT].

ANALOG AND DIGITAL VLSI CIRCUIT DESIGN
Oct'2017
- Power and delay optimized Design of an 8:1 multiplexer using Transmission Gate logic style in Cadence Virtuoso.
- Implementation of the non-restoring algorithm for dividing a six-bit number by three-bit number in VHDL.
- Design of three-stage CMOS Operational Amplifier for given parameters i.e. unity gain bandwidth, gain and phase margin.

[PROJECT REPORT]

GENDER DETECTION USING DIGITAL SIGNAL PROCESSING
Oct'2017
- Implemented the FFT(Fast Fourier Transform) algorithm on the recorded voice signal to determine the fundamental frequency.
- Observed the effect of white noise on the fundamental frequency of recorded signal at a suitably low and high value of SNRs.

[PROJECT REPORT]

ORGANISATIONS

PUBLIC POLICY CLUB
CORE TEAM MEMBER | Aug 2016 - Present
- The work involves discussion on various government policies and brainstorming to generate innovative and practical solutions to the flaws in the policies.

ACHIEVEMENTS

- Awarded the iNSPIRE Scholarship by Dept. of Science & Technology, India for being in Top 1% in Class XII Exams.
- JEE Mains All India Rank - 8188 [13 Lakh Students had appeared for the exam.]