HW04 [ECE 720]

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Q1.

Solution:

Setting up the silicon compiler to run 'Rocket' design:

hw04/pdrm/dcrm/rm_setup/common_setup.tcl:

Modifications [in bold]

```
set DESIGN_NAME "Rocket"

set DESIGN_REF_DATA_PATH "../src/rtl/rocketchip_default" ;#

Absolute path prefix variable for library/design data.
...

set ADDITIONAL_SEARCH_PATH "../src/rtl/rocketchip_default" ;#

Additional search path to be added to the default search path
...
```

hw04/pdrm/dcrm/rm_setup/dc_setup.tcl:

```
set RTL_SOURCE_FILES {"rocketchip_default.v" "AsyncResetReg.v"
"plusarg_reader.v"};# Enter the list of source RTL files if reading from RTL
...
```

\$ cp hw04/pdrm/template/counter.constratints.tcl hw04/pdrm/template/Rocket.constratints.tcl

hw04/pdrm/template/icc2 common setup.tcl:

```
set DESIGN_NAME "Rocket" ;# Required; name of the design to be worked on; also used as the block name when scripts save or copy a block ...
```

hw04/pdrm/Makefile:

```
DESIGN=Rocket
```

```
CLK PER=5
UTIL=0.5
MAXLYR=met5
MAXTRANS=0.45
CLKUNCERT=0.2
```

hw04/pdrm/set constraints.py:

```
dest=open(f'src/rtl/rocketchip default/{design}.constraints.tcl','w')
```

Requirements:

[sufficient] viol_tot: viol_tot < 10

[sufficient] hold slack: hold_uncert + whs >= max_clk_trans

MAXLYR = met5; UTIL = 0.5 (constant) Observations:

Table: Minimize critical path delay by setting correct constraints and characterizing observed values as valid / not-valid

set con	straints:		observed statistics:			valid / not-valid:		
CLK _PER	MAX TRANS	CLK UNCERT	max_ clk_trans	hold_ uncert	whs	[sufficient] viol_tot	[sufficient] hold slack	crit path
5	0.45	0.2	0.19	0.2	0	9	0.2	5.06
5	0.5	0.2	0.21	0.2	-0.01	11	0.19	4.65
5	0.5	0.1	0.21	0.1	0	2	0.1	4.9
5	0.45	0.1	0.19	0.1	0	4	0.1	4.99
5	0.4	0.15	0.18	0.15	0	8	0.15	5.03
5	0.55	0.1	0.22	0.1	0	10	0.1	5.18
<u>5</u>	<u>0.45</u>	0.2	0.19	0.2	<u>0</u>	<u>1</u>	0.2	<u>5.27</u>
5	0.5	0.2	0.21	0.2	0	8	0.2	5.29
5	0.4	0.2	0.18	0.2	0	1	0.2	5.33
5	0.5	0.15	0.22	0.15	0	0	0.15	5.35
5	0.45	0.15	0.19	0.15	0	5	0.15	5.35
5	0.4	0.1	0.18	0.1	0	5	0.1	5.42

<u>5</u>	0.45	0.2	0.19	0.2	<u>0</u>	<u>3</u>	0.2	<u>5.46</u>
25	0.52	0.2	0.21	0.2	0	0	0.2	23.82
25	0.57	0.2	0.23	0.2	0	1	0.2	24.51
25	0.6	0.2	0.24	0.2	0	1	0.2	24.52
25	0.52	0.22	0.21	0.22	0	0	0.22	24.52
25	0.55	0.2	0.22	0.2	0	0	0.2	24.76
25	0.5	0.22	0.2	0.22	0	0	0.22	24.9
30	0.5	0.25	0.21	0.25	0	0	0.25	28.77
30	0.5	0.3	0.21	0.3	0	2	0.3	28.91
30	0.5	0.27	0.21	0.27	0	0	0.27	29.16
30	0.6	0.2	0.24	0.2	0	0	0.2	29.44
30	0.6	0.27	0.25	0.27	0	0	0.27	29.45
30	0.6	0.22	0.25	0.22	-0.01	0	0.21	29.46
30	0.57	0.25	0.23	0.25	0	1	0.25	29.52
30	0.57	0.27	0.23	0.27	-0.01	0	0.26	29.52
30	0.55	0.22	0.22	0.22	0	2	0.22	29.54
30	0.55	0.25	0.22	0.25	0	2	0.25	29.54
30	0.55	0.3	0.23	0.3	0	0	0.3	29.54
30	0.52	0.25	0.21	0.25	-0.01	0	0.24	29.55
30	0.52	0.2	0.23	0.2	-0.01	0	0.19	29.57
30	0.55	0.27	0.23	0.27	0	2	0.27	29.59
30	0.5	0.2	0.21	0.2	0	0	0.2	29.63
30	0.5	0.25	0.2	0.25	0	1	0.25	29.63
30	0.6	0.25	0.24	0.25	-0.01	2	0.24	29.63
30	0.5	0.22	0.2	0.22	-0.01	0	0.21	29.64
30	0.52	0.22	0.23	0.22	0	0	0.22	29.65
30	0.52	0.27	0.23	0.27	0	0	0.27	29.65

30	0.52	0.3	0.21	0.3	0	1	0.3	29.65
30	0.57	0.2	0.23	0.2	0	0	0.2	29.75
30	0.57	0.22	0.23	0.22	0	1	0.22	29.78
30	0.55	0.2	0.23	0.2	0	0	0.2	29.8

Result:

Constraints:

CLK_PER=5

UTIL=0.5

MAXLYR=met5

MAXTRANS=0.45

CLKUNCERT=0.2

Minimum critical path:

- 5.06 [best run]
 5.27 [2nd run with same constraints]
 5.46 [3rd run with same constraints]