VDF PROJECT PART 2

Problem Statement No.2

2. If C=6'o00 to 6'o14, BCD Counter

C=6'o15 to 6'o30, 1x8 Demux

C=6'o31 to 6'o46, 4 bit even parity generator

C=6'o47 to 6'o77, A+B[12:10]

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Interpretations

For utilization of 0.5

Step	Setup Slack	Hold Slack	No. of Cells	Area of Standard Cells	Power (mW)
Before Physical Design	3.692	-0.755	108	940.827	0.1114
After Placement	3.589	-0.186	108	940.827	0.1433
CTS Pre Optimisation	-	-	116	1013.489	0.1481
CTS Post Optimisation	3.596	0.037	121	1058.146	0.1517
After Detailed Routing	3.578	0.037	121	1058.146	0.1518

For utilization of 0.8

Step	Setup Slack	Hold Slack	No. of Cells	Area of Standard Cells	Power (mW)
Before Physical Design	3.692	-0.755	108	940.827	0.1114
After Placement	3.592	-0.187	108	940.827	0.1453
CTS Pre Optimisation	-	-	116	1013.489	0.1545
CTS Post Optimisation	3.572	0.038	119	1039.224	0.1575
After Detailed Routing	3.572	0.038	119	1039.224	0.1575

Interpretation of Results obtained in various steps of Physical Design:

- Timing slacks may change after every step of Physical Design. The placement tool is optimised for minimum wire length using and optimally chooses the location of input and output pins. This affects a change of Arrival Time from Before Physical Design to Placement.
- The **Worst path for timing slack need not be the same** throughout the physical design flow. Because of the wire estimates to a more accurate model, adding a more definitive clock path and its slew changes the critical path.
- The area of the Standard cells remains the same from before starting of physical design to the end of routing. In the steps, the tool optimally places the standard cells, adds buffers and takes care of the physical Routability of cells, but doesn't change or optimise the area of the cells used.
- **Area of other standard cells remains the same from Post Placement, and Post CTS steps**, this is highly intuitive. The standard cells, once placed, are not being modified in any of the steps. In the subsequent CTS and Routing steps, only connections are being made to the standard cells. While, there basic area and structure is never meddled with.
- **Addition of new components in CTS step**: After CTS, some new components have been added, such as buffers, inverters etc. These buffers are depicted in the change of area of standard cells. The CTS Step consists of two parts, first being the synthesis of

the Clock tree, while the second being the optimization of the clock tree synthesis. Now, the second step optimizes the design and handles and balances the skew. Generally, it adds buffers to resort the skew imbalance. This will also improve the timing violations. Further, the timings will be corrected in the routing stage.

Interpretation of Routability on the change in floorplan:

- In the 0.5 utilization the half area is reserved for the routing and in 0.8 utilization only one fifth of total area is reserved for the routing.
- Hence, in 0.5 Utilization, the tool does not use the M5-M7 for wiring (but uses it for pins). In contrast, 0.8 Utilization uses it for wiring.
- The **Routability is highly affected due to change of core utilization of the floorplan**. The floorplan with large utilization results into a denser layout, with closely packed interconnects, and hence, consequently, a higher amount of parasitic. On the contrary, the wire length is also small.

Before starting Physical Design

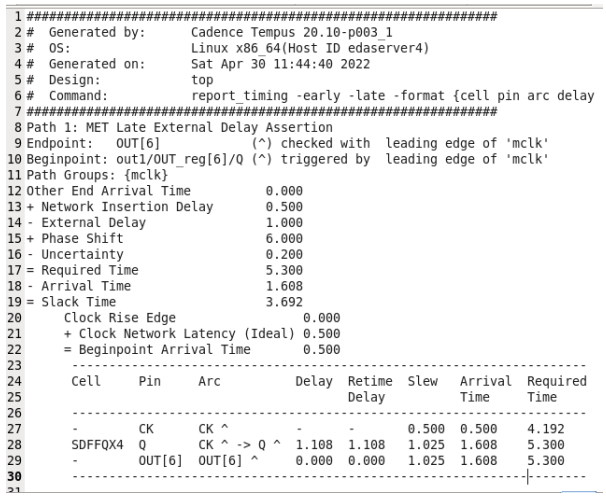
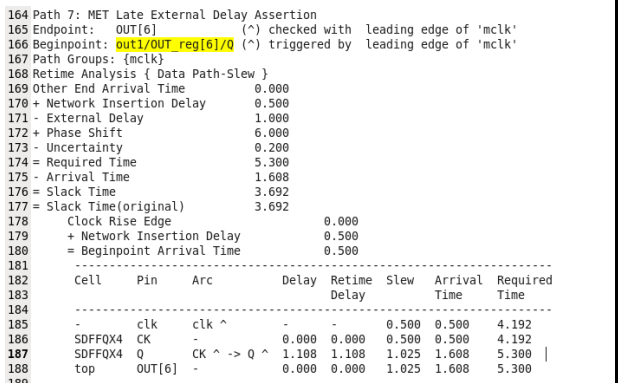
Timing Report of Worst Path

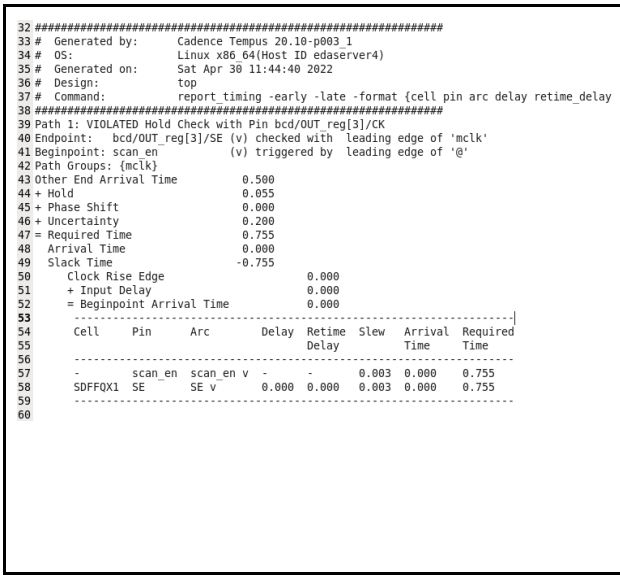
- **Before Physical Design**

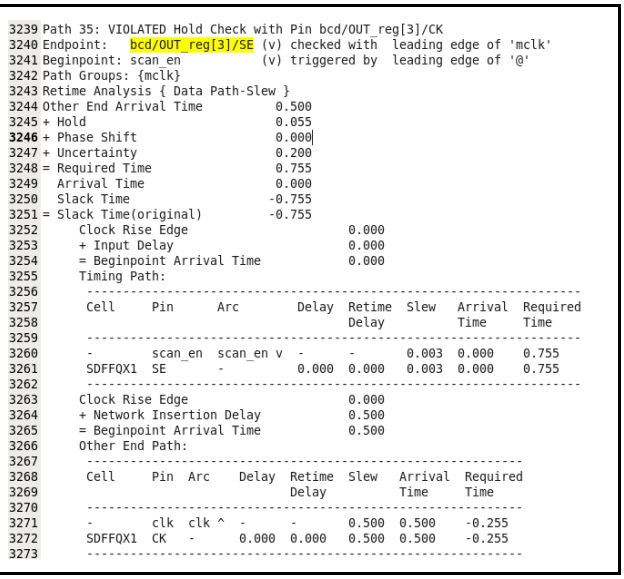
Here for the analysis synthesized netlist of intermediate case in DFT has been used.

GBA/PBA

- In Graph Based Analysis (GBA) in the path maximum slew and delay are considered, In GBA the worst slew propagation is ON, and the timing engine computes the worst-case delays of all standard cells assuming the worst-case slew for all the inputs of a gate.
- Where as in PBA (path-based analysis) the tool takes into account the actual slew for the arcs encountered while traversing any particular timing path.

GBA	PBA
	





Reason for their same slack values is: -

- Both PBA and GBA considers same path of AT and slew. This is because in the path which was considered by PBA, we got the maximum slew and the delay values from the constraint file.
- And as both are doing the analysis for same path, Hence slack values are also same.

- **Effect of Slew:**

GBA

```
#############################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 18:40:08 2022
#  Design:            top
#  Command:           report_timing -early -late -format {cell pin arc delay retime_delay
#############################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.405
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.895
- Arrival Time                  5.121
= Slack Time                    0.774
     Clock Rise Edge                     0.000
     + Input Delay                       1.000
     + Network Insertion Delay           0.500
     = Beginpoint Arrival Time           1.500
     ------------------------------------------------------------------------
     Cell      Pin  Arc          Delay  Retime  Slew    Arrival  Required
                                       Delay           Time     Time
     ------------------------------------------------------------------------
     -         rst  rst v        -      -       10.000  1.500    2.274
     NOR2XL    Y    B v -> Y ^   3.004  3.004   2.540   4.504    5.278
     AOI32X1   Y    B1 ^ -> Y v  0.275  0.275   0.673   4.779    5.553
     OAI211X1  Y    A1 v -> Y ^  0.199  0.199   0.220   4.978    5.752
     NOR2BXL   Y    AN ^ -> Y ^  0.143  0.143   1.866   5.121    5.895
     SDFFQX4   D    D ^          0.000  0.000   1.866   5.121    5.895
     ------------------------------------------------------------------------
```

PBA

```
Path 5: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Retime Analysis { Data Path-Slew }
Other End Arrival Time          0.500
- Setup                         0.223
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.077
- Arrival Time                  4.600
= Slack Time                    1.477
= Slack Time(original)          1.290
     Clock Rise Edge                     0.000
     + Input Delay                       1.000
     + Network Insertion Delay           0.500
     = Beginpoint Arrival Time           1.500
     Timing Path:
     ------------------------------------------------------------------------
     Cell      Pin  Arc          Delay  Retime  Slew    Arrival  Required
                                       Delay           Time     Time
     ------------------------------------------------------------------------
     -         rst  rst v        -      -       10.000  1.500    2.977
     NOR2XL    B    -            0.000  0.000   10.000  1.500    2.977
     NOR2XL    Y    B v -> Y ^   2.553  2.553   2.618   4.053    5.530
     NAND2XL   A    -            0.000  0.000   2.618   4.053    5.530
     NAND2XL   Y    A ^ -> Y v   0.304  0.304   0.529   4.357    5.834
     OAI211X1  C0   -            0.000  0.000   0.529   4.357    5.834
     OAI211X1  Y    C0 v -> Y ^  0.105  0.105   0.220   4.462    5.939
     NOR2BXL   AN   -            0.000  0.000   0.220   4.462    5.939
     NOR2BXL   Y    AN ^ -> Y ^  0.143  0.139   1.866   4.600    6.077
     SDFFQX4   D    -            0.000  0.000   1.866   4.600    6.077
     ------------------------------------------------------------------------
     Clock Rise Edge                     0.000
     + Network Insertion Delay           0.500
     = Beginpoint Arrival Time           0.500
     Other End Path:
     ------------------------------------------------------------
     Cell      Pin  Arc    Delay  Retime  Slew   Arrival  Required
                                 Delay           Time     Time
     ------------------------------------------------------------
     -         clk  clk ^  -      -       0.500  0.500    -0.977
     SDFFQX4   CK   -      0.000  0.000   0.500  0.500    -0.977
     ------------------------------------------------------------
```

- In the constraint file the slew of input transition of reset has been changed from 0.01 to 5.
- Now, GBA and PBA shows different setup slack for the critical path involving reset port so the difference in both the slack is due the fact that the data reaches late in GBA, and hence the arrival time will be more in GBA with respect to the setup analysis.

Effect of Load:

```
1 ############################################################
2 #  Generated by:      Cadence Tempus 20.10-p003_1
3 #  OS:                Linux x86_64(Host ID edaserver4)
4 #  Generated on:      Sat Apr 30 23:15:03 2022
5 #  Design:            top
6 #  Command:           report_timing -early -late -format {cell pin arc delay reti
7 ############################################################
8 Path 1: VIOLATED Setup Check with Pin out1/OUT_reg[4]/CK
9 Endpoint:   out1/OUT_reg[4]/SI (v) checked with  leading edge of 'mclk'
10 Beginpoint: out1/OUT_reg[3]/Q  (v) triggered by  leading edge of 'mclk'
11 Path Groups: {mclk}
12 Other End Arrival Time          0.500
13 - Setup                         3.438
14 + Phase Shift                   6.000
15 - Uncertainty                   0.200
16 = Required Time                 2.862
17 - Arrival Time                  6.968
18 = Slack Time                   -4.106
19      Clock Rise Edge                 0.000
20      + Clock Network Latency (Ideal) 0.500
21      = Beginpoint Arrival Time       0.500
22       -------------------------------------------------------------------
23       Cell     Pin  Arc          Delay  Retime  Slew   Arrival  Required
24                                         Delay          Time     Time
25       -------------------------------------------------------------------
26       -        CK   CK ^         -      -       0.500  0.500    -3.606
27       SDFFQX4  Q    CK ^ -> Q v  6.468  6.468   8.372  6.968    2.862
28       SDFFQX4  SI   SI v         0.000  0.000   8.372  6.968    2.862
29       -------------------------------------------------------------------
30
```

Delay on a given path depends on the load at the output pin of the device. For an accurate static timing analysis of a given design, it is important to set the load on the port which can be taken into account for delay calculations. As the load increases the delay will increase.

Effect Of Unateness

Unateness: is a very important property of timing arc, Unateness determines the relation between the two elements of timing arc. It is specified in the library.

Positive Unate: Transition on output same, as transition in input. Ex: buffer
Negative-Unate: Transition on output is opposite to transition in input. Ex: not gate
Non-Unate: No defined relation between transitions of input and output. Ex: XOR gate.

Area of Standard Cells:

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 05 2022  03:14:42 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================


   Gate    Instances   Area   Library
-------------------------------------
```

```
ADDFX1           2   39.359    slow
ADDHX1           1   12.110    slow
AND2XL           1    4.541    slow
AND3XL           1    6.055    slow
AOI21XL          1    4.541    slow
AOI31X1          1    6.055    slow
AOI32X1          2   13.624    slow
CLKINVX1         4    9.083    slow
CLKXOR2X1        1    8.326    slow
INVX1            2    4.541    slow
MXI2XL           2   12.110    slow
NAND2BX1         4   18.166    slow
NAND2XL         12   36.331    slow
NAND3X1          1    4.541    slow
NAND4XL          1    5.298    slow
NOR2BX1         15   68.121    slow
NOR2BXL          8   36.331    slow
NOR2XL          13   39.359    slow
NOR3BX1          1    6.055    slow
NOR3X1           1    4.541    slow
OAI211X1         3   15.895    slow
OAI21X1          1    4.541    slow
OAI2BB1X1        1    5.298    slow
OAI31X1          2   12.110    slow
SDFFQX1         17  347.417    slow
SDFFQX4          8  199.822    slow
XNOR2X1          1    8.326    slow
XNOR2XL          1    8.326    slow
----------------------------------------
total          108  940.827


    Type      Instances   Area  Area %
----------------------------------------
sequential           25 547.239   58.2
inverter              6  13.624    1.4
logic                77 379.964   40.4
physical_cells        0   0.000    0.0
----------------------------------------
total               108 940.827  100.0
```

```
 1 ============================================================
 2   Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
 3   Generated on:           Apr 05 2022  03:14:42 pm
 4   Module:                 top
 5   Technology library:     slow
 6   Operating conditions:   slow (balanced_tree)
 7   Wireload mode:          enclosed
 8   Area mode:              timing library
 9 ============================================================
10
11
12    Gate    Instances   Area   Library
13 ---------------------------------------
14 ADDFX1              2   39.359    slow
15 ADDHX1              1   12.110    slow
16 AND2XL              1    4.541    slow
17 AND3XL              1    6.055    slow
18 AOI21XL             1    4.541    slow
19 AOI31X1             1    6.055    slow
20 AOI32X1             2   13.624    slow
21 CLKINVX1            4    9.083    slow
22 CLKXOR2X1           1    8.326    slow
23 INVX1               2    4.541    slow
24 MXI2XL              2   12.110    slow
25 NAND2BX1            4   18.166    slow
26 NAND2XL            12   36.331    slow
27 NAND3X1             1    4.541    slow
28 NAND4XL             1    5.298    slow
29 NOR2BX1            15   68.121    slow
30 NOR2BXL             8   36.331    slow
31 NOR2XL             13   39.359    slow
32 NOR3BX1             1    6.055    slow
33 NOR3X1              1    4.541    slow
34 OAI211X1            3   15.895    slow
35 OAI21X1             1    4.541    slow
36 OAI2BB1X1           1    5.298    slow
37 OAI31X1             2   12.110    slow
38 SDFFQX1            17  347.417    slow
39 SDFFQX4             8  199.822    slow
40 XNOR2X1             1    8.326    slow
41 XNOR2XL             1    8.326    slow
42 ---------------------------------------
```

```
42 ----------------------------------------
43 total             108  940.827
44
45
46
47      Type       Instances   Area  Area %
48 ----------------------------------------
49 sequential             25 547.239   58.2
50 inverter                6  13.624    1.4
51 logic                  77 379.964   40.4
52 physical_cells          0   0.000    0.0
53 ----------------------------------------
54 total                 108 940.827  100.0
```

Power

```
 1 Instance: /top
 2 Power Unit: W
 3 PDB Frames: /stim#0/frame#0
 4   ------------------------------------------------------------------------
 5     Category         Leakage     Internal    Switching        Total    Row%
 6   ------------------------------------------------------------------------
 7        memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
 8     register     4.05387e-06  6.85854e-05  1.81588e-05  9.07981e-05  81.35%
 9        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
10        logic     1.73795e-06  9.46587e-06  3.98785e-06  1.51917e-05  13.61%
11         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
12        clock     0.00000e+00  0.00000e+00  5.62950e-06  5.62950e-06   5.04%
13          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
14           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
15   ------------------------------------------------------------------------
16     Subtotal     5.79182e-06  7.80513e-05  2.77762e-05  1.11619e-04 100.00%
17   Percentage           5.19%       69.93%       24.88%      100.00% 100.00%
18   ------------------------------------------------------------------------
```

Utilization of 0.5

Floor planning is done with small utilization of 0.5 or considering large die area.

❖ **After Placement**

- "Placement" usually refers to the initial placement of the standard cells.
- After the cells are placed, they are not "locked"–they can be moved around by the tool during subsequent optimization steps. However, initial placement tries its best to place the cells optimally, obeying the floorplan constraints and using complex heuristics to minimize the parasitic delay caused by the connecting wires between cells and timing skew between synchronous elements (e.g. flip-flops, memories).
- Poor placement (as well as poor aspect ratio of the floorplan) can result in congestion of wires later on in the design, which may prevent successful routing.

Timing report of worst path:

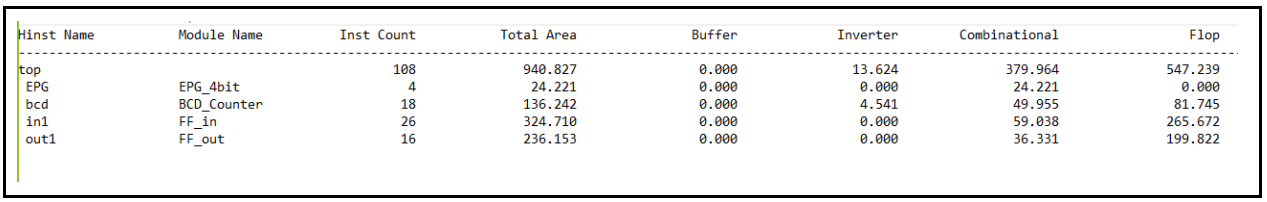
```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:55:28 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/placement/timi
#####################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
- Setup                         0.242
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.559
- Arrival Time                  1.970
= Slack Time                    3.589
     Clock Rise Edge                     0.000
     + Input Delay                       1.000
     = Beginpoint Arrival Time           1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.589 |
     | g1418           | A v -> Y ^  | INVX1     | 0.046 |   1.046 |    4.635 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.156 |   1.202 |    4.791 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.311 |   1.513 |    5.102 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.222 |   1.735 |    5.325 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.085 |   1.820 |    5.410 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.149 |   1.970 |    5.559 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.970 |    5.559 |
     +-------------------------------------------------------------------------+
```

- In the complete timing report, a total of 83 paths have been analyzed.
- Out of which, the worst set up slack has been reported by path 1 with start point as rst and end point as out1/OUT_reg[2]/D with a slack of 3.589.

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:55:28 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > report
timing_post_PnR_early.txt
#####################################################################
Path 1: VIOLATED Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                        -0.015
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.186
  Arrival Time                 0.000
  Slack Time                  -0.186
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------+
     |     Instance     |     Arc     |  Cell   | Delay | Arrival | Required |
     |                  |             |         |       |  Time   |   Time   |
     |------------------+-------------+---------+-------+---------+----------|
     |                  | DFT_sdi_2 v |         |       |   0.000 |    0.186 |
     | in1/C_reg_reg[2] | SI v        | SDFFQX1 | 0.000 |   0.000 |    0.186 |
     +-------------------------------------------------------------------------+
```

- In the hold report, 26 hold violations have been found.
- Out of which, the worst hold slack path has been reported above which is in path1 from start point DFT_sdi_2 and endpoint in1/C_reg_reg[2]/SI with a slack value of -0.186.
- Also here, it can be noted that Arrival Time has been assumed to be 0.000ns.
- However, this assumption will be proven wrong, when the clock path will be created by the CTS, and hence, buffers will be added, resulting in an increase in the Arrival Time and hence, an accurate measurement of hold violations.
- Hence. We are not much worried about these violations in this stage as these will get resolved in the subsequent stages.

Area of standard cells:



Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		108	940.827	0.000	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	18	136.242	0.000	4.541	49.955	81.745
in1	FF_in	26	324.710	0.000	0.000	59.038	265.672
out1	FF_out	16	236.153	0.000	0.000	36.331	199.822

The area of standard cells associated with post Placement step is given as follows.

Cell Type	Instance Count	Area per instance of cell(um^2)
MXI2XL	2	6.055200
NAND4XL	1	5.298300
AOI32X1	2	6.812100
AOI21XL	1	4.541400
NOR2BXL	8	4.541400
SDFFQX4	8	24.977700
NOR2XL	13	3.027600
INVX1	2	2.270700
NOR3X1	1	4.54140
AOI31X1	1	6.055200
NOR3BX1	1	6.055200
NOR2BX1	15	4.541400
ADDHX1	1	12.110400
NAND2XL	12	3.027600
NAND3X1	1	4.541400
ADDFX1	2	19.679400
XNOR2XL	1	8.325900
NAND2BX1	4	4.541400
CLKINVX1	4	2.270700

OAI31X1	2	6.055200
AND3XL	1	6.055200
OAI21X1	1	4.541400
AND2XL	1	4.541400
XNOR2X1	1	8.325900
SDFFQX1	17	20.436300
OAI211X1	3	5.298300
CLKXOR2X1	1	8.325900
OAI2BB1X1	1	5.125470

Power:

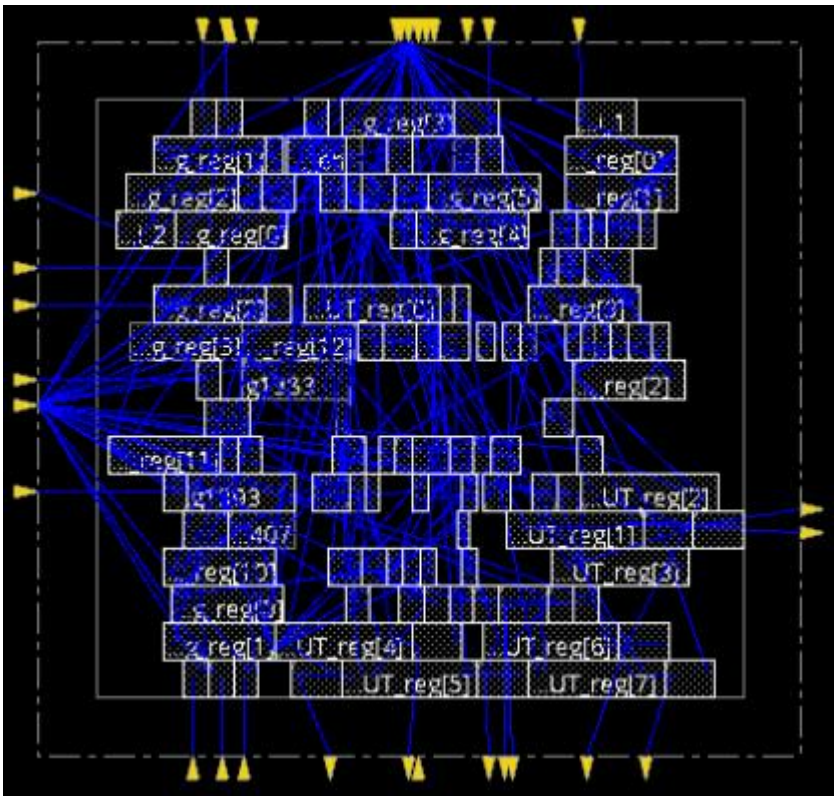
```
--------------------------------------------------------------------------------
Cell                 Internal  Switching    Total   Leakage  Cell
                     Power     Power        Power   Power    Name
--------------------------------------------------------------------------------
out1/OUT_reg[0]      0.004199  0.01005      0.01447 0.0002172 SDFFQX4
out1/OUT_reg[4]      0.003616  0.006076     0.009908 0.0002172 SDFFQX4
out1/OUT_reg[3]      0.003342  0.004556     0.008115 0.0002172 SDFFQX4
out1/OUT_reg[2]      0.003317  0.004442     0.007977 0.0002172 SDFFQX4
out1/OUT_reg[1]      0.003203  0.003848     0.007268 0.0002172 SDFFQX4
out1/OUT_reg[5]      0.003164  0.0035 0.006882 0.0002172 SDFFQX4
out1/OUT_reg[7]      0.002988  0.002454     0.005659 0.0002172 SDFFQX4
out1/OUT_reg[6]      0.002904  0.002044     0.005166 0.0002172 SDFFQX4
in1/A_reg_reg[1]     0.003081  0.00046950.003687 0.0001363 SDFFQX1
in1/A_reg_reg[2]     0.003081  0.000418     0.003636 0.0001363 SDFFQX1
bcd/OUT_reg[2]       0.003153  0.000324     0.003613 0.0001363 SDFFQX1
in1/A_reg_reg[0]     0.003084  0.00034110.003562 0.0001363 SDFFQX1
bcd/OUT_reg[1]       0.00313   0.0002393  0.003506 0.0001363 SDFFQX1
bcd/OUT_reg[3]       0.00313   0.0002049  0.003471 0.0001363 SDFFQX1
in1/A_reg_reg[3]     0.003079  0.00023280.003448 0.0001363 SDFFQX1
in1/C_reg_reg[5]     0.003068  0.00024360.003448 0.0001363 SDFFQX1
in1/B_reg_reg[11]    0.003082  0.00020820.003427 0.0001363 SDFFQX1
in1/B_reg_reg[12]    0.00308   0.0001836  0.0034  0.0001363 SDFFQX1
in1/C_reg_reg[4]     0.003041  0.00022060.003397 0.0001363 SDFFQX1
in1/B_reg_reg[10]    0.003102  0.0001417        0.00338  0.0001363 SDFFQX1
in1/C_reg_reg[0]     0.003083  0.000119     0.003338 0.0001363 SDFFQX1
in1/C_reg_reg[1]     0.003081  0.00011390.003331 0.0001363 SDFFQX1
bcd/OUT_reg[0]       0.002908  0.00026050.003305 0.0001363 SDFFQX1
in1/C_reg_reg[3]     0.002974  0.00019350.003303 0.0001363 SDFFQX1
in1/C_reg_reg[2]     0.002815  0.00013070.003082 0.0001363 SDFFQX1
g1402          0.0006632  0.0002313  0.0009163  2.186e-05 NOR3BX1
```

g1383	0.0005566	0.000204	0.000845	8.448e-05	ADDFX1
g1393	0.000523	0.0001602	0.0007676	8.448e-05	ADDFX1
g1409	0.0005292	0.0001769	0.0007264	2.034e-05	NOR3X1
g1407	0.0004127	0.000122	0.0006302	9.553e-05	ADDHX1
EPG/g40	0.0003694	0.0001248	0.0005668	7.254e-05	CLKXOR2X1
EPG/g39	0.0003691	0.0001189	0.0005586	7.055e-05	XNOR2X1
g1405	0.0002784	0.0002309	0.0005272	1.789e-05	AOI31X1
g1392	0.000321	0.0001348	0.0004743	1.851e-05	AOI32X1
EPG/g37	0.0002649	0.0001204	0.0003983	1.299e-05	OAI21X1
g1404	0.0001929	0.0001863	0.0003933	1.402e-05	OAI31X1
bcd/g210	0.0002528	4.592e-05	0.0003618	6.308e-05	XNOR2XL
g1415	0.000204	0.0001373	0.0003537	1.236e-05	NOR2XL
bcd/g219	0.0001512	0.0001631	0.0003493	3.499e-05	NAND2BX1
g1406	0.0001588	0.0001583	0.0003294	1.236e-05	NOR2XL
g1384	0.0002386	6.902e-05	0.0003218	1.41e-05	OAI211X1
g1410	0.0001814	8.229e-05	0.0002987	3.499e-05	NAND2BX1
g1408	0.0001519	0.0001279	0.0002928	1.301e-05	CLKINVX1
g1381	0.0002092	4.828e-05	0.0002845	2.704e-05	MXI2XL
g1397	0.0001107	0.0001504	0.0002704	9.289e-06	NAND2XL
bcd/g221	0.000186	4.788e-05	0.0002609	2.704e-05	MXI2XL
in1/g21	0.000201	3.919e-05	0.0002602	2.004e-05	NOR2BX1
in1/g18	0.000201	3.909e-05	0.0002601	2.004e-05	NOR2BX1
in1/g23	0.000201	3.858e-05	0.0002596	2.004e-05	NOR2BX1
g1414	0.0001032	0.0001439	0.0002594	1.236e-05	NOR2XL
in1/g27	0.0002009	3.596e-05	0.0002569	2.004e-05	NOR2BX1
in1/g29	0.0002009	3.554e-05	0.0002565	2.004e-05	NOR2BX1
in1/g22	0.0002009	3.343e-05	0.0002543	2.004e-05	NOR2BX1
in1/g28	0.0002009	3.293e-05	0.0002538	2.004e-05	NOR2BX1
in1/g20	0.0002009	3.292e-05	0.0002538	2.004e-05	NOR2BX1
in1/g30	0.0002008	3.19e-05	0.0002528	2.004e-05	NOR2BX1
in1/g25	0.0002008	3.139e-05	0.0002522	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.044e-05	0.0002513	2.004e-05	NOR2BX1
in1/g24	0.0002008	2.988e-05	0.0002507	2.004e-05	NOR2BX1
in1/g19	0.0002008	2.935e-05	0.0002502	2.004e-05	NOR2BX1
bcd/g213	0.0001852	4.237e-05	0.0002397	1.22e-05	AOI21XL
bcd/g226	0.000125	8.979e-05	0.0002279	1.301e-05	CLKINVX1
out1/g12	0.0001721	3.616e-05	0.0002249	1.662e-05	NOR2BXL
bcd/g218	0.0001648	4.477e-05	0.000222	1.236e-05	NOR2XL
bcd/g224	0.0001182	9.035e-05	0.0002216	1.301e-05	INVX1
g1419	0.0001277	7.776e-05	0.0002184	1.301e-05	CLKINVX1
g1403	9.174e-05	0.0001121	0.0002162	1.236e-05	NOR2XL
bcd/g217	0.0001495	4.834e-05	0.0002102	1.236e-05	NOR2XL
g1382	9.657e-05	9.93e-05	0.0002089	1.301e-05	CLKINVX1
g1401	9.814e-05	8.258e-05	0.0001958	1.511e-05	NAND3X1
g1379	0.0001339	3.511e-05	0.0001903	2.127e-05	OAI2BB1X1
bcd/g211	0.0001353	3.72e-05	0.0001848	1.236e-05	NOR2XL
g1385	0.0001336	3.7e-05	0.0001847	1.41e-05	OAI211X1
bcd/g208	0.000125	3.586e-05	0.0001732	1.236e-05	NOR2XL
EPG/g38	8.941e-05	7.384e-05	0.0001725	9.289e-06	NAND2XL
g1396	0.0001021	4.645e-05	0.0001609	1.236e-05	NOR2XL

g1418	7.865e-05	6.642e-05	0.0001581	1.301e-05	INVX1
g1411	4.598e-05	7.5e-05	0.000156	3.499e-05	NAND2BX1
g1376	0.0001064	3.511e-05	0.0001556	1.41e-05	OAI211X1
g1417	4.853e-05	9.722e-05	0.000155	9.289e-06	NAND2XL
out1/g14	0.000112	2.31e-05	0.0001517	1.662e-05	NOR2BXL
bcd/g215	0.0001083	2.567e-05	0.0001463	1.236e-05	NOR2XL
g1380	8.769e-05	3.308e-05	0.0001393	1.851e-05	AOI32X1
out1/g17	9.756e-05	2.485e-05	0.000139	1.662e-05	NOR2BXL
bcd/g222	5.028e-05	7.413e-05	0.0001337	9.289e-06	NAND2XL
out1/g16	9.086e-05	2.507e-05	0.0001326	1.662e-05	NOR2BXL
g1412	6.579e-05	2.876e-05	0.0001069	1.236e-05	NOR2XL
g1398	4.173e-05	4.895e-05	9.997e-05	9.289e-06	NAND2XL
g1390	4.324e-05	1.969e-05	9.792e-05	3.499e-05	NAND2BX1
g1395	4.876e-05	3.369e-05	9.174e-05	9.289e-06	NAND2XL
g1399	4.495e-05	3.614e-05	9.038e-05	9.289e-06	NAND2XL
bcd/g216	4.646e-05	2.36e-05	8.242e-05	1.236e-05	NOR2XL
bcd/g220	4.072e-05	2.999e-05	8.118e-05	1.046e-05	NAND4XL
g1400	3.618e-05	3.488e-05	8.035e-05	9.289e-06	NAND2XL
g1413	3.521e-05	1.662e-05	7.716e-05	2.533e-05	AND3XL
g1394	4.208e-05	2.176e-05	7.62e-05	1.236e-05	NOR2XL
g1416	4.224e-05	2.389e-05	7.542e-05	9.289e-06	NAND2XL
g1387	2.424e-05	2.006e-05	5.359e-05	9.289e-06	NAND2XL
g1377	2.004e-05	1.788e-05	4.72e-05	9.289e-06	NAND2XL
g1378	2.474e-05	5.16e-06	4.392e-05	1.402e-05	OAI31X1
out1/g15	1.585e-05	3.071e-06	3.555e-05	1.662e-05	NOR2BXL
g1391	1.074e-05	1.504e-06	3.228e-05	2.004e-05	NOR2BX1
g1388	5.389e-06	1.425e-06	3.148e-05	2.466e-05	AND2XL
g1389	3.976e-06	6.025e-07	2.462e-05	2.004e-05	NOR2BX1
g1386	7.958e-06	6.731e-06	2.398e-05	9.289e-06	NAND2XL
out1/g18	4.462e-06	9.052e-07	2.199e-05	1.662e-05	NOR2BXL
out1/g11	4.295e-06	9.052e-07	2.182e-05	1.662e-05	NOR2BXL
out1/g13	1.554e-06	3.749e-07	1.855e-05	1.662e-05	NOR2BXL
Total (108 of 108)	0.09123	0.04629	0.1433	0.005792	
Total Capacitance	4.592e-12 F***				

- **Total Power** reported here is = 0.1433mW.
- **Total capacitance** = 4.592e-12F

Layout Snapshot with Fly Lines:



❖ Clock Tree Synthesis Pre-Optimization

After the Clock Tree Synthesis (CTS) the real clock network gets created. There might be extra timing violations that may show up after CTS that needs to handled and fixed using further optimization techniques.

Area:

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		116	1013.489	72.662	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	18	136.242	0.000	4.541	49.955	81.745
in1	FF_in	26	324.710	0.000	0.000	59.038	265.672
out1	FF_out	23	299.732	63.580	0.000	36.331	199.822

Primitives:

Cell Type	Instance Count	Area per instance of cell(um^2)
MXI2XL	2	6.055200

NAND4XL	1	5.298300
AOI32X1	2	6.812100
AOI21XL	1	4.541400
NOR2BXL	8	4.541400
SDFFQX4	8	24.977700
NOR2XL	13	3.027600
INVX1	2	2.270700
NOR3X1	1	4.54140
AOI31X1	1	6.055200
NOR3BX1	1	6.055200
NOR2BX1	15	4.541400
ADDHX1	1	12.110400
NAND2XL	12	3.027600
NAND3X1	1	4.541400
ADDFX1	2	19.679400
XNOR2XL	1	8.325900
NAND2BX1	4	4.541400
CLKINVX1	4	2.270700
OAI31X1	2	6.055200
AND3XL	1	6.055200
OAI21X1	1	4.541400
CLKBUFX6	8	9.082800
AND2XL	1	4.541400
XNOR2X1	1	8.325900
SDFFQX1	17	20.436300

OAI211X1	3	5.298300
CLKXOR2X1	1	8.325900
OAI2BB1X1	1	5.424700

- Here, it is observed that in the CTS before optimization extra clock buffers have been added represented as CLKBUFX6 highlighted in the above image.
- **Total net length** = 1.605e+03 (7.561e+02 8.491e+02)

Power:

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Name
out1/FE_OFC0_OUT_0	0.001044	0.009961	0.01113	0.0001212	CLKBUFX6
out1/FE_OFC5_OUT_4	0.0006353	0.006059	0.006815	0.0001212	CLKBUFX6
out1/FE_OFC2_OUT_1	0.0004821	0.004612	0.005216	0.0001212	CLKBUFX6
out1/FE_OFC4_OUT_3	0.000467	0.004457	0.005045	0.0001212	CLKBUFX6
out1/OUT_reg[0]	0.0042	0.0001694	0.004586	0.0002172	SDFFQX4
out1/FE_OFC3_OUT_2	0.000376	0.003594	0.004091	0.0001212	CLKBUFX6
out1/FE_OFC6_OUT_5	0.0003665	0.003496	0.003984	0.0001212	CLKBUFX6
out1/OUT_reg[4]	0.003594	7.221e-05	0.003883	0.0002172	SDFFQX4
in1/A_reg_reg[1]	0.00308	0.0004682	0.003685	0.0001363	SDFFQX1
in1/A_reg_reg[2]	0.003081	0.0004173	0.003635	0.0001363	SDFFQX1
out1/OUT_reg[1]	0.00334	4.968e-05	0.003607	0.0002172	SDFFQX4
out1/OUT_reg[3]	0.00332	5.969e-05	0.003597	0.0002172	SDFFQX4
bcd/OUT_reg[3]	0.00315	0.0002816	0.003567	0.0001363	SDFFQX1
in1/A_reg_reg[0]	0.003083	0.00034	0.003559	0.0001363	SDFFQX1
bcd/OUT_reg[1]	0.003131	0.0002648	0.003532	0.0001363	SDFFQX1
bcd/OUT_reg[2]	0.003151	0.0002392	0.003526	0.0001363	SDFFQX1
in1/A_reg_reg[3]	0.003079	0.0002318	0.003447	0.0001363	SDFFQX1
in1/C_reg_reg[3]	0.003068	0.000228	0.003432	0.0001363	SDFFQX1
in1/B_reg_reg[11]	0.003082	0.0002074	0.003425	0.0001363	SDFFQX1
out1/OUT_reg[2]	0.00316	4.114e-05	0.003418	0.0002172	SDFFQX4
out1/OUT_reg[5]	0.003152	3.854e-05	0.003408	0.0002172	SDFFQX4
in1/B_reg_reg[12]	0.00308	0.0001818	0.003398	0.0001363	SDFFQX1
in1/C_reg_reg[5]	0.003041	0.000219	0.003396	0.0001363	SDFFQX1
in1/B_reg_reg[10]	0.003099	0.000141	0.003377	0.0001363	SDFFQX1
in1/C_reg_reg[0]	0.003083	0.0001188	0.003338	0.0001363	SDFFQX1
in1/C_reg_reg[1]	0.003081	0.0001135	0.00333	0.0001363	SDFFQX1
in1/C_reg_reg[4]	0.002974	0.0002088	0.003319	0.0001363	SDFFQX1
bcd/OUT_reg[0]	0.002909	0.0002603	0.003305	0.0001363	SDFFQX1
out1/OUT_reg[7]	0.00297	2.572e-05	0.003213	0.0002172	SDFFQX4
out1/OUT_reg[6]	0.002898	2.167e-05	0.003137	0.0002172	SDFFQX4
in1/C_reg_reg[2]	0.002815	0.0001424	0.003094	0.0001363	SDFFQX1
FE_OFC7_DFT_sdo_2	0.000253	0.002405	0.002779	0.0001212	CLKBUFX6
out1/FE_OFC1_OUT_6	0.0002137	0.002048	0.002383	0.0001212	CLKBUFX6

g1402	0.0006649	0.0002307	0.0009174	2.186e-05	NOR3BX1
g1383	0.0005561	0.0002046	0.0008452	8.448e-05	ADDFX1
g1393	0.0005221	0.0001592	0.0007658	8.448e-05	ADDFX1
g1409	0.0005167	0.0001709	0.0007079	2.034e-05	NOR3X1
g1407	0.0004113	0.0001213	0.0006281	9.553e-05	ADDHX1
EPG/g40	0.0003688	0.0001242	0.0005655	7.254e-05	CLKXOR2X1
EPG/g39	0.000369	0.0001187	0.0005583	7.055e-05	XNOR2X1
g1405	0.0002701	0.0002268	0.0005147	1.789e-05	AOI31X1
g1392	0.0003208	0.0001341	0.0004734	1.851e-05	AOI32X1
g1404	0.0001991	0.0001873	0.0004004	1.402e-05	OAI31X1
EPG/g37	0.0002649	0.00012	0.0003979	1.299e-05	OAI21X1
bcd/g210	0.000267	4.829e-05	0.0003783	6.308e-05	XNOR2XL
g1415	0.000204	0.0001372	0.0003536	1.236e-05	NOR2XL
bcd/g219	0.0001516	0.0001635	0.0003501	3.499e-05	NAND2BX1
g1406	0.0001533	0.0001617	0.0003273	1.236e-05	NOR2XL
g1384	0.0002381	6.881e-05	0.000321	1.41e-05	OAI211X1
g1410	0.0001816	8.235e-05	0.0002989	3.499e-05	NAND2BX1
g1381	0.0002092	4.824e-05	0.0002845	2.704e-05	MXI2XL
g1408	0.000148	0.0001225	0.0002836	1.301e-05	CLKINVX1
g1397	0.0001114	0.0001515	0.0002722	9.289e-06	NAND2XL
bcd/g221	0.0001861	4.795e-05	0.0002611	2.704e-05	MXI2XL
in1/g21	0.000201	3.879e-05	0.0002598	2.004e-05	NOR2BX1
in1/g18	0.000201	3.87e-05	0.0002597	2.004e-05	NOR2BX1
g1414	0.0001032	0.0001438	0.0002594	1.236e-05	NOR2XL
in1/g23	0.000201	3.829e-05	0.0002593	2.004e-05	NOR2BX1
in1/g27	0.0002009	3.599e-05	0.0002569	2.004e-05	NOR2BX1
in1/g29	0.0002009	3.529e-05	0.0002562	2.004e-05	NOR2BX1
in1/g22	0.0002009	3.334e-05	0.0002542	2.004e-05	NOR2BX1
in1/g20	0.0002008	3.285e-05	0.0002537	2.004e-05	NOR2BX1
in1/g28	0.0002008	3.279e-05	0.0002537	2.004e-05	NOR2BX1
in1/g25	0.0002008	3.234e-05	0.0002532	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.02e-05	0.000251	2.004e-05	NOR2BX1
in1/g30	0.0002008	2.978e-05	0.0002506	2.004e-05	NOR2BX1
in1/g24	0.0002008	2.976e-05	0.0002506	2.004e-05	NOR2BX1
in1/g19	0.0002008	2.926e-05	0.0002501	2.004e-05	NOR2BX1
bcd/g213	0.0001817	4.121e-05	0.0002351	1.22e-05	AOI21XL
bcd/g226	0.0001231	9.722e-05	0.0002333	1.301e-05	CLKINVX1
out1/g12	0.0001709	3.578e-05	0.0002233	1.662e-05	NOR2BXL
bcd/g224	0.0001192	9.017e-05	0.0002224	1.301e-05	INVX1
bcd/g218	0.0001653	4.455e-05	0.0002222	1.236e-05	NOR2XL
g1403	9.302e-05	0.0001136	0.000219	1.236e-05	NOR2XL
g1419	0.0001275	7.756e-05	0.0002181	1.301e-05	CLKINVX1
bcd/g217	0.0001498	4.784e-05	0.00021	1.236e-05	NOR2XL
g1382	9.642e-05	9.726e-05	0.0002067	1.301e-05	CLKINVX1
g1401	9.946e-05	8.361e-05	0.0001982	1.511e-05	NAND3X1
g1379	0.0001394	3.512e-05	0.0001958	2.127e-05	OAI2BB1X1
bcd/g211	0.0001348	3.683e-05	0.000184	1.236e-05	NOR2XL
g1385	0.0001314	3.639e-05	0.0001819	1.41e-05	OAI211X1
bcd/g208	0.0001272	3.63e-05	0.0001758	1.236e-05	NOR2XL
EPG/g38	8.927e-05	7.372e-05	0.0001723	9.289e-06	NAND2XL

g1396	0.0001037	4.713e-05	0.0001632	1.236e-05	NOR2XL
g1418	7.864e-05	6.639e-05	0.000158	1.301e-05	INVX1
g1417	4.852e-05	9.793e-05	0.0001557	9.289e-06	NAND2XL
g1411	4.588e-05	7.478e-05	0.0001556	3.499e-05	NAND2BX1
out1/g14	0.0001099	2.264e-05	0.0001492	1.662e-05	NOR2BXL
g1376	9.907e-05	3.265e-05	0.0001458	1.41e-05	OAI211X1
out1/g17	0.0001017	2.602e-05	0.0001444	1.662e-05	NOR2BXL
g1380	8.953e-05	3.325e-05	0.0001413	1.851e-05	AOI32X1
bcd/g215	0.0001036	2.458e-05	0.0001405	1.236e-05	NOR2XL
bcd/g222	5.036e-05	7.416e-05	0.0001338	9.289e-06	NAND2XL
out1/g16	8.362e-05	2.189e-05	0.0001221	1.662e-05	NOR2BXL
g1412	6.196e-05	2.756e-05	0.0001019	1.236e-05	NOR2XL
g1390	4.415e-05	2.004e-05	9.917e-05	3.499e-05	NAND2BX1
g1398	4.001e-05	4.575e-05	9.505e-05	9.289e-06	NAND2XL
g1395	4.938e-05	3.418e-05	9.284e-05	9.289e-06	NAND2XL
g1399	4.319e-05	3.465e-05	8.713e-05	9.289e-06	NAND2XL
bcd/g216	4.501e-05	2.277e-05	8.014e-05	1.236e-05	NOR2XL
bcd/g220	3.943e-05	2.874e-05	7.863e-05	1.046e-05	NAND4XL
g1394	4.289e-05	2.217e-05	7.741e-05	1.236e-05	NOR2XL
g1413	3.522e-05	1.664e-05	7.719e-05	2.533e-05	AND3XL
g1400	3.181e-05	3.374e-05	7.485e-05	9.289e-06	NAND2XL
g1416	4.176e-05	2.361e-05	7.466e-05	9.289e-06	NAND2XL
g1387	2.47e-05	2.051e-05	5.449e-05	9.289e-06	NAND2XL
g1377	2.046e-05	1.831e-05	4.805e-05	9.289e-06	NAND2XL
g1378	2.535e-05	5.265e-06	4.463e-05	1.402e-05	OAI31X1
out1/g15	1.625e-05	3.135e-06	3.601e-05	1.662e-05	NOR2BXL
g1391	1.098e-05	1.537e-06	3.255e-05	2.004e-05	NOR2BX1
g1388	5.523e-06	1.461e-06	3.165e-05	2.466e-05	AND2XL
g1389	4.06e-06	6.173e-07	2.472e-05	2.004e-05	NOR2BX1
g1386	8.171e-06	6.905e-06	2.437e-05	9.289e-06	NAND2XL
out1/g18	4.567e-06	9.255e-07	2.212e-05	1.662e-05	NOR2BXL
out1/g11	4.393e-06	1.018e-06	2.204e-05	1.662e-05	NOR2BXL
out1/g13	1.587e-06	3.822e-07	1.859e-05	1.662e-05	NOR2BXL

Total (116 of 116)	0.09495	0.04642	0.1481	0.006762
Total Capacitance	4.639e-12 F			

- **Total power** here is reported as: 0.1481mW.

❖ Clock Tree Synthesis Post-Optimization

- The CTS algorithm tries to ensure that the delay from the top-level clock pin to the sequential element called leaves are all the same. It accomplishes this by adding and sizing clock buffers between the top-level pin and the leaves.
- Now, Post-CTS optimization is performed, where the clock is now a real signal that is being distributed to different parts of the design.

- In this step, the tool fixes setup and hold time violations simultaneously.
- **Timing Report of Worst Path**

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:56:10 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/postcts_ao/timin
#####################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
- Setup                         0.242
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.559
- Arrival Time                  1.963
= Slack Time                    3.596
     Clock Rise Edge                          0.000
     + Input Delay                            1.000
     = Beginpoint Arrival Time                1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.596 |
     | g1418           | A v -> Y ^  | INVX1     | 0.046 |   1.046 |    4.641 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.156 |   1.202 |    4.798 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.307 |   1.509 |    5.105 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.220 |   1.730 |    5.325 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.084 |   1.814 |    5.409 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.149 |   1.963 |    5.559 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.963 |    5.559 |
     +-------------------------------------------------------------------------+
```

- In the complete timing report, a total of 83 paths have been analyzed.
- The path with the worst slack, i.e., most slack, turns out to be Path-1, with a slack of **3.596 ns** in the path with a start point from ***start point of rst to end point out1/OUT_reg[2]/D.***

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:56:09 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/post
timing_post_PnR_early.txt
#############################################################
Path 1: MET Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         0.015
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.215
  Arrival Time                 0.253
  Slack Time                   0.037
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +-------------------------------------------------------------------------------+
     |        Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                        |             |         |       |  Time   |   Time   |
     |------------------------+-------------+---------+-------+---------+----------|
     |                        | DFT_sdi_2 v |         |       |   0.000 |   -0.037 |
     | in1/FE_PHC10_DFT_sdi_2 | A v -> Y v  | DLY1X4  | 0.253 |   0.253 |    0.215 |
     | in1/C_reg_reg[2]       | SI v        | SDFFQX1 | 0.000 |   0.253 |    0.215 |
```

- Here, Path 1, with Starpoint as DFT_sdi_2 and end point as in1/C_reg_reg[2]/SI is reported as the critical path with a slack of 0.037ns.

Comparison of hold violation after placement and after optimize CTS.

Post Optimize Clock Tree Synthesis	Post Placement

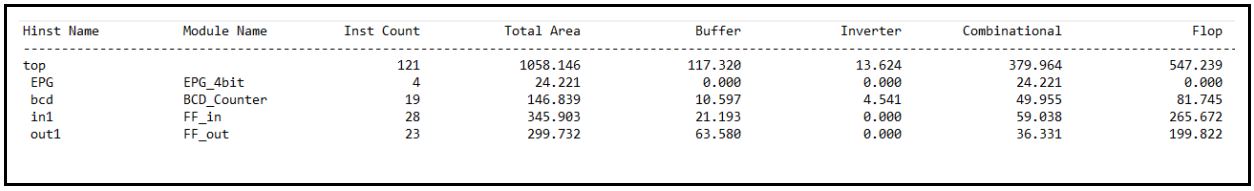
```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:56:09 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/post
timing_post_PnR_early.txt
#############################################################
Path 1: MET Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         0.015
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.215
  Arrival Time                 0.253
  Slack Time                   0.037
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +-------------------------------------------------------------------------+
     |       Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                       |             |         |       |  Time   |   Time   |
     |-----------------------+-------------+---------+-------+---------+----------|
     |                       | DFT_sdi_2 v |         |       |   0.000 |   -0.037 |
     | in1/FE_PHC10_DFT_sdi_2 | A v -> Y v  | DLY1X4  | 0.253 |   0.253 |    0.215 |
     | in1/C_reg_reg[2]      | SI v        | SDFFQX1 | 0.000 |   0.253 |    0.215 |
```

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:55:48 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > repo
timing_post_PnR_early.txt
#############################################################
Path 1: VIOLATED Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         -0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.200
= Required Time                 0.186
  Arrival Time                  0.000
  Slack Time                   -0.186
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +-------------------------------------------------------------------------+
     |     Instance     |     Arc     |  Cell   | Delay | Arrival | Required |
     |                  |             |         |       |  Time   |   Time   |
     |------------------+-------------+---------+-------+---------+----------|
     |                  | DFT_sdi_2 v |         |       |   0.000 |    0.186 |
     | in1/C_reg_reg[2] | SI v        | SDFFQX1 | 0.000 |   0.000 |    0.186 |
     +-------------------------------------------------------------------------+
```

- Here, it is to be noted that the Path 1, with Starpoint as DFT_sdi_2 and end point as in1/C_reg_reg[2]/SI earlier had a timing violation in the placement report as shown above.
- However, the post CTS critical path is still the same as shown in the above comparison (i.e., from Starpoint as DFT_sdi_2 and end point as in1/C_reg_reg[2]/SI) which has been resolved post CTS.
- Also, in the previous step i.e., in placement, the Hold violations were 27, whereas this step results in 0 hold violations. Reason is:
  - Many buffers have been added during the CTS step.
  - These buffers, in turn increase the time taken by the clock to reach the launching flip flop, and hence, resulting in an increased arrival time.
  - As a consequence, the slack given by (Arrival Time - Required Time) for the hold case, turns out to be a positive value, and handles all violations.
  - However, the routing has not been considered accurately yet, which will be taken care of in the subsequent stage.

Area of Standard Cells

The area of standard cells post-CTS is given as:



Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		121	1058.146	117.320	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	19	146.839	10.597	4.541	49.955	81.745
in1	FF_in	28	345.903	21.193	0.000	59.038	265.672
out1	FF_out	23	299.732	63.580	0.000	36.331	199.822

- Area of individual components still remain the same.
- However, some **new components have been added in post-CTS design**.
- This majorly include buffers which are added by the tool in order to handle the hold violations which has been shown in the following table.

Cell Type	Instance Count	Area
MXI2XL	2	6.0552
DLY1X1	1	19.961
NAND4XL	1	5.2983
AOI32X1	2	6.8121
AOI21XL	1	4.5414
NOR2BXL	8	4.5414
SDFFQX4	8	24.9777
NOR2XL	13	3.0276
INVX1	2	2.2707
NOR3X1	1	4.5414
AOI31X1	1	6.0552
NOR3BX1	1	6.0552
NOR2BX1	15	4.5414
ADDHX1	1	12.1104
NAND2XL	12	3.0276
NAND3X1	1	4.5414
ADDFX1	2	19.6794
XNOR2XL	1	8.3259
NAND2BX1	4	4.5414
CLKINVX1	4	2.2707
OAI31X1	2	6.0552
AND3XL	1	6.0552
OAI21X1	1	4.5414
CLKBUFX6	8	9.0828
DLY1X4	3	19.97
AND2XL	1	4.5414
XNOR2X1	1	8.3259
SDFFQX1	17	20.4363
OAI211X1	3	5.2983
CLKXOR2X1	1	8.3259
OAI2BB1X1	1	5.4247

- The following image depicts a comparison of the components in both the cases.

Post Placement

Cell Type	Cell Type
MXI2XL	MXI2XL
NAND4XL	DLY1X1
AOI32X1	NAND4XL
AOI21XL	AOI32X1
NOR2BXL	AOI21XL
SDFFQX4	NOR2BXL
NOR2XL	SDFFQX4
INVX1	NOR2XL
NOR3X1	INVX1
AOI31X1	NOR3X1
NOR3BX1	AOI31X1
NOR2BX1	NOR3BX1
ADDHX1	NOR2BX1
NAND2XL	ADDHX1
NAND3X1	NAND2XL
ADDFX1	NAND3X1
XNOR2XL	ADDFX1
NAND2BX1	XNOR2XL
CLKINVX1	NAND2BX1
OAI31X1	CLKINVX1
AND3XL	OAI31X1
OAI21X1	AND3XL
AND2XL	OAI21X1
XNOR2X1	CLKBUFX6
SDFFQX1	DLY1X4
OAI211X1	AND2XL
CLKXOR2X1	XNOR2X1
OAI2BB1X1	SDFFQX1
	OAI211X1
	CLKXOR2X1
	OAI2BB1X1

Post CTS

- The blue highlighted components give the report of additional components in the post CTS design. As noticed, most of these are related to Clock Buffers (DLY1X1 and DLY14 are also buffers) having area same as in the small utilization case.
- These clock buffers are added to ensure that the delay from the top-level clock pin to the sequential element are all the same .

POWER

Cell	Internal Power	Switching Power	Total Power	Leakage Power	Cell Power	Name
out1/FE_OFC0_OUT_0		0.001047	0.00999	0.01116	0.0001212	CLKBUFX6
out1/FE_OFC5_OUT_4	0.0006381	0.006089	0.006849	0.0001212	CLKBUFX6	
out1/FE_OFC2_OUT_1	0.0004875	0.004667	0.005275	0.0001212	CLKBUFX6	
out1/FE_OFC4_OUT_3	0.0004831	0.004607	0.005211	0.0001212	CLKBUFX6	
out1/OUT_reg[0]	0.004221	0.00017260	0.004611	0.0002172	SDFFQX4	
out1/FE_OFC3_OUT_2	0.0003797	0.003633	0.004134	0.0001212	CLKBUFX6	
out1/FE_OFC6_OUT_5	0.0003684	0.003515	0.004004	0.0001212	CLKBUFX6	
out1/OUT_reg[4]	0.003615	7.258e-05	0.003904	0.0002172	SDFFQX4	
in1/A_reg_reg[1]	0.003091	0.00046510	0.003693	0.0001363	SDFFQX1	
in1/A_reg_reg[2]	0.003097	0.00041550	0.003649	0.0001363	SDFFQX1	
out1/OUT_reg[1]	0.003364	5.854e-05	0.00364	0.0002172	SDFFQX4	
out1/OUT_reg[3]	0.003362	6.033e-05	0.003639	0.0002172	SDFFQX4	
in1/A_reg_reg[0]	0.003084	0.00033530	0.003556	0.0001363	SDFFQX1	
bcd/OUT_reg[1]	0.003141	0.00026630	0.003544	0.0001363	SDFFQX1	
bcd/OUT_reg[2]	0.003153	0.00023640	0.003525	0.0001363	SDFFQX1	
bcd/OUT_reg[3]	0.00311	0.0002568	0.003503	0.0001363	SDFFQX1	
in1/A_reg_reg[3]	0.003095	0.00023070	0.003462	0.0001363	SDFFQX1	
out1/OUT_reg[2]	0.003182	4.638e-05	0.003445	0.0002172	SDFFQX4	
in1/B_reg_reg[11]	0.003096	0.00020640	0.003439	0.0001363	SDFFQX1	
out1/OUT_reg[5]	0.003171	4.11e-05	0.00343	0.0002172	SDFFQX4	
in1/C_reg_reg[3]	0.003066	0.0002269	0.00343	0.0001363	SDFFQX1	
in1/B_reg_reg[12]	0.003096	0.00018150	0.003414	0.0001363	SDFFQX1	
in1/C_reg_reg[5]	0.003045	0.0002183	0.0034	0.0001363	SDFFQX1	
in1/C_reg_reg[0]	0.003099	0.00011840	0.003353	0.0001363	SDFFQX1	
in1/B_reg_reg[10]	0.003076	0.00013590	0.003348	0.0001363	SDFFQX1	
in1/C_reg_reg[1]	0.003096	0.00011160	0.003344	0.0001363	SDFFQX1	
in1/C_reg_reg[4]	0.002978	0.00020850	0.003323	0.0001363	SDFFQX1	
bcd/OUT_reg[0]	0.002914	0.00026090	0.003311	0.0001363	SDFFQX1	
out1/OUT_reg[7]	0.003002	2.992e-05	0.003249	0.0002172	SDFFQX4	
out1/OUT_reg[6]	0.002916	2.398e-05	0.003157	0.0002172	SDFFQX4	
in1/C_reg_reg[2]	0.002831	0.00014170	0.003108	0.0001363	SDFFQX1	
FE_OFC7_DFT_sdo_2	0.0002627	0.002501	0.002885	0.0001212	CLKBUFX6	
out1/FE_OFC1_OUT_6		0.000215	0.00206	0.002396	0.0001212	CLKBUFX6
g1402	0.0006646	0.0002305	0.000917	2.186e-05	NOR3BX1	
FE_PHC8_scan_en	0.0001441	0.000722	0.0009074	4.129e-05	CLKBUFX2	
g1383	0.0005611	0.0002059	0.0008515	8.448e-05	ADDFX1	
g1393	0.0005295	0.0001624	0.0007764	8.448e-05	ADDFX1	
g1409	0.0005167	0.0001704	0.0007075	2.034e-05	NOR3X1	
g1407	0.0004106	0.0001219	0.000628	9.553e-05	ADDHX1	
EPG/g40	0.0003668	0.0001231	0.0005624	7.254e-05	CLKXOR2X1	
EPG/g39	0.0003691	0.0001185	0.0005582	7.055e-05	XNOR2X1	
g1405	0.00027	0.0002257	0.0005136	1.789e-05	AOI31X1	
in1/FE_PHC12_scan_en	0.0003579	3.443e-05	0.0004936	0.0001012	DLY1X4	

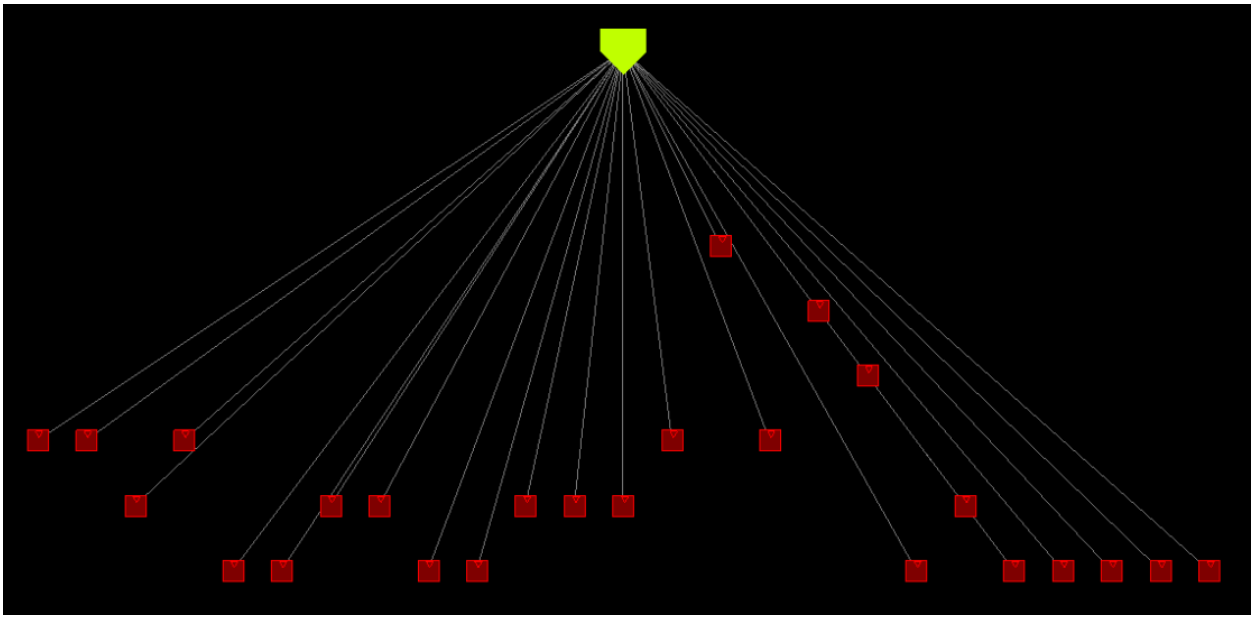
bcd/FE_PHC9_DFT_sdi_1	0.0003605	1.871e-05	0.0004804	0.0001012	DLY1X4
in1/FE_PHC10_DFT_sdi_2	0.0003608	1.716e-05	0.0004792	0.0001012	DLY1X4
g1392	0.0003253	0.0001349	0.0004787	1.851e-05	AOI32X1
EPG/g37	0.0002668	0.0001205	0.0004004	1.299e-05	OAI21X1
g1404	0.0001991	0.0001856	0.0003988	1.402e-05	OAI31X1
bcd/g210	0.0002689	4.865e-05	0.0003806	6.308e-05	XNOR2XL
FE_PHC11_scan_en	0.0001341	0.0001905	0.000379	5.435e-05	DLY1X1
g1415	0.0002041	0.0001368	0.0003532	1.236e-05	NOR2XL
bcd/g219	0.0001521	0.0001634	0.0003506	3.499e-05	NAND2BX1
g1406	0.0001533	0.0001616	0.0003272	1.236e-05	NOR2XL
g1384	0.0002403	6.915e-05	0.0003235	1.41e-05	OAI211X1
g1410	0.0001815	8.207e-05	0.0002986	3.499e-05	NAND2BX1
g1408	0.000148	0.0001225	0.0002835	1.301e-05	CLKINVX1
g1381	0.0002083	4.808e-05	0.0002834	2.704e-05	MXI2XL
g1397	0.0001105	0.0001504	0.0002701	9.289e-06	NAND2XL
bcd/g213	0.0002042	4.629e-05	0.0002627	1.22e-05	AOI21XL
bcd/g221	0.0001869	4.825e-05	0.0002622	2.704e-05	MXI2XL
in1/g18	0.000201	3.866e-05	0.0002597	2.004e-05	NOR2BX1
in1/g21	0.000201	3.85e-05	0.0002595	2.004e-05	NOR2BX1
in1/g23	0.000201	3.789e-05	0.0002589	2.004e-05	NOR2BX1
in1/g27	0.0002009	3.579e-05	0.0002567	2.004e-05	NOR2BX1
in1/g29	0.0002009	3.507e-05	0.000256	2.004e-05	NOR2BX1
g1414	0.0001028	0.0001408	0.0002559	1.236e-05	NOR2XL
in1/g22	0.0002009	3.314e-05	0.000254	2.004e-05	NOR2BX1
in1/g20	0.0002008	3.267e-05	0.0002536	2.004e-05	NOR2BX1
in1/g28	0.0002008	3.263e-05	0.0002535	2.004e-05	NOR2BX1
in1/g25	0.0002008	3.216e-05	0.000253	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.017e-05	0.000251	2.004e-05	NOR2BX1
in1/g24	0.0002008	3.015e-05	0.000251	2.004e-05	NOR2BX1
in1/g30	0.0002008	2.964e-05	0.0002505	2.004e-05	NOR2BX1
in1/g19	0.0002008	2.913e-05	0.0002499	2.004e-05	NOR2BX1
bcd/g226	0.0001217	9.608e-05	0.0002308	1.301e-05	CLKINVX1
out1/g12	0.0001722	3.581e-05	0.0002247	1.662e-05	NOR2BXL
bcd/g218	0.0001667	4.489e-05	0.0002239	1.236e-05	NOR2XL
bcd/g224	0.0001199	9.071e-05	0.0002236	1.301e-05	INVX1
g1403	9.298e-05	0.0001134	0.0002187	1.236e-05	NOR2XL
g1419	0.000127	7.722e-05	0.0002172	1.301e-05	CLKINVX1
g1382	9.849e-05	9.883e-05	0.0002103	1.301e-05	CLKINVX1
bcd/g217	0.0001499	4.783e-05	0.0002101	1.236e-05	NOR2XL
g1401	9.953e-05	8.353e-05	0.0001982	1.511e-05	NAND3X1
g1379	0.0001406	3.538e-05	0.0001973	2.127e-05	OAI2BB1X1
g1385	0.000133	3.682e-05	0.0001839	1.41e-05	OAI211X1
bcd/g211	0.000129	3.516e-05	0.0001766	1.236e-05	NOR2XL
EPG/g38	8.987e-05	7.402e-05	0.0001732	9.289e-06	NAND2XL
bcd/g208	0.0001246	3.56e-05	0.0001725	1.236e-05	NOR2XL
g1396	0.000103	4.773e-05	0.0001631	1.236e-05	NOR2XL
g1411	4.749e-05	7.731e-05	0.0001598	3.499e-05	NAND2BX1
g1418	7.865e-05	6.627e-05	0.0001579	1.301e-05	INVX1
g1417	4.862e-05	9.781e-05	0.0001557	9.289e-06	NAND2XL
g1376	0.0001029	3.387e-05	0.0001509	1.41e-05	OAI211X1

out1/g14	0.0001112	2.178e-05	0.0001496	1.662e-05	NOR2BXL
out1/g17	0.0001028	2.63e-05	0.0001457	1.662e-05	NOR2BXL
g1380	9.025e-05	3.354e-05	0.0001423	1.851e-05	AOI32X1
bcd/g215	0.0001039	2.466e-05	0.000141	1.236e-05	NOR2XL
bcd/g222	5.103e-05	7.516e-05	0.0001355	9.289e-06	NAND2XL
out1/g16	8.783e-05	2.306e-05	0.0001275	1.662e-05	NOR2BXL
g1412	6.198e-05	2.741e-05	0.0001017	1.236e-05	NOR2XL
g1390	4.382e-05	1.989e-05	9.869e-05	3.499e-05	NAND2BX1
g1398	4.036e-05	4.606e-05	9.571e-05	9.289e-06	NAND2XL
g1395	5.005e-05	3.462e-05	9.396e-05	9.289e-06	NAND2XL
g1399	4.343e-05	3.485e-05	8.757e-05	9.289e-06	NAND2XL
bcd/g216	4.637e-05	2.345e-05	8.217e-05	1.236e-05	NOR2XL
g1394	4.363e-05	2.275e-05	7.874e-05	1.236e-05	NOR2XL
g1400	3.355e-05	3.583e-05	7.866e-05	9.289e-06	NAND2XL
g1413	3.525e-05	1.659e-05	7.718e-05	2.533e-05	AND3XL
bcd/g220	3.74e-05	2.739e-05	7.525e-05	1.046e-05	NAND4XL
g1416	4.175e-05	2.346e-05	7.449e-05	9.289e-06	NAND2XL
g1387	2.5e-05	2.077e-05	5.505e-05	9.289e-06	NAND2XL
g1377	2.057e-05	1.842e-05	4.828e-05	9.289e-06	NAND2XL
g1378	2.61e-05	5.382e-06	4.55e-05	1.402e-05	OAI31X1
out1/g15	1.665e-05	3.145e-06	3.642e-05	1.662e-05	NOR2BXL
g1391	1.144e-05	1.456e-06	3.294e-05	2.004e-05	NOR2BX1
g1388	5.654e-06	1.847e-06	3.216e-05	2.466e-05	AND2XL
g1389	4.355e-06	7.889e-07	2.518e-05	2.004e-05	NOR2BX1
g1386	8.127e-06	6.863e-06	2.428e-05	9.289e-06	NAND2XL
out1/g11	4.579e-06	1.165e-06	2.237e-05	1.662e-05	NOR2BXL
out1/g18	4.691e-06	1.028e-06	2.234e-05	1.662e-05	NOR2BXL
out1/g13	1.709e-06	4.199e-07	1.875e-05	1.662e-05	NOR2BXL

Total (121 of 121)	0.09669	0.04783	0.1517	0.007161	
Total Capacitance	4.764e-12 F				

- Clock Network consumes a lot of power, as it is desired to have sharp transitions in clock path to have lesser delay. The added power from placement is being consumed by the power hungry large buffers that has been added in the CTS path.
- Hence, there is an increment in the power consumption from **0.1481mW to 0.1517mW** while going from **placement stage to clock tree synthesis stage**.

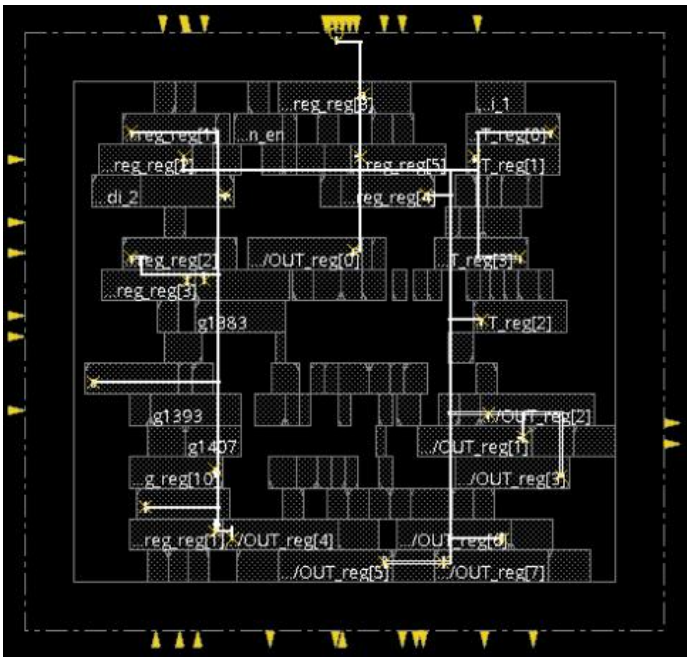
- We can also see the clock tree in its “tree” form by going to the menu Clock → CCOpt Clock Tree Debugger and pressing OK in the popup dialog. A window should pop up looking approximately like this:



- **This is the layout with clock path in bold white line after removing all the layers:**

- The red dots are the **“leaves”** and the green pin on top is the **clock pin** or the clock **“root”.** After clicking the arc we are able to observe the clock path in the layout.

Snapshot of Clock Tree Synthesis



❖ After Detailed Routing

Setup Timing Analysis:

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:56:13 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/route/timing/timing
#####################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
- Setup                         0.242
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.558
- Arrival Time                  1.980
= Slack Time                    3.578
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     = Beginpoint Arrival Time            1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.578 |
     | g1418           | A v -> Y ^  | INVX1     | 0.048 |   1.048 |    4.626 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.161 |   1.209 |    4.787 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.316 |   1.525 |    5.103 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.222 |   1.747 |    5.325 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.084 |   1.831 |    5.409 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.149 |   1.980 |    5.558 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.980 |    5.558 |
     +-------------------------------------------------------------------------+
```

- The **Arrival time has increased from post CTS to detailed routing,** the change in delay in the cells is due to more precise wire delay being considered after the detailed routing of all cells.
- The path with the worst slack is from **out1/OUT_reg[2]/D to rst** and the slack is **3.578**.

Hold Timing Analysis:

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:56:13 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/rout
timing_post_PnR_early.txt
#############################################################
Path 1: MET Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         0.015
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.215
  Arrival Time                 0.253
  Slack Time                   0.037
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------------+
     |        Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                        |             |         |       |  Time   |   Time   |
     |------------------------+-------------+---------+-------+---------+----------|
     |                        | DFT_sdi_2 v |         |       |   0.000 |   -0.037 |
     | in1/FE_PHC10_DFT_sdi_2 | A v -> Y v  | DLY1X4  | 0.253 |   0.253 |    0.215 |
     | in1/C_reg_reg[2]       | SI v        | SDFFQX1 | 0.000 |   0.253 |    0.215 |
```

- The path with the worst hold slack is from DFT_sdi_2 to in1/C_reg_reg[2]/SI and the slack is 0.037.

● Effect of different metal layer on the timing of the path

➢ Routing with M2 to M7

- For detailed routing, metal 2 to metal 7 has been used where metal 2 is top routing layer and metal 7 is bottom routing layer.

Worst Case Setup timing Report

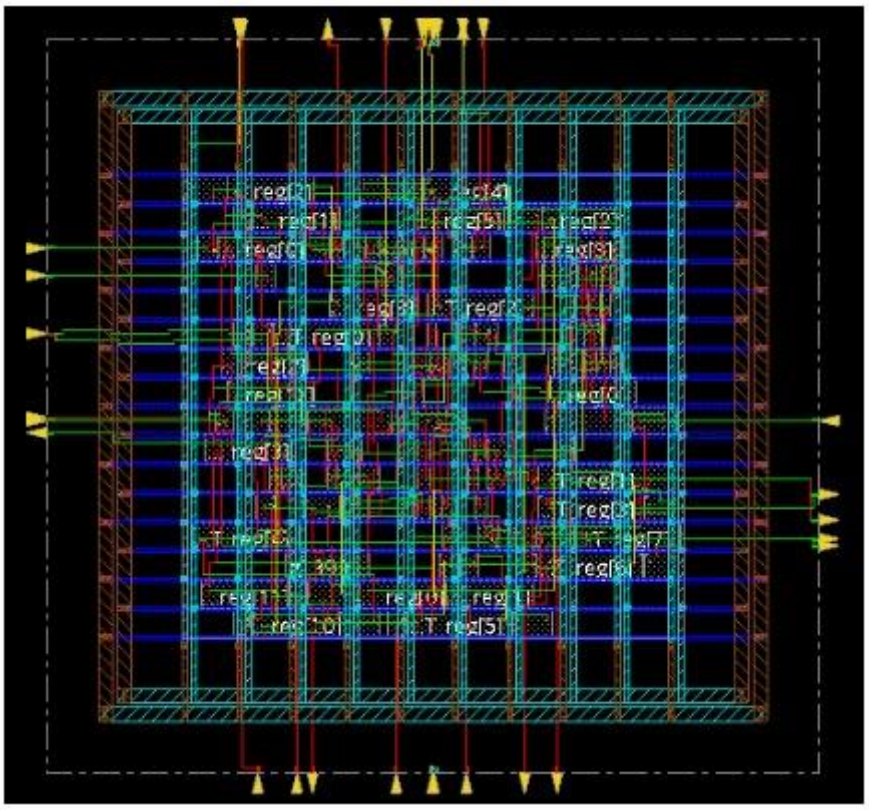
```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 19:37:48 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/route/timing/timing_post_PnR_late.txt
#############################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
- Setup                         0.234
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.567
- Arrival Time                  1.969
= Slack Time                    3.598
     Clock Rise Edge                     0.000
     + Input Delay                       1.000
     = Beginpoint Arrival Time           1.000
     +--------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.598 |
     | g1418           | A v -> Y ^  | INVX1     | 0.047 |   1.047 |    4.645 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.163 |   1.210 |    4.808 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.316 |   1.526 |    5.124 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.226 |   1.752 |    5.350 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.082 |   1.834 |    5.432 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.135 |   1.969 |    5.567 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.969 |    5.567 |
     +--------------------------------------------------------------------------+
```

- **Slack increased 3.578 to 5.598**
- When we specify the metal layer limits, the router routes all the nets within those limits.
- If there is a pin outside the limits, the router uses vias to access pins which leads to the increase in the delay so that arrival time at a point changes, so slack will change accordingly as shown above.

Worst Case Setup timing Report

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 19:37:48 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/route/timing/timing_post_PnR_early.txt
#############################################################
Path 1: MET Hold Check with Pin bcd/OUT_reg[1]/CK
Endpoint:   bcd/OUT_reg[1]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_1         (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                          0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.200
= Required Time                 0.216
  Arrival Time                  0.253
  Slack Time                    0.037
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +--------------------------------------------------------------------------+
     |       Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                       |             |         |       |  Time   |   Time   |
     |-----------------------+-------------+---------+-------+---------+----------|
     |                       | DFT_sdi_1 v |         |       |   0.000 |   -0.037 |
     | bcd/FE_PHC9_DFT_sdi_1 | A v -> Y v  | DLY1X4  | 0.253 |   0.253 |    0.216 |
     | bcd/OUT_reg[1]        | SI v        | SDFFQX1 | 0.000 |   0.253 |    0.216 |
     +--------------------------------------------------------------------------+
```

- The given hold path from **DFT_sdi_1 to bcd/OUT_reg[1]/SI** does not use metal 1 for routing even before limiting the use of metal 1 hence no change in the worst case hold slack has been observed while limiting the use of metal layers.



Layout of Design using routing from M2-M7

AREA

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		121	1058.146	117.320	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	19	146.839	10.597	4.541	49.955	81.745
in1	FF_in	28	345.903	21.193	0.000	59.038	265.672
out1	FF_out	23	299.732	63.580	0.000	36.331	199.822

- Comparing the area of the standard cells obtained after post-routing, and the post-CTS stage, it is noticed that the area remains the same.

Primitives:

*** 32 Primitives used:
Primitive MXI2XL (2 insts)
Primitive NAND4XL (1 insts)
Primitive DLY1X1 (1 insts)
Primitive AOI32X1 (2 insts)

```
Primitive AOI21XL (1 insts)
Primitive NOR2BXL (8 insts)
Primitive SDFFQX4 (8 insts)
Primitive NOR2XL (13 insts)
Primitive INVX1 (2 insts)
Primitive NOR3X1 (1 insts)
Primitive AOI31X1 (1 insts)
Primitive NOR3BX1 (1 insts)
Primitive NOR2BX1 (15 insts)
Primitive ADDHX1 (1 insts)
Primitive NAND2XL (12 insts)
Primitive NAND3X1 (1 insts)
Primitive ADDFX1 (2 insts)
Primitive XNOR2XL (1 insts)
Primitive NAND2BX1 (4 insts)
Primitive CLKINVX1 (4 insts)
Primitive OAI31X1 (2 insts)
Primitive AND3XL (1 insts)
Primitive OAI21X1 (1 insts)
Primitive CLKBUFX6 (8 insts)
Primitive AND2XL (1 insts)
Primitive DLY1X4 (3 insts)
Primitive XNOR2X1 (1 insts)
Primitive SDFFQX1 (17 insts)
Primitive OAI211X1 (3 insts)
Primitive CLKXOR2X1 (1 insts)
Primitive CLKBUFX2 (1 insts)
Primitive OAI2BB1X1 (1 insts)
************
*** Net length and connection length statistics (cell top) ***

Total net length = 1.665e+03 (7.673e+02 8.977e+02)
```

Power:

```
----------------------------------------------------------------------------------------
Cell                    Internal  Switching    Total     Leakage   Cell
                        Power     Power        Power     Power     Name
----------------------------------------------------------------------------------------
out1/FE_OFC0_OUT_0                0.001047     0.009991  0.01116   0.0001212
CLKBUFX6
out1/FE_OFC5_OUT_4      0.0006381 0.006092     0.006851  0.0001212 CLKBUFX6
out1/FE_OFC2_OUT_1      0.0004875 0.004664     0.005273  0.0001212 CLKBUFX6
out1/FE_OFC4_OUT_3      0.0004831 0.004607     0.005211  0.0001212 CLKBUFX6
out1/OUT_reg[0]         0.004222  0.00017850.004617  0.0002172 SDFFQX4
out1/FE_OFC3_OUT_2      0.0003797 0.003632     0.004133  0.0001212 CLKBUFX6
out1/FE_OFC6_OUT_5      0.0003684 0.003514     0.004004  0.0001212 CLKBUFX6
out1/OUT_reg[4]         0.003615  7.266e-05 0.003905  0.0002172 SDFFQX4
in1/A_reg_reg[1]        0.003092  0.00046450.003693  0.0001363 SDFFQX1
in1/A_reg_reg[2]        0.003098  0.000425   0.003659  0.0001363 SDFFQX1
```

out1/OUT_reg[1]	0.003364	6.096e-05	0.003643	0.0002172	SDFFQX4
out1/OUT_reg[3]	0.003362	6.016e-05	0.00364	0.0002172	SDFFQX4
in1/A_reg_reg[0]	0.003085	0.0003323	0.003553	0.0001363	SDFFQX1
bcd/OUT_reg[1]	0.003141	0.0002684	0.003546	0.0001363	SDFFQX1
bcd/OUT_reg[2]	0.003153	0.000238	0.003528	0.0001363	SDFFQX1
bcd/OUT_reg[3]	0.00311	0.0002778	0.003524	0.0001363	SDFFQX1
in1/B_reg_reg[11]	0.003097	0.0002334	0.003467	0.0001363	SDFFQX1
in1/A_reg_reg[3]	0.003096	0.0002341	0.003466	0.0001363	SDFFQX1
out1/OUT_reg[2]	0.003182	4.614e-05	0.003446	0.0002172	SDFFQX4
in1/C_reg_reg[3]	0.003067	0.0002365	0.003439	0.0001363	SDFFQX1
out1/OUT_reg[5]	0.003172	4.194e-05	0.003431	0.0002172	SDFFQX4
in1/B_reg_reg[12]	0.003097	0.0001937	0.003427	0.0001363	SDFFQX1
in1/C_reg_reg[5]	0.003045	0.0002302	0.003412	0.0001363	SDFFQX1
in1/C_reg_reg[0]	0.0031	0.0001226	0.003358	0.0001363	SDFFQX1
in1/B_reg_reg[10]	0.003077	0.0001373	0.00335	0.0001363	SDFFQX1
in1/C_reg_reg[1]	0.003097	0.000113	0.003346	0.0001363	SDFFQX1
in1/C_reg_reg[4]	0.002978	0.000208	0.003323	0.0001363	SDFFQX1
bcd/OUT_reg[0]	0.002914	0.0002534	0.003304	0.0001363	SDFFQX1
out1/OUT_reg[7]	0.003003	3.032e-05	0.00325	0.0002172	SDFFQX4
out1/OUT_reg[6]	0.002917	2.478e-05	0.003159	0.0002172	SDFFQX4
in1/C_reg_reg[2]	0.002831	0.0001503	0.003118	0.0001363	SDFFQX1
FE_OFC7_DFT_sdo_2	0.0002627	0.002499	0.002883	0.0001212	CLKBUFX6
out1/FE_OFC1_OUT_6	0.000215	0.002061	0.002397	0.0001212	CLKBUFX6
FE_PHC8_scan_en	0.0001441	0.0007407	0.0009261	4.129e-05	CLKBUFX2
g1402	0.0006645	0.0002373	0.0009237	2.186e-05	NOR3BX1
g1383	0.0005617	0.0001976	0.0008438	8.448e-05	ADDFX1
g1393	0.0005296	0.0001614	0.0007755	8.448e-05	ADDFX1
g1409	0.0005167	0.0001642	0.0007012	2.034e-05	NOR3X1
g1407	0.0004105	0.0001236	0.0006296	9.553e-05	ADDHX1
EPG/g39	0.0003695	0.0001248	0.0005648	7.055e-05	XNOR2X1
EPG/g40	0.0003666	0.0001239	0.0005631	7.254e-05	CLKXOR2X1
g1405	0.0002702	0.0002258	0.0005139	1.789e-05	AOI31X1
in1/FE_PHC12_scan_en	0.0003578	3.512e-05	0.0004941	0.0001012	DLY1X4
g1392	0.0003256	0.0001411	0.0004852	1.851e-05	AOI32X1
bcd/FE_PHC9_DFT_sdi_1	0.0003605	1.923e-05	0.0004809	0.0001012	DLY1X4
in1/FE_PHC10_DFT_sdi_2	0.0003607	1.786e-05	0.0004797	0.0001012	DLY1X4
g1404	0.0001992	0.0001918	0.000405	1.402e-05	OAI31X1
EPG/g37	0.0002668	0.0001161	0.0003959	1.299e-05	OAI21X1
FE_PHC11_scan_en	0.0001341	0.0001932	0.0003816	5.435e-05	DLY1X1
bcd/g210	0.0002694	4.83e-05	0.0003808	6.308e-05	XNOR2XL
g1415	0.0002041	0.0001407	0.0003572	1.236e-05	NOR2XL
bcd/g219	0.0001521	0.0001533	0.0003404	3.499e-05	NAND2BX1
g1384	0.0002403	7.248e-05	0.0003269	1.41e-05	OAI211X1
g1406	0.0001532	0.0001558	0.0003214	1.236e-05	NOR2XL
g1410	0.0001819	7.943e-05	0.0002964	3.499e-05	NAND2BX1
g1381	0.0002083	4.704e-05	0.0002824	2.704e-05	MXI2XL
g1408	0.0001474	0.0001215	0.0002819	1.301e-05	CLKINVX1
bcd/g221	0.0001868	5.101e-05	0.0002649	2.704e-05	MXI2XL
in1/g21	0.000201	4.036e-05	0.0002614	2.004e-05	NOR2BX1

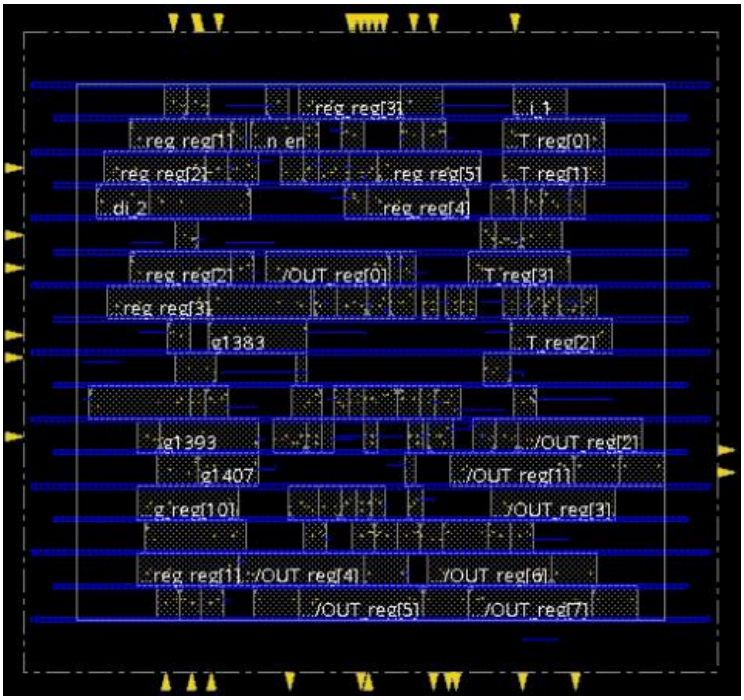
g1414	0.0001028	0.0001453	0.0002604	1.236e-05	NOR2XL
in1/g23	0.000201	3.841e-05	0.0002594	2.004e-05	NOR2BX1
bcd/g213	0.0002041	4.277e-05	0.0002591	1.22e-05	AOI21XL
in1/g29	0.0002009	3.664e-05	0.0002576	2.004e-05	NOR2BX1
in1/g27	0.0002009	3.479e-05	0.0002557	2.004e-05	NOR2BX1
in1/g18	0.0002009	3.476e-05	0.0002557	2.004e-05	NOR2BX1
g1397	0.0001108	0.0001343	0.0002543	9.289e-06	NAND2XL
in1/g30	0.0002009	3.283e-05	0.0002537	2.004e-05	NOR2BX1
in1/g20	0.0002009	3.28e-05	0.0002537	2.004e-05	NOR2BX1
in1/g22	0.0002008	3.232e-05	0.0002532	2.004e-05	NOR2BX1
in1/g24	0.0002008	3.045e-05	0.0002513	2.004e-05	NOR2BX1
in1/g19	0.0002008	3.029e-05	0.0002511	2.004e-05	NOR2BX1
in1/g25	0.0002008	3.028e-05	0.0002511	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.021e-05	0.000251	2.004e-05	NOR2BX1
in1/g28	0.0002008	2.993e-05	0.0002508	2.004e-05	NOR2BX1
bcd/g218	0.0001667	4.503e-05	0.0002241	1.236e-05	NOR2XL
bcd/g224	0.00012	9.037e-05	0.0002234	1.301e-05	INVX1
out1/g12	0.0001723	3.439e-05	0.0002233	1.662e-05	NOR2BXL
g1403	9.31e-05	0.0001175	0.0002229	1.236e-05	NOR2XL
bcd/g226	0.0001219	8.681e-05	0.0002217	1.301e-05	CLKINVX1
g1419	0.000127	7.707e-05	0.000217	1.301e-05	CLKINVX1
g1382	9.829e-05	0.0001014	0.0002127	1.301e-05	CLKINVX1
bcd/g217	0.0001498	4.806e-05	0.0002102	1.236e-05	NOR2XL
g1379	0.0001406	3.535e-05	0.0001972	2.127e-05	OAI2BB1X1
g1401	9.962e-05	8.151e-05	0.0001962	1.511e-05	NAND3X1
g1385	0.0001331	3.927e-05	0.0001865	1.41e-05	OAI211X1
bcd/g211	0.0001289	3.527e-05	0.0001765	1.236e-05	NOR2XL
EPG/g38	8.988e-05	7.528e-05	0.0001744	9.289e-06	NAND2XL
bcd/g208	0.0001246	3.57e-05	0.0001726	1.236e-05	NOR2XL
g1396	0.000103	4.97e-05	0.000165	1.236e-05	NOR2XL
g1418	7.872e-05	7.249e-05	0.0001642	1.301e-05	INVX1
g1411	4.755e-05	7.975e-05	0.0001623	3.499e-05	NAND2BX1
g1417	4.863e-05	0.0001007	0.0001586	9.289e-06	NAND2XL
g1376	0.0001028	3.378e-05	0.0001507	1.41e-05	OAI211X1
out1/g14	0.0001113	2.145e-05	0.0001493	1.662e-05	NOR2BXL
out1/g17	0.0001028	2.643e-05	0.0001458	1.662e-05	NOR2BXL
g1380	9.054e-05	3.338e-05	0.0001424	1.851e-05	AOI32X1
bcd/g215	0.0001038	2.507e-05	0.0001413	1.236e-05	NOR2XL
bcd/g222	5.102e-05	7.342e-05	0.0001337	9.289e-06	NAND2XL
out1/g16	8.782e-05	1.861e-05	0.000123	1.662e-05	NOR2BXL
g1412	6.2e-05	2.643e-05	0.0001008	1.236e-05	NOR2XL
g1390	4.388e-05	1.955e-05	9.842e-05	3.499e-05	NAND2BX1
g1398	4.026e-05	4.847e-05	9.802e-05	9.289e-06	NAND2XL
g1395	5.015e-05	3.324e-05	9.268e-05	9.289e-06	NAND2XL
g1399	4.328e-05	3.484e-05	8.741e-05	9.289e-06	NAND2XL
bcd/g216	4.635e-05	2.352e-05	8.222e-05	1.236e-05	NOR2XL
g1394	4.361e-05	2.411e-05	8.008e-05	1.236e-05	NOR2XL
g1413	3.526e-05	1.676e-05	7.735e-05	2.533e-05	AND3XL
bcd/g220	3.741e-05	2.746e-05	7.533e-05	1.046e-05	NAND4XL
g1400	3.358e-05	3.207e-05	7.494e-05	9.289e-06	NAND2XL

g1416	4.183e-05	2.198e-05	7.309e-05	9.289e-06	NAND2XL
g1387	2.518e-05	2.005e-05	5.452e-05	9.289e-06	NAND2XL
g1377	2.064e-05	1.985e-05	4.977e-05	9.289e-06	NAND2XL
g1378	2.611e-05	5.528e-06	4.566e-05	1.402e-05	OAI31X1
out1/g15	1.667e-05	3.213e-06	3.65e-05	1.662e-05	NOR2BXL
g1391	1.145e-05	1.568e-06	3.306e-05	2.004e-05	NOR2BX1
g1388	5.672e-06	1.897e-06	3.223e-05	2.466e-05	AND2XL
g1389	4.361e-06	7.834e-07	2.518e-05	2.004e-05	NOR2BX1
g1386	8.161e-06	6.689e-06	2.414e-05	9.289e-06	NAND2XL
out1/g11	4.581e-06	1.141e-06	2.235e-05	1.662e-05	NOR2BXL
out1/g18	4.691e-06	9.74e-07	2.229e-05	1.662e-05	NOR2BXL
out1/g13	1.709e-06	4.144e-07	1.875e-05	1.662e-05	NOR2BXL
Total (121 of 121)	0.09671	0.04794	0.1518	0.007161	
Total Capacitance	4.772e-12 F				

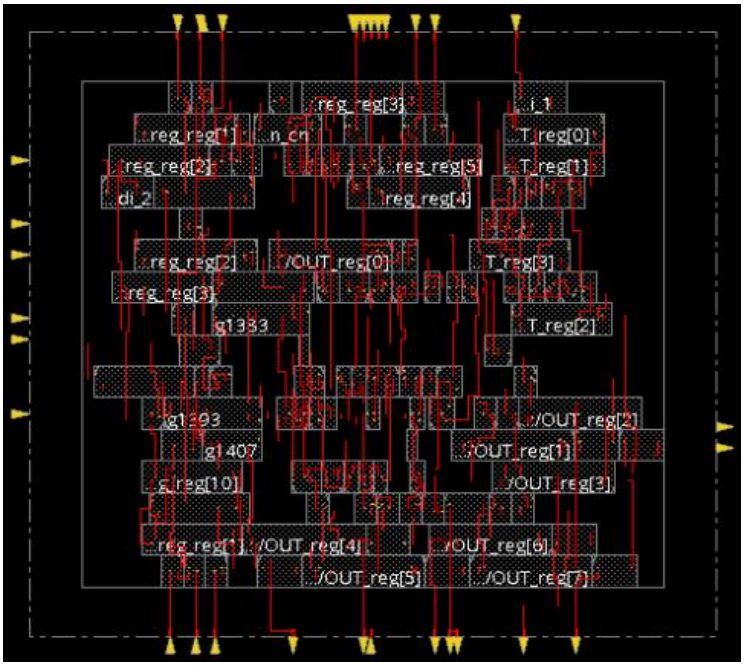
- Here, as expected, the power consumed compared to the post_CTS stage has increased and the power consumed is 0.1518mW.
- Also the parasitic capacitance has increased, from 4.764e-12 F to 4.772e-12 F. This is very much expected, due to the proximity of the interconnects and hence the resulting lateral and fringe capacitances.

Connectivity of different metal layers in layout

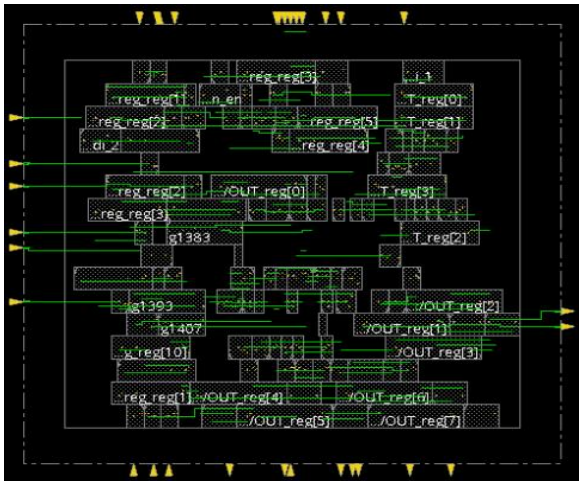
M1



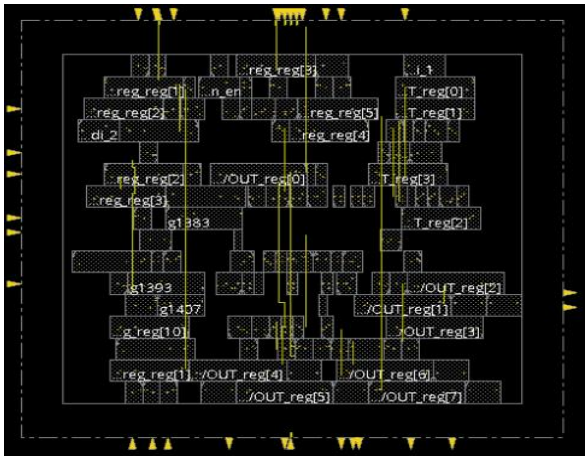
M2



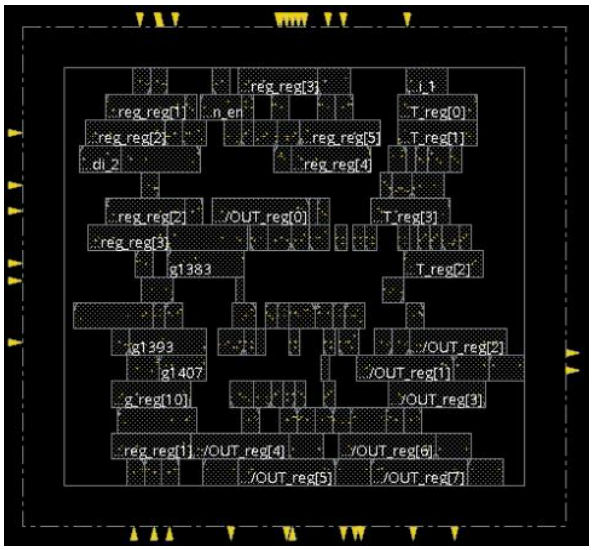
M3


reg_reg[3]
i_1
reg_reg[1]
n_en
T_reg[0]
reg_reg[2]
reg_reg[5]
T_reg[1]
di_2
reg_reg[4]
reg_reg[2]
/OUT_reg[0]
T_reg[3]
reg_reg[3]
g1383
T_reg[2]
g1393
/OUT_reg[2]
g1407
/OUT_reg[1]
x_reg[10]
/OUT_reg[3]
reg_reg[1]
/OUT_reg[4]
/OUT_reg[6]
/OUT_reg[5]
/OUT_reg[7]

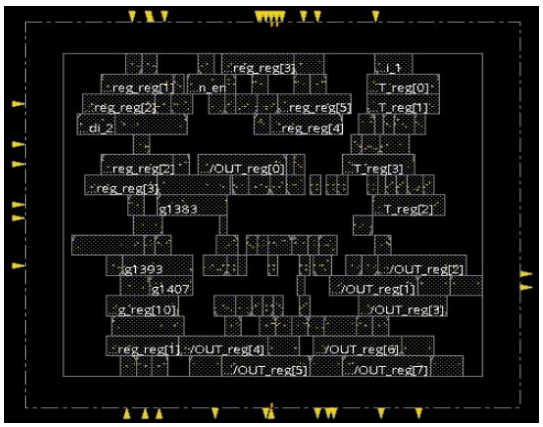
M4


reg_reg[3]
i_1
reg_reg[1]
n_en
T_reg[0]
reg_reg[2]
reg_reg[5]
T_reg[1]
di_2
reg_reg[4]
reg_reg[2]
/OUT_reg[0]
T_reg[3]
reg_reg[3]
g1383
T_reg[2]
g1393
/OUT_reg[2]
g1407
/OUT_reg[1]
g_reg[10]
/OUT_reg[3]
reg_reg[1]
/OUT_reg[4]
/OUT_reg[6]
/OUT_reg[5]
/OUT_reg[7]

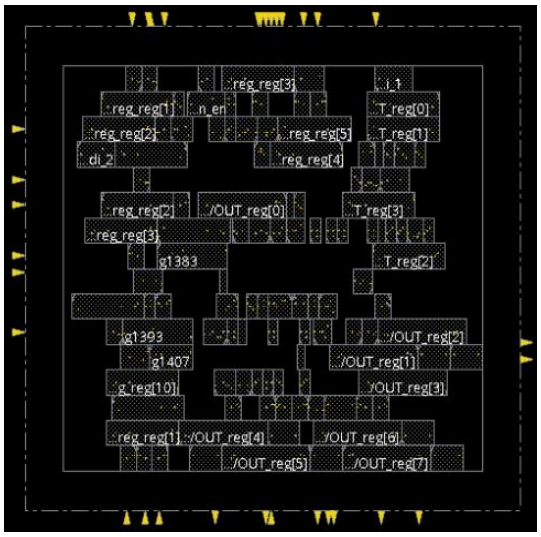
M5


reg_reg[3]
i_1
reg_reg[1]
n_en
T_reg[0]
reg_reg[2]
reg_reg[5]
T_reg[1]
di_2
reg_reg[4]
reg_reg[2]
/OUT_reg[0]
T_reg[3]
reg_reg[3]
g1383
T_reg[2]
g1393
/OUT_reg[2]
g1407
/OUT_reg[1]
g_reg[10]
/OUT_reg[3]
reg_reg[1]
/OUT_reg[4]
/OUT_reg[6]
/OUT_reg[5]
/OUT_reg[7]

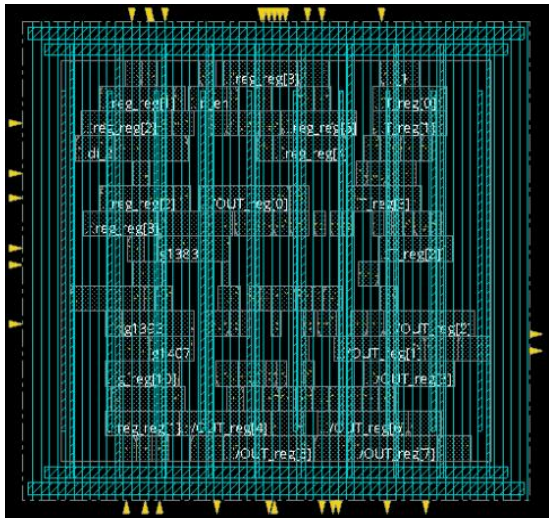
M6


reg_reg[3]
i_1
reg_reg[1]
n_en
T_reg[0]
reg_reg[2]
reg_reg[5]
T_reg[1]
di_2
reg_reg[4]
reg_reg[2]
/OUT_reg[0]
T_reg[3]
reg_reg[3]
g1383
T_reg[2]
g1393
/OUT_reg[2]
g1407
/OUT_reg[1]
g_reg[10]
/OUT_reg[3]
reg_reg[1]
/OUT_reg[4]
/OUT_reg[6]
/OUT_reg[5]
/OUT_reg[7]

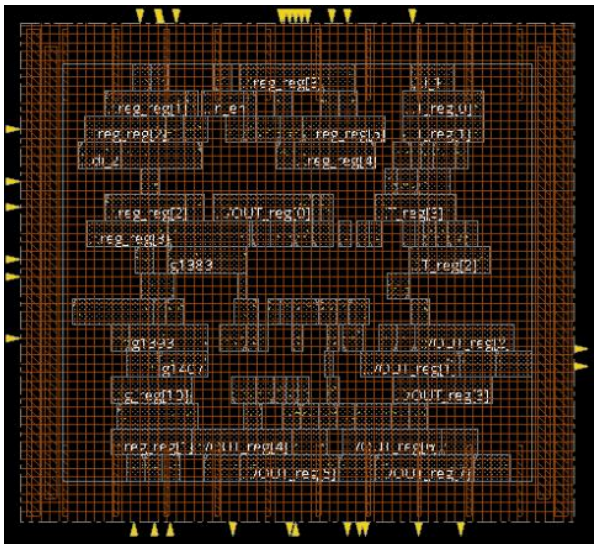
M7


reg_reg[3]
i_1
reg_reg[1]
n_en
T_reg[0]
reg_reg[2]
reg_reg[5]
T_reg[1]
di_2
reg_reg[4]
reg_reg[2]
/OUT_reg[0]
T_reg[3]
reg_reg[3]
g1383
T_reg[2]
g1393
/OUT_reg[2]
g1407
/OUT_reg[1]
g_reg[10]
/OUT_reg[3]
reg_reg[1]
/OUT_reg[4]
/OUT_reg[6]
/OUT_reg[5]
/OUT_reg[7]

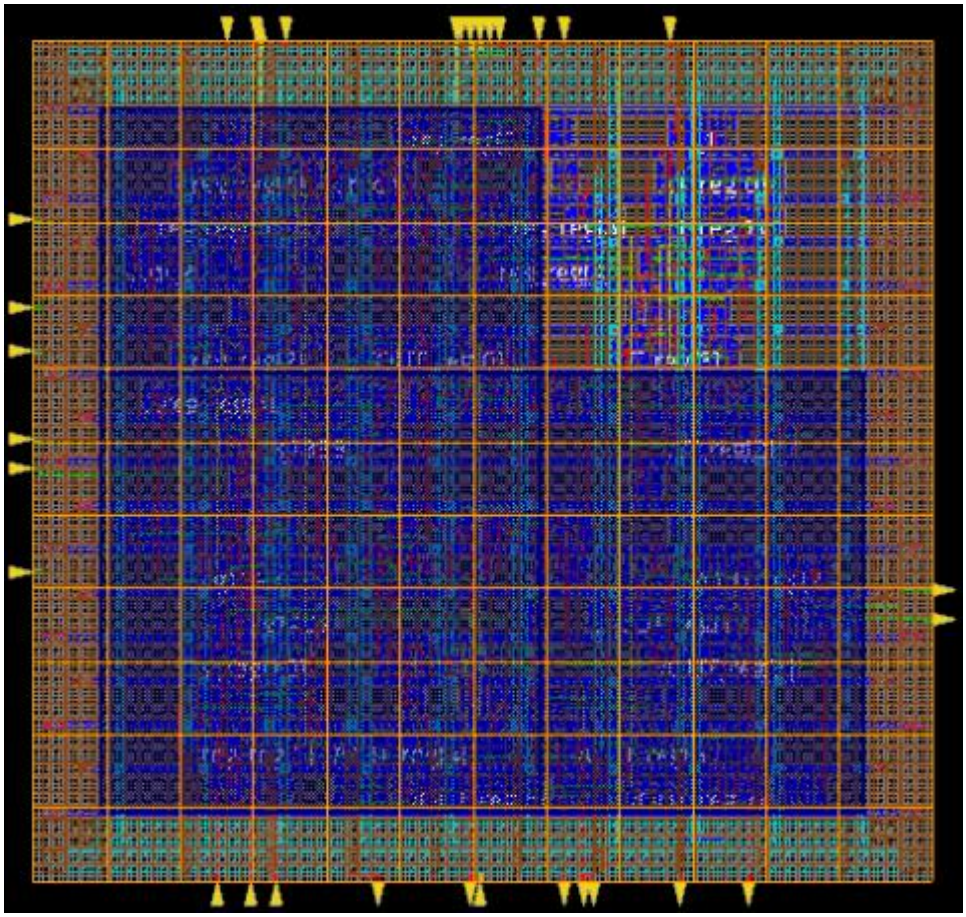
M8


reg_reg[3]
reg_reg[2]
reg_reg[5]
di_2
reg_reg[4]
reg_reg[2]
reg_reg[3]
g1383
g1393
g1407
g_reg[10]
reg_reg[1]

M9



Layout of the design:



Utilization of 0.8

Floor planning is done with large utilization of 0.8 or considering small die area.

❖ After Placement

Placement is the process of placing the synthesized design (structural connection of standard cells) onto the specified floor plan. While there is placement of minor cells (such as bulk connection cells, antenna-effect prevention cells, I/O buffers...) that take place separately and in between various stages of design.

Initial placement tries its best to place the cells optimally, obeying the floorplan constraints and using complex heuristics to minimize the parasitic delay caused by the connecting wires between cells and timing skew between synchronous elements (e.g. flip-flops, memories). Poor placement (as well as poor aspect ratio of the floorplan) can result in congestion of wires later on in the design, which may prevent successful routing.

❖ Time Design Summary after Placement

A summary of **setup report** of the **timing design** of the post-placement design is given as follows:

```
#####################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:58:17 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/placement/timing/timing_post_PnR_late.txt
#####################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
- Setup                         0.239
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.561
- Arrival Time                  1.969
= Slack Time                    3.592
     Clock Rise Edge                     0.000
     + Input Delay                       1.000
     = Beginpoint Arrival Time           1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.592 |
     | g1418           | A v -> Y ^  | INVX1     | 0.053 |   1.053 |    4.645 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.155 |   1.207 |    4.800 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.316 |   1.524 |    5.116 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.215 |   1.738 |    5.330 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.087 |   1.825 |    5.418 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.144 |   1.969 |    5.561 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.969 |    5.561 |
     +-------------------------------------------------------------------------+
```

A summary of **hold report** of the **timing design** of the post-placement design is given as follows:

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:58:17 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/placement/timing/timing_post_PnR_early.txt
#############################################################
Path 1: VIOLATED Hold Check with Pin bcd/OUT_reg[0]/CK
Endpoint:   bcd/OUT_reg[0]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_1         (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.002
+ Hold                         -0.015
+ Phase Shift                   0.000
+ Uncertainty                   0.200
= Required Time                 0.187
  Arrival Time                  0.000
  Slack Time                   -0.187
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +-------------------------------------------------------------------+
     |    Instance    |     Arc     |  Cell   | Delay | Arrival | Required |
     |                |             |         |       |  Time   |   Time   |
     |----------------+-------------+---------+-------+---------+----------|
     |                | DFT_sdi_1 v |         |       |   0.000 |    0.187 |
     | bcd/OUT_reg[0] | SI v        | SDFFQX1 | 0.000 |   0.000 |    0.187 |
     +-------------------------------------------------------------------+
```

Analysis of Timing Reports

- Firstly, analyzing the summary of the timing reports. Here, it is noticeable, that similar to the case of small utilization, here also we have violated timing constraints.
- Further, analyzing the worst path reports, here, it is also noticeable that **compared to the small utilization, the worst path is exactly the same**. Also, in this large utilization case, the slack of the critical path is **-0.187ns**.
- Additionally, the cause is also the same, wherein the arrival time has been taken as 0.00, since the clock path and resulting buffer delays have not been accounted for yet.

Area

Inst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		108	940.827	0.000	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	18	136.242	0.000	4.541	49.955	81.745
in1	FF_in	26	324.710	0.000	0.000	59.038	265.672
out1	FF_out	16	236.153	0.000	0.000	36.331	199.822

Total area for the top module comes out to be 940.827um^2 for a total of 108 instances and 28 Primitives which are shown below after the following table.

Cell Type	Instance Count	Area per instance of cell(um^2)

MXI2XL	2	6.055200
NAND4XL	1	5.298300
AOI32X1	2	6.812100
AOI21XL	1	4.541400
NOR2BXL	8	4.541400
SDFFQX4	8	24.977700
NOR2XL	13	3.027600
INVX1	2	2.270700
NOR3X1	1	4.54140
AOI31X1	1	6.055200
NOR3BX1	1	6.055200
NOR2BX1	15	4.541400
ADDHX1	1	12.110400
NAND2XL	12	3.027600
NAND3X1	1	4.541400
ADDFX1	2	19.679400
XNOR2XL	1	8.325900
NAND2BX1	4	4.541400
CLKINVX1	4	2.270700
OAI31X1	2	6.055200
AND3XL	1	6.055200
OAI21X1	1	4.541400
AND2XL	1	4.541400
XNOR2X1	1	8.325900
SDFFQX1	17	20.436300

OAI211X1	3	5.298300
CLKXOR2X1	1	8.325900
OAI2BB1X1	1	5.424700

- Here, the areas of all standard cells are the same as the area in case of small utilization of 0.5.

Primitives

*** 28 Primitives used:***
Primitive MXI2XL (2 insts)
Primitive NAND4XL (1 insts)
Primitive AOI32X1 (2 insts)
Primitive AOI21XL (1 insts)
Primitive NOR2BXL (8 insts)
Primitive SDFFQX4 (8 insts)
Primitive NOR2XL (13 insts)
Primitive INVX1 (2 insts)
Primitive NOR3X1 (1 insts)
Primitive AOI31X1 (1 insts)
Primitive NOR3BX1 (1 insts)
Primitive NOR2BX1 (15 insts)
Primitive ADDHX1 (1 insts)
Primitive NAND2XL (12 insts)
Primitive NAND3X1 (1 insts)
Primitive ADDFX1 (2 insts)
Primitive XNOR2XL (1 insts)
Primitive NAND2BX1 (4 insts)
Primitive CLKINVX1 (4 insts)
Primitive OAI31X1 (2 insts)
Primitive AND3XL (1 insts)
Primitive OAI21X1 (1 insts)
Primitive AND2XL (1 insts)
Primitive XNOR2X1 (1 insts)
Primitive SDFFQX1 (17 insts)
Primitive OAI211X1 (3 insts)
Primitive CLKXOR2X1 (1 insts)
Primitive OAI2BB1X1 (1 insts**)**
****
*** Net length and connection length statistics (cell top) ***

Total net length = 1.390e+03 (6.511e+02 7.385e+02)

- Here, the total net length is **1390um**, **while in small utilization, it was 1503um.**

- ❖ This result is as per the expectation. I.e., Since the design is more closely packed, the wire length required to connect two cells becomes small, and hence, correctly exemplified by above numbers

Power Analysis

Power must be delivered to the cells from the topmost metal layers all the way down to the transistors, in a fashion that minimizes the overall resistance of the power wires without eating up all the resources that are needed for wiring the cells together.

Power Report

```
*-----------------------------------------------------------------------------------------
*    Innovus 20.10-p004_1 (64bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*-----------------------------------------------------------------------------------------
*
*    Design: top
*
*    Power Domain used:
*         Rail:    VDD    Voltage:         0.9
*
*         Primary Input Activity: 0.200000
*
*    Power Units = 1mW
*
*    Time Units = 1e-09 secs
*
*         Temperature = 125
*
-----------------------------------------------------------------------------------------
Cell                    Internal   Switching    Total    Leakage   Cell
                        Power          Power          Power          Power   Name
-----------------------------------------------------------------------------
out1/OUT_reg[0]              0.0042       0.01002       0.01444    0.0002172  SDFFQX4
out1/OUT_reg[1]              0.004015     0.008413      0.01265    0.0002172  SDFFQX4
out1/OUT_reg[2]              0.003773     0.006978      0.01097    0.0002172  SDFFQX4
out1/OUT_reg[3]              0.003597     0.006024      0.009839   0.0002172  SDFFQX4
out1/OUT_reg[4]              0.003186     0.003572      0.006974   0.0002172  SDFFQX4
out1/OUT_reg[5]              0.002903     0.002002      0.005122   0.0002172  SDFFQX4
out1/OUT_reg[6]              0.002749     0.001157      0.004123   0.0002172  SDFFQX4
in1/A_reg_reg[1]             0.00308      0.0004482     0.003664   0.0001363  SDFFQX1
in1/A_reg_reg[2]             0.003103     0.0004245     0.003663   0.0001363  SDFFQX1
in1/A_reg_reg[0]             0.003082     0.0003897     0.003608   0.0001363  SDFFQX1
bcd/OUT_reg[2]               0.003153     0.0002511     0.00354    0.0001363  SDFFQX1
out1/OUT_reg[7]              0.002656     0.0006441     0.003518   0.0002172  SDFFQX4
bcd/OUT_reg[1]               0.00313      0.0002469     0.003514   0.0001363  SDFFQX1
bcd/OUT_reg[3]               0.003131     0.0002041     0.003471   0.0001363  SDFFQX1
in1/C_reg_reg[5]             0.003068     0.0002648     0.003469   0.0001363  SDFFQX1
```

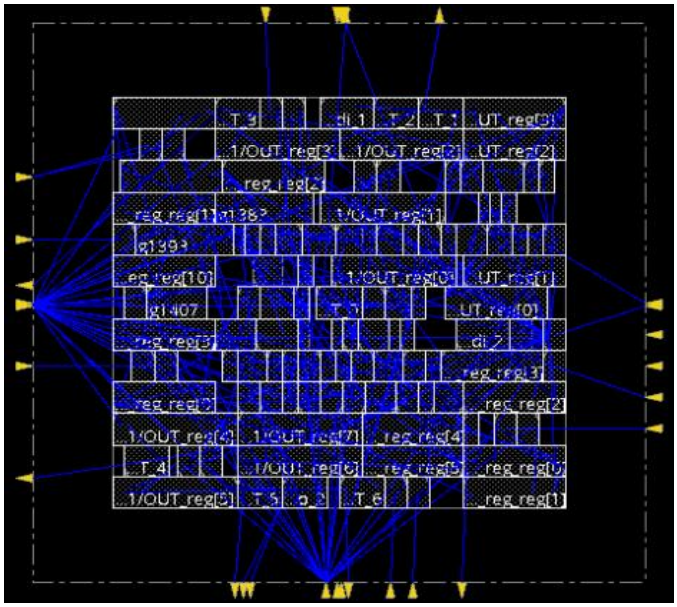
in1/A_reg_reg[3]	0.00308	0.0002266	0.003443	0.0001363	SDFFQX1
in1/B_reg_reg[12]	0.003087	0.0002042	0.003427	0.0001363	SDFFQX1
in1/B_reg_reg[11]	0.003079	0.0001995	0.003415	0.0001363	SDFFQX1
in1/C_reg_reg[4]	0.003041	0.0002209	0.003398	0.0001363	SDFFQX1
in1/C_reg_reg[0]	0.003083	0.0001481	0.003367	0.0001363	SDFFQX1
in1/B_reg_reg[10]	0.003082	0.0001472	0.003366	0.0001363	SDFFQX1
in1/C_reg_reg[1]	0.003081	0.0001149	0.003332	0.0001363	SDFFQX1
in1/C_reg_reg[3]	0.002974	0.0001864	0.003297	0.0001363	SDFFQX1
bcd/OUT_reg[0]	0.002909	0.0002356	0.00328	0.0001363	SDFFQX1
in1/C_reg_reg[2]	0.002816	0.0001304	0.003082	0.0001363	SDFFQX1
g1402	0.0006886	0.0002396	0.00095	2.186e-05	NOR3BX1
g1383	0.0005546	0.000165	0.0008041	8.448e-05	ADDFX1
g1393	0.0005334	0.000135	0.0007528	8.448e-05	ADDFX1
g1409	0.0005291	0.0001656	0.0007151	2.034e-05	NOR3X1
g1407	0.0004223	0.0001379	0.0006557	9.553e-05	ADDHX1
EPG/g39	0.0003736	0.0001324	0.0005765	7.055e-05	XNOR2X1
EPG/g40	0.0003708	0.0001303	0.0005736	7.254e-05	CLKXOR2X1
g1405	0.0002788	0.0002073	0.0005039	1.789e-05	AOI31X1
g1392	0.000322	0.0001016	0.0004421	1.851e-05	AOI32X1
EPG/g37	0.0002655	9.316e-05	0.0003716	1.299e-05	OAI21X1
g1404	0.000193	0.0001623	0.0003693	1.402e-05	OAI31X1
g1415	0.000204	0.0001462	0.0003626	1.236e-05	NOR2XL
bcd/g210	0.0002528	4.312e-05	0.0003589	6.308e-05	XNOR2XL
g1406	0.0001588	0.0001508	0.000322	1.236e-05	NOR2XL
g1384	0.0002381	6.855e-05	0.0003208	1.41e-05	OAI211X1
bcd/g219	0.000151	0.0001318	0.0003178	3.499e-05	NAND2BX1
g1381	0.0002118	5.921e-05	0.0002981	2.704e-05	MXI2XL
g1397	0.0001145	0.0001715	0.0002953	9.289e-06	NAND2XL
g1410	0.0001822	7.15e-05	0.0002887	3.499e-05	NAND2BX1
g1408	0.0001509	0.0001241	0.000288	1.301e-05	CLKINVX1
bcd/g221	0.0001857	5.433e-05	0.0002671	2.704e-05	MXI2XL
g1414	0.0001016	0.0001461	0.00026	1.236e-05	NOR2XL
in1/g29	0.000201	3.748e-05	0.0002585	2.004e-05	NOR2BX1
in1/g28	0.0002009	3.683e-05	0.0002578	2.004e-05	NOR2BX1
in1/g30	0.0002009	3.487e-05	0.0002558	2.004e-05	NOR2BX1
in1/g21	0.0002009	3.429e-05	0.0002552	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.181e-05	0.0002527	2.004e-05	NOR2BX1
in1/g27	0.0002008	3.131e-05	0.0002522	2.004e-05	NOR2BX1
in1/g23	0.0002008	3.031e-05	0.0002511	2.004e-05	NOR2BX1
in1/g19	0.0002008	3.006e-05	0.0002509	2.004e-05	NOR2BX1
in1/g22	0.0002008	3.006e-05	0.0002509	2.004e-05	NOR2BX1
in1/g20	0.0002008	3.002e-05	0.0002509	2.004e-05	NOR2BX1
in1/g18	0.0002008	2.981e-05	0.0002506	2.004e-05	NOR2BX1
in1/g24	0.0002008	2.909e-05	0.0002499	2.004e-05	NOR2BX1
in1/g25	0.0002008	2.879e-05	0.0002496	2.004e-05	NOR2BX1
bcd/g213	0.0001851	5.103e-05	0.0002484	1.22e-05	AOI21XL
g1403	9.119e-05	0.0001187	0.0002223	1.236e-05	NOR2XL
out1/g12	0.0001721	3.2e-05	0.0002207	1.662e-05	NOR2BXL
bcd/g218	0.0001647	4.209e-05	0.0002192	1.236e-05	NOR2XL
bcd/g224	0.0001186	8.265e-05	0.0002143	1.301e-05	INVX1

bcd/g217	0.000149	5.015e-05	0.0002115	1.236e-05	NOR2XL
g1419	0.0001269	7.081e-05	0.0002107	1.301e-05	CLKINVX1
bcd/g226	0.0001225	7.427e-05	0.0002098	1.301e-05	CLKINVX1
g1382	9.212e-05	9.24e-05	0.0001975	1.301e-05	CLKINVX1
EPG/g38	9.278e-05	9.525e-05	0.0001973	9.289e-06	NAND2XL
g1379	0.0001325	3.925e-05	0.000193	2.127e-05	OAI2BB1X1
g1385	0.000135	4.074e-05	0.0001898	1.41e-05	OAI211X1
bcd/g208	0.0001249	4.524e-05	0.0001825	1.236e-05	NOR2XL
bcd/g211	0.0001353	3.49e-05	0.0001825	1.236e-05	NOR2XL
g1418	7.885e-05	8.369e-05	0.0001756	1.301e-05	INVX1
g1411	4.852e-05	8.074e-05	0.0001642	3.499e-05	NAND2BX1
g1376	0.0001069	3.991e-05	0.0001609	1.41e-05	OAI211X1
g1401	9.138e-05	4.895e-05	0.0001554	1.511e-05	NAND3X1
out1/g14	0.0001133	2.358e-05	0.0001535	1.662e-05	NOR2BXL
g1396	9.283e-05	4.814e-05	0.0001533	1.236e-05	NOR2XL
g1417	4.86e-05	9.436e-05	0.0001523	9.289e-06	NAND2XL
bcd/g215	0.0001087	2.541e-05	0.0001464	1.236e-05	NOR2XL
bcd/g222	5.029e-05	8.527e-05	0.0001449	9.289e-06	NAND2XL
out1/g17	9.685e-05	2.223e-05	0.0001357	1.662e-05	NOR2BXL
g1380	8.692e-05	2.781e-05	0.0001332	1.851e-05	AOI32X1
out1/g16	9.113e-05	1.741e-05	0.0001252	1.662e-05	NOR2BXL
g1412	6.584e-05	2.313e-05	0.0001013	1.236e-05	NOR2XL
g1395	5.118e-05	4.063e-05	0.0001011	9.289e-06	NAND2XL
g1390	4.458e-05	1.585e-05	9.541e-05	3.499e-05	NAND2BX1
g1399	4.473e-05	3.532e-05	8.934e-05	9.289e-06	NAND2XL
g1398	4.176e-05	3.449e-05	8.555e-05	9.289e-06	NAND2XL
bcd/g216	4.656e-05	2.206e-05	8.098e-05	1.236e-05	NOR2XL
bcd/g220	4.071e-05	2.891e-05	8.008e-05	1.046e-05	NAND4XL
g1400	3.61e-05	3.374e-05	7.913e-05	9.289e-06	NAND2XL
g1413	3.518e-05	1.571e-05	7.623e-05	2.533e-05	AND3XL
g1416	4.22e-05	2.34e-05	7.489e-05	9.289e-06	NAND2XL
g1394	3.843e-05	1.908e-05	6.986e-05	1.236e-05	NOR2XL
g1387	2.453e-05	2.067e-05	5.45e-05	9.289e-06	NAND2XL
g1378	2.45e-05	7.26e-06	4.578e-05	1.402e-05	OAI31X1
g1377	2.003e-05	1.536e-05	4.468e-05	9.289e-06	NAND2XL
out1/g15	1.56e-05	2.927e-06	3.515e-05	1.662e-05	NOR2BXL
g1391	1.018e-05	1.82e-06	3.204e-05	2.004e-05	NOR2BX1
g1388	4.775e-06	1.657e-06	3.109e-05	2.466e-05	AND2XL
g1389	3.825e-06	5.369e-07	2.44e-05	2.004e-05	NOR2BX1
g1386	6.949e-06	6.483e-06	2.272e-05	9.289e-06	NAND2XL
out1/g11	4.037e-06	1.006e-06	2.167e-05	1.662e-05	NOR2BXL
out1/g18	3.95e-06	9.336e-07	2.151e-05	1.662e-05	NOR2BXL
out1/g13	1.488e-06	2.779e-07	1.839e-05	1.662e-05	NOR2BXL

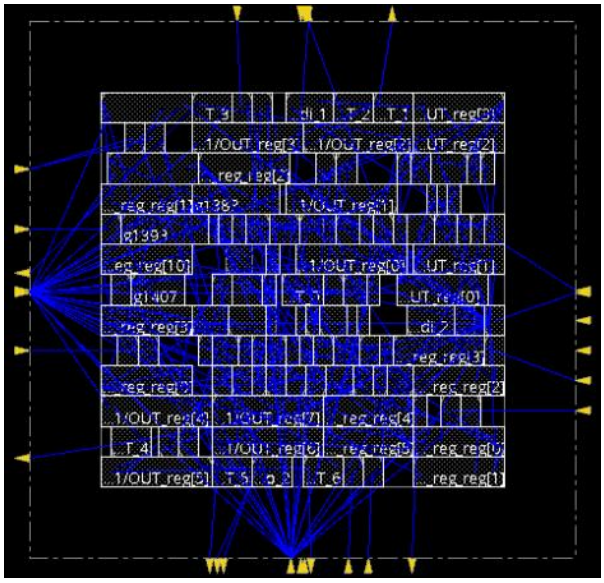
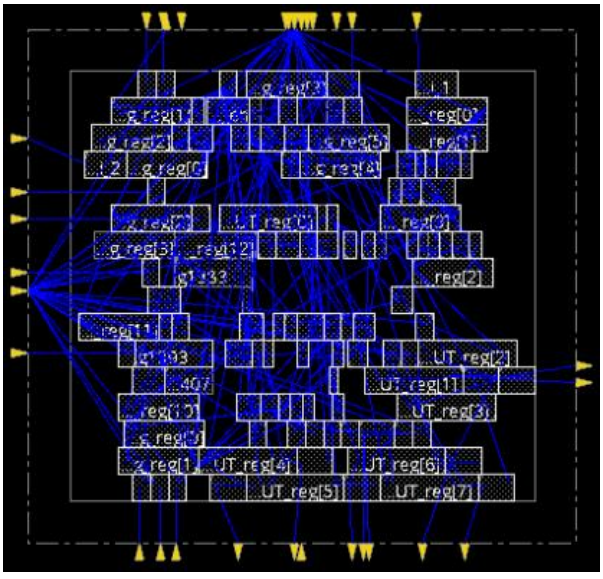
Total (108 of 108)	0.09162	0.04793	0.1453	0.005792
Total Capacitance	4.58e-12 F			
Power Density	*** No Die Area ***			

- As can be seen from the report after the placement the power comes out to be **0.1453mW**
- **In the case of small utilization**, the power reported was **0.1433mW**.
- Hence, a slight increase in power has been reported. It is expected that this slight increase can be attributed to the increased parasitic, as a consequence of more closely packed cells.

Layout Snapshot with Fly Lines:



Comparison of Layouts obtained in the different core utilization cases:

	
0.8 utilization	**0.5 utilization**

- In a design with high core utilization, it is expected that hotspots will be more dense (And hence, can be referred to as a Containment Zone) which is clearly visible from the above 2 images.
- Since the cells are more closely packed in high core utilization. There will be a huge cluster of connections from the cells, as there is less scope for keeping highly connected cells together. It can be done only to a very limited extent. Similar is exemplified by the following screenshot.

Clock Tree Synthesis Pre-Optimization

Time Design Summary after Clock Tree Synthesis Pre-Optimization

Pre-CTS optimization is the first round of Static Timing Analysis (STA) and optimization performed on the design. It has a large freedom to move the cells around to optimize your design to meet setup checks, and is performed after the initial cell placement. Hold errors are not checked during pre-CTS optimization. Because we do not have a clock tree in place yet, we do not know when the clocks will arrive to each sequential element, hence we don't know if there are hold violations. The tool therefore assumes that every sequential element receives the clock ideally at the same time, and tries to balance out the delays in data paths to ensure no setup violations occur.

A summary of **setup report** of the **timing design** of the post-placement design is given as follows:

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:58:39 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/postcts_bo/timing/timing_post_PnR_late.txt
#############################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.000
- Setup                         0.239
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.561
- Arrival Time                  1.971
= Slack Time                    3.590
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     = Beginpoint Arrival Time            1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.590 |
     | g1418           | A v -> Y ^  | INVX1     | 0.053 |   1.053 |    4.643 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.155 |   1.208 |    4.798 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.317 |   1.524 |    5.115 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.215 |   1.739 |    5.329 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.087 |   1.827 |    5.417 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.144 |   1.971 |    5.561 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.971 |    5.561 |
     +-------------------------------------------------------------------------+
```

Without routing optimization, the worst path gives a negative slack. The corresponding report is as follows:

```
#####################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:58:39 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/postcts_bo/timing/timing_post_PnR_early.txt
#####################################################
Path 1: VIOLATED Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                        -0.015
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.186
  Arrival Time                 0.000
  Slack Time                  -0.186
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------+
     |     Instance     |     Arc     |  Cell   | Delay | Arrival | Required |
     |                  |             |         |       |  Time   |   Time   |
     |------------------+-------------+---------+-------+---------+----------|
     |                  | DFT_sdi_2 v |         |       |   0.000 |    0.186 |
     | in1/C_reg_reg[2] | SI v        | SDFFQX1 | 0.000 |   0.000 |    0.186 |
     +-------------------------------------------------------------------------+
```

Area

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		116	1013.489	72.662	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	18	136.242	0.000	4.541	49.955	81.745
in1	FF_in	26	324.710	0.000	0.000	59.038	265.672
out1	FF_out	22	290.650	54.497	0.000	36.331	199.822

The total area that comes out to be 1013.489um^2 for total of 116 instances and they are for individual area of instances and number of primitives are:

Cell Type	Instance Count	Area per instance of cell(um^2)
MXI2XL	2	6.055200
NAND4XL	1	5.298300
AOI32X1	2	6.812100
AOI21XL	1	4.541400
NOR2BXL	8	4.541400
SDFFQX4	8	24.977700

NOR2XL	13	3.027600
INVX1	2	2.270700
NOR3X1	1	4.54140
AOI31X1	1	6.055200
NOR3BX1	1	6.055200
NOR2BX1	15	4.541400
ADDHX1	1	12.110400
NAND2XL	12	3.027600
NAND3X1	1	4.541400
ADDFX1	2	19.679400
XNOR2XL	1	8.325900
NAND2BX1	4	4.541400
CLKINVX1	4	2.270700
OAI31X1	2	6.055200
AND3XL	1	6.055200
OAI21X1	1	4.541400
CLKBUFX6	8	9.082800
AND2XL	1	4.541400
XNOR2X1	1	8.325900
SDFFQX1	17	20.436300
OAI211X1	3	5.298300
CLKXOR2X1	1	8.325900
OAI2BB1X1	1	5.424700

Power

```
*-----------------------------------------------------------------------------------
*
*   Power Domain used:
*         Rail:    VDD    Voltage:         0.9
*
*         Primary Input Activity: 0.200000
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*         Temperature = 125
*
*         report_power -outfile reports/postcts_bo/power/rtl_module.rpt -rail_analysis_format VS
*
-----------------------------------------------------------------------------------
Cell                    Internal  Switching    Total   Leakage   Cell
                        Power     Power        Power     Power   Name
-----------------------------------------------------------------------------
out1/FE_OFC5_OUT_1      0.0008673    0.008287      0.009276  0.0001212
CLKBUFX6
FE_OFC1_OUT_0           0.0008065    0.007757      0.008685  0.0001212
CLKBUFX6
out1/FE_OFC0_OUT_3      0.0007583    0.007302      0.008182  0.0001212
CLKBUFX6
out1/FE_OFC2_OUT_2      0.0006942    0.006652      0.007468  0.0001212
CLKBUFX6
out1/FE_OFC4_OUT_6      0.0005702    0.005463      0.006154  0.0001212
CLKBUFX6
out1/OUT_reg[1]         0.003901  9.779e-05 0.004216  0.0002172  SDFFQX4
out1/OUT_reg[0]         0.003871  8.166e-05 0.00417   0.0002172  SDFFQX4
out1/OUT_reg[3]         0.003783  7.678e-05 0.004077  0.0002172  SDFFQX4
out1/OUT_reg[2]         0.003689  7.341e-05 0.003979  0.0002172  SDFFQX4
out1/OUT_reg[6]         0.003437  5.796e-05 0.003713  0.0002172  SDFFQX4
in1/A_reg_reg[2]        0.003133     0.000436      0.003706  0.0001363  SDFFQX1
out1/FE_OFC6_OUT_5      0.0003395    0.00324       0.003701  0.0001212
CLKBUFX6
in1/A_reg_reg[1]        0.003089  0.00044980.003675  0.0001363  SDFFQX1
bcd/OUT_reg[0]          0.003205  0.00029590.003637  0.0001363  SDFFQX1
bcd/OUT_reg[1]          0.003223     0.000274      0.003634  0.0001363  SDFFQX1
in1/A_reg_reg[0]        0.003083     0.000393      0.003613  0.0001363  SDFFQX1
in1/B_reg_reg[12]       0.00311   0.0002101  0.003456  0.0001363  SDFFQX1
in1/A_reg_reg[3]        0.003083  0.00023110.003451  0.0001363  SDFFQX1
in1/B_reg_reg[11]       0.003095  0.00020370.003435  0.0001363  SDFFQX1
bcd/OUT_reg[2]          0.003046  0.00024240.003425  0.0001363  SDFFQX1
in1/C_reg_reg[5]        0.003005  0.00025980.003401  0.0001363  SDFFQX1
in1/B_reg_reg[10]       0.003088  0.00014780.003372  0.0001363  SDFFQX1
in1/C_reg_reg[0]        0.003084  0.00014510.003365  0.0001363  SDFFQX1
out1/OUT_reg[5]         0.0031   3.444e-05    0.003351  0.0002172  SDFFQX4
```

in1/C_reg_reg[1]	0.003081	0.0001144	0.003332	0.0001363	SDFFQX1
in1/C_reg_reg[4]	0.002992	0.0001972	0.003325	0.0001363	SDFFQX1
in1/C_reg_reg[3]	0.002974	0.000214	0.003324	0.0001363	SDFFQX1
out1/OUT_reg[4]	0.002915	2.292e-05	0.003155	0.0002172	SDFFQX4
bcd/OUT_reg[3]	0.002847	0.0001583	0.003142	0.0001363	SDFFQX1
in1/C_reg_reg[2]	0.002815	0.0001303	0.003082	0.0001363	SDFFQX1
out1/OUT_reg[7]	0.002755	1.386e-05	0.002986	0.0002172	SDFFQX4
out1/FE_OFC3_OUT_4	0.0002263	0.00217	0.002518	0.0001212	CLKBUFX6
FE_OFC7_DFT_sdo_2	0.0001288	0.001225	0.001475	0.0001212	CLKBUFX6
g1383	0.0005939	0.0001794	0.0008578	8.448e-05	ADDFX1
g1402	0.0005689	0.0002021	0.0007928	2.186e-05	NOR3BX1
g1393	0.0005466	0.0001394	0.0007705	8.448e-05	ADDFX1
g1409	0.0004916	0.0001538	0.0006657	2.034e-05	NOR3X1
g1407	0.000425	0.0001394	0.00066	9.553e-05	ADDHX1
EPG/g39	0.0003884	0.0001399	0.0005989	7.055e-05	XNOR2X1
EPG/g40	0.0003738	0.0001335	0.0005799	7.254e-05	CLKXOR2X1
g1405	0.000249	0.000189	0.0004559	1.789e-05	AOI31X1
g1392	0.0003299	0.0001043	0.0004527	1.851e-05	AOI32X1
EPG/g37	0.0002781	9.72e-05	0.0003883	1.299e-05	OAI21X1
g1415	0.0002041	0.0001478	0.0003643	1.236e-05	NOR2XL
g1406	0.0001649	0.0001571	0.0003344	1.236e-05	NOR2XL
bcd/g219	0.0001507	0.0001345	0.0003201	3.499e-05	NAND2BX1
bcd/g210	0.0002061	3.521e-05	0.0003044	6.308e-05	XNOR2XL
g1404	0.0001561	0.0001311	0.0003012	1.402e-05	OAI31X1
g1384	0.0002199	6.422e-05	0.0002983	1.41e-05	OAI211X1
bcd/g221	0.0002093	5.896e-05	0.0002953	2.704e-05	MXI2XL
g1381	0.0002069	5.961e-05	0.0002936	2.704e-05	MXI2XL
g1410	0.0001824	7.15e-05	0.0002888	3.499e-05	NAND2BX1
g1408	0.0001403	0.0001154	0.0002687	1.301e-05	CLKINVX1
g1414	0.000102	0.0001469	0.0002613	1.236e-05	NOR2XL
in1/g29	0.000201	3.769e-05	0.0002587	2.004e-05	NOR2BX1
in1/g28	0.0002009	3.679e-05	0.0002578	2.004e-05	NOR2BX1
in1/g30	0.0002009	3.472e-05	0.0002557	2.004e-05	NOR2BX1
in1/g21	0.0002009	3.444e-05	0.0002554	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.176e-05	0.0002526	2.004e-05	NOR2BX1
in1/g27	0.0002008	3.124e-05	0.0002521	2.004e-05	NOR2BX1
in1/g20	0.0002008	3.108e-05	0.0002519	2.004e-05	NOR2BX1
bcd/g217	0.0001792	6.026e-05	0.0002518	1.236e-05	NOR2XL
in1/g23	0.0002008	3.023e-05	0.0002511	2.004e-05	NOR2BX1
in1/g19	0.0002008	3.003e-05	0.0002509	2.004e-05	NOR2BX1
in1/g22	0.0002008	3.003e-05	0.0002509	2.004e-05	NOR2BX1
in1/g18	0.0002008	2.973e-05	0.0002505	2.004e-05	NOR2BX1
in1/g24	0.0002008	2.905e-05	0.0002499	2.004e-05	NOR2BX1
in1/g25	0.0002008	2.873e-05	0.0002495	2.004e-05	NOR2BX1
g1397	9.517e-05	0.000145	0.0002495	9.289e-06	NAND2XL
bcd/g213	0.0001772	4.796e-05	0.0002374	1.22e-05	AOI21XL
bcd/g224	0.0001285	8.578e-05	0.0002273	1.301e-05	INVX1
g1382	0.0001033	0.0001034	0.0002197	1.301e-05	CLKINVX1

bcd/g218	0.0001647	4.202e-05	0.000219	1.236e-05	NOR2XL
g1419	0.0001277	7.646e-05	0.0002172	1.301e-05	CLKINVX1
g1379	0.000148	4.122e-05	0.0002105	2.127e-05	OAI2BB1X1
out1/g12	0.0001627	3.04e-05	0.0002097	1.662e-05	NOR2BXL
EPG/g38	9.328e-05	9.555e-05	0.0001981	9.289e-06	NAND2XL
bcd/g226	0.000113	6.833e-05	0.0001944	1.301e-05	CLKINVX1
g1385	0.0001305	3.852e-05	0.0001832	1.41e-05	OAI211X1
bcd/g211	0.0001356	3.517e-05	0.0001832	1.236e-05	NOR2XL
bcd/g208	0.0001226	4.433e-05	0.0001792	1.236e-05	NOR2XL
g1403	7.154e-05	9.316e-05	0.0001771	1.236e-05	NOR2XL
g1418	7.885e-05	8.4e-05	0.0001759	1.301e-05	INVX1
g1411	4.887e-05	8.141e-05	0.0001653	3.499e-05	NAND2BX1
g1376	0.0001079	4.006e-05	0.0001621	1.41e-05	OAI211X1
g1417	4.881e-05	9.492e-05	0.000153	9.289e-06	NAND2XL
g1396	8.814e-05	4.985e-05	0.0001503	1.236e-05	NOR2XL
out1/g14	0.0001097	2.284e-05	0.0001492	1.662e-05	NOR2BXL
g1401	8.591e-05	4.654e-05	0.0001476	1.511e-05	NAND3X1
out1/g17	0.0001036	2.409e-05	0.0001443	1.662e-05	NOR2BXL
out1/g16	9.674e-05	1.878e-05	0.0001321	1.662e-05	NOR2BXL
bcd/g222	4.517e-05	7.75e-05	0.000132	9.289e-06	NAND2XL
bcd/g215	8.463e-05	1.987e-05	0.0001169	1.236e-05	NOR2XL
g1380	7.06e-05	2.25e-05	0.0001116	1.851e-05	AOI32X1
g1412	6.589e-05	2.372e-05	0.000102	1.236e-05	NOR2XL
g1400	4.426e-05	4.2e-05	9.555e-05	9.289e-06	NAND2XL
g1399	4.804e-05	3.733e-05	9.466e-05	9.289e-06	NAND2XL
g1398	4.607e-05	3.772e-05	9.308e-05	9.289e-06	NAND2XL
g1395	4.279e-05	3.389e-05	8.597e-05	9.289e-06	NAND2XL
g1390	3.574e-05	1.265e-05	8.338e-05	3.499e-05	NAND2BX1
bcd/g220	4.168e-05	3.006e-05	8.221e-05	1.046e-05	NAND4XL
g1413	3.524e-05	1.575e-05	7.631e-05	2.533e-05	AND3XL
g1416	4.233e-05	2.332e-05	7.494e-05	9.289e-06	NAND2XL
bcd/g216	4.07e-05	1.948e-05	7.254e-05	1.236e-05	NOR2XL
g1394	3.752e-05	1.864e-05	6.852e-05	1.236e-05	NOR2XL
g1387	1.893e-05	1.589e-05	4.411e-05	9.289e-06	NAND2XL
g1378	2.173e-05	6.578e-06	4.233e-05	1.402e-05	OAI31X1
g1377	1.546e-05	1.176e-05	3.651e-05	9.289e-06	NAND2XL
out1/g15	1.414e-05	2.655e-06	3.342e-05	1.662e-05	NOR2BXL
g1391	9.881e-06	1.781e-06	3.17e-05	2.004e-05	NOR2BX1
g1388	5.162e-06	1.853e-06	3.168e-05	2.466e-05	AND2XL
g1389	3.806e-06	5.356e-07	2.438e-05	2.004e-05	NOR2BX1
g1386	6.735e-06	6.137e-06	2.216e-05	9.289e-06	NAND2XL
out1/g18	4.286e-06	1.016e-06	2.193e-05	1.662e-05	NOR2BXL
out1/g11	3.927e-06	1.008e-06	2.156e-05	1.662e-05	NOR2BXL
out1/g13	1.483e-06	2.769e-07	1.838e-05	1.662e-05	NOR2BXL

Total (116 of 116)	0.0961	0.05161	0.1545	0.006762
Total Capacitance	4.638e-12 F			
Power Density	*** No Die Area****			

- Power consumed is 0.1545mW and total capacitance reported as 4.638pF.

❖ Clock Tree Synthesis Post-Optimization

Timing Report of Worst Path

- ❖ The worst path timing report of setup and hold time after CTS and optimization step has been given as follows. Kindly note, that all violating paths have been resolved by optimization step in the tool.

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:59:02 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/postcts_ao/timing/timing_post_PnR_late.txt
#####################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.000
- Setup                         0.240
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.560
- Arrival Time                  1.988
= Slack Time                    3.572
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     = Beginpoint Arrival Time            1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.572 |
     | g1418           | A v -> Y ^  | INVX1     | 0.055 |   1.055 |    4.627 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.158 |   1.213 |    4.785 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.330 |   1.543 |    5.115 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.214 |   1.757 |    5.329 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.086 |   1.843 |    5.415 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.145 |   1.988 |    5.560 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.988 |    5.560 |
     +-------------------------------------------------------------------------+
```

```
#############################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:59:02 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/postcts_ao/timing/timing_post_PnR_early.txt
#############################################################
Path 1: MET Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         0.016
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.216
  Arrival Time                 0.254
  Slack Time                   0.038
     Clock Rise Edge                     0.000
     + Input Delay                       0.000
     = Beginpoint Arrival Time           0.000
     +-------------------------------------------------------------------------------+
     |       Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                       |             |         |       |  Time   |   Time   |
     |-----------------------+-------------+---------+-------+---------+----------|
     |                       | DFT_sdi_2 v |         |       |   0.000 |   -0.038 |
     | in1/FE_PHC9_DFT_sdi_2 | A v -> Y v  | DLY1X4  | 0.254 |   0.254 |    0.216 |
     | in1/C_reg_reg[2]      | SI v        | SDFFQX1 | 0.000 |   0.254 |    0.216 |
     +-------------------------------------------------------------------------------+
```

- ❖ After the post clock optimization, the static timing violations are resolved the slack time in the setup timing analysis comes out to be 3.572 and the slack time in hold timing violation is positive now and comes out to be 0.030.
- ❖ This optimization of the violations is resolved by adding some additional clocked buffers in the violated circuit.
- ❖ Here, for the hold violations, the violations have been sorted by the tool using the opt command. As highlighted in the snapshot below snapshot, some instances of CLKBUFX4, DLY1X4, DLY1X1 have been inserted to increase the Arrival Time of the signal. Consequently, the slack associated with Hold calculations improve, and violations are handled.

Area of Standard Cells

```
Hinst Name          Module Name          Inst Count          Total Area              Buffer            Inverter         Combinational               Flop
-------------------------------------------------------------------------------------------------------------------------------------------------------
top                                             119            1039.224              98.397              13.624              379.964             547.239
 EPG                EPG_4bit                     4              24.221               0.000               0.000               24.221               0.000
 bcd                BCD_Counter                 19             146.839              10.597               4.541               49.955              81.745
 in1                FF_in                       27             335.307              10.597               0.000               59.038             265.672
 out1               FF_out                      22             290.650              54.497               0.000               36.331             199.822
```

Cell Type	Instance Count	Area per instance of cell(um^2)
MXI2XL	2	6.0552
DLY1X1	1	19.961
NAND4XL	1	5.2983
AOI32X1	2	6.8121

AOI21XL	1	4.5414
NOR2BXL	8	4.5414
SDFFQX4	8	24.9777
NOR2XL	13	3.0276
INVX1	2	2.2707
NOR3X1	1	4.5414
AOI31X1	1	6.0552
NOR3BX1	1	6.0552
NOR2BX1	15	4.5414
ADDHX1	1	12.1104
NAND2XL	12	3.0276
NAND3X1	1	4.5414
ADDFX1	2	19.6794
XNOR2XL	1	8.3259
NAND2BX1	4	4.5414
CLKINVX1	4	2.2707
OAI31X1	2	6.0552
AND3XL	1	6.0552
OAI21X1	1	4.5414
CLKBUFX6	8	9.0828
DLY1X4	3	19.97
AND2XL	1	4.5414
XNOR2X1	1	8.3259
SDFFQX1	17	20.4363
OAI211X1	3	5.2983
CLKXOR2X1	1	8.3259
OAI2BB1X1	1	5.4247

- Here also, the area of the individual cells is same as that of the post_Placement step. However, the additional components added are depicted in the following comparison:

Post Placement

Cell Type	Cell Type
MXI2XL	MXI2XL
NAND4XL	DLY1X1
AOI32X1	NAND4XL
AOI21XL	AOI32X1
NOR2BXL	AOI21XL
SDFFQX4	NOR2BXL
NOR2XL	SDFFQX4
INVX1	NOR2XL
NOR3X1	INVX1
AOI31X1	NOR3X1
NOR3BX1	AOI31X1
NOR2BX1	NOR3BX1
ADDHX1	NOR2BX1
NAND2XL	ADDHX1
NAND3X1	NAND2XL
ADDFX1	NAND3X1
XNOR2XL	ADDFX1
NAND2BX1	XNOR2XL
CLKINVX1	NAND2BX1
OAI31X1	CLKINVX1
AND3XL	OAI31X1
OAI21X1	AND3XL
AND2XL	OAI21X1
XNOR2X1	CLKBUFX6
SDFFQX1	DLY1X4
OAI211X1	AND2XL
CLKXOR2X1	XNOR2X1
OAI2BB1X1	SDFFQX1
	OAI211X1
	CLKXOR2X1
	OAI2BB1X1

Post CTS

Standard cell Counts:

*** 31 Primitives used Post-Optimize:	*** 28 Primitives used Pre-Optimize:
Primitive MXI2XL (2 insts)	Primitive MXI2XL (2 insts)
Primitive NAND4XL (1 insts)	Primitive NAND4XL (1 insts)
Primitive AOI32X1 (2 insts)	Primitive AOI32X1 (2 insts)
Primitive AOI21XL (1 insts)	Primitive AOI21XL (1 insts)
Primitive NOR2BXL (8 insts)	Primitive NOR2BXL (8 insts)
Primitive SDFFQX4 (8 insts)	Primitive SDFFQX4 (8 insts)
Primitive NOR2XL (13 insts)	Primitive NOR2XL (13 insts)
Primitive INVX1 (2 insts)	Primitive INVX1 (2 insts)
Primitive NOR3X1 (1 insts)	Primitive NOR3X1 (1 insts)
Primitive AOI31X1 (1 insts)	Primitive AOI31X1 (1 insts)
Primitive NOR3BX1 (1 insts)	Primitive NOR3BX1 (1 insts)
Primitive NOR2BX1 (15 insts)	Primitive NOR2BX1 (15 insts)
Primitive ADDHX1 (1 insts)	Primitive ADDHX1 (1 insts)
Primitive NAND2XL (12 insts)	Primitive NAND2XL (12 insts)
Primitive NAND3X1 (1 insts)	Primitive NAND3X1 (1 insts)
Primitive ADDFX1 (2 insts)	Primitive ADDFX1 (2 insts)
Primitive XNOR2XL (1 insts)	Primitive XNOR2XL (1 insts)
Primitive NAND2BX1 (4 insts)	Primitive NAND2BX1 (4 insts)
Primitive CLKINVX1 (4 insts)	Primitive CLKINVX1 (4 insts)
Primitive OAI31X1 (2 insts)	Primitive OAI31X1 (2 insts)
Primitive AND3XL (1 insts)	Primitive AND3XL (1 insts)
Primitive OAI21X1 (1 insts)	Primitive OAI21X1 (1 insts)
Primitive CLKBUFX6 (8 insts)	Primitive CLKBUFX6 (8 insts)
Primitive AND2XL (1 insts)	Primitive AND2XL (1 insts)
Primitive DLY1X4 (2 insts)	
Primitive XNOR2X1 (1 insts)	Primitive XNOR2X1 (1 insts)
Primitive SDFFQX1 (17 insts)	Primitive SDFFQX1 (17 insts)
Primitive OAI211X1 (3 insts)	Primitive OAI211X1 (3 insts)
Primitive CLKXOR2X1 (1 insts)	Primitive CLKXOR2X1 (1 insts)
Primitive CLKBUFX2 (1 insts)	
Primitive OAI2BB1X1 (1 insts)	Primitive OAI2BB1X1 (1 insts)

Power

```
*-----------------------------------------------------------------------------
*    Innovus 20.10-p004_1 (64 bit) 05/07/2020 20:02 (Linux 2.6.32-431.11.2.el6.x86_64)
*
*
*     Date & Time:    2022-Apr-30 12:58:59 (2022-Apr-30 07:28:59 GMT)
*
*-----------------------------------------------------------------------------
*
*    Power Domain used:
*          Rail:     VDD    Voltage:          0.9
*
```

```
*        Primary Input Activity: 0.200000
*
*   Power Units = 1mW
*
*   Time Units = 1e-09 secs
*
*        Temperature = 125
*
--------------------------------------------------------------------------------
Cell                    Internal  Switching    Total    Leakage   Cell
                        Power     Power        Power    Power     Name
--------------------------------------------------------------------------------
out1/FE_OFC5_OUT_1      0.0008651 0.008273     0.00926  0.0001212 CLKBUFX6
FE_OFC1_OUT_0           0.0007896 0.007598     0.008509 0.0001212 CLKBUFX6
out1/FE_OFC0_OUT_3      0.0007555 0.007278     0.008155 0.0001212 CLKBUFX6
out1/FE_OFC2_OUT_2      0.000697  0.00668      0.007498 0.0001212 CLKBUFX6
out1/FE_OFC4_OUT_6      0.0005677 0.00544      0.006129 0.0001212 CLKBUFX6
out1/OUT_reg[1]         0.00392   0.0001144    0.004252 0.0002172 SDFFQX4
out1/OUT_reg[0]         0.00387   8.603e-05    0.004173 0.0002172 SDFFQX4
out1/OUT_reg[3]         0.003802  8.593e-05    0.004105 0.0002172 SDFFQX4
out1/OUT_reg[2]         0.003713  8.448e-05    0.004015 0.0002172 SDFFQX4
out1/OUT_reg[6]         0.003457  6.376e-05    0.003738 0.0002172 SDFFQX4
in1/A_reg_reg[2]        0.003156  0.0004277    0.00372  0.0001363 SDFFQX1
in1/A_reg_reg[1]        0.003098  0.0004504    0.003685 0.0001363 SDFFQX1
out1/FE_OFC6_OUT_5      0.0003365 0.003215     0.003673 0.0001212 CLKBUFX6
bcd/OUT_reg[1]          0.003238  0.0002755    0.00365  0.0001363 SDFFQX1
in1/A_reg_reg[0]        0.003107  0.0003964    0.00364  0.0001363 SDFFQX1
bcd/OUT_reg[0]          0.00321   0.0002918    0.003638 0.0001363 SDFFQX1
in1/B_reg_reg[12]       0.003132  0.0002109    0.00348  0.0001363 SDFFQX1
in1/A_reg_reg[3]        0.003105  0.0002275    0.003469 0.0001363 SDFFQX1
in1/B_reg_reg[11]       0.003107  0.0001968    0.003441 0.0001363 SDFFQX1
bcd/OUT_reg[2]          0.003052  0.0002403    0.003428 0.0001363 SDFFQX1
in1/C_reg_reg[5]        0.003024  0.0002465    0.003407 0.0001363 SDFFQX1
in1/C_reg_reg[0]        0.003108  0.000145     0.003389 0.0001363 SDFFQX1
in1/B_reg_reg[10]       0.003104  0.0001473    0.003388 0.0001363 SDFFQX1
out1/OUT_reg[5]         0.00312   3.783e-05    0.003375 0.0002172 SDFFQX4
in1/C_reg_reg[1]        0.003105  0.0001128    0.003354 0.0001363 SDFFQX1
in1/C_reg_reg[3]        0.002998  0.0002104    0.003344 0.0001363 SDFFQX1
in1/C_reg_reg[4]        0.003006  0.0001876    0.00333  0.0001363 SDFFQX1
out1/OUT_reg[4]         0.002971  3.05e-05     0.003219 0.0002172 SDFFQX4
bcd/OUT_reg[3]          0.002869  0.0001584    0.003164 0.0001363 SDFFQX1
in1/C_reg_reg[2]        0.002839  0.0001292    0.003104 0.0001363 SDFFQX1
out1/OUT_reg[7]         0.002818  2.039e-05    0.003055 0.0002172 SDFFQX4
out1/FE_OFC3_OUT_4      0.0002602 0.002496     0.002877 0.0001212 CLKBUFX6
FE_OFC7_DFT_sdo_2       0.0001547 0.001473     0.001749 0.0001212 CLKBUFX6
FE_PHC8_scan_en         0.000144  0.0009357    0.001121 4.129e-05 CLKBUFX2
g1383                   0.0005952 0.0001767    0.0008563 8.448e-05 ADDFX1
g1402                   0.0005654 0.0002002    0.0007875 2.186e-05 NOR3BX1
g1393                   0.000543  0.00014      0.0007675 8.448e-05 ADDFX1
g1407                   0.0004265 0.0001391    0.0006611 9.553e-05 ADDHX1
```

g1409	0.000485	0.00014960.000655	2.034e-05	NOR3X1	
EPG/g39	0.0003874	0.00014	0.000598	7.055e-05	XNOR2X1
EPG/g40	0.0003719	0.0001332	0.0005777	7.254e-05	CLKXOR2X1
bcd/FE_PHC10_DFT_sdi_1	0.0003597	2.376e-05	0.0004847	0.0001012	DLY1X4
in1/FE_PHC9_DFT_sdi_2	0.0003598	2.336e-05	0.0004843	0.0001012	DLY1X4
g1405	0.0002463	0.0001891	0.0004534	1.789e-05	AOI31X1
g1392	0.0003239	0.000104	0.0004463	1.851e-05	AOI32X1
EPG/g37	0.000277	9.696e-05	0.0003869	1.299e-05	OAI21X1
g1415	0.0002042	0.0001472	0.0003638	1.236e-05	NOR2XL
g1406	0.0001635	0.0001611	0.0003369	1.236e-05	NOR2XL
bcd/g210	0.0002201	3.768e-05	0.0003209	6.308e-05	XNOR2XL
bcd/g219	0.0001507	0.0001345	0.0003201	3.499e-05	NAND2BX1
g1384	0.0002171	7.686e-05	0.0003081	1.41e-05	OAI211X1
g1404	0.0001544	0.0001293	0.0002977	1.402e-05	OAI31X1
bcd/g221	0.0002084	5.905e-05	0.0002945	2.704e-05	MXI2XL
g1381	0.0002063	5.613e-05	0.0002895	2.704e-05	MXI2XL
g1410	0.0001822	7.136e-05	0.0002886	3.499e-05	NAND2BX1
g1414	0.0001024	0.0001551	0.0002699	1.236e-05	NOR2XL
g1408	0.0001382	0.0001152	0.0002664	1.301e-05	CLKINVX1
in1/g29	0.0002009	3.75e-05	0.0002585	2.004e-05	NOR2BX1
in1/g19	0.0002009	3.619e-05	0.0002571	2.004e-05	NOR2BX1
in1/g30	0.0002009	3.454e-05	0.0002555	2.004e-05	NOR2BX1
in1/g21	0.0002009	3.429e-05	0.0002552	2.004e-05	NOR2BX1
in1/g18	0.0002009	3.356e-05	0.0002545	2.004e-05	NOR2BX1
in1/g28	0.0002008	3.241e-05	0.0002533	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.212e-05	0.000253	2.004e-05	NOR2BX1
in1/g27	0.0002008	3.112e-05	0.000252	2.004e-05	NOR2BX1
in1/g20	0.0002008	3.094e-05	0.0002518	2.004e-05	NOR2BX1
in1/g23	0.0002008	3.063e-05	0.0002515	2.004e-05	NOR2BX1
in1/g24	0.0002008	3e-05	0.0002508	2.004e-05	NOR2BX1
in1/g22	0.0002008	2.952e-05	0.0002503	2.004e-05	NOR2BX1
in1/g25	0.0002007	2.866e-05	0.0002494	2.004e-05	NOR2BX1
bcd/g213	0.0001845	5.008e-05	0.0002468	1.22e-05	AOI21XL
bcd/g217	0.0001786	5.368e-05	0.0002446	1.236e-05	NOR2XL
g1397	9.286e-05	0.0001392	0.0002413	9.289e-06	NAND2XL
bcd/g224	0.0001283	8.867e-05	0.00023	1.301e-05	INVX1
g1382	0.000104	0.0001058	0.0002228	1.301e-05	CLKINVX1
bcd/g218	0.0001639	4.174e-05	0.000218	1.236e-05	NOR2XL
g1419	0.0001264	7.021e-05	0.0002096	1.301e-05	CLKINVX1
g1379	0.0001465	3.908e-05	0.0002068	2.127e-05	OAI2BB1X1
out1/g12	0.0001581	3.025e-05	0.000205	1.662e-05	NOR2BXL
EPG/g38	9.371e-05	9.638e-05	0.0001994	9.289e-06	NAND2XL
bcd/g226	0.0001097	7.078e-05	0.0001935	1.301e-05	CLKINVX1
g1385	0.0001299	4.591e-05	0.0001899	1.41e-05	OAI211X1
bcd/g211	0.0001334	3.445e-05	0.0001802	1.236e-05	NOR2XL
bcd/g208	0.0001231	4.464e-05	0.0001801	1.236e-05	NOR2XL
g1418	7.884e-05	8.588e-05	0.0001777	1.301e-05	INVX1
g1403	7.094e-05	8.718e-05	0.0001705	1.236e-05	NOR2XL
g1411	4.952e-05	8.488e-05	0.0001694	3.499e-05	NAND2BX1
g1376	0.0001072	4.619e-05	0.0001675	1.41e-05	OAI211X1

g1417	4.897e-05	9.762e-05	0.0001559	9.289e-06	NAND2XL
out1/g14	0.0001091	2.228e-05	0.000148	1.662e-05	NOR2BXL
g1401	8.509e-05	4.607e-05	0.0001463	1.511e-05	NAND3X1
g1396	8.564e-05	4.654e-05	0.0001445	1.236e-05	NOR2XL
out1/g17	0.0001029	2.454e-05	0.0001441	1.662e-05	NOR2BXL
out1/g16	9.62e-05	1.831e-05	0.0001311	1.662e-05	NOR2BXL
bcd/g222	4.377e-05	7.426e-05	0.0001273	9.289e-06	NAND2XL
bcd/g215	8.122e-05	1.911e-05	0.0001127	1.236e-05	NOR2XL
g1380	7.116e-05	2.115e-05	0.0001108	1.851e-05	AOI32X1
g1412	6.598e-05	2.314e-05	0.0001015	1.236e-05	NOR2XL
g1398	4.559e-05	4.182e-05	9.67e-05	9.289e-06	NAND2XL
g1400	4.394e-05	4.229e-05	9.551e-05	9.289e-06	NAND2XL
g1399	4.678e-05	3.71e-05	9.318e-05	9.289e-06	NAND2XL
g1395	4.415e-05	3.361e-05	8.705e-05	9.289e-06	NAND2XL
g1390	3.615e-05	1.269e-05	8.382e-05	3.499e-05	NAND2BX1
bcd/g220	4.183e-05	3.089e-05	8.318e-05	1.046e-05	NAND4XL
g1413	3.535e-05	1.574e-05	7.642e-05	2.533e-05	AND3XL
g1416	4.231e-05	2.323e-05	7.483e-05	9.289e-06	NAND2XL
g1394	3.855e-05	2.184e-05	7.274e-05	1.236e-05	NOR2XL
bcd/g216	3.473e-05	1.664e-05	6.373e-05	1.236e-05	NOR2XL
g1387	1.888e-05	1.591e-05	4.407e-05	9.289e-06	NAND2XL
g1378	2.048e-05	7.123e-06	4.163e-05	1.402e-05	OAI31X1
g1377	1.532e-05	1.2e-05	3.661e-05	9.289e-06	NAND2XL
out1/g15	1.327e-05	2.469e-06	3.236e-05	1.662e-05	NOR2BXL
g1391	9.786e-06	1.921e-06	3.175e-05	2.004e-05	NOR2BX1
g1388	4.983e-06	1.733e-06	3.138e-05	2.466e-05	AND2XL
g1389	4.032e-06	5.878e-07	2.466e-05	2.004e-05	NOR2BX1
out1/g18	4.1e-06	9.487e-07	2.167e-05	1.662e-05	NOR2BXL
g1386	6.65e-06	5.513e-06	2.145e-05	9.289e-06	NAND2XL
out1/g11	3.891e-06	8.477e-07	2.136e-05	1.662e-05	NOR2BXL
out1/g13	1.567e-06	2.964e-07	1.849e-05	1.662e-05	NOR2BXL

Total (119 of 119)	0.09748	0.05298	0.1575	0.007005
Total Capacitance	4.769e-12 F			
Power Density	*** No Die Area ***			

- Here, the results are as per the expectations.
- After the clock optimization it is observed that the total power is increased to 0.1575mW and so is the total capacitance to 4.769pF this is due to the fact that post clock optimization added some additional clocked buffer to the path.

Clock Tree Synthesis (CTS)

CTS is arguably the next most important step in Place and Route behind floor planning. Recalling that up until this point, we have not talked about the clock that triggers all the sequential logic in our design. This is because the clock signal is assumed to arrive at every

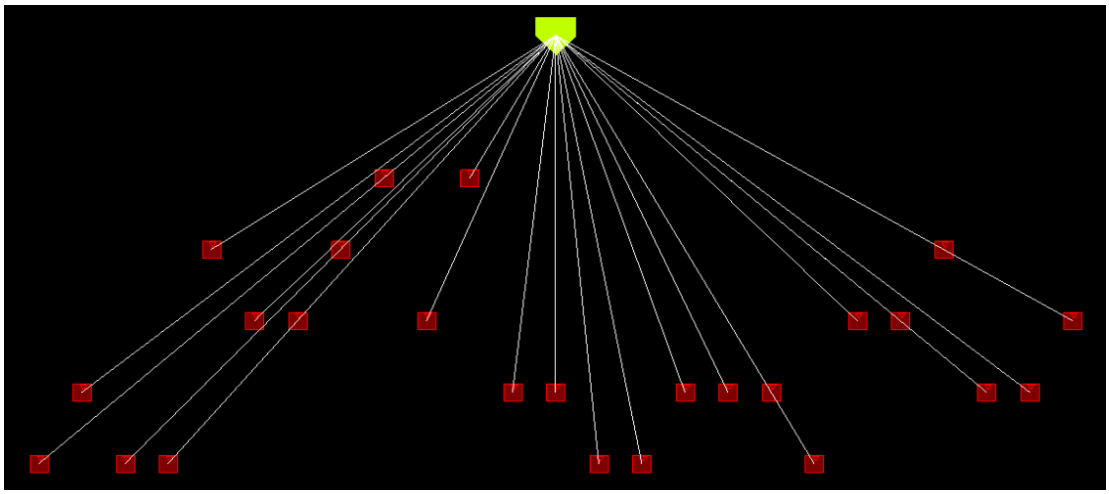
sequential element in our design at the same time. The synthesis tool makes this assumption and so does the initial cell placement algorithm. In reality, the sequential elements have to be placed wherever makes the most sense (e.g., to minimize delays between them). As a result, there is a different amount of delay to every element from the top-level clock pin that must be “balanced” to maintain the timing results from synthesis. Here complete routing of the clock is done. The main job of the CTS is to insert a clocked buffer and interconnections from the clock source to the register clock pin.

The meat of CTS is accomplished after initial optimization. The CTS algorithm first clusters groups of sequential elements together, mostly based on where they are in the design relative to the top-level clock pin and common clock gating logic. The number of elements in each cluster is selected so that it does not present too large of a load to a driving cell. These clusters of sequential elements are the “leaves” of the clock tree attached to branches.

Next, the CTS algorithm tries to ensure that the delay from the top-level clock pin to the leaves are all the same. It accomplishes this by adding and sizing clock buffers between the top-level pin and the leaves. There may be multiple stages of clock buffering, depending on how physically large the design is. Each clock buffer that drives multiple loads is a branching point in the clock tree, and strings of clock buffers in a row are essentially the “trunks”. Finally, the top-level clock pin is considered the “root” of the clock tree.

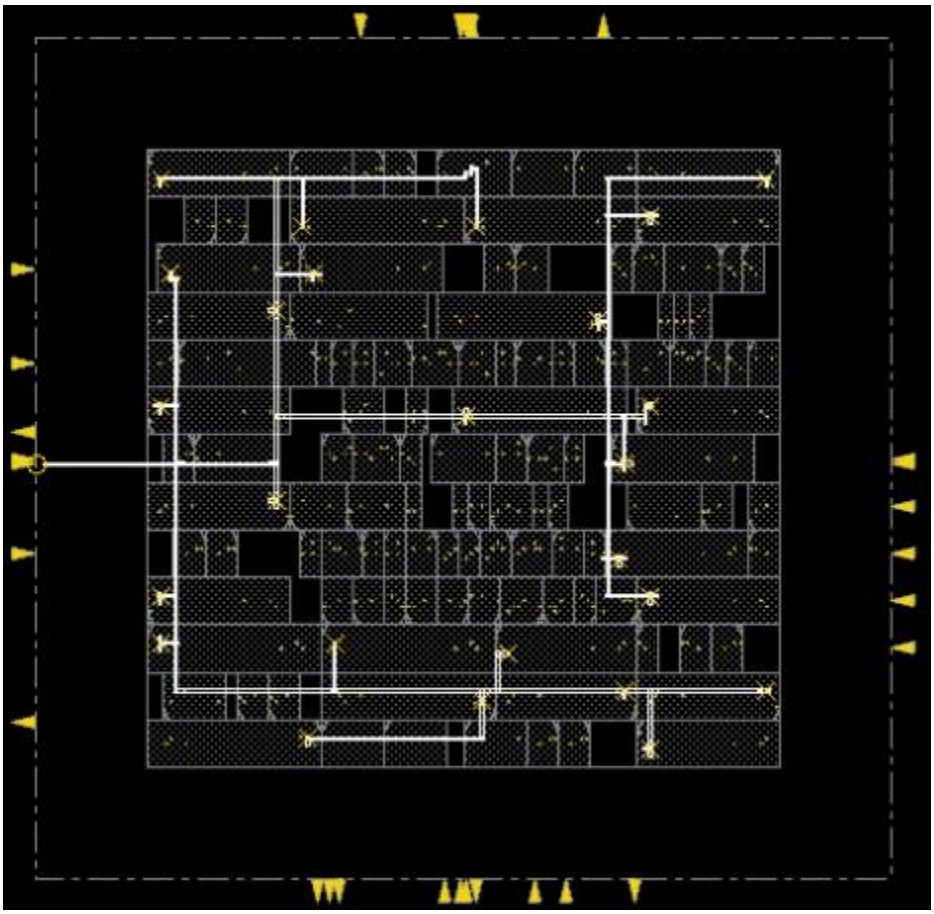
Post-CTS optimization is then performed, where clock is now a real signal that is being distributed unequally to different parts of the design. In this step, the tool fixes setup and hold time violations simultaneously.

We can also see the clock tree in its “tree” form by going to the menu Clock → CCOpt Clock Tree Debugger and pressing OK in the popup dialog. A window should pop up looking approximately like this:



The red dots are the “leaves” and the green pin on top is the clock pin or the clock “root”. After clicking the arc, we are able to observe the clock path in the layout.

This is the layout with clock path in bold white line after removing all the layers:



❖ Routing

In routing, given a placement, a netlist and technology information, it determines the necessary wiring, e.g., net topologies and specific routing segments, to connect these cells, while respecting constraints, e.g., design rules and routing resource capacities, and optimizing routing objectives, e.g., minimizing total wirelength and maximizing timing slack.

Time Design Summary

A summary of **setup report** of the timing design of the post-placement design is given as follows:

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:59:07 2022
#  Design:            top
#  Command:           report_timing -late  -max_paths 100 > reports/route/timing/timing_post_PnR_late.txt
#####################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.000
- Setup                         0.239
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.562
- Arrival Time                  1.990
= Slack Time                    3.572
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     = Beginpoint Arrival Time            1.000
     +-------------------------------------------------------------------------+
     |    Instance     |     Arc     |   Cell    | Delay | Arrival | Required |
     |                 |             |           |       |  Time   |   Time   |
     |-----------------+-------------+-----------+-------+---------+----------|
     |                 | rst v       |           |       |   1.000 |    4.572 |
     | g1418           | A v -> Y ^  | INVX1     | 0.049 |   1.049 |    4.621 |
     | g1417           | B ^ -> Y v  | NAND2XL   | 0.157 |   1.205 |    4.777 |
     | g1414           | B v -> Y ^  | NOR2XL    | 0.338 |   1.543 |    5.115 |
     | g1380           | A2 ^ -> Y v | AOI32X1   | 0.217 |   1.760 |    5.332 |
     | g1379           | B0 v -> Y ^ | OAI2BB1X1 | 0.087 |   1.847 |    5.419 |
     | out1/g17        | AN ^ -> Y ^ | NOR2BXL   | 0.143 |   1.990 |    5.562 |
     | out1/OUT_reg[2] | D ^         | SDFFQX4   | 0.000 |   1.990 |    5.562 |
     +-------------------------------------------------------------------------+
```

A summary of **hold report** of the timing design of the post-placement design is given as follows:

```
#####################################################################
#  Generated by:      Cadence Innovus 20.10-p004_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Sat Apr 30 12:59:07 2022
#  Design:            top
#  Command:           report_timing -early -view {view1} -max_paths 100 > reports/route/
#####################################################################
Path 1: MET Hold Check with Pin in1/C_reg_reg[2]/CK
Endpoint:   in1/C_reg_reg[2]/SI (v) checked with  leading edge of 'mclk'
Beginpoint: DFT_sdi_2           (v) triggered by  leading edge of '@'
Path Groups: {mclk}
Analysis View: view1
Other End Arrival Time          0.001
+ Hold                         0.016
+ Phase Shift                  0.000
+ Uncertainty                  0.200
= Required Time                0.217
  Arrival Time                 0.254
  Slack Time                   0.038
     Clock Rise Edge                      0.000
     + Input Delay                        0.000
     = Beginpoint Arrival Time            0.000
     +-------------------------------------------------------------------------------+
     |       Instance        |     Arc     |  Cell   | Delay | Arrival | Required |
     |                       |             |         |       |  Time   |   Time   |
     |-----------------------+-------------+---------+-------+---------+----------|
     |                       | DFT_sdi_2 v |         |       |   0.000 |   -0.038 |
     | in1/FE_PHC9_DFT_sdi_2 | A v -> Y v  | DLY1X4  | 0.254 |   0.254 |    0.217 |
     | in1/C_reg_reg[2]      | SI v        | SDFFQX1 | 0.000 |   0.254 |    0.217 |
     +-------------------------------------------------------------------------------+
```

In case of Hold Violations, the routing step has considered the buffers added in the CTS stage, and correspondingly, no hold violations have been found in routing steps.

Area

Hinst Name	Module Name	Inst Count	Total Area	Buffer	Inverter	Combinational	Flop
top		119	1039.224	98.397	13.624	379.964	547.239
EPG	EPG_4bit	4	24.221	0.000	0.000	24.221	0.000
bcd	BCD_Counter	19	146.839	10.597	4.541	49.955	81.745
in1	FF_in	27	335.307	10.597	0.000	59.038	265.672
out1	FF_out	22	290.650	54.497	0.000	36.331	199.822

- Now, comparing the area of the standard cells obtained after post-routing, and the post-CTS stage, it is noticed that though the area remains as it is for most of the cells.

Power

The power consumption for this design are as follows:

```
*    Power Domain used:
*          Rail:    VDD    Voltage:         0.9
*
```

```
*
*         Primary Input Activity: 0.200000
*
*          Power Units = 1mW
*
*          Time Units = 1e-09 secs
*
*         Temperature = 125
*
--------------------------------------------------------------------------------
Cell                    Internal  Switching    Total          Leakage    Cell
                Power          Power          Power          Power      Name
--------------------------------------------------------------------------------
out1/FE_OFC5_OUT_1      0.0008652     0.008273 0.009259   0.0001212  CLKBUFX6
FE_OFC1_OUT_0           0.0007896     0.007599 0.00851    0.0001212  CLKBUFX6
out1/FE_OFC0_OUT_3      0.0007555     0.007282 0.008159   0.0001212  CLKBUFX6
out1/FE_OFC2_OUT_2     0.000697    0.006679    0.007498   0.0001212  CLKBUFX6
out1/FE_OFC4_OUT_6      0.0005678     0.00544  0.006129   0.0001212  CLKBUFX6
out1/OUT_reg[1]        0.003922   0.0001097          0.004248   0.0002172  SDFFQX4
out1/OUT_reg[0]        0.00387   8.578e-05   0.004173   0.0002172  SDFFQX4
out1/OUT_reg[3]        0.003802   8.573e-05 0.004105   0.0002172  SDFFQX4
out1/OUT_reg[2]        0.003714   8.326e-05 0.004014   0.0002172  SDFFQX4
out1/OUT_reg[6]        0.003458   6.361e-05 0.003738   0.0002172  SDFFQX4
in1/A_reg_reg[2]       0.003157   0.0004275 0.00372    0.0001363  SDFFQX1
in1/A_reg_reg[1]       0.003099    0.00044670.003682   0.0001363  SDFFQX1
out1/FE_OFC6_OUT_5      0.0003365     0.003215    0.003673   0.0001212  CLKBUFX6
bcd/OUT_reg[1]         0.003239    0.0002788          0.003654   0.0001363  SDFFQX1
in1/A_reg_reg[0]       0.003108    0.0004072          0.003651   0.0001363  SDFFQX1
bcd/OUT_reg[0]         0.003211    0.0002941          0.003641   0.0001363  SDFFQX1
in1/B_reg_reg[12]      0.003133    0.0002305          0.0035     0.0001363  SDFFQX1
in1/A_reg_reg[3]       0.003106       0.000228        0.00347    0.0001363  SDFFQX1
in1/B_reg_reg[11]      0.003108    0.0002128          0.003457   0.0001363  SDFFQX1
bcd/OUT_reg[2]         0.003052    0.0002412          0.00343    0.0001363  SDFFQX1
in1/C_reg_reg[5]       0.003025    0.0002454          0.003407   0.0001363  SDFFQX1
in1/C_reg_reg[0]       0.003109    0.0001486          0.003394   0.0001363  SDFFQX1
in1/B_reg_reg[10]      0.003105    0.0001483          0.00339    0.0001363  SDFFQX1
out1/OUT_reg[5]        0.00312     4.116e-05          0.003379   0.0002172  SDFFQX4
in1/C_reg_reg[3]       0.002998    0.0002183          0.003353   0.0001363  SDFFQX1
in1/C_reg_reg[1]       0.003106    0.0001069          0.003349   0.0001363  SDFFQX1
in1/C_reg_reg[4]       0.003007    0.0001894          0.003333   0.0001363  SDFFQX1
out1/OUT_reg[4]        0.002971    3.045e-05          0.003219   0.0002172  SDFFQX4
bcd/OUT_reg[3]         0.00287     0.0001566          0.003163   0.0001363  SDFFQX1
in1/C_reg_reg[2]       0.002839    0.0001254          0.003101   0.0001363  SDFFQX1
out1/OUT_reg[7]        0.002818    2.069e-05          0.003056   0.0002172  SDFFQX4
out1/FE_OFC3_OUT_4      0.0002602     0.002496    0.002877   0.0001212  CLKBUFX6
FE_OFC7_DFT_sdo_2       0.0001547     0.001472    0.001748   0.0001212  CLKBUFX6
FE_PHC8_scan_en       0.000144   0.000954       0.001139   4.129e-05  CLKBUFX2
g1383                  0.0005956   0.0001733   0.0008534   8.448e-05  ADDFX1
g1402                  0.0005656   0.0001952   0.0007826   2.186e-05  NOR3BX1
g1393                  0.0005431      0.00014     0.0007675   8.448e-05  ADDFX1
```

g1407	0.0004266	0.000147	0.0006692	9.553e-05	ADDHX1
g1409	0.000485	0.000153	0.0006583	2.034e-05	NOR3X1
EPG/g39	0.0003874	0.0001416	0.0005996	7.055e-05	XNOR2X1
EPG/g40	0.0003722	0.0001305	0.0005753	7.254e-05	CLKXOR2X1
in1/FE_PHC9_DFT_sdi_2	0.0003597	2.396e-05	0.0004848	0.0001012	DLY1X4
bcd/FE_PHC10_DFT_sdi_1	0.0003597	2.357e-05	0.0004845	0.0001012	DLY1X4
g1405	0.0002463	0.0001895	0.0004537	1.789e-05	AOI31X1
g1392	0.0003242	0.0001038	0.0004465	1.851e-05	AOI32X1
EPG/g37	0.0002768	9.692e-05	0.0003867	1.299e-05	OAI21X1
g1415	0.0002042	0.0001446	0.0003611	1.236e-05	NOR2XL
g1406	0.0001635	0.0001589	0.0003348	1.236e-05	NOR2XL
bcd/g210	0.0002199	4.577e-05	0.0003288	6.308e-05	XNOR2XL
bcd/g219	0.0001506	0.0001357	0.0003213	3.499e-05	NAND2BX1
g1404	0.0001544	0.0001296	0.000298	1.402e-05	OAI31X1
g1384	0.000217	6.666e-05	0.0002978	1.41e-05	OAI211X1
bcd/g221	0.0002084	5.776e-05	0.0002932	2.704e-05	MXI2XL
g1410	0.000182	7.049e-05	0.0002874	3.499e-05	NAND2BX1
g1381	0.0002064	4.994e-05	0.0002833	2.704e-05	MXI2XL
g1414	0.0001024	0.00016	0.0002748	1.236e-05	NOR2XL
g1408	0.0001385	0.0001125	0.0002641	1.301e-05	CLKINVX1
in1/g19	0.0002009	3.534e-05	0.0002563	2.004e-05	NOR2BX1
in1/g30	0.0002009	3.458e-05	0.0002555	2.004e-05	NOR2BX1
in1/g18	0.0002009	3.458e-05	0.0002555	2.004e-05	NOR2BX1
in1/g21	0.0002009	3.437e-05	0.0002553	2.004e-05	NOR2BX1
in1/g28	0.0002008	3.245e-05	0.0002533	2.004e-05	NOR2BX1
in1/g27	0.0002008	3.113e-05	0.000252	2.004e-05	NOR2BX1
in1/g26	0.0002008	3.014e-05	0.000251	2.004e-05	NOR2BX1
in1/g29	0.0002008	3.003e-05	0.0002509	2.004e-05	NOR2BX1
in1/g24	0.0002008	3.003e-05	0.0002509	2.004e-05	NOR2BX1
in1/g20	0.0002008	2.997e-05	0.0002508	2.004e-05	NOR2BX1
in1/g23	0.0002008	2.965e-05	0.0002505	2.004e-05	NOR2BX1
in1/g25	0.0002008	2.965e-05	0.0002505	2.004e-05	NOR2BX1
in1/g22	0.0002008	2.958e-05	0.0002504	2.004e-05	NOR2BX1
bcd/g213	0.0001845	4.844e-05	0.0002452	1.22e-05	AOI21XL
bcd/g217	0.0001786	5.376e-05	0.0002447	1.236e-05	NOR2XL
g1397	9.276e-05	0.0001342	0.0002363	9.289e-06	NAND2XL
bcd/g224	0.0001285	8.675e-05	0.0002282	1.301e-05	INVX1
g1382	0.000104	0.0001084	0.0002254	1.301e-05	CLKINVX1
bcd/g218	0.0001639	4.175e-05	0.000218	1.236e-05	NOR2XL
g1419	0.0001261	7.156e-05	0.0002106	1.301e-05	CLKINVX1
g1379	0.0001466	3.914e-05	0.000207	2.127e-05	OAI2BB1X1
out1/g12	0.0001578	2.96e-05	0.000204	1.662e-05	NOR2BXL
EPG/g38	9.364e-05	9.183e-05	0.0001948	9.289e-06	NAND2XL
bcd/g226	0.0001099	6.605e-05	0.000189	1.301e-05	CLKINVX1
g1385	0.0001298	4.244e-05	0.0001864	1.41e-05	OAI211X1
bcd/g211	0.0001334	3.449e-05	0.0001802	1.236e-05	NOR2XL
bcd/g208	0.0001231	4.451e-05	0.0001799	1.236e-05	NOR2XL
g1403	7.09e-05	9.312e-05	0.0001764	1.236e-05	NOR2XL
g1411	4.957e-05	9.118e-05	0.0001757	3.499e-05	NAND2BX1
g1376	0.0001071	4.651e-05	0.0001677	1.41e-05	OAI211X1

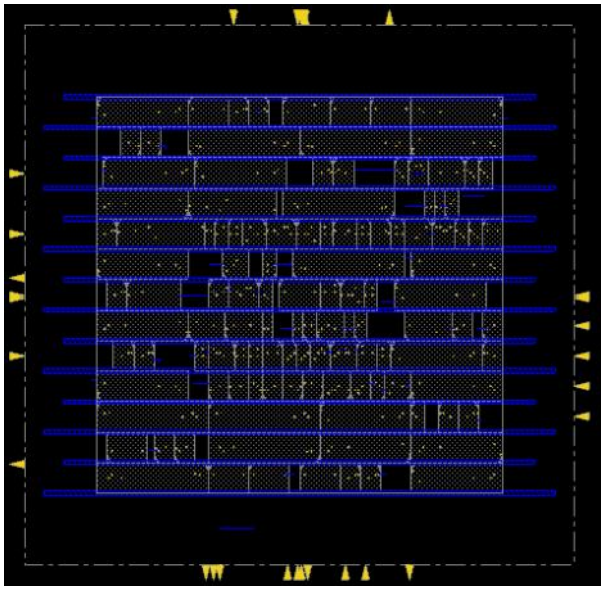
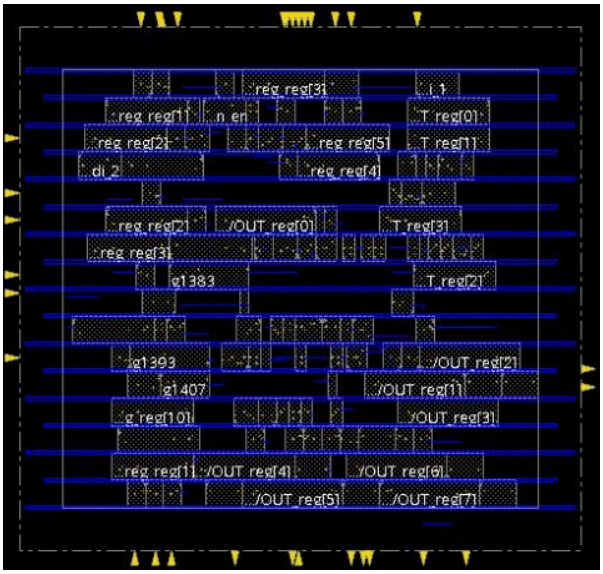
g1418	7.876e-05	7.543e-05	0.0001672	1.301e-05	INVX1
g1417	4.898e-05	9.769e-05	0.000156	9.289e-06	NAND2XL
g1401	8.509e-05	4.75e-05	0.0001477	1.511e-05	NAND3X1
out1/g14	0.0001091	2.188e-05	0.0001476	1.662e-05	NOR2BXL
g1396	8.565e-05	4.827e-05	0.0001463	1.236e-05	NOR2XL
out1/g17	0.0001029	2.345e-05	0.000143	1.662e-05	NOR2BXL
out1/g16	9.625e-05	1.794e-05	0.0001308	1.662e-05	NOR2BXL
bcd/g222	4.378e-05	7.421e-05	0.0001273	9.289e-06	NAND2XL
bcd/g215	8.122e-05	1.943e-05	0.000113	1.236e-05	NOR2XL
g1380	7.152e-05	2.163e-05	0.0001117	1.851e-05	AOI32X1
g1412	6.597e-05	2.371e-05	0.000102	1.236e-05	NOR2XL
g1398	4.559e-05	4.014e-05	9.502e-05	9.289e-06	NAND2XL
g1400	4.39e-05	4.165e-05	9.484e-05	9.289e-06	NAND2XL
g1399	4.675e-05	3.796e-05	9.401e-05	9.289e-06	NAND2XL
g1395	4.41e-05	3.199e-05	8.538e-05	9.289e-06	NAND2XL
g1390	3.627e-05	1.239e-05	8.364e-05	3.499e-05	NAND2BX1
bcd/g220	4.183e-05	3.014e-05	8.243e-05	1.046e-05	NAND4XL
g1413	3.535e-05	1.555e-05	7.624e-05	2.533e-05	AND3XL
g1416	4.234e-05	2.409e-05	7.571e-05	9.289e-06	NAND2XL
g1394	3.855e-05	2.101e-05	7.192e-05	1.236e-05	NOR2XL
bcd/g216	3.473e-05	1.635e-05	6.344e-05	1.236e-05	NOR2XL
g1387	1.907e-05	1.628e-05	4.464e-05	9.289e-06	NAND2XL
g1378	2.052e-05	6.562e-06	4.11e-05	1.402e-05	OAI31X1
g1377	1.55e-05	1.112e-05	3.592e-05	9.289e-06	NAND2XL
out1/g15	1.324e-05	2.417e-06	3.228e-05	1.662e-05	NOR2BXL
g1391	9.811e-06	1.928e-06	3.178e-05	2.004e-05	NOR2BX1
g1388	4.992e-06	2.048e-06	3.17e-05	2.466e-05	AND2XL
g1389	4.038e-06	5.678e-07	2.464e-05	2.004e-05	NOR2BX1
out1/g18	4.102e-06	9.054e-07	2.163e-05	1.662e-05	NOR2BXL
g1386	6.679e-06	5.576e-06	2.154e-05	9.289e-06	NAND2XL
out1/g11	3.893e-06	8.287e-07	2.135e-05	1.662e-05	NOR2BXL
out1/g13	1.567e-06	2.901e-07	1.848e-05	1.662e-05	NOR2BXL
Total (119 of 119)	0.0975	0.05301	0.1575	0.007005	
Total Capacitance	4.773e-12 F				
Power Density	*** No Die Area ***				

- Here, as expected, the power consumed compared to the before optimized CTS stage has increased. Earlier it was 0.1545mW, whereas now, it has increased to 0.1575mW. Also, the parasitic capacitance has increased, from 4.638pF to 4.773pF.
- This is very much expected, due to the proximity of the interconnects and hence the resulting lateral and fringe capacitances.

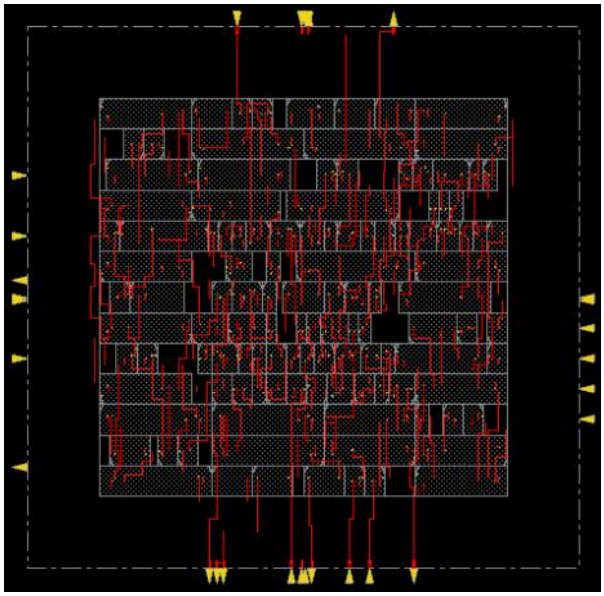
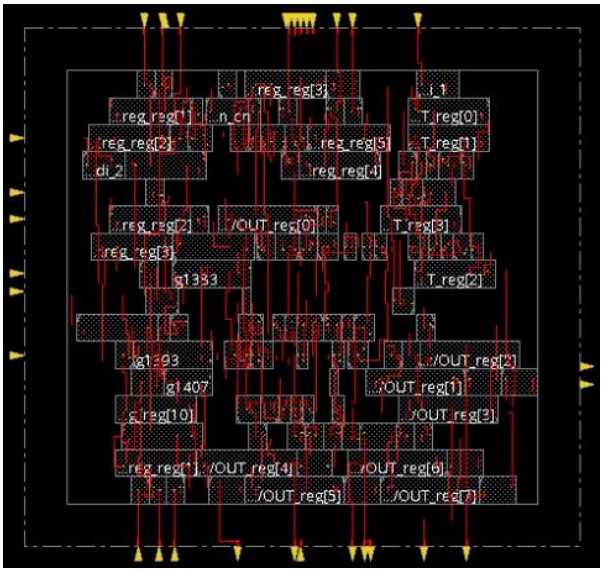
Layout Snapshot with connectivity by different metal layers

- Here, the layout snapshots of different metal layers are depicted. The comparison w.r.t to the similar layouts of small utilization case has been done along with.
- Layout with utilization of 0.8 has more congestion hence uses more metal layers compared to 0.5 utilization.

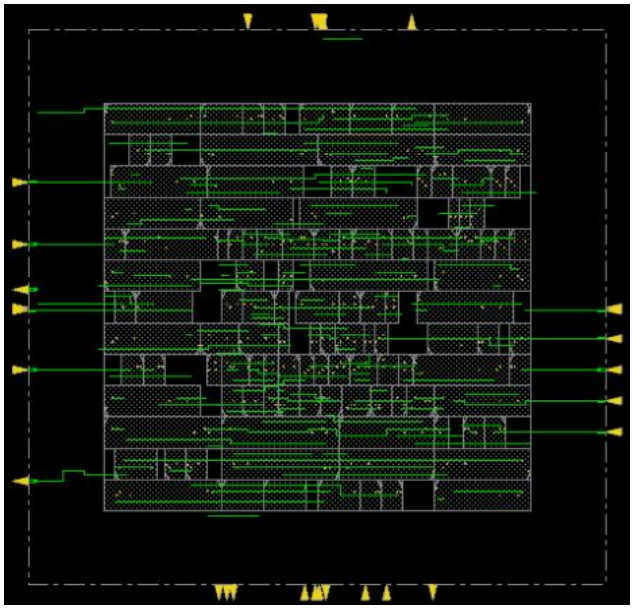
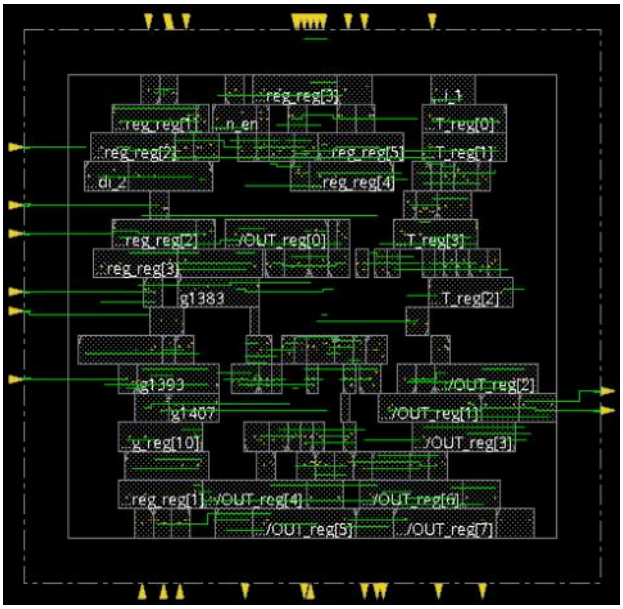
M1:

	
0.8 Utilization	**0.5 Utilization**

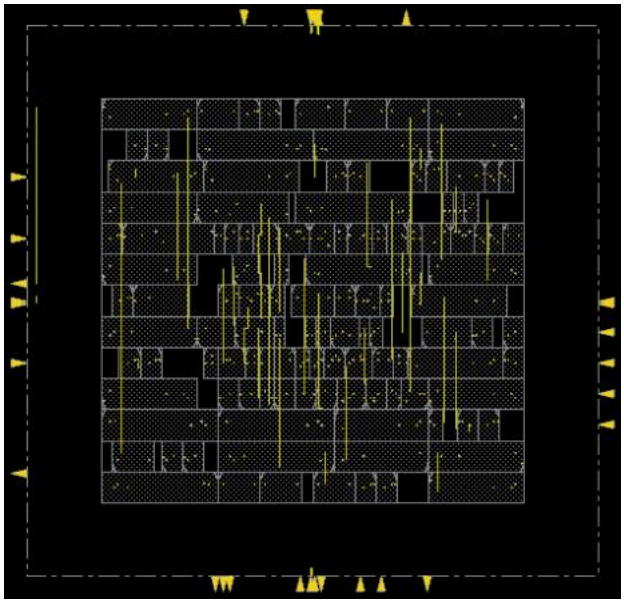
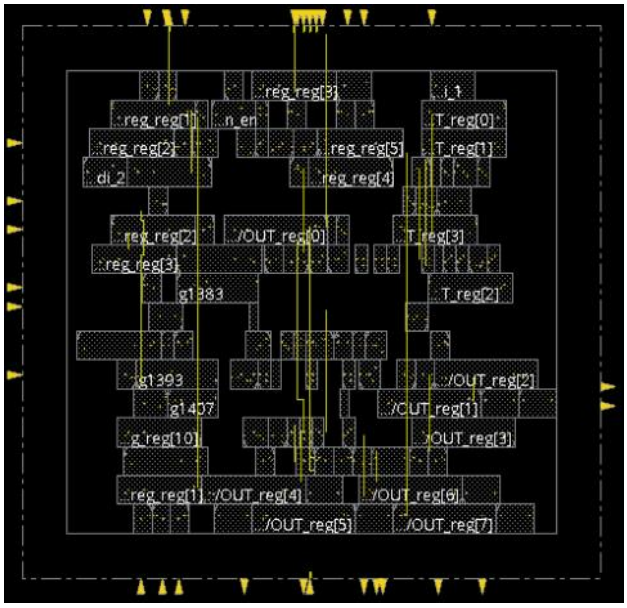
M2:

	
0.8 Utilization	**0.5 Utilization**

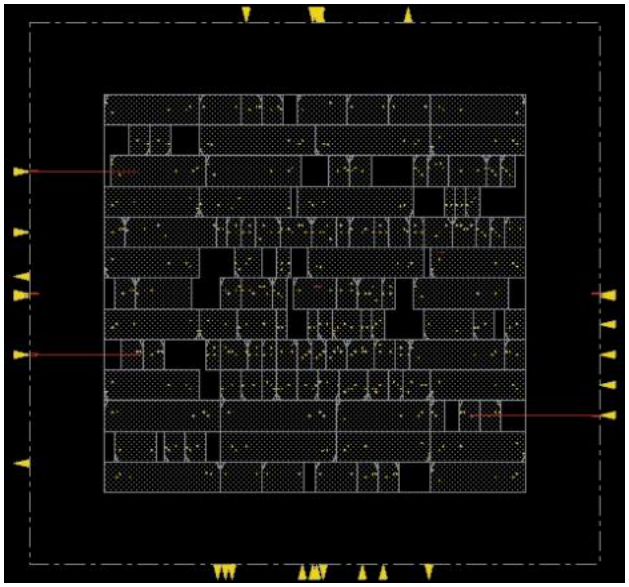
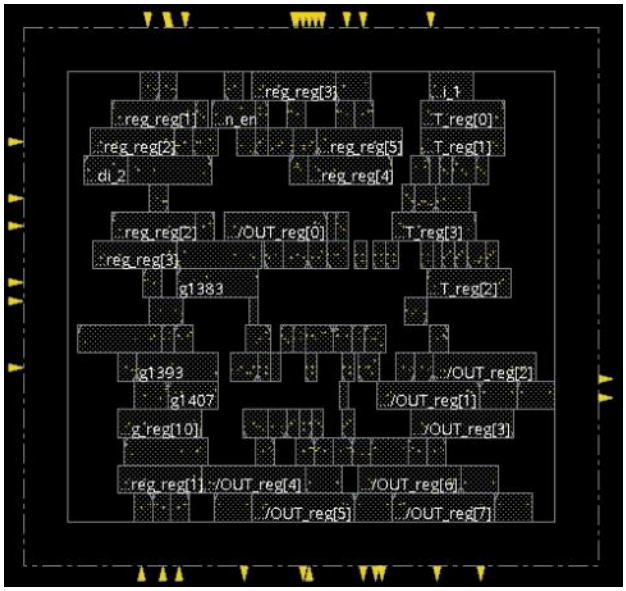
M3:

	
0.8 Utilization	**0.5 Utilization**

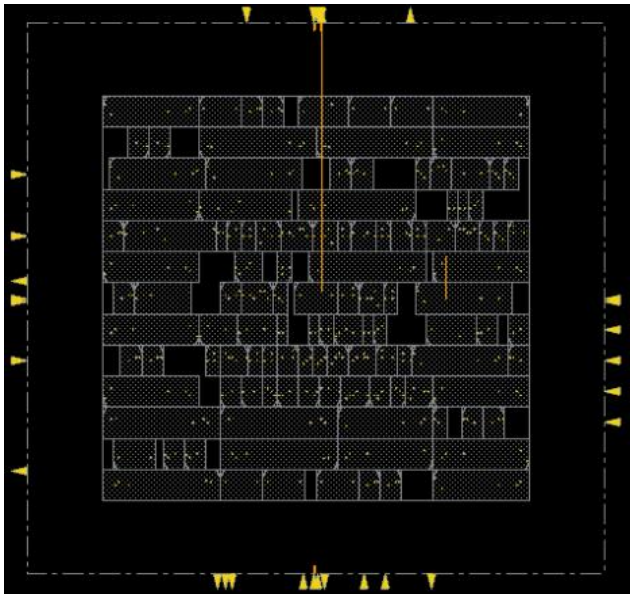
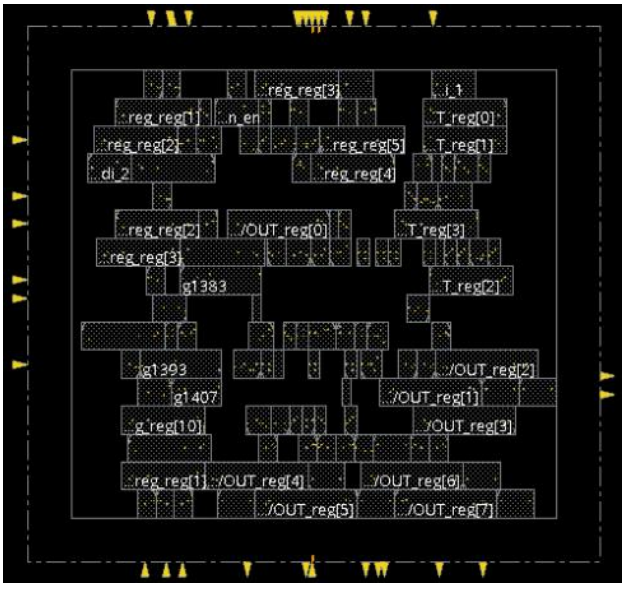
M4:

	
0.8 Utilization	**0.5 Utilization**

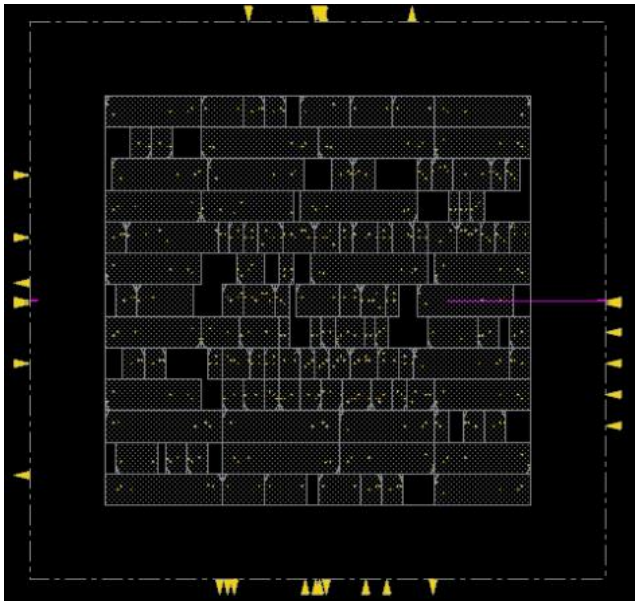
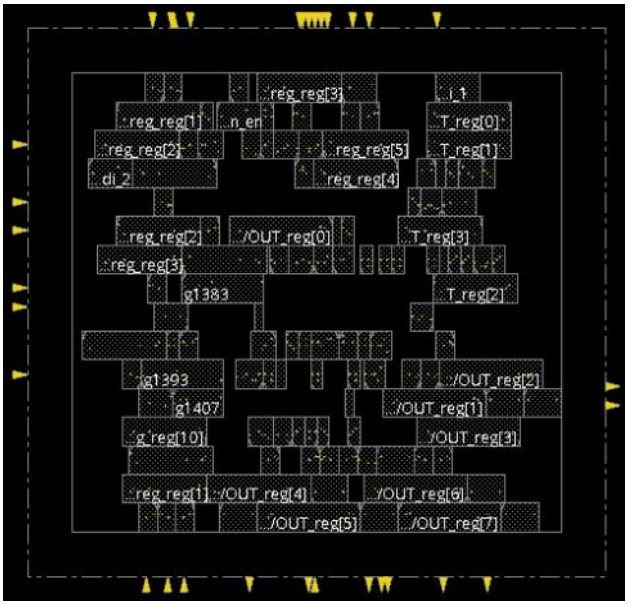
M5:

	
0.8 Utilization	**0.5 Utilization**

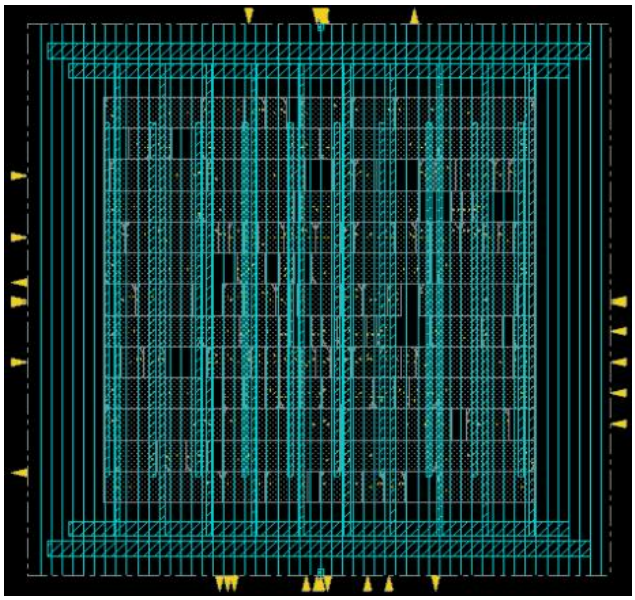
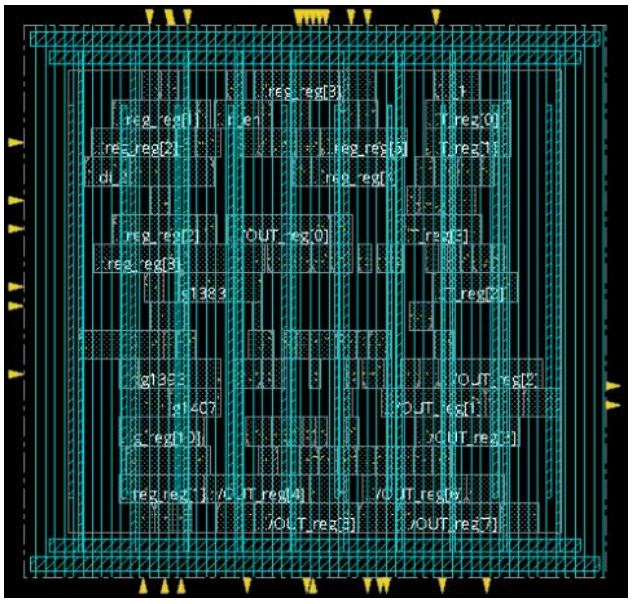
M6:

	
0.8 Utilization	**0.5 Utilization**

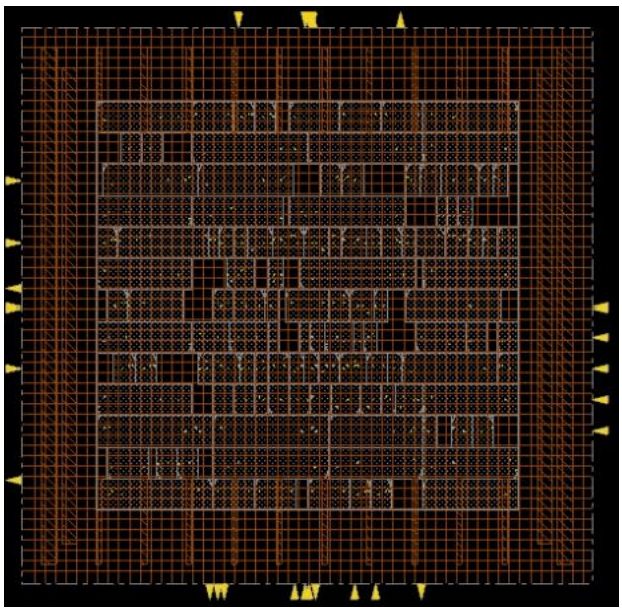
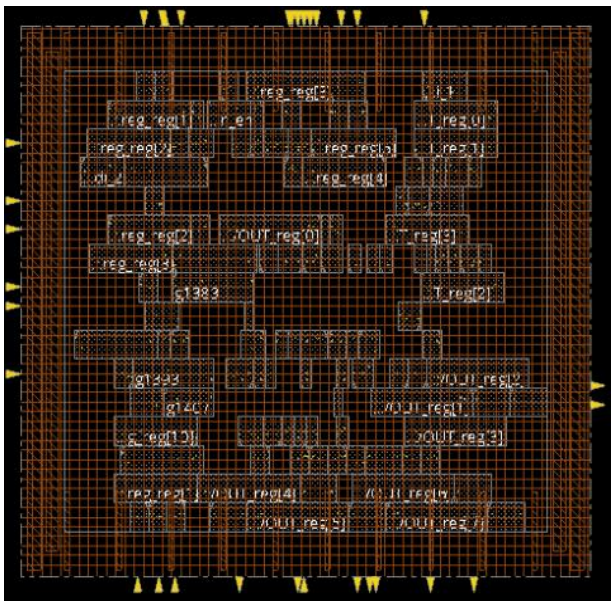
M7:

	
0.8 Utilization	**0.5 Utilization**

M8:

	
0.8 Utilization	**0.5 Utilization**

M9:

	
0.8 Utilization	**0.5 Utilization**

<u>Complete view of Large Utilization based layout</u>: