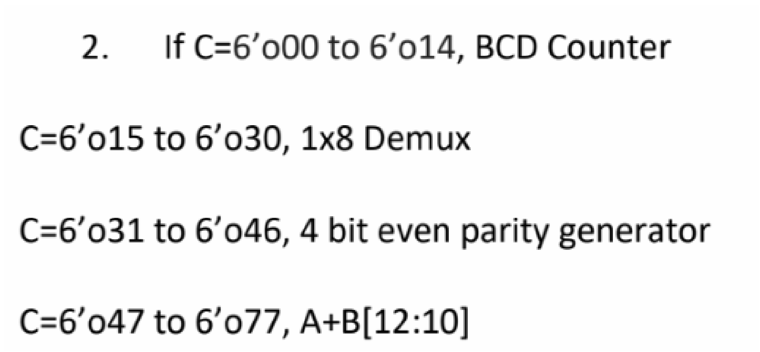
VDF PROJECT PART 1

Problem Statement No.2



2. If C=6’o00 to 6’o14, BCD Counter

C=6’o15 to 6’o30, 1x8 Demux

C=6’o31 to 6’o46, 4 bit even parity generator

C=6’o47 to 6’o77, A+B[12:10]

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SPECICATIONS AND ASSUMPTIONS

1.1 Specifications

[1] Input ports: [3:0]A, [12:0]B, [5:0]C, clk, rst. A and B are data lines and C is control line

[2] Output port: [7:0] OUT

[3] Four functions need to be implemented by design:

I. **BCD Counter:** C=6’o00 to 6’o14

II. **1x8 DeMux:** C=6’o15 to 6’o30

III. **4 bit even parity generator:** C=6’o31 to 6’o46

IV. **A+B[12:10]:** C=6’o47 to 6’o77

1.2 Assumptions

[1] BCD counter uses clk and reset as input ports and output is given to OUT[3:0].

[2] 1x8 DeMux the select lines are given by A[2:0] and the input is A[3]. The output is given to OUT[7:0].

[3] For 4-bit even parity generator, the four input bits are A[3:0] and the output is given to OUT[0]

[4] For the operation of A+B[12:0], where A is four bits A[3:0] taken as one input and other input is three bits of B[12:10]. The output of carry and sum is stored in OUT[4:0]

[5] Our Verilog code is written has 8 modules; the top module is named as top.

[6] FF_in and FF_out modules are used for the synchronization of input and output connected to the FlipFlops. Synchronous Reset logic is also been implemented here, when the reset signal is made high then all the input and output are cleared to 0.

VERILOG CODE AND TEST BENCH

2.1 Verilog Code:

```
`timescale 1ns / 1ps
//////////////////////TOP MODULE//////////////////////////////////
module top(clk,rst,A,B,C,OUT);
	input clk,rst;
	input [3:0]A;
	input [12:0]B;
	input [5:0]C;
	output [7:0]OUT;
	wire [3:0]OUT1;///BCD
	wire [7:0]OUT2;//1x8dmux
	wire OUT3;  ///4BIT EVEN PARITY GEN
	wire [4:0]OUT4;
	wire [3:0]A_reg; wire [12:0]B_reg;wire [5:0]C_reg; wire [7:0]OUT_reg;
	///////GETTING IP FROM FF  /////////


	FF_in in1(clk,rst,A,B,C,A_reg,B_reg,C_reg);

	//data data_in
(.clk(clk),.rst(rst),.A(A_Reg),.B(B_Reg),.OUT1(OUT1),.OUT2(OUT2),.OUT3(OUT3),.OUT4
(OUT4));
	BCD_Counter bcd(.clk(clk),.rst(rst),.OUT(OUT1));
	DeMux8x1 demux(.A(A_reg),.OUT_DEMUX(OUT2));
	EPG_4bit EPG(.A(A_reg),.OUT(OUT3));
	AplusB_12to10 aplusb(.A(A_reg),.B(B_reg),.OUT(OUT4));

	Controller
control(.clk(clk),.rst(rst),.C(C_reg),.Q1(OUT1), .Q2(OUT2), .Q3(OUT3), .Q4(OUT4),.
OUT(OUT_reg));

	FF_out out1(clk,rst,OUT_reg,OUT);
endmodule
```

```
////////////FF input/////////////////////////
module FF_in(clk,rst,A,B,C,A_reg,B_reg,C_reg);
	input clk,rst;
	input [3:0]A;
	input [12:0]B;
	input [5:0]C;
	output reg [3:0]A_reg;
	output reg [12:0]B_reg;
	output reg [5:0]C_reg;
	always@(posedge clk)//Synchronous Reset
	begin
		if(rst)
		begin
			A_reg<=0;B_reg<=0;C_reg<=0;
		end
		else
		begin
			A_reg<=A;B_reg<=B;C_reg<=C;
		end
	end
endmodule
```

```
/////////////FF Output////////////
module FF_out(clk,rst,OUT_reg,OUT);
       input clk,rst;
       input [7:0]OUT_reg;
       output reg [7:0]OUT;
       always@(posedge clk)//Synchronous Reset
       begin
              if(rst) OUT<=8'b0;
              else OUT<=OUT_reg;
       end
endmodule
```

```
///////Controller/////////////
module Controller(clk,rst,C,Q1,Q2,Q3,Q4,OUT);
       input clk,rst;
       input [5:0]C;
       input [3:0]Q1;///BCD Counter
       input [7:0]Q2;//1x8dmux
       input Q3;  ///4BIT EVEN PARITY GEN
       input [4:0]Q4;//A+B[12:10]
       output reg [7:0] OUT;
       always@(*)
       begin
              if(rst) OUT = 1'b0;
              else begin
              if(C>= 6'o00 && C<=6'o14) OUT=Q1;
              else if(C>= 6'o15 && C<=6'o30) OUT=Q2;
              else if(C>= 6'o31 && C<=6'o46) OUT=Q3;
              else OUT=Q4;
              end
       end
endmodule
```

```
////////////////////BCD
COUNTER////////////////////////////////////////////////////////////////////
module BCD_Counter(clk,rst,OUT);
       //0,1,...8,9,0,1,2..
       input clk,rst;
       output reg [3:0]OUT;
       always@(posedge clk)
       begin
              if(rst) OUT[3:0]<=4'b0;////reset input
              else if(OUT[3:0]==4'd9) OUT[3:0]<=4'b0;
              else OUT[3:0]<=OUT[3:0]+1'b1;
       end
endmodule
```

```
/////////////////8X1 MUX/////////////////////////////////////
module DeMux8x1(A,OUT_DEMUX);
       //B[2:0] as Select Bits
       //B[3] is data input
       input [3:0]A;
       output reg [7:0]OUT_DEMUX;
       always@(*)
```

```
	begin
		case(A[2:0])
			3'd0:begin OUT_DEMUX[0]=A[3];OUT_DEMUX[7:1]=0;end
			3'd1:begin OUT_DEMUX[1]=A[3];OUT_DEMUX[0]=0;OUT_DEMUX[7:2]=0;end
			3'd2:begin OUT_DEMUX[2]=A[3];OUT_DEMUX[1:0]=0;OUT_DEMUX[7:3]=0;end
			3'd3:begin OUT_DEMUX[3]=A[3];OUT_DEMUX[2:0]=0;OUT_DEMUX[7:4]=0;end
			3'd4:begin OUT_DEMUX[4]=A[3];OUT_DEMUX[3:0]=0;OUT_DEMUX[7:5]=0;end
			3'd5:begin OUT_DEMUX[5]=A[3];OUT_DEMUX[4:0]=0;OUT_DEMUX[7:6]=0;end
			3'd6:begin OUT_DEMUX[6]=A[3];OUT_DEMUX[5:0]=0;OUT_DEMUX[7]=0;end
			default:begin OUT_DEMUX[7]=A[3];OUT_DEMUX[6:0]=0; end

		endcase
	end
endmodule
///////////////////////////////////////////////////////////////
```

```
//////////////////4- bit EVEN PARITY GEN//////////////////////
module EPG_4bit(A,OUT);
input [3:0]A;
output [0:0]OUT;
assign OUT[0]=A[0]^A[1]^A[2]^A[3];
endmodule
/////////////////////////////////////////////////
```

```
//////////////////A+B[12:10]/////////////////////
module AplusB_12to10(A,B,OUT);
	input [3:0]A;
	input [12:0]B;
	output wire [4:0]OUT;
	assign OUT[4:0]=A+B[12:10];
endmodule
////////////////////////////////////////////////////
```

2.2 TEST BENCH AND SIMULATION WAVEFORM

A. Testbench-1:

```
`timescale 1ns / 1ps
module TB2();
	reg clk,rst;
	reg [3:0]A; reg[12:0]B; reg[5:0]C;
	wire[7:0]OUT;
	top instance2(.clk(clk),.rst(rst),.A(A),.B(B),.C(C),.OUT(OUT));
	initial begin
	$dumpfile("TB2.vcd");
	$dumpvars;
	#0	clk=0	;
	#5 rst=1;
	#5 rst=0;
	#5  A=4'b0101;
		B=13'b0_0000_0000_0000;
		C=6'o00; //000_000
	#10 C = 6'o03;//000_011
		A=4'b0100;
		B=13'b1_1111_1111_1111;// for checking bcd
	#10 C = 6'o10; // for checking bcd 001_000
		A=4'b1110;
		B=13'b0_0000_0000_0000;
	#10 C = 6'o11; // for checking bcd 001_001
```

```
              A=4'b0101;
              B=13'b0_1110_0111_1010;

       #10 C = 6'o17; // for checking 8X1 DEMUX 001_101
              A=4'b1000;
       #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
              A=4'b1111;
       #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
              A=4'b1101;
       #10 C = 6'o25; // for checking 8X1 DEMUX 010_101
              A=4'b1110;
       #10 C = 6'o15; // for checking 8X1 DEMUX 001_101
              A=4'b1001;
       #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
              A=4'b1010;
       #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
              A=4'b1100;

       #30 $finish;
       end
       always #5 clk=~clk;//Clock Period is 10 with 50% duty cycle
endmodule
```

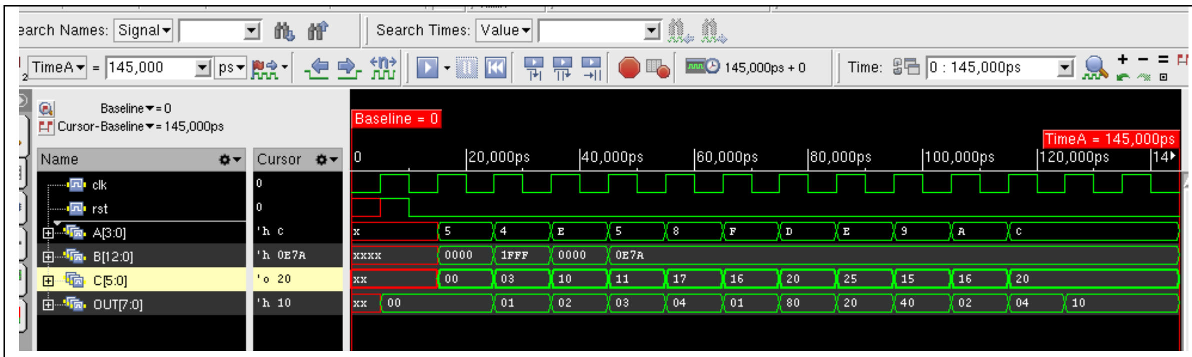

Search Names: Signal
Search Times: Value
TimeA = 145,000 ps
145,000ps + 0
Time: 0 : 145,000ps
Baseline = 0
Cursor-Baseline = 145,000ps
Baseline = 0
TimeA = 145,000ps
Name
Cursor
0 |20,000ps |40,000ps |60,000ps |80,000ps |100,000ps |120,000ps |14
clk 0
rst 0
A[3:0] 'h c x 5 4 E 5 8 F D E 9 A c
B[12:0] 'h 0E7A xxxx 0000 1FFF 0000 0E7A
C[5:0] 'o 20 xx 00 03 10 11 17 16 20 25 15 16 20
OUT[7:0] 'h 10 xx 00 01 02 03 04 01 80 20 40 02 04 10

Fig2.1 Simulation Waveform-1

- The simulation waveform corresponding to the testbench-1, verifies the given functionality.

B. Testbench-2:

```
`timescale 1ns / 1ps
module TB2();
       reg clk,rst;
       reg [3:0]A; reg[12:0]B; reg[5:0]C;
       wire[7:0]OUT;
       top instance2(.clk(clk),.rst(rst),.A(A),.B(B),.C(C),.OUT(OUT));
       initial begin
       $dumpfile("TB2.vcd");
       $dumpvars;
       #0     clk=0        ;
       #5 rst=1;
       #5 rst=0;
       #5  A=4'b0101;
              B=13'b0_0000_0000_0000;
```

```
                C=6'o00; //000_000
        #10 C = 6'o03;//000_011
                A=4'b0100;
                B=13'b1_1111_1111_1111;// for checking bcd
        #10 C = 6'o10; // for checking bcd 001_000
                A=4'b1110;
                B=13'b0_0000_0000_0000;
        #10 C = 6'o11; // for checking bcd 001_001
                A=4'b0101;
                B=13'b0_1110_0111_1010;

        #10 C = 6'o17; // for checking 8X1 DEMUX 001_101
                A=4'b1000;
        #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
                A=4'b1111;
        #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
                //A=4'b1101;
        #10 C = 6'o25; // for checking 8X1 DEMUX 010_101
                A=4'b1110;
        #10 C = 6'o15; // for checking 8X1 DEMUX 001_101
                A=4'b1001;
        #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
                A=4'b1010;
        #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
                A=4'b1100;
        #10 C = 6'o25; // for checking 8X1 DEMUX 010_101
                A=4'b1011;
        #10 C=6'o77; //111_111
                A=6'b1010;
                B=13'b1_0000_1111_0000;
        #10 C=6'o55;//101_101
                A=6'b1100;
                B=13'b1_0111_0000_1111;
        #10 rst=1;
        #10 rst=0;
        #30 $finish;
        end
        always #5 clk=~clk;//Clock Period is 10 with 50% duty cycle
endmodule
```

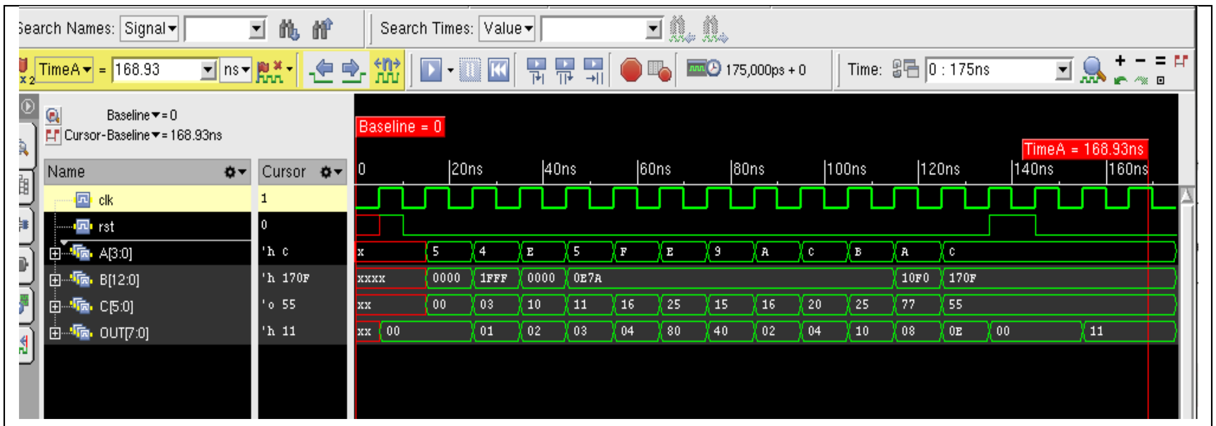


Fig2.2 Simulation Waveform-2

- The simulation waveform corresponding to the testbench-2, verifies the given functionality.

C. Testbench-3:

```
`timescale 1ns / 1ps
module TB2();
       reg clk,rst;
       reg [3:0]A; reg[12:0]B; reg[5:0]C;
       wire[7:0]OUT;
       top instance2(.clk(clk),.rst(rst),.A(A),.B(B),.C(C),.OUT(OUT));
       initial begin
       $dumpfile("TB2.vcd");
       $dumpvars;
       #0     clk=0        ;
       #5 rst=1;
       #5 rst=0;
       #5  A=4'b0101;
              B=13'b0_0000_0000_0000;
              C=6'o00; //000_000
       #10 C = 6'o03;//000_011
              A=4'b0100;
              B=13'b1_1111_1111_1111;// for checking bcd
       #10 C = 6'o10; // for checking bcd 001_000
              A=4'b1110;
              B=13'b0_0000_0000_0000;
       #10 C = 6'o11; // for checking bcd 001_001
              A=4'b0101;
              B=13'b0_1110_0111_1010;

       #10 C = 6'o17; // for checking 8X1 DEMUX 001_101
              A=4'b1000;
       #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
              A=4'b1111;
       #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
              A=4'b1101;
       #10 C = 6'o25; // for checking 8X1 DEMUX 010_101
              A=4'b1110;
       #10 C = 6'o15; // for checking 8X1 DEMUX 001_101
              A=4'b1001;
       #10 C = 6'o16; // for checking 8X1 DEMUX 001_110
              A=4'b1010;
       #10 C = 6'o20; // for checking 8X1 DEMUX 001_100
              A=4'b1100;
       #10 C = 6'o25; // for checking 8X1 DEMUX 010_101
              A=4'b1011;

       #10 C = 6'o32; // for checking Even parity Gen 011_100

       #10 C=6'o77; //111_111
              A=6'b1010;
              B=13'b1_0000_1111_0000;
       #10 C=6'o55;//101_101
              A=6'b1100;
              B=13'b1_0111_0000_1111;
       #10 C=6'o37;//011_111

       #10 rst=1;
       #10 rst=0;
       #30 $finish;
       end
       always #5 clk=~clk;//Clock Period is 10 with 50% duty cycle
endmodule
```

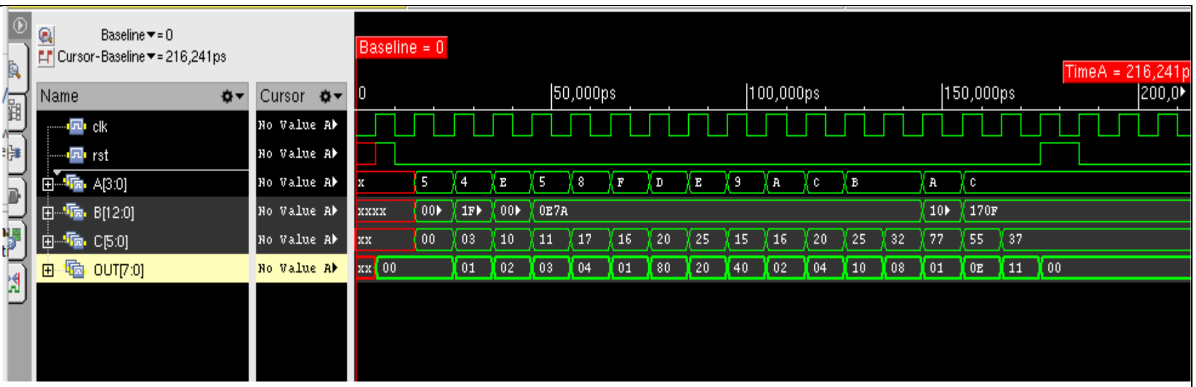
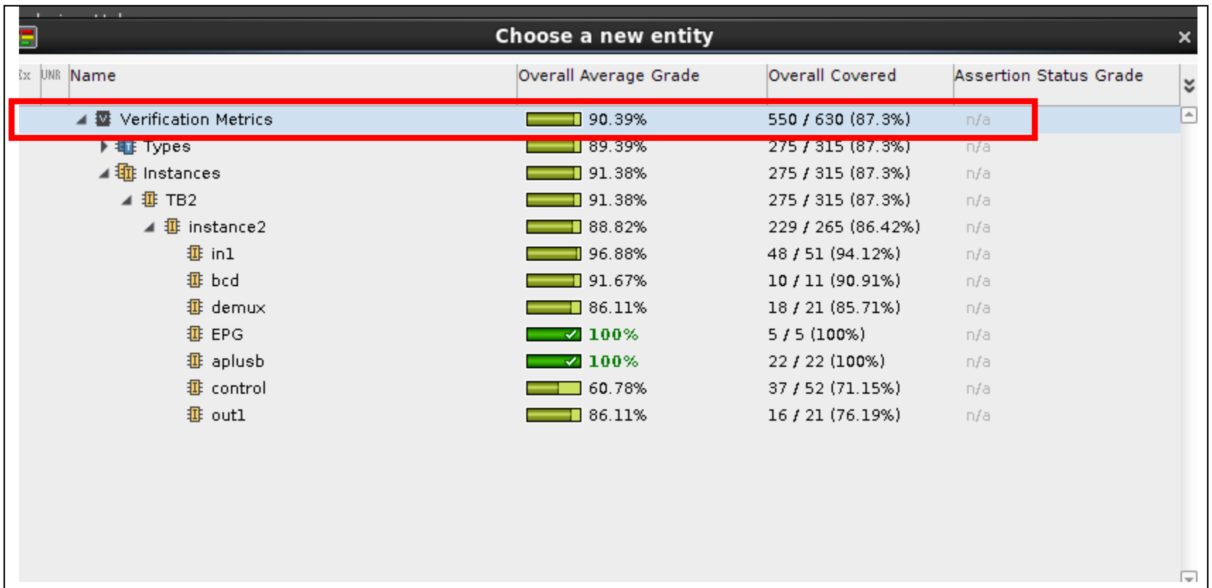

Baseline = 0
Cursor-Baseline = 216,241ps
Name
Cursor
clk
rst
A[3:0]
B[12:0]
C[5:0]
OUT[7:0]
No Value
Baseline = 0
TimeA = 216,241p
0
50,000ps
100,000ps
150,000ps
200,0
x 5 4 E 5 8 F D E 9 A C B A C
xxxx 00 1F 00 0E7A 10 170F
xx 00 03 10 11 17 16 20 25 15 16 20 25 32 77 55 37
xx 00 01 02 03 04 01 80 20 40 02 04 10 08 01 0E 11 00

Fig 2.3 Simulation Waveform-3

CODE COVERAGE

3.1 Code Coverage Testbench-1: (90.39%)



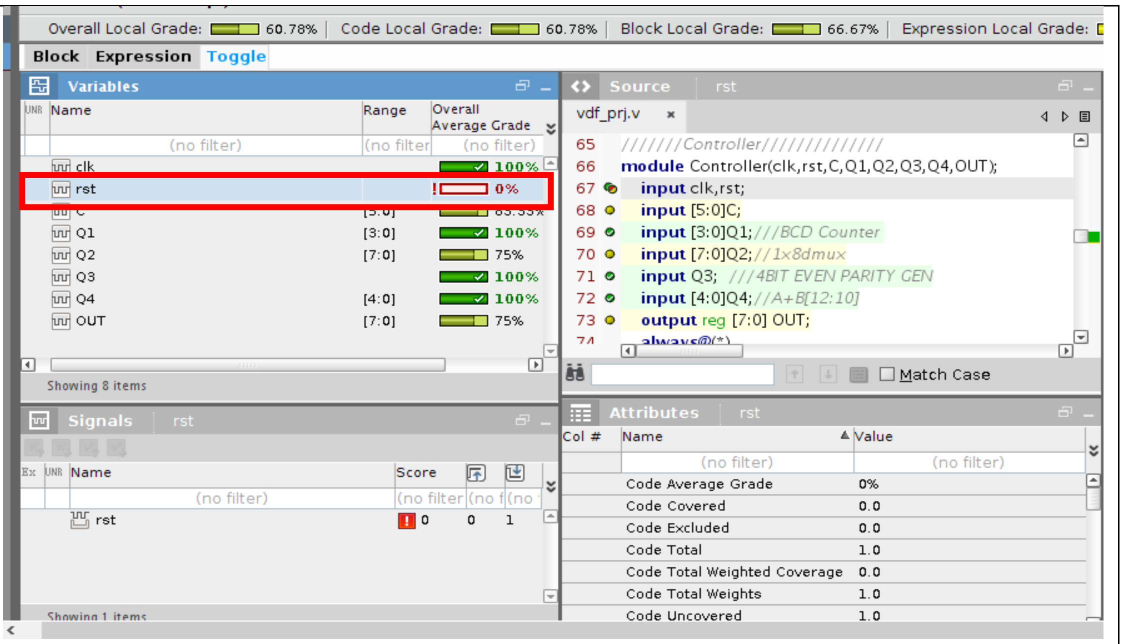
Choose a new entity

Name	Overall Average Grade	Overall Covered	Assertion Status Grade
Verification Metrics	90.39%	550 / 630 (87.3%)	n/a
Types	89.39%	275 / 315 (87.3%)	n/a
Instances	91.38%	275 / 315 (87.3%)	n/a
TB2	91.38%	275 / 315 (87.3%)	n/a
instance2	88.82%	229 / 265 (86.42%)	n/a
in1	96.88%	48 / 51 (94.12%)	n/a
bcd	91.67%	10 / 11 (90.91%)	n/a
demux	86.11%	18 / 21 (85.71%)	n/a
EPG	✓ 100%	5 / 5 (100%)	n/a
aplusb	✓ 100%	22 / 22 (100%)	n/a
control	60.78%	37 / 52 (71.15%)	n/a
out1	86.11%	16 / 21 (76.19%)	n/a

Fig 3.1.1 CODE COVERAGE SUMMARY

- Code Coverage of the Testbench1 is 90.39%.

3.1.1 Analysis of The Report:



Overall Local Grade: 60.78% | Code Local Grade: 60.78% | Block Local Grade: 66.67% | Expression Local Grade:

Block Expression Toggle

Variables

Name	Range	Overall Average Grade
clk		✓ 100%
rst		! 0%
C	[5:0]	83.33%
Q1	[3:0]	✓ 100%
Q2	[7:0]	75%
Q3		✓ 100%
Q4	[4:0]	✓ 100%
OUT	[7:0]	75%

Showing 8 items

Signals rst

Name	Score		
rst	! 0	0	1

Showing 1 items

Source rst

vdf_prj.v

```
///////Controller/////////////
module Controller(clk,rst,C,Q1,Q2,Q3,Q4,OUT);
  input clk,rst;
  input [5:0]C;
  input [3:0]Q1;///BCD Counter
  input [7:0]Q2;//1x8dmux
  input Q3;  ///4BIT EVEN PARITY GEN
  input [4:0]Q4;//A+B[12:10]
  output reg [7:0] OUT;
  always@(*)
```

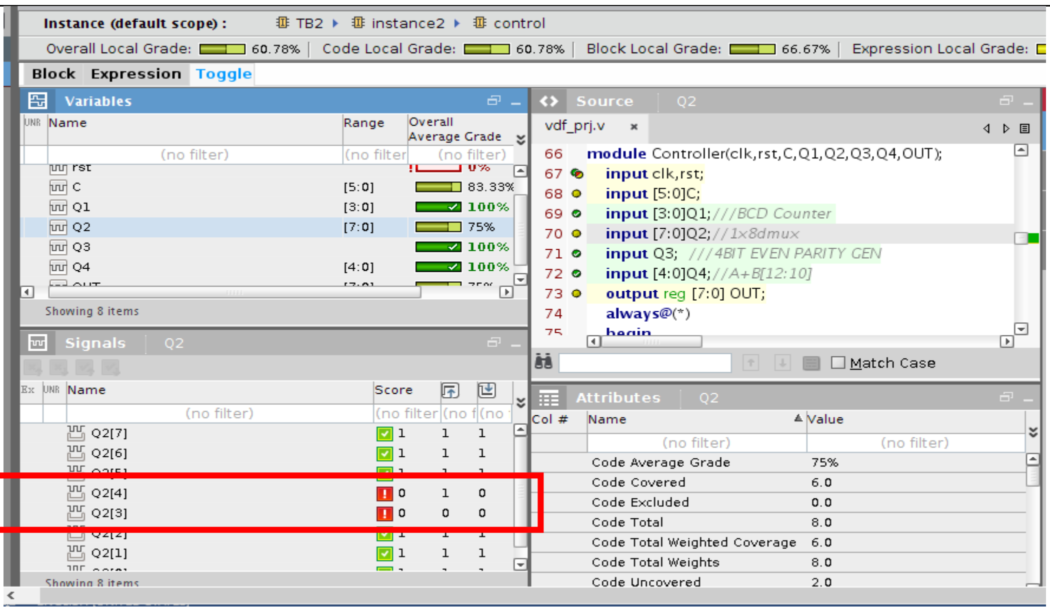
Match Case

Attributes rst

Col #	Name	Value
	Code Average Grade	0%
	Code Covered	0.0
	Code Excluded	0.0
	Code Total	1.0
	Code Total Weighted Coverage	0.0
	Code Total Weights	1.0
	Code Uncovered	1.0

Fig3.1.2 -TOGGLE REPORT

- The above toggle report is indicating that ***"rst"*** signal has not been toggled so its toggle report is 0%.



Instance (default scope) : TB2 ▸ instance2 ▸ control

Overall Local Grade: 60.78% | Code Local Grade: 60.78% | Block Local Grade: 66.67% | Expression Local Grade:

Block Expression Toggle

Variables

Name	Range	Overall Average Grade
rst		0%
C	[5:0]	83.33%
Q1	[3:0]	100%
Q2	[7:0]	75%
Q3		100%
Q4	[4:0]	100%
OUT	[7:0]	75%

Showing 8 items

Signals Q2

Name	Score		
Q2[7]	✓ 1	1	1
Q2[6]	✓ 1	1	1
Q2[5]	✓ 1	1	1
Q2[4]	! 0	1	0
Q2[3]	! 0	0	0
Q2[2]	✓ 1	1	1
Q2[1]	✓ 1	1	1
Q2[0]			

Showing 8 items

Source Q2

vdf_prj.v

```
module Controller(clk,rst,C,Q1,Q2,Q3,Q4,OUT);
  input clk,rst;
  input [5:0]C;
  input [3:0]Q1;///BCD Counter
  input [7:0]Q2;//1x8dmux
  input Q3;  ///4BIT EVEN PARITY GEN
  input [4:0]Q4;//A+B[12:10]
  output reg [7:0] OUT;
  always@(*)
  begin
```

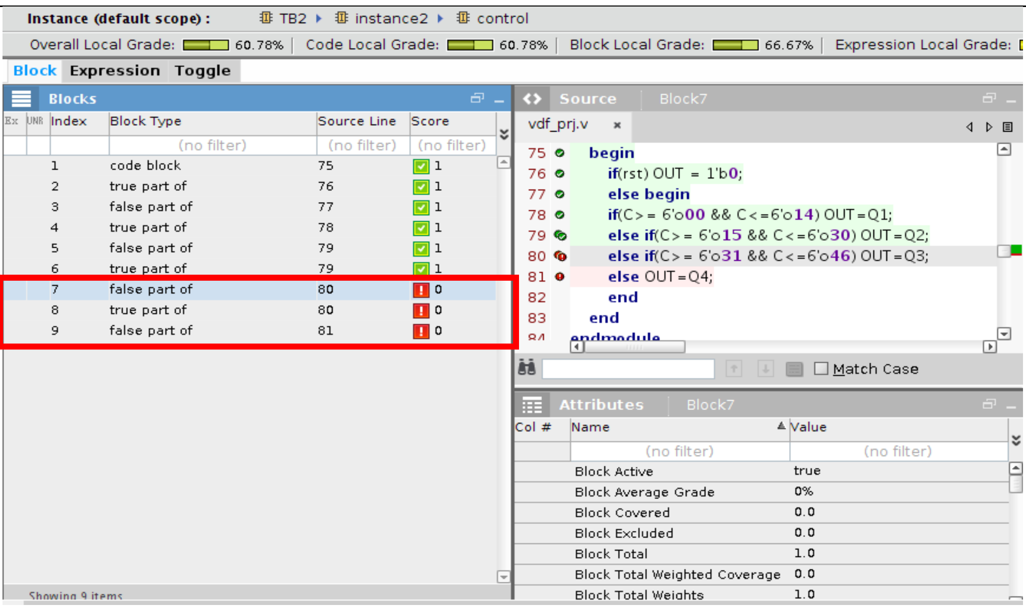
Match Case

Attributes Q2

Name	Value
Code Average Grade	75%
Code Covered	6.0
Code Excluded	0.0
Code Total	8.0
Code Total Weighted Coverage	6.0
Code Total Weights	8.0
Code Uncovered	2.0

Fig3.1.3 -TOGGLE REPORT

➢ From here, we can see that the few bits of input Q2 of 1x8 demux have not been toggled by test cases we give in testbench hence toggle coverage of input vector Q2 is 75%.



Instance (default scope) : TB2 ▸ instance2 ▸ control

Overall Local Grade: 60.78% | Code Local Grade: 60.78% | Block Local Grade: 66.67% | Expression Local Grade:

Block Expression Toggle

Blocks

Index	Block Type	Source Line	Score
1	code block	75	✓ 1
2	true part of	76	✓ 1
3	false part of	77	✓ 1
4	true part of	78	✓ 1
5	false part of	79	✓ 1
6	true part of	79	✓ 1
7	false part of	80	! 0
8	true part of	80	! 0
9	false part of	81	! 0

Showing 9 items

Source Block7

vdf_prj.v

```
75    begin
76      if(rst) OUT = 1'b0;
77      else begin
78      if(C>= 6'o00 && C<=6'o14) OUT=Q1;
79      else if(C>= 6'o15 && C<=6'o30) OUT=Q2;
80      else if(C>= 6'o31 && C<=6'o46) OUT=Q3;
81      else OUT=Q4;
82      end
83    end
84  endmodule
```

Match Case

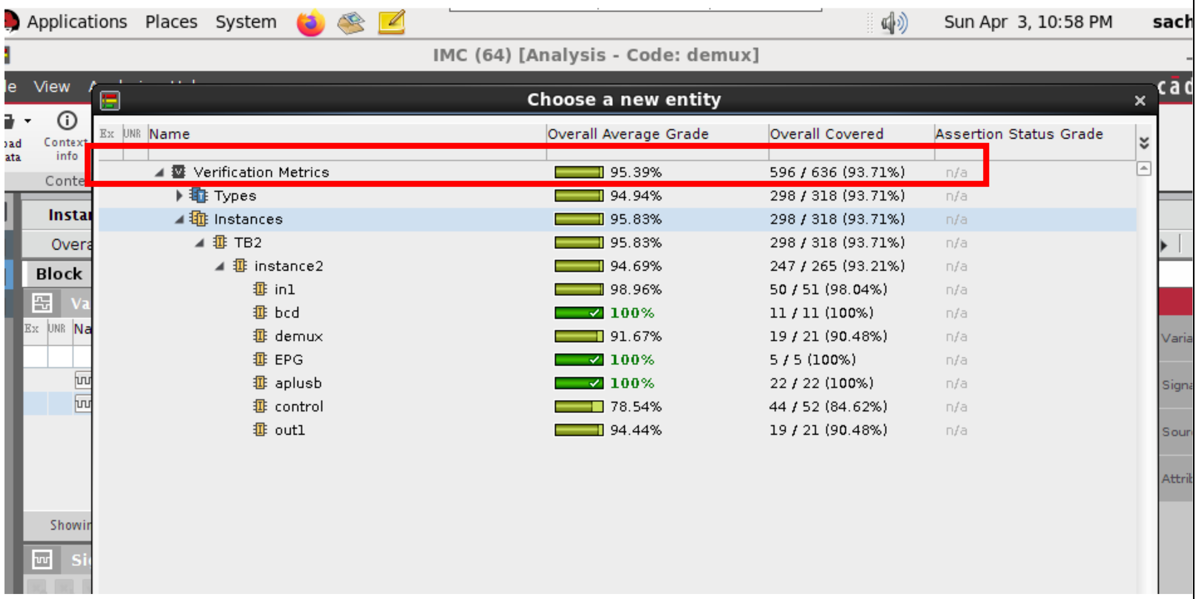
Attributes Block7

Name	Value
Block Active	true
Block Average Grade	0%
Block Covered	0.0
Block Excluded	0.0
Block Total	1.0
Block Total Weighted Coverage	0.0
Block Total Weights	1.0

Fig3.1.4 BLOCK REPORT

➢ From the above block report, we are observing that line-80,81 of the "controller" module in our Verilog code have not been covered properly in the test bench. Hence, it is contributing to the declining of block coverage.

3.2 Code Coverage Testbench-2: (95.39%)



Applications Places System · Sun Apr 3, 10:58 PM

IMC (64) [Analysis - Code: demux]

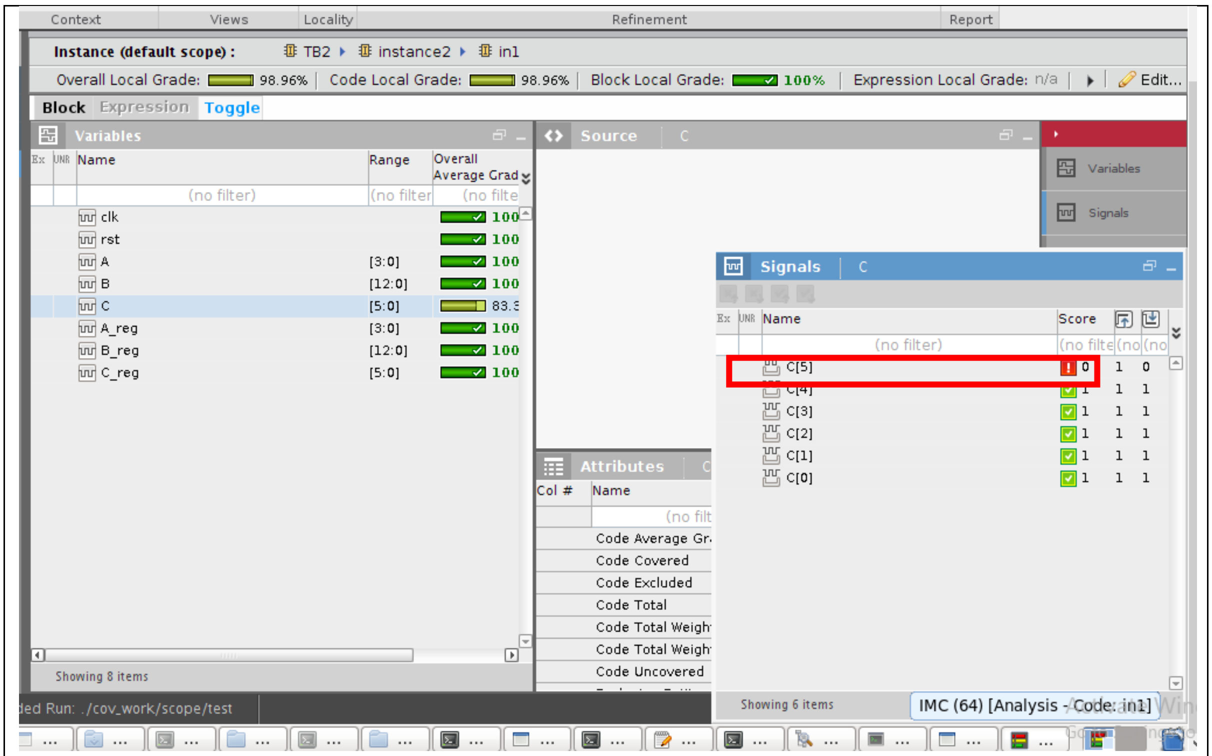
Choose a new entity

Name	Overall Average Grade	Overall Covered	Assertion Status Grade
Verification Metrics	95.39%	596 / 636 (93.71%)	n/a
Types	94.94%	298 / 318 (93.71%)	n/a
Instances	95.83%	298 / 318 (93.71%)	n/a
TB2	95.83%	298 / 318 (93.71%)	n/a
instance2	94.69%	247 / 265 (93.21%)	n/a
in1	98.96%	50 / 51 (98.04%)	n/a
bcd	✓ 100%	11 / 11 (100%)	n/a
demux	91.67%	19 / 21 (90.48%)	n/a
EPG	✓ 100%	5 / 5 (100%)	n/a
aplusb	✓ 100%	22 / 22 (100%)	n/a
control	78.54%	44 / 52 (84.62%)	n/a
out1	94.44%	19 / 21 (90.48%)	n/a

Fig3.2.1 CODE COVERAGE SUMMARY

❖ Overall Code coverage that we obtained from this test bench is 95.39%.

3.2.1 Analysis of The Report:



Instance (default scope) : TB2 ▸ instance2 ▸ in1

Overall Local Grade: 98.96% | Code Local Grade: 98.96% | Block Local Grade: 100% | Expression Local Grade: n/a

Block Expression Toggle

Variables

Name	Range	Overall Average Grade
clk		✓ 100
rst		✓ 100
A	[3:0]	✓ 100
B	[12:0]	✓ 100
C	[5:0]	83.3
A_reg	[3:0]	✓ 100
B_reg	[12:0]	✓ 100
C_reg	[5:0]	✓ 100

Showing 8 items

Signals

Name	Score		
C[5]	! 0	1	0
C[4]	✓ 1	1	1
C[3]	✓ 1	1	1
C[2]	✓ 1	1	1
C[1]	✓ 1	1	1
C[0]	✓ 1	1	1

Showing 6 items

Attributes: Code Average Gr, Code Covered, Code Excluded, Code Total, Code Total Weigh, Code Total Weigh, Code Uncovered

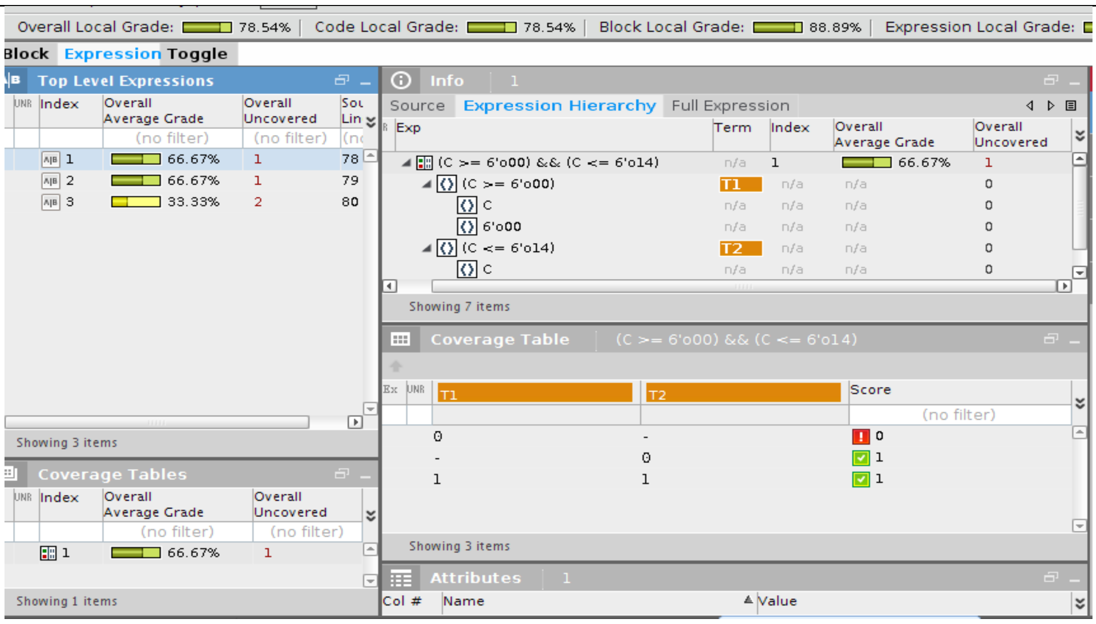
ded Run: ./cov_work/scope/test

IMC (64) [Analysis - Code: in1]

Fig3.2.2 TOGGLE REPORT

❖ Here, we can see that test cases that we had given for the test bench do not toggle all the bits of vector C in “in1” module, hence we can see a drop in toggle percentage.

❖ And, from the above report we can observe that bit 5 of vector C has not been toggled from 1→0 or 0→1.



Overall Local Grade: 78.54% | Code Local Grade: 78.54% | Block Local Grade: 88.89% | Expression Local Grade:

Block Expression Toggle

Top Level Expressions

Index	Overall Average Grade	Overall Uncovered	Sou Lin
1	66.67%	1	78
2	66.67%	1	79
3	33.33%	2	80

Showing 3 items

Coverage Tables

Index	Overall Average Grade	Overall Uncovered
1	66.67%	1

Showing 1 items

Info 1

Source Expression Hierarchy Full Expression

Exp	Term	Index	Overall Average Grade	Overall Uncovered
(C >= 6'o00) && (C <= 6'o14)	n/a	1	66.67%	1
(C >= 6'o00)	T1	n/a	n/a	0
C	n/a	n/a	n/a	0
6'o00	n/a	n/a	n/a	0
(C <= 6'o14)	T2	n/a	n/a	0
C	n/a	n/a	n/a	0

Showing 7 items

Coverage Table (C >= 6'o00) && (C <= 6'o14)

T1	T2	Score
0	-	0
-	0	1
1	1	1

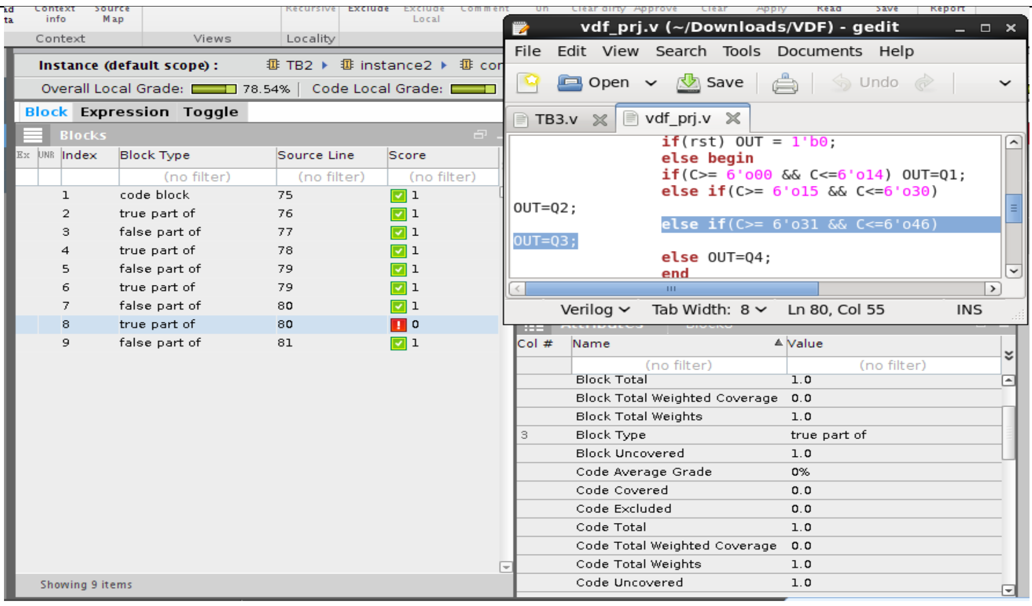
Showing 3 items

Attributes 1

Col # Name Value

Fig3.2.3 Expression Coverage

- ❖ Here, because we are not using all the values of control signal C hence true or false conditions of above expressions have missed out resulting in decreased coverage percentage in “Control” module.
- ❖ For example, here for the expression C>=6’o00, we don't have a false case where C<6’o00 hence overall coverage grade has been decreased.



Instance (default scope) : TB2 ▸ instance2 ▸

Overall Local Grade: 78.54% | Code Local Grade:

Block Expression Toggle

Blocks

Index	Block Type	Source Line	Score
1	code block	75	✓ 1
2	true part of	76	✓ 1
3	false part of	77	✓ 1
4	true part of	78	✓ 1
5	false part of	79	✓ 1
6	true part of	79	✓ 1
7	false part of	80	✓ 1
8	true part of	80	! 0
9	false part of	81	✓ 1

Showing 9 items

vdf_prj.v (~/Downloads/VDF) - gedit

```
                if(rst) OUT = 1'b0;
                else begin
                if(C>= 6'o00 && C<=6'o14) OUT=Q1;
                else if(C>= 6'o15 && C<=6'o30)
OUT=Q2;
                else if(C>= 6'o31 && C<=6'o46)
OUT=Q3;
                else OUT=Q4;
                end
```

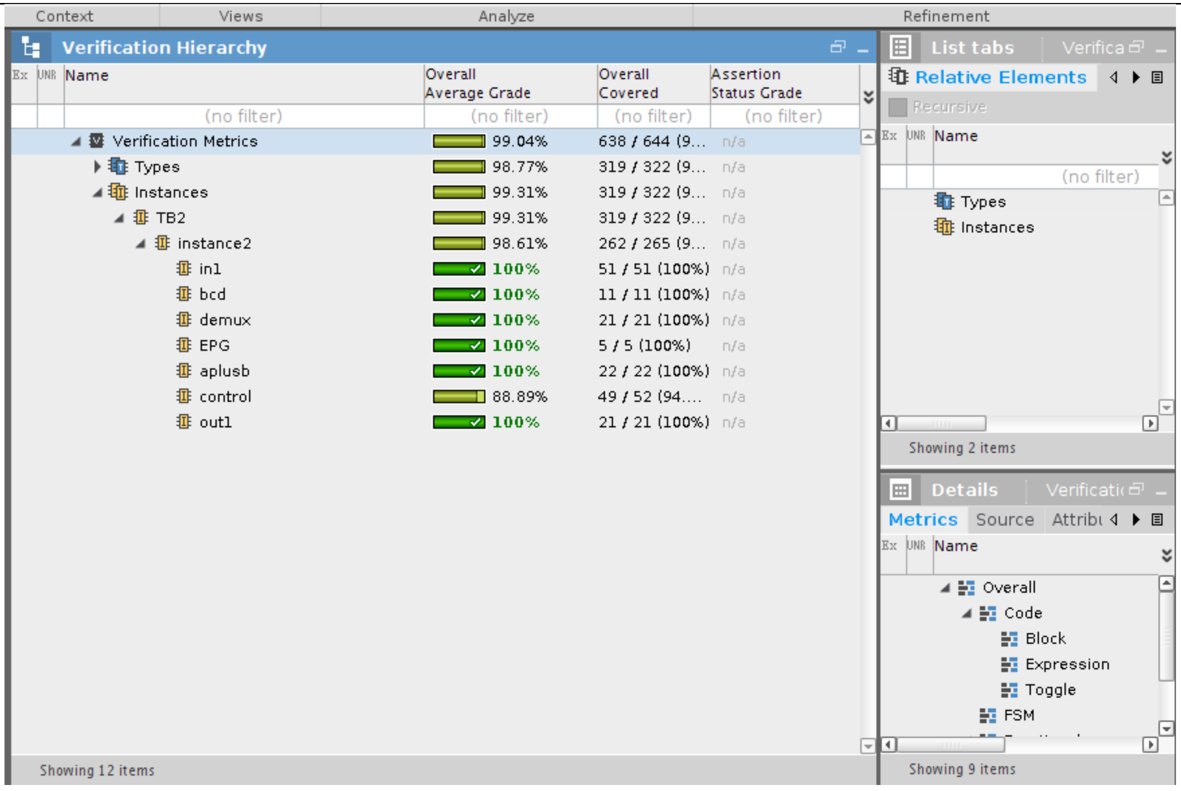
Verilog Tab Width: 8 Ln 80, Col 55 INS

Col #	Name	Value
	Block Total	1.0
	Block Total Weighted Coverage	0.0
	Block Total Weights	1.0
3	Block Type	true part of
	Block Uncovered	1.0
	Code Average Grade	0%
	Code Covered	0.0
	Code Excluded	0.0
	Code Total	1.0
	Code Total Weighted Coverage	0.0
	Code Total Weights	1.0
	Code Uncovered	1.0

Fig3.2.4 Block Coverage

- ❖ Here, we can see that in “control” module one of the “elseif” block has not been covered as our test cases are not as such to cover this elseif condition where C>=6’o31 and C<=6’o46 i.e., for checking even parity generator hence we get block coverage less than 100% here.

3.3 Code Coverage Testbench-3: (99.04%)



Context | Views | Analyze | Refinement

Verification Hierarchy

Name	Overall Average Grade	Overall Covered	Assertion Status Grade
(no filter)	(no filter)	(no filter)	(no filter)
Verification Metrics	99.04%	638 / 644 (9...	n/a
Types	98.77%	319 / 322 (9...	n/a
Instances	99.31%	319 / 322 (9...	n/a
TB2	99.31%	319 / 322 (9...	n/a
instance2	98.61%	262 / 265 (9...	n/a
in1	✓ 100%	51 / 51 (100%)	n/a
bcd	✓ 100%	11 / 11 (100%)	n/a
demux	✓ 100%	21 / 21 (100%)	n/a
EPG	✓ 100%	5 / 5 (100%)	n/a
aplusb	✓ 100%	22 / 22 (100%)	n/a
control	88.89%	49 / 52 (94....	n/a
out1	✓ 100%	21 / 21 (100%)	n/a

Showing 12 items

List tabs — Relative Elements — Recursive

Name (no filter)
- Types
- Instances

Showing 2 items

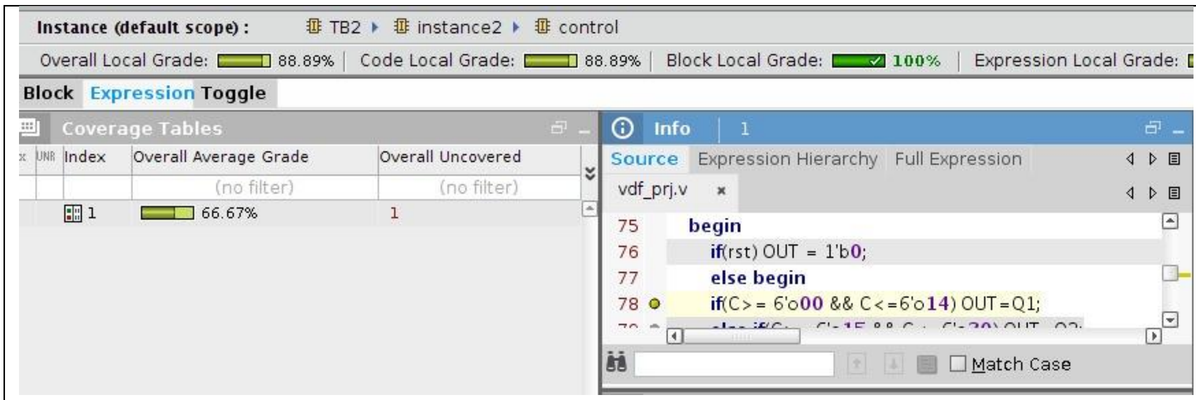
Details — Metrics | Source | Attribu

Name
- Overall
  - Code
    - Block
    - Expression
    - Toggle
  - FSM

Showing 9 items

Fig3.3.1 Code Coverage Summary

❖ Overall Code coverage we obtained from this test bench is 99.04%



Instance (default scope) : TB2 ▸ instance2 ▸ control

Overall Local Grade: 88.89% | Code Local Grade: 88.89% | Block Local Grade: ✓ 100% | Expression Local Grade:

Block | Expression | Toggle

Coverage Tables

Index	Overall Average Grade	Overall Uncovered
	(no filter)	(no filter)
1	66.67%	1

Info 1 — Source | Expression Hierarchy | Full Expression — vdf_prj.v

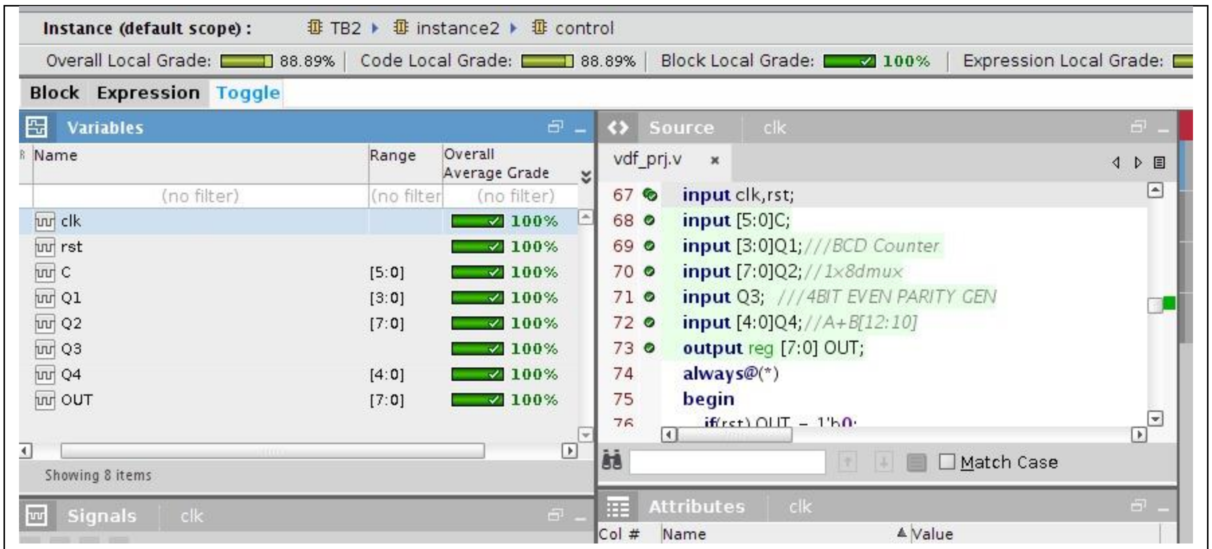
```
begin
  if(rst) OUT = 1'b0;
  else begin
  if(C>= 6'o00 && C<=6'o14) OUT=Q1;
```

Match Case

Fig3.3.2 Expression Coverage

❖ Here, because we are not using all the values of control signal C hence true or false conditions of above expressions have missed out resulting in decreased coverage percentage in “Control” module.

❖ For example, here for the expression C>=6’o00, we don't have a false case where C<6’o00 hence overall coverage grade has been decreased.



Instance (default scope) : TB2 ▸ instance2 ▸ control

Overall Local Grade: 88.89% | Code Local Grade: 88.89% | Block Local Grade: ✓ 100% | Expression Local Grade:

Block Expression Toggle

Variables

Name	Range	Overall Average Grade
(no filter)	(no filter)	(no filter)
clk		✓ 100%
rst		✓ 100%
C	[5:0]	✓ 100%
Q1	[3:0]	✓ 100%
Q2	[7:0]	✓ 100%
Q3		✓ 100%
Q4	[4:0]	✓ 100%
OUT	[7:0]	✓ 100%

Showing 8 items

Source clk — vdf_prj.v

```
input clk,rst;
input [5:0]C;
input [3:0]Q1;///BCD Counter
input [7:0]Q2;//1x8dmux
input Q3;  ///4BIT EVEN PARITY GEN
input [4:0]Q4;//A+B[12:10]
output reg [7:0] OUT;
always@(*)
begin
  if(rst) OUT = 1'b0;
```

Fig3.3.3 Toggle Coverage

Toggle Coverage is shown as 100%

SYNTHESIS

Using the RTL code written for the functionality specified in the code coverage part, now the RTL is synthesised into netlists using technology library file, constraints specified.

Command:

```
genus -legacy_ui
source script.tcl
```

Script:

```
set_attr library slow.lib
read_hdl vdf_prj.v
elaborate
read_sdc constraints.sdc
synthesize -to_mapped -effort medium
write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge >
Report/delays.sdf
write_hdl > Report/synthesised_netlist.v
write_sdc > Report/dc_file_for_physical_design.sdc
write_script > Report/synthesis_script_sdc.g
report timing > Report/synthesis_timing_report.rep
report power > Report/synthesis_power_report.rep
report gates > Report/synthesis_cell_report.rep
report area > Report/synthesis_area_report.rep
gui_show
```

4.(a) Minimum area, Keeping timing constraints highly relaxed.

SDC:

```
create_clock -name mclk -period 9 [get_ports clk]

set_clock_transition -rise 0.05 [get_clocks mclk]
set_clock_transition -fall 0.05 [get_clocks mclk]
set_clock_uncertainty 0.2 [get_clocks mclk]
set_clock_latency 0.5 [get_clocks mclk]

set_input_delay -clock [get_clocks mclk] 1 [get_ports A]
set_input_delay -clock [get_clocks mclk] 1 [get_ports B]
set_input_delay -clock [get_clocks mclk] 1 [get_ports C]
set_input_delay -clock [get_clocks mclk] 1 [get_ports rst]

set_input_transition 0.01 [get_ports A]
set_input_transition 0.01 [get_ports B]
set_input_transition 0.01 [get_ports C]
set_input_transition 0.01 [get_ports rst]

set_output_delay -clock [get_clocks mclk] 1 [get_ports OUT]

set_load 0.5 [get_ports OUT]
```

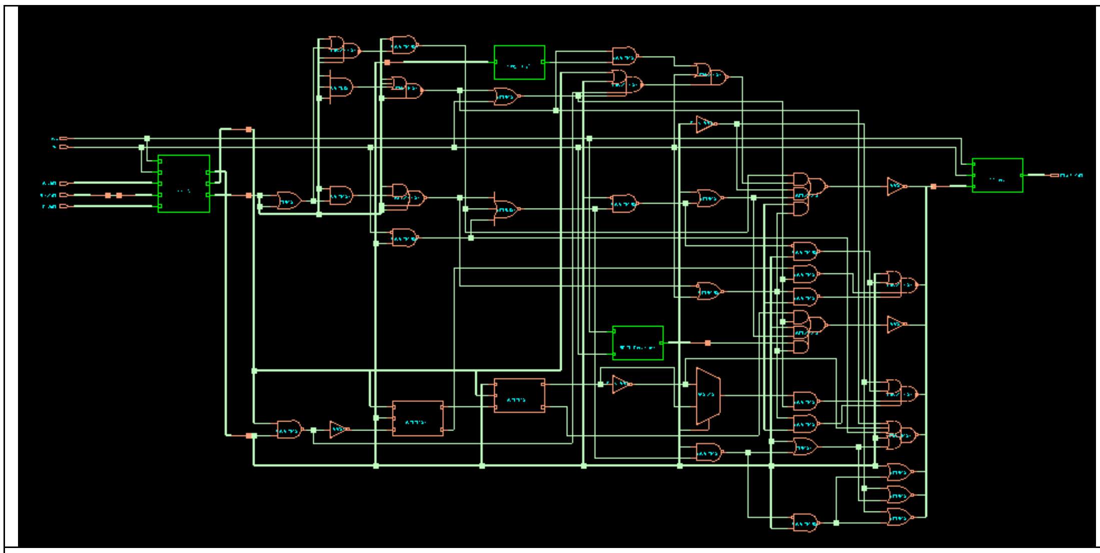


Fig4.1 Synthesized Netlist Schematic View (top module)

- The Synthesized netlist, has four blocks of design namely: FF_in, FF_out, EPG, BCD Counter. The detailed view of these blocks is shown below.

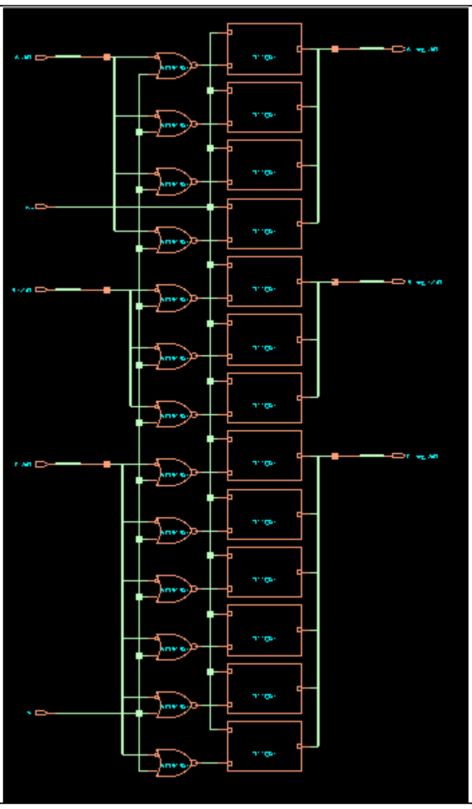


Fig4.2 FF_in block inside the synthesized netlist Schematic

- As specified, the inputs are driven by FF before being used by some other combinational blocks.

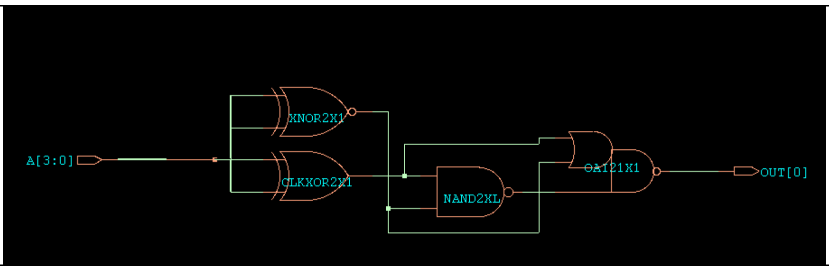


Fig4.3 EPG block inside the synthesized netlist Schematic

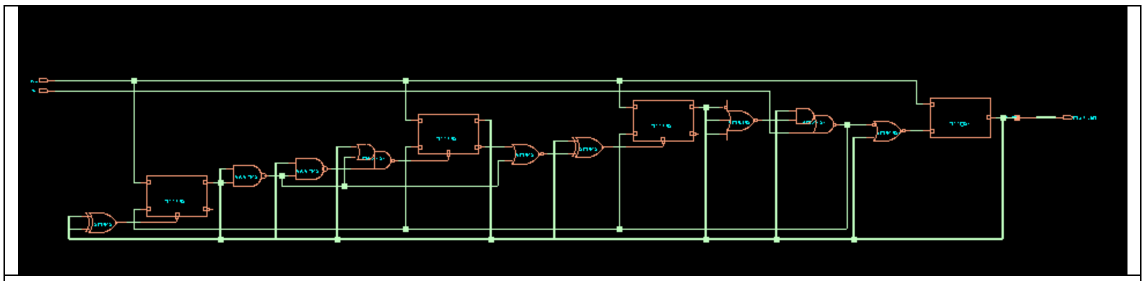


Fig4.4 BCD_Counter block inside the synthesized netlist Schematic

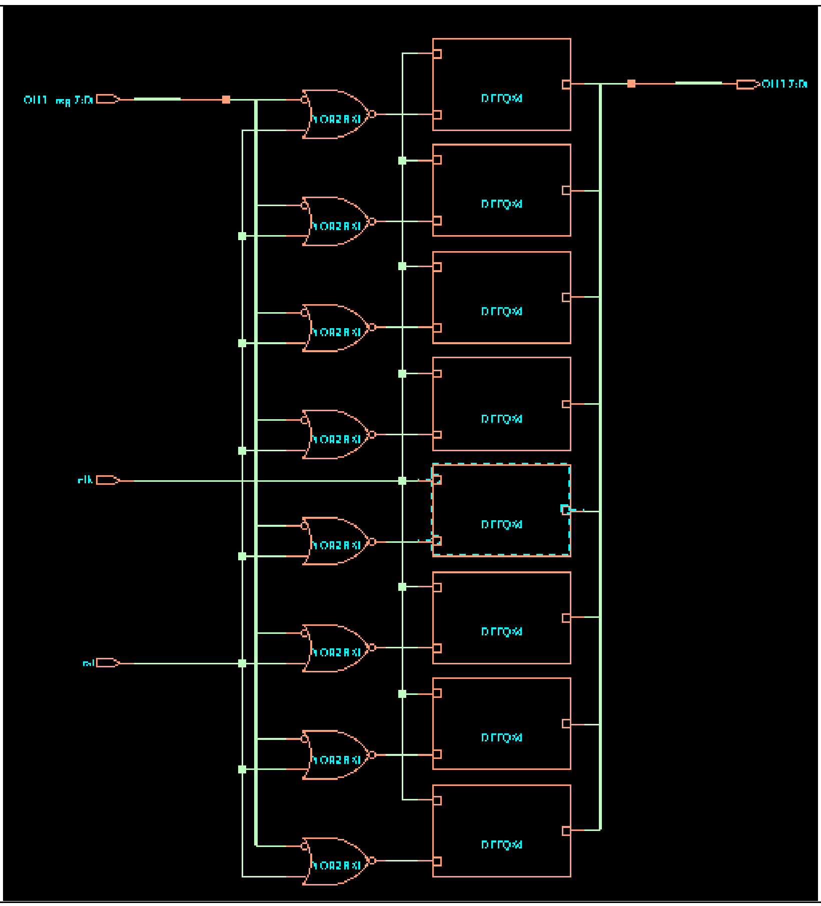
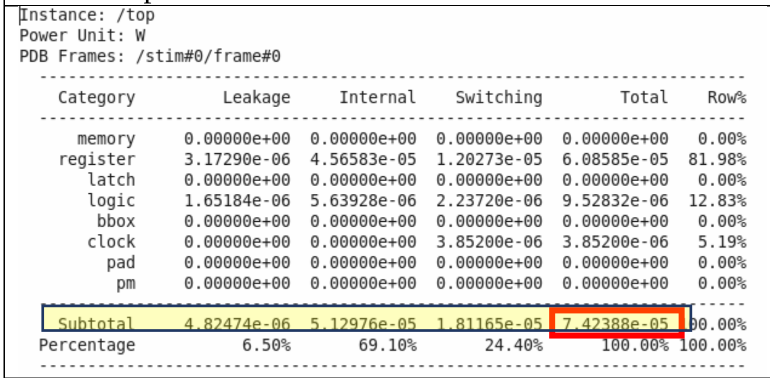


Fig4.5 FF_out block inside the synthesized netlist Schematic

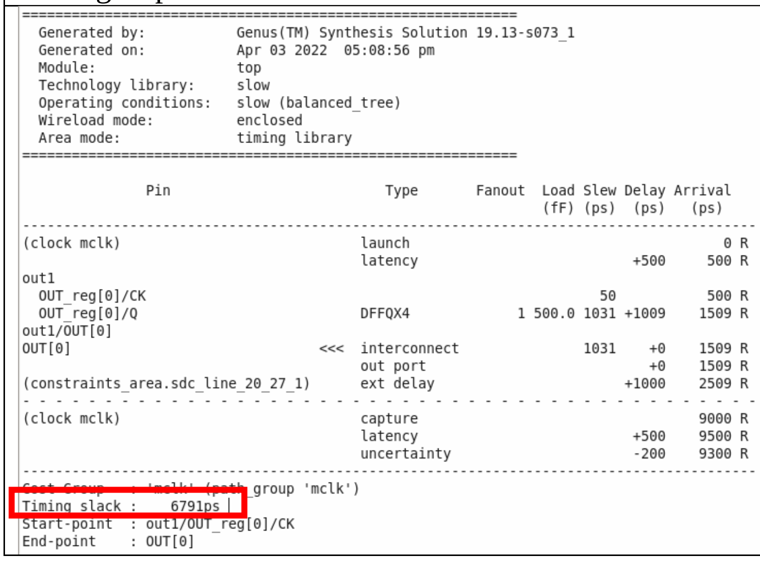
- As written in RTL code, the input is driven from Flipflops and output is taken from Flipflop.

Power Report



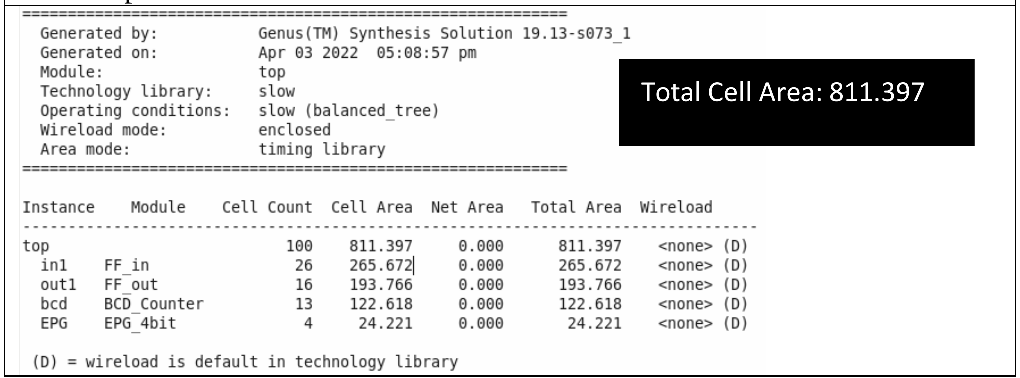
```
Instance: /top
Power Unit: W
PDB Frames: /stim#0/frame#0
  -------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  -------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     3.17290e-06  4.56583e-05  1.20273e-05  6.08585e-05  81.98%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.65184e-06  5.63928e-06  2.23720e-06  9.52832e-06  12.83%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  3.85200e-06  3.85200e-06   5.19%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  -------------------------------------------------------------------------
    Subtotal     4.82474e-06  5.12976e-05  1.81165e-05  7.42388e-05 100.00%
  Percentage           6.50%       69.10%       24.40%      100.00% 100.00%
  -------------------------------------------------------------------------
```

Timing Report



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 03 2022  05:08:56 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

              Pin                          Type       Fanout  Load Slew Delay Arrival
                                                              (fF) (ps)  (ps)   (ps)
-----------------------------------------------------------------------------------------
(clock mclk)                          launch                                     0 R
                                      latency                        +500      500 R
out1
  OUT_reg[0]/CK                                                     50         500 R
  OUT_reg[0]/Q                        DFFQX4            1 500.0 1031 +1009    1509 R
out1/OUT[0]
OUT[0]                           <<<  interconnect                1031   +0    1509 R
                                      out port                           +0    1509 R
(constraints_area.sdc_line_20_27_1)   ext delay                        +1000    2509 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock mclk)                          capture                                  9000 R
                                      latency                        +500     9500 R
                                      uncertainty                    -200     9300 R
-----------------------------------------------------------------------------------------
Cost Group   : 'mclk' (path_group 'mclk')
Timing slack :    6791ps
Start-point  : out1/OUT_reg[0]/CK
End-point    : OUT[0]
```

Area Report



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 03 2022  05:08:57 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance    Module      Cell Count  Cell Area  Net Area   Total Area  Wireload
--------------------------------------------------------------------------------
top                           100    811.397     0.000     811.397    <none> (D)
  in1     FF_in                26    265.672     0.000     265.672    <none> (D)
  out1    FF_out               16    193.766     0.000     193.766    <none> (D)
  bcd     BCD_Counter          13    122.618     0.000     122.618    <none> (D)
  EPG     EPG_4bit              4     24.221     0.000      24.221    <none> (D)

 (D) = wireload is default in technology library
```

Total Cell Area: 811.397

- In general, tool tries to optimize the design for minimum area for the given constraints.
- To have relaxed timing constraint attaining a larger positive slack, the time period has been increased to 9units.
- It's observed that after 9ns of time period the area remains constant and only the slack keeps on increasing.

4.(b) BEST TIMING, keeping timing constraints tight

SDC

```
create_clock -name mclk -period 1.795 [get_ports clk]

set_clock_transition -rise 0.05 [get_clocks mclk]
set_clock_transition -fall 0.05 [get_clocks mclk]
set_clock_uncertainty 0.2 [get_clocks mclk]
set_clock_latency 0.5 [get_clocks mclk]

set_input_delay -clock [get_clocks mclk] 1 [get_ports A]
set_input_delay -clock [get_clocks mclk] 1 [get_ports B]
set_input_delay -clock [get_clocks mclk] 1 [get_ports C]
set_input_delay -clock [get_clocks mclk] 1 [get_ports rst]

set_input_transition 0.01 [get_ports A]
set_input_transition 0.01 [get_ports B]
set_input_transition 0.01 [get_ports C]
set_input_transition 0.01 [get_ports rst]

set_output_delay -clock [get_clocks mclk] 1 [get_ports OUT]

set_load 0.5 [get_ports OUT]
```

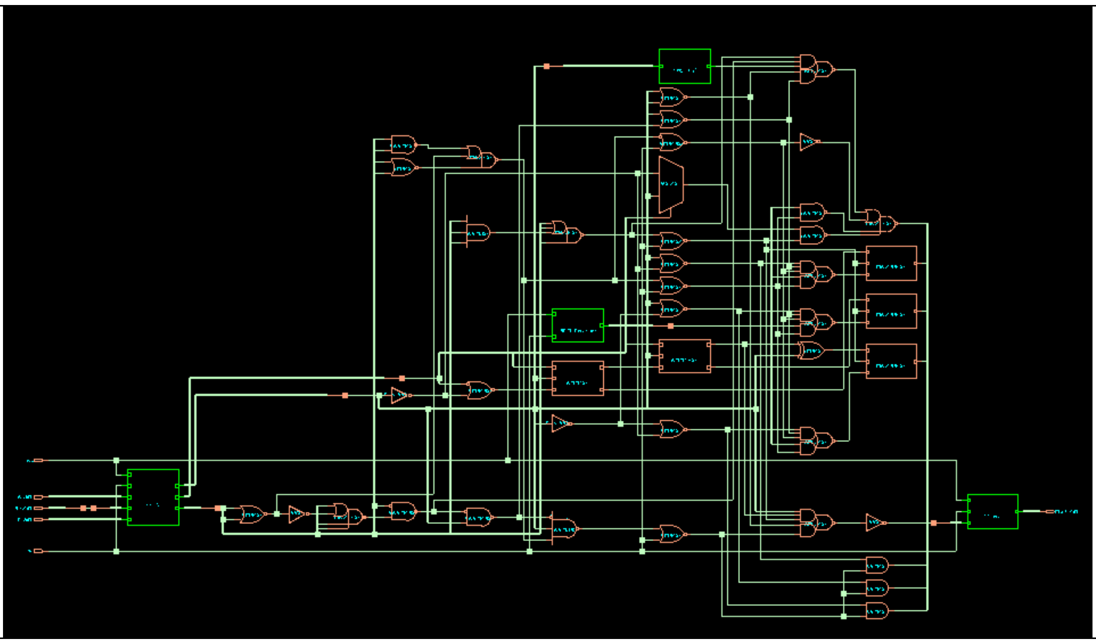


Fig4.6 Synthesised Netlist Schematic View (top module)

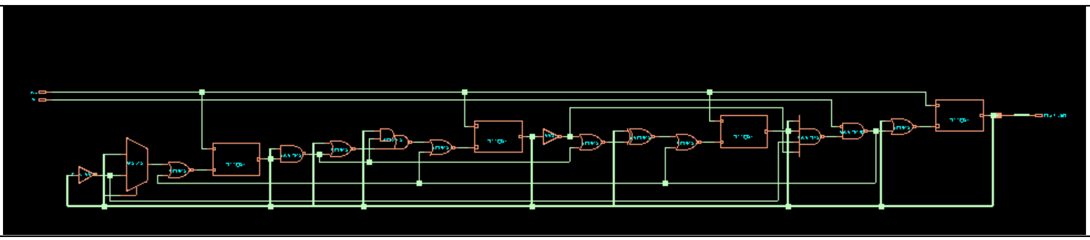


Fig4.7 BCD_Counter block inside the synthesized netlist Schematic

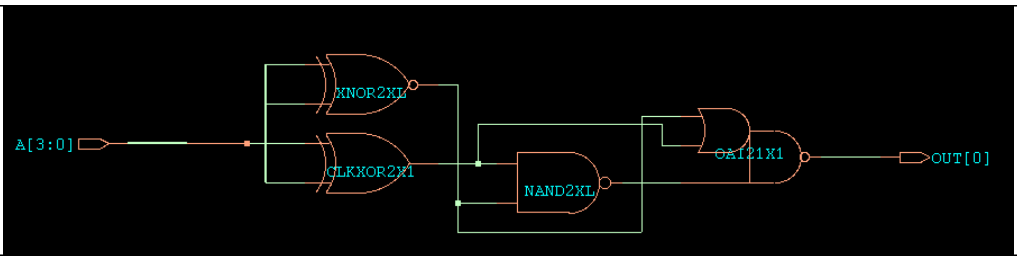


Fig4.8 EPG block inside the synthesized netlist Schematic

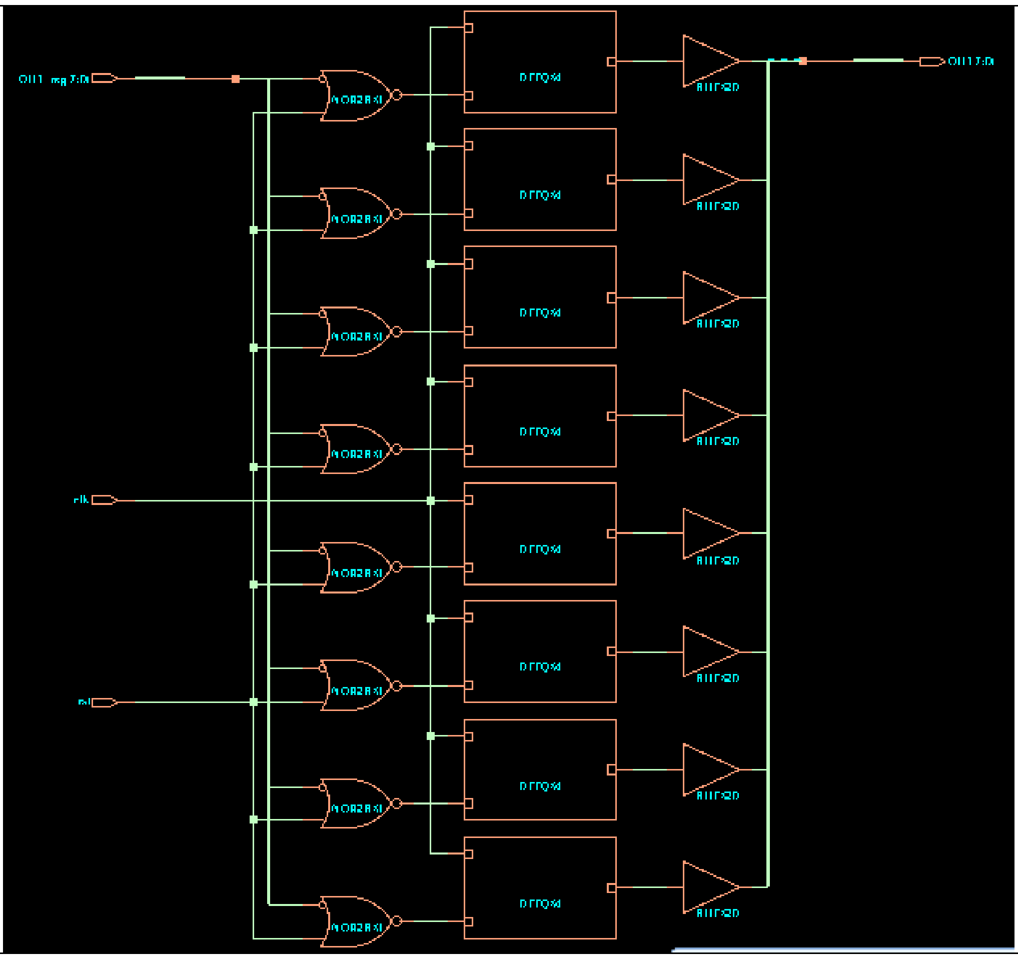
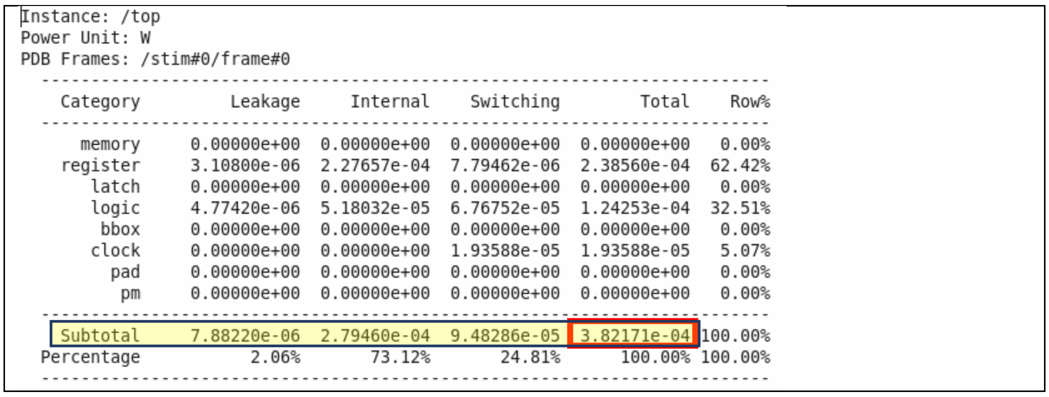
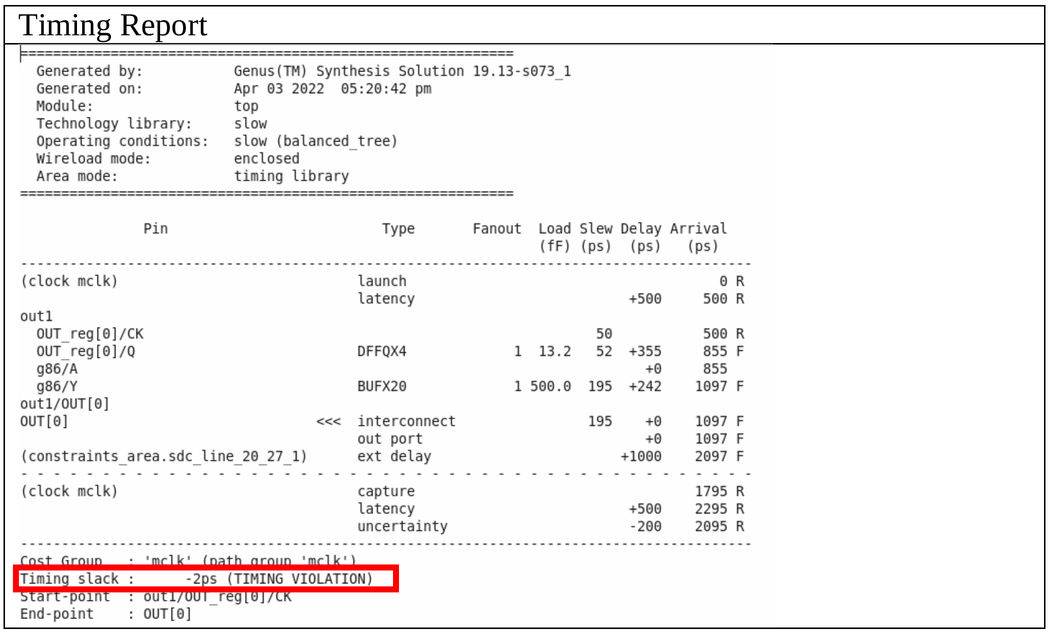


Fig 4.9 FF_out block inside the synthesized netlist Schematic

Power Report



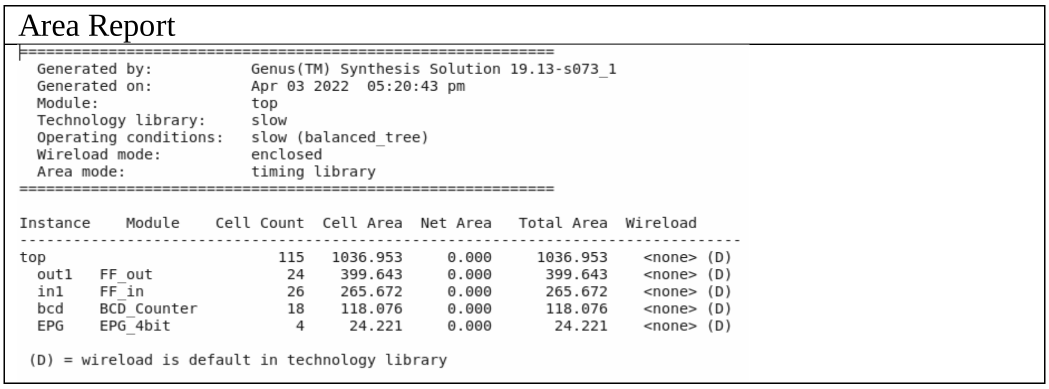
```
Instance: /top
Power Unit: W
PDB Frames: /stim#0/frame#0
  -------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  -------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     3.10800e-06  2.27657e-04  7.79462e-06  2.38560e-04  62.42%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     4.77420e-06  5.18032e-05  6.76752e-05  1.24253e-04  32.51%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  1.93588e-05  1.93588e-05   5.07%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  -------------------------------------------------------------------------
    Subtotal     7.88220e-06  2.79460e-04  9.48286e-05  3.82171e-04 100.00%
  Percentage           2.06%       73.12%       24.81%      100.00% 100.00%
  -------------------------------------------------------------------------
```



Timing Report

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 03 2022  05:20:42 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

               Pin                         Type       Fanout  Load Slew Delay Arrival
                                                              (fF) (ps)  (ps)   (ps)
-----------------------------------------------------------------------------------------
(clock mclk)                           launch                                    0 R
                                       latency                          +500   500 R
out1
  OUT_reg[0]/CK                                                    50          500 R
  OUT_reg[0]/Q                         DFFQX4              1  13.2  52  +355   855 F
  g86/A                                                                 +0     855
  g86/Y                                BUFX20              1 500.0 195  +242  1097 F
out1/OUT[0]
OUT[0]                            <<<  interconnect                 195   +0  1097 F
                                       out port                            +0  1097 F
(constraints_area.sdc_line_20_27_1)    ext delay                       +1000  2097 F
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock mclk)                           capture                                1795 R
                                       latency                          +500  2295 R
                                       uncertainty                      -200  2095 R
-----------------------------------------------------------------------------------------
Cost Group   : 'mclk' (path_group 'mclk')
Timing slack :      -2ps (TIMING VIOLATION)
Start-point  : out1/OUT_reg[0]/CK
End-point    : OUT[0]
```

- To have the best timing performance for the synthesised netlist, the time period of clock is reduced.
- The value has been chosen accordingly so that the there is a very offset of being to violate hold time analysis.



Area Report

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 03 2022  05:20:43 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance    Module    Cell Count  Cell Area  Net Area  Total Area  Wireload
---------------------------------------------------------------------------------
top                          115   1036.953     0.000    1036.953    <none> (D)
  out1    FF_out              24    399.643     0.000     399.643    <none> (D)
  in1     FF_in               26    265.672     0.000     265.672    <none> (D)
  bcd     BCD_Counter         18    118.076     0.000     118.076    <none> (D)
  EPG     EPG_4bit             4     24.221     0.000      24.221    <none> (D)

 (D) = wireload is default in technology library
```

4.(c) INTERMEDIATE SLACK

SDC

```
create_clock -name mclk -period 6 [get_ports clk]

set_clock_transition -rise 0.05 [get_clocks mclk]
set_clock_transition -fall 0.05 [get_clocks mclk]
set_clock_uncertainty 0.2 [get_clocks mclk]
set_clock_latency 0.5 [get_clocks mclk]

set_input_delay -clock [get_clocks mclk] 1 [get_ports A]
set_input_delay -clock [get_clocks mclk] 1 [get_ports B]
set_input_delay -clock [get_clocks mclk] 1 [get_ports C]
set_input_delay -clock [get_clocks mclk] 1 [get_ports rst]

set_input_transition 0.01 [get_ports A]
set_input_transition 0.01 [get_ports B]
set_input_transition 0.01 [get_ports C]
set_input_transition 0.01 [get_ports rst]

set_output_delay -clock [get_clocks mclk] 1 [get_ports OUT]

set_load 0.5 [get_ports OUT]
```

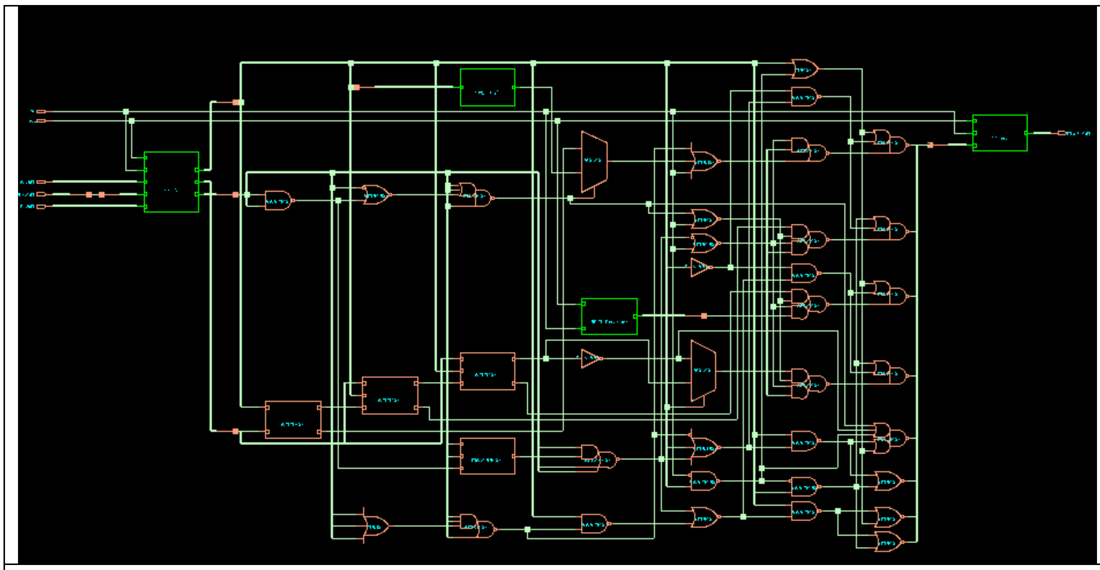


Fig4.10 Synthesised Netlist Schematic View (top module)

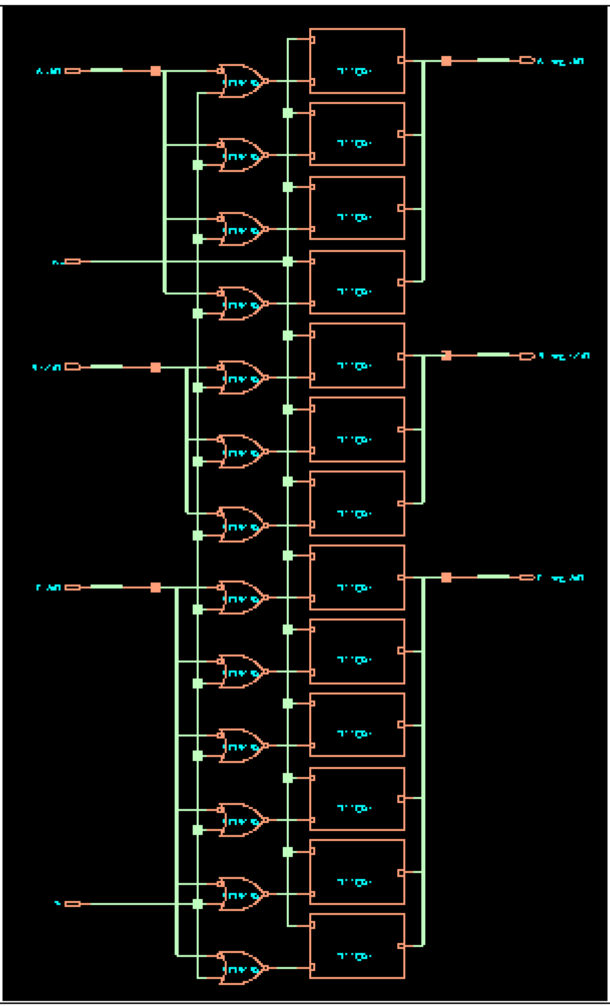


Fig4.11 FF_in block inside the synthesized netlist Schematic

BCD_COUNTER

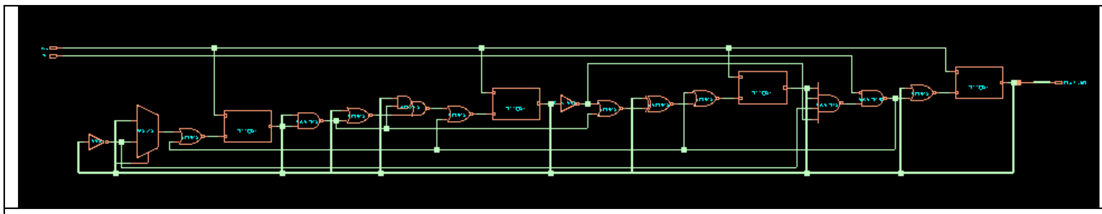


Fig4.12 BCD_Counter block inside the synthesized netlist Schematic

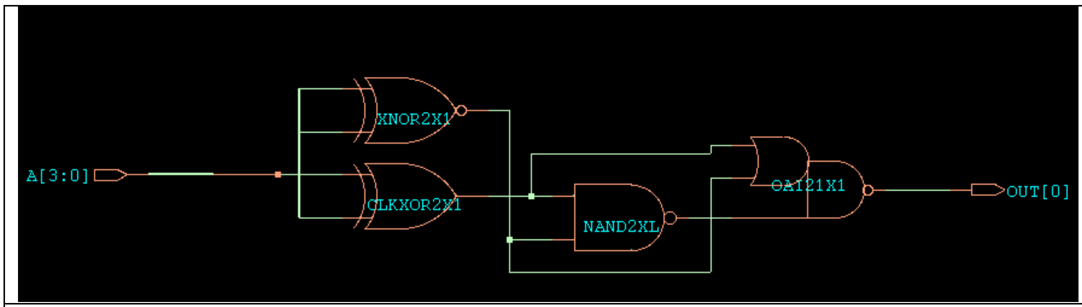


Fig4.13 EPG block inside the synthesized netlist Schematic

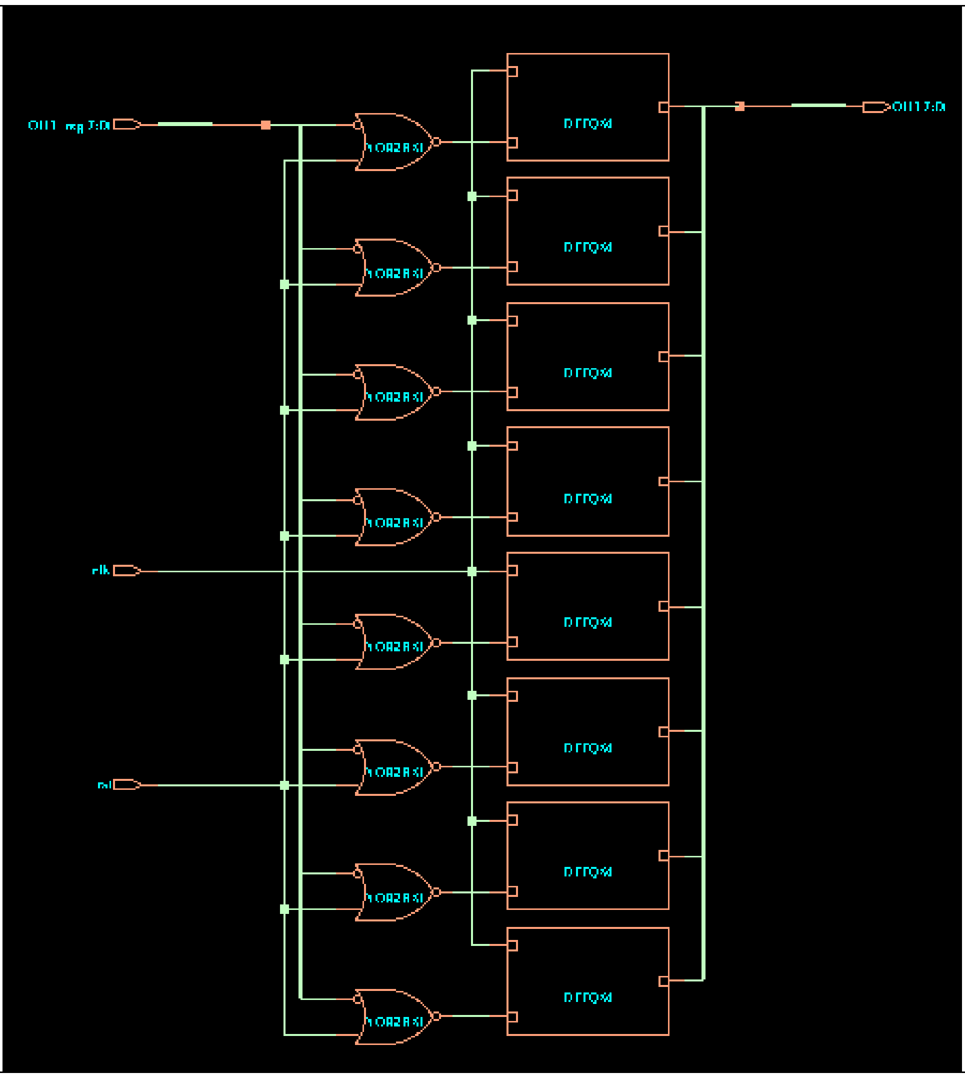
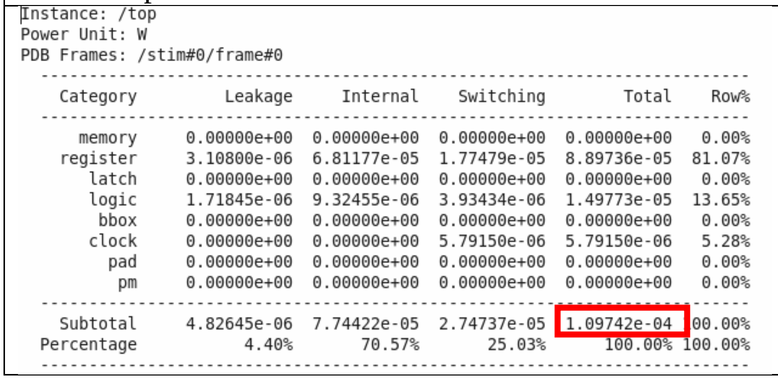


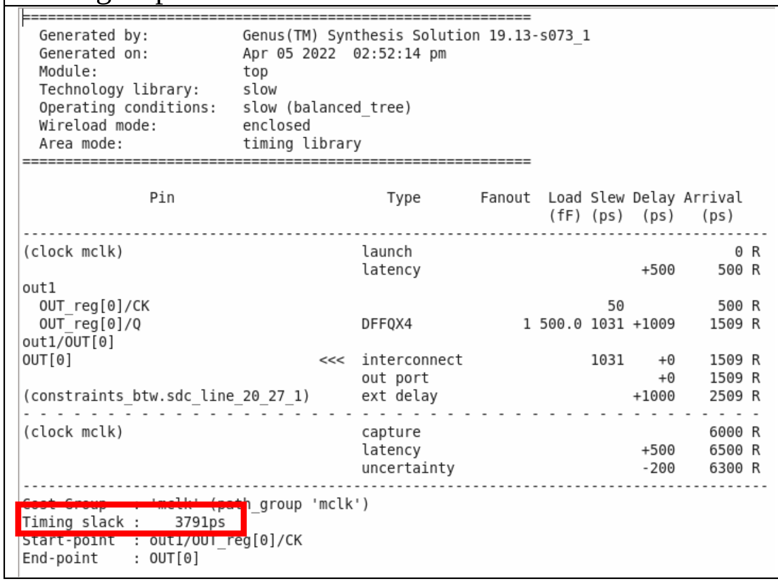
Fig4.14 FF_out block inside the synthesized netlist Schematic

Power Report



```
Instance: /top
Power Unit: W
PDB Frames: /stim#0/frame#0
  -------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  -------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     3.10800e-06  6.81177e-05  1.77479e-05  8.89736e-05  81.07%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     1.71845e-06  9.32455e-06  3.93434e-06  1.49773e-05  13.65%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  5.79150e-06  5.79150e-06   5.28%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  -------------------------------------------------------------------------
    Subtotal     4.82645e-06  7.74422e-05  2.74737e-05  1.09742e-04 100.00%
  Percentage           4.40%       70.57%       25.03%      100.00% 100.00%
  -------------------------------------------------------------------------
```

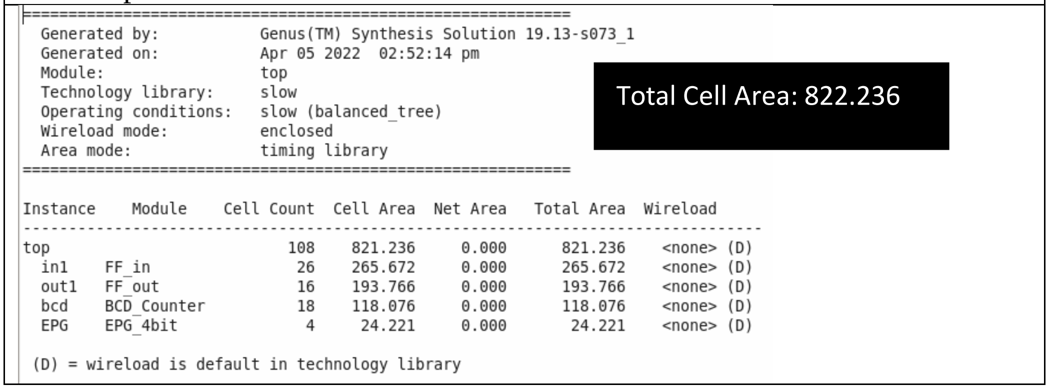
Timing Report



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 05 2022  02:52:14 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

              Pin                        Type       Fanout  Load Slew Delay Arrival
                                                             (fF) (ps)  (ps)   (ps)
---------------------------------------------------------------------------------------
(clock mclk)                           launch                                  0 R
                                       latency                        +500   500 R
out1
  OUT_reg[0]/CK                                                   50           500 R
  OUT_reg[0]/Q                         DFFQX4            1 500.0 1031 +1009   1509 R
out1/OUT[0]
OUT[0]                            <<<  interconnect                 1031    +0   1509 R
                                       out port                             +0   1509 R
(constraints_btw.sdc_line_20_27_1)     ext delay                         +1000   2509 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock mclk)                           capture                                6000 R
                                       latency                          +500   6500 R
                                       uncertainty                      -200   6300 R
---------------------------------------------------------------------------------------
Cost Group   : 'mclk' (path_group 'mclk')
Timing slack :    3791ps
Start-point  : out1/OUT_reg[0]/CK
End-point    : OUT[0]
```

The time period has been chosen accordingly, so that the slack is in between the to cases of minimum area and best timing.

Area Report



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 05 2022  02:52:14 pm
  Module:                 top
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

Instance    Module    Cell Count  Cell Area  Net Area   Total Area  Wireload
---------------------------------------------------------------------------------
top                          108    821.236     0.000      821.236    <none> (D)
  in1     FF_in               26    265.672     0.000      265.672    <none> (D)
  out1    FF_out              16    193.766     0.000      193.766    <none> (D)
  bcd     BCD_Counter         18    118.076     0.000      118.076    <none> (D)
  EPG     EPG_4bit             4     24.221     0.000       24.221    <none> (D)

 (D) = wireload is default in technology library
```

Total Cell Area: 822.236

4.2 Quality of Results (QoR)

	Time Period (ns)	Power (μ W)	Slack (ps)	Area
Minimum Area	9	74.238	6791	811.397
Best Timing	1.795	382.171	-2	1036.953
Intermediate Slack	6	109.742	3791	822.236

[1] The major attribute to the QoR of all the three constraints is time period.

[2] For minimum area with relaxed timing constraint the tool chooses the best possible resources to have minimum area for the given constraints specified for the RTL code. Hence, the area obtained for the minimum area netlist is 811.397.

[3] As time period is decreased in constraint file, the tool chooses the resources accordingly from the library file to meet the timing constraints for the given RTL code. Hence maximum area is synthesized for the best timing case.

[4] To conclude for the best timing constraint with the same RTL code, the tool chooses different cells from the library for best timing performance

[5] As expected, increasing the time period increases the slack.

[6] Decreasing clock period reduces the circuit propagation time for the signal. Due to which the required time (RT) decreases. Hence the setup slack decreases to a negative value.

[7] Changing constraints also results in optimized use of resources from library. As in case of minimum area because of relaxed timing constraints, the half adder is replaced by logic gates to implement the functionality.

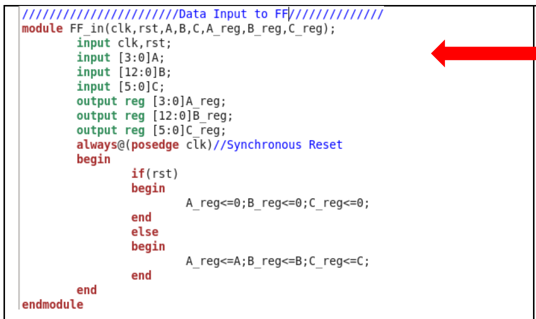
[8] Total Power increases as the cell count increases from decreasing the time period.

[9] Switching power increases as the time period is decreased, i.e., operating at higher frequency leading to more toggling of bits that then consume more power.

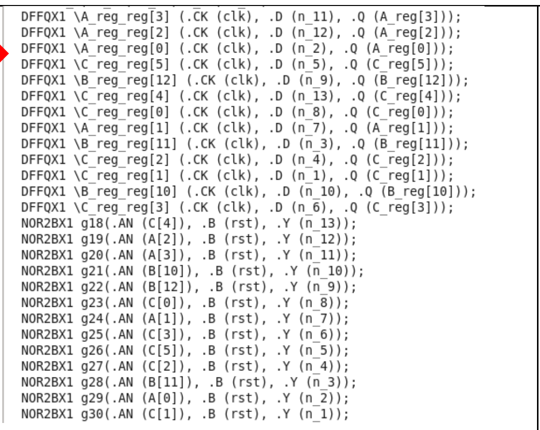
[10] The intermediate slack case has all the QoR in between the minimum area and best timing cases.

4.3 Mapping of RTL into Netlist:

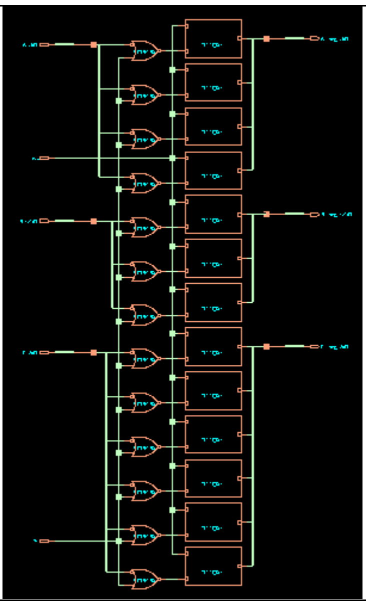
The following analysis is done for the Intermediate slack netlist



```
///////////////////////Data Input to FF//////////////
module FF_in(clk,rst,A,B,C,A_reg,B_reg,C_reg);
        input clk,rst;
        input [3:0]A;
        input [12:0]B;
        input [5:0]C;
        output reg [3:0]A_reg;
        output reg [12:0]B_reg;
        output reg [5:0]C_reg;
        always@(posedge clk)//Synchronous Reset
        begin
                if(rst)
                begin
                        A_reg<=0;B_reg<=0;C_reg<=0;
                end
                else
                begin
                        A_reg<=A;B_reg<=B;C_reg<=C;
                end
        end
endmodule
```



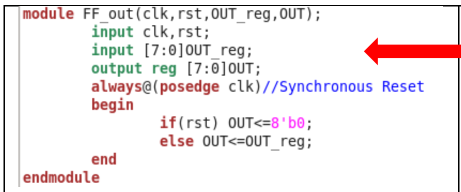
```
DFFQX1 \A_reg_reg[3] (.CK (clk), .D (n_11), .Q (A_reg[3]));
DFFQX1 \A_reg_reg[2] (.CK (clk), .D (n_12), .Q (A_reg[2]));
DFFQX1 \A_reg_reg[0] (.CK (clk), .D (n_2), .Q (A_reg[0]));
DFFQX1 \C_reg_reg[5] (.CK (clk), .D (n_5), .Q (C_reg[5]));
DFFQX1 \B_reg_reg[12] (.CK (clk), .D (n_9), .Q (B_reg[12]));
DFFQX1 \C_reg_reg[4] (.CK (clk), .D (n_13), .Q (C_reg[4]));
DFFQX1 \C_reg_reg[0] (.CK (clk), .D (n_8), .Q (C_reg[0]));
DFFQX1 \A_reg_reg[1] (.CK (clk), .D (n_7), .Q (A_reg[1]));
DFFQX1 \B_reg_reg[11] (.CK (clk), .D (n_3), .Q (B_reg[11]));
DFFQX1 \C_reg_reg[2] (.CK (clk), .D (n_4), .Q (C_reg[2]));
DFFQX1 \C_reg_reg[1] (.CK (clk), .D (n_1), .Q (C_reg[1]));
DFFQX1 \B_reg_reg[10] (.CK (clk), .D (n_10), .Q (B_reg[10]));
DFFQX1 \C_reg_reg[3] (.CK (clk), .D (n_6), .Q (C_reg[3]));
NOR2BX1 g18(.AN (C[4]), .B (rst), .Y (n_13));
NOR2BX1 g19(.AN (A[2]), .B (rst), .Y (n_12));
NOR2BX1 g20(.AN (A[3]), .B (rst), .Y (n_11));
NOR2BX1 g21(.AN (B[10]), .B (rst), .Y (n_10));
NOR2BX1 g22(.AN (B[12]), .B (rst), .Y (n_9));
NOR2BX1 g23(.AN (C[0]), .B (rst), .Y (n_8));
NOR2BX1 g24(.AN (A[1]), .B (rst), .Y (n_7));
NOR2BX1 g25(.AN (C[3]), .B (rst), .Y (n_6));
NOR2BX1 g26(.AN (C[5]), .B (rst), .Y (n_5));
NOR2BX1 g27(.AN (C[2]), .B (rst), .Y (n_4));
NOR2BX1 g28(.AN (B[11]), .B (rst), .Y (n_3));
NOR2BX1 g29(.AN (A[0]), .B (rst), .Y (n_2));
NOR2BX1 g30(.AN (C[1]), .B (rst), .Y (n_1));
```



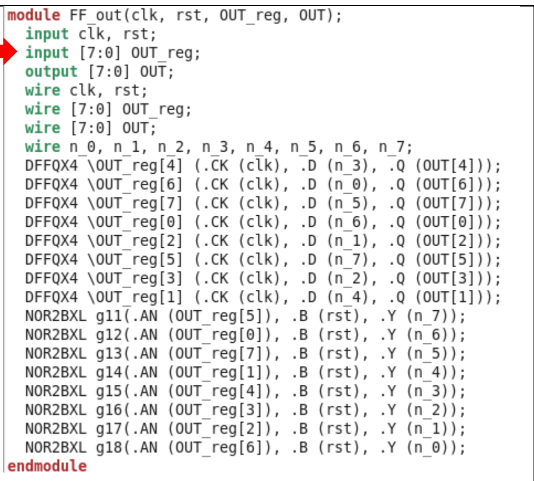
- RTL code above is used to take inputs (A, B, C) to the flip flops, the tool maps the flipflop DFFQX1.

- The netlist uses NOR2BX1 gate for the reset logic in RTL code, i.e., one input to nor gate is 'rst' signal and second input is one bit of inputs.

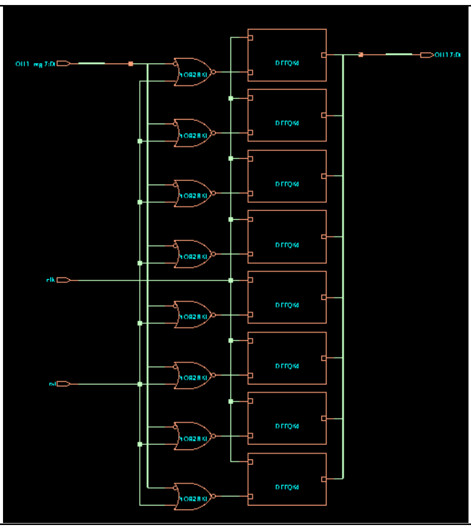
- As in the RTL code only B[12:10] i.e, three bits of 13 bits of B being used, the netlist only considers 3 flip flops to take in input from B for those bits.



```
module FF_out(clk,rst,OUT_reg,OUT);
        input clk,rst;
        input [7:0]OUT_reg;
        output reg [7:0]OUT;
        always@(posedge clk)//Synchronous Reset
        begin
                if(rst) OUT<=8'b0;
                else OUT<=OUT_reg;
        end
endmodule
```

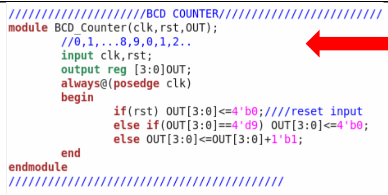


```
module FF_out(clk, rst, OUT_reg, OUT);
  input clk, rst;
  input [7:0] OUT_reg;
  output [7:0] OUT;
  wire clk, rst;
  wire [7:0] OUT_reg;
  wire [7:0] OUT;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  DFFQX4 \OUT_reg[4] (.CK (clk), .D (n_3), .Q (OUT[4]));
  DFFQX4 \OUT_reg[6] (.CK (clk), .D (n_0), .Q (OUT[6]));
  DFFQX4 \OUT_reg[7] (.CK (clk), .D (n_5), .Q (OUT[7]));
  DFFQX4 \OUT_reg[0] (.CK (clk), .D (n_6), .Q (OUT[0]));
  DFFQX4 \OUT_reg[2] (.CK (clk), .D (n_1), .Q (OUT[2]));
  DFFQX4 \OUT_reg[5] (.CK (clk), .D (n_7), .Q (OUT[5]));
  DFFQX4 \OUT_reg[3] (.CK (clk), .D (n_2), .Q (OUT[3]));
  DFFQX4 \OUT_reg[1] (.CK (clk), .D (n_4), .Q (OUT[1]));
  NOR2BXL g11(.AN (OUT_reg[5]), .B (rst), .Y (n_7));
  NOR2BXL g12(.AN (OUT_reg[0]), .B (rst), .Y (n_6));
  NOR2BXL g13(.AN (OUT_reg[7]), .B (rst), .Y (n_5));
  NOR2BXL g14(.AN (OUT_reg[1]), .B (rst), .Y (n_4));
  NOR2BXL g15(.AN (OUT_reg[4]), .B (rst), .Y (n_3));
  NOR2BXL g16(.AN (OUT_reg[3]), .B (rst), .Y (n_2));
  NOR2BXL g17(.AN (OUT_reg[2]), .B (rst), .Y (n_1));
  NOR2BXL g18(.AN (OUT_reg[6]), .B (rst), .Y (n_0));
endmodule
```

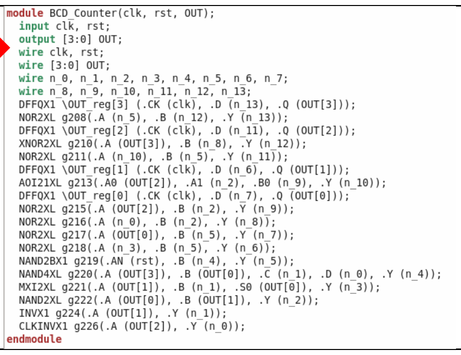


- As defined in the RTL code the outputs are driven by the Flip Flop DFFQX4.

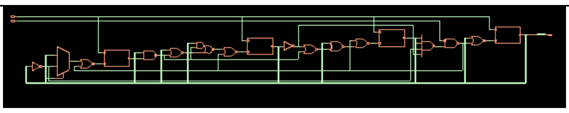
- The output is of eight bits; hence 8 Flip flops are used. For each FF the input is given from a NOR2BXL gate for the reset logic in RTL code. i.e., when the reset signal is high then the output of NOR or the input to D-FF is '0'.

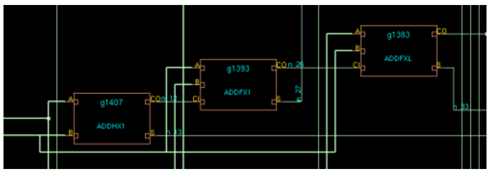


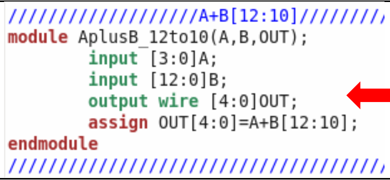
```
//////////////////////BCD COUNTER////////////////////////
module BCD_Counter(clk,rst,OUT);
        //0,1,...8,9,0,1,2..
        input clk,rst;
        output reg [3:0]OUT;
        always@(posedge clk)
        begin
                if(rst) OUT[3:0]<=4'b0;////reset input
                else if(OUT[3:0]==4'd9) OUT[3:0]<=4'b0;
                else OUT[3:0]<=OUT[3:0]+1'b1;
        end
endmodule
/////////////////////////////////////////
```



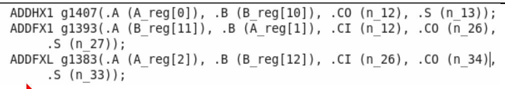
```
module BCD_Counter(clk, rst, OUT);
  input clk, rst;
  output [3:0] OUT;
  wire clk, rst;
  wire [3:0] OUT;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  wire n_8, n_9, n_10, n_11, n_12, n_13;
  DFFQX1 \OUT_reg[3] (.CK (clk), .D (n_13), .Q (OUT[3]));
  NOR2XL g208(.A (n_5), .B (n_12), .Y (n_13));
  DFFQX1 \OUT_reg[2] (.CK (clk), .D (n_11), .Q (OUT[2]));
  XNOR2XL g210(.A (OUT[3]), .B (n_8), .Y (n_12));
  NOR2XL g211(.A (n_10), .B (n_5), .Y (n_11));
  DFFQX1 \OUT_reg[1] (.CK (clk), .D (n_6), .Q (OUT[1]));
  AOI21XL g213(.A0 (OUT[2]), .A1 (n_2), .B0 (n_9), .Y (n_10));
  DFFQX1 \OUT_reg[0] (.CK (clk), .D (n_7), .Q (OUT[0]));
  NOR2XL g215(.A (OUT[2]), .B (n_2), .Y (n_9));
  NOR2XL g216(.A (n_0), .B (n_2), .Y (n_8));
  NOR2XL g217(.A (OUT[0]), .B (n_5), .Y (n_7));
  NOR2XL g218(.A (n_3), .B (n_5), .Y (n_6));
  NAND2BX1 g219(.AN (rst), .B (n_4), .Y (n_5));
  NAND4XL g220(.A (OUT[3]), .B (OUT[0]), .C (n_1), .D (n_0), .Y (n_4));
  MXI2XL g221(.A (OUT[1]), .B (n_1), .S0 (OUT[0]), .Y (n_3));
  NAND2XL g222(.A (OUT[0]), .B (OUT[1]), .Y (n_2));
  INVX1 g224(.A (OUT[1]), .Y (n_1));
  CLKINVX1 g226(.A (OUT[2]), .Y (n_0));
endmodule
```





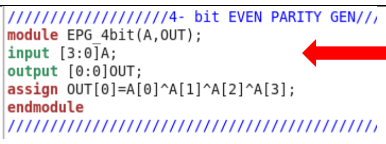


```
///////////////////A+B[12:10]/////////
module AplusB_12to10(A,B,OUT);
        input [3:0]A;
        input [12:0]B;
        output wire [4:0]OUT;
        assign OUT[4:0]=A+B[12:10];
endmodule
/////////////////////////////////////
```

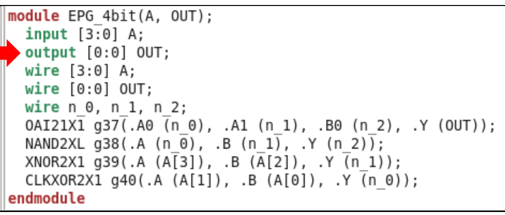


```
ADDHX1 g1407(.A (A_reg[0]), .B (B_reg[10]), .CO (n_12), .S (n_13));
ADDFX1 g1393(.A (B_reg[11]), .B (A_reg[1]), .CI (n_12), .CO (n_26),
      .S (n_27));
ADDFXL g1383(.A (A_reg[2]), .B (B_reg[12]), .CI (n_26), .CO (n_34),
      .S (n_33));
```

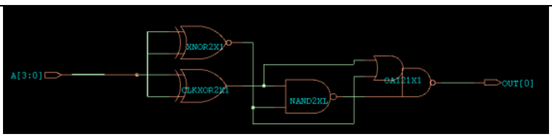
- In the RTL code the operation need to be performed is A+B[12:10]. The netlist synthesised by the tool uses one half adder and two full adders for computing addition of the three bits, for the MSB of A the addition is performed with the carry is performed using MUX and combinational logic.



```
///////////////////4- bit EVEN PARITY GEN//
module EPG_4bit(A,OUT);
input [3:0]A;
output [0:0]OUT;
assign OUT[0]=A[0]^A[1]^A[2]^A[3];
endmodule
//////////////////////////////////////////
```



```
module EPG_4bit(A, OUT);
  input [3:0] A;
  output [0:0] OUT;
  wire [3:0] A;
  wire [0:0] OUT;
  wire n_0, n_1, n_2;
  OAI21X1 g37(.A0 (n_0), .A1 (n_1), .B0 (n_2), .Y (OUT));
  NAND2XL g38(.A (n_0), .B (n_1), .Y (n_2));
  XNOR2X1 g39(.A (A[3]), .B (A[2]), .Y (n_1));
  CLKXOR2X1 g40(.A (A[1]), .B (A[0]), .Y (n_0));
endmodule
```



- For the even parity generator, the behavioural level code in RTL is optimised by the tool to perform the desired functionality using OAI, NAND, XOR and XNOR.

LOGICAL EQUIVALENCE CHECKING

Command:

lec -lpgxl script.tcl

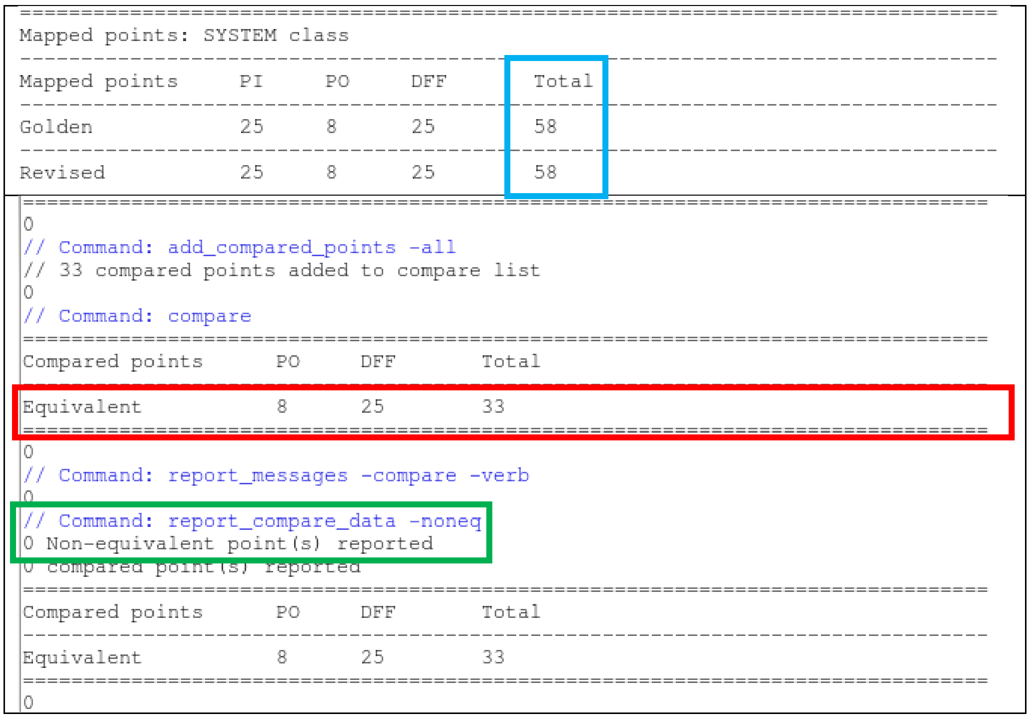
Script:

```
set_attr library slow.lib
read_hdl vdf_prj.v
elaborate
read_sdc constraints_area.sdc
report timing -lint
set_attribute dft_scan_style muxed_scan
define_dft shift_enable -active high -create_port scan_en
define_dft test_mode -active high -create_port test_mode
define_dft test_clock clk
report dft_setup
check_dft_rules > dft_report/dft_rules_report
fix_dft_violations -test_control test_mode -async_set -async_reset -clock
synthesize -to_mapped
set_attr dft_min_number_of_scan_chains 2 top
set_attr dft_mix_clock_edges_in_scan_chains true top
#replace_scan
connect_scan_chains -auto_create_chains -preview
connect_scan_chains -auto_create_chains
report qor
write_atpg -cadence > top.atpg
write_atpg -stil > top_still.atpg
write_scandef > dft_report/top.def
write_sdf -timescale ns -nonegchecks -recrem split -edges check_edge >
syn_report/delays.sdf
write_hdl > dft_report/synthesised_netlist.v
write_sdc > dft_report/sdc_file_for_physical_design.sdc
write_script > dft_report/synthesis_script_sdc.g
report timing > dft_report/synthesis_timing_report.rep
report power > dft_report/synthesis_power_report.rep
report gates > dft_report/synthesis_cell_report.rep
report area > dft_report/synthesis_area_report.rep
gui_show
```

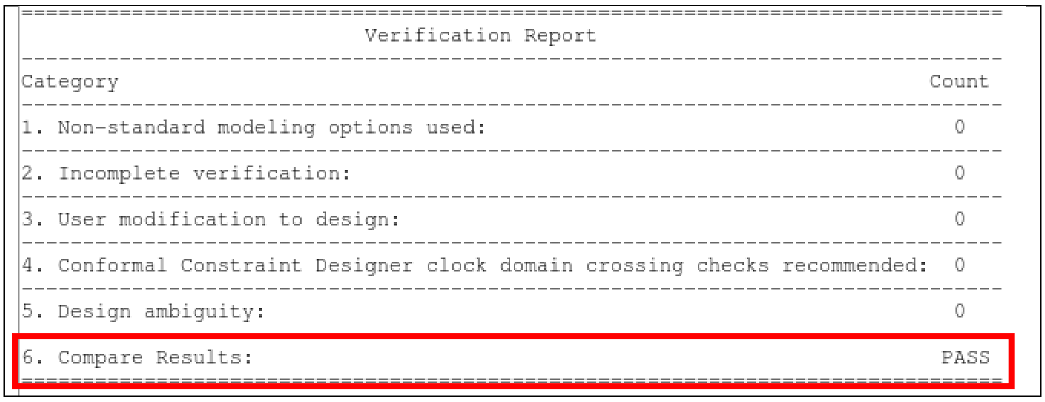
5.1.1 Equivalence checking of netlist generated for minimum area

- ❖ The image shown below shows the total mapped points and compared points while performing the LEC.
  - We can see that total of 58 points of golden netlist (RTL) can be mapped to the revised netlist.
  - Then total 33 points have been compared which includes output ports and DFFs also.

- ❖ Also, from the verification report we can see that generated netlist is equivalent to the golden netlist (RTL).



```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points     PI      PO      DFF       Total
--------------------------------------------------------------------------------
Golden            25      8       25        58
--------------------------------------------------------------------------------
Revised           25      8       25        58
================================================================================
0
// Command: add_compared_points -all
// 33 compared points added to compare list
0
// Command: compare
================================================================================
Compared points       PO      DFF        Total
Equivalent            8       25         33
================================================================================
0
// Command: report_messages -compare -verb
0
// Command: report_compare_data -noneq
0 Non-equivalent point(s) reported
0 compared point(s) reported
================================================================================
Compared points       PO      DFF        Total
--------------------------------------------------------------------------------
Equivalent            8       25         33
================================================================================
0
```

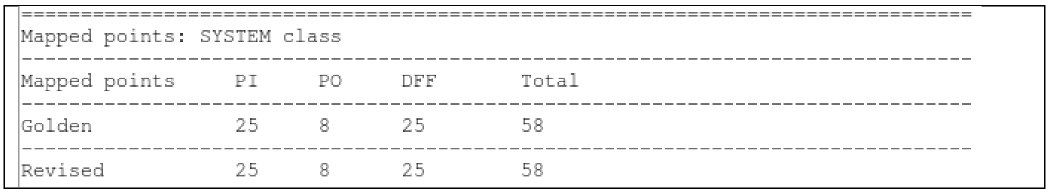


```
================================================================================
                           Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                 0
--------------------------------------------------------------------------------
3. User modification to design:                                             0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                        0

6. Compare Results:                                                      PASS
================================================================================
```

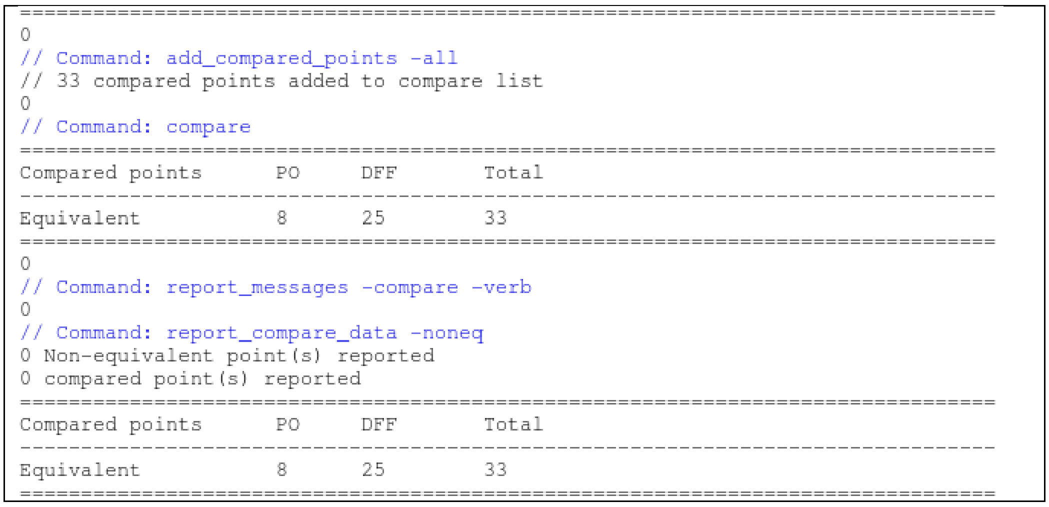
5.1.2 Equivalence checking of netlist generated for best timing

❖ Similarly, the reports for best timing netlist compared with golden netlist is shown below which shows that:
- All the 58 points in golden netlist can be mapped into the revised netlist.
- All the 33 points that have been compared between the two netlists have found to be equivalent.

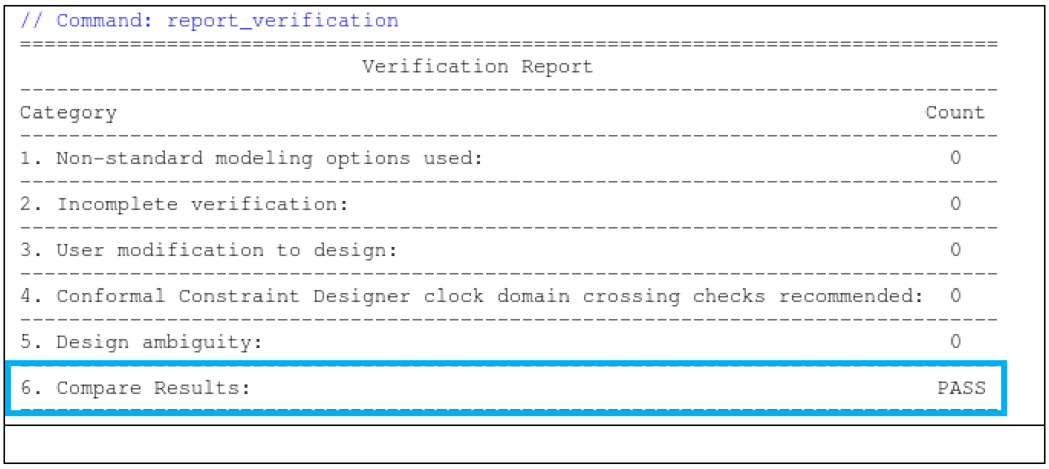
❖ Also, from the verification report we can see that generated netlist is equivalent to the golden netlist (RTL) and it has shown the PASS result.



```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points     PI      PO      DFF        Total
--------------------------------------------------------------------------------
Golden            25      8       25         58
--------------------------------------------------------------------------------
Revised           25      8       25         58
```



```
================================================================================
0
// Command: add_compared_points -all
// 33 compared points added to compare list
0
// Command: compare
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           8      25        33
================================================================================
0
// Command: report_messages -compare -verb
0
// Command: report_compare_data -noneq
0 Non-equivalent point(s) reported
0 compared point(s) reported
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           8      25        33
================================================================================
```

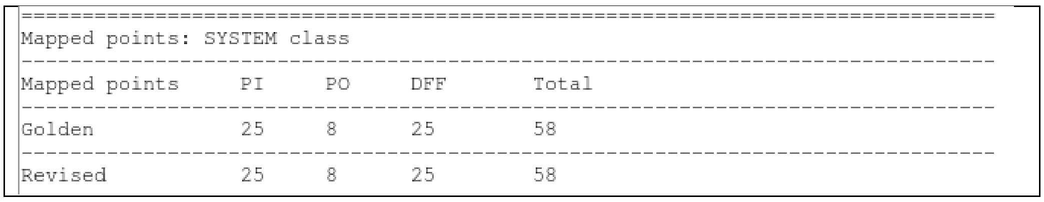


```
// Command: report_verification
================================================================================
                            Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                 0
--------------------------------------------------------------------------------
3. User modification to design:                                             0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                        0
--------------------------------------------------------------------------------
6. Compare Results:                                                      PASS
--------------------------------------------------------------------------------
```

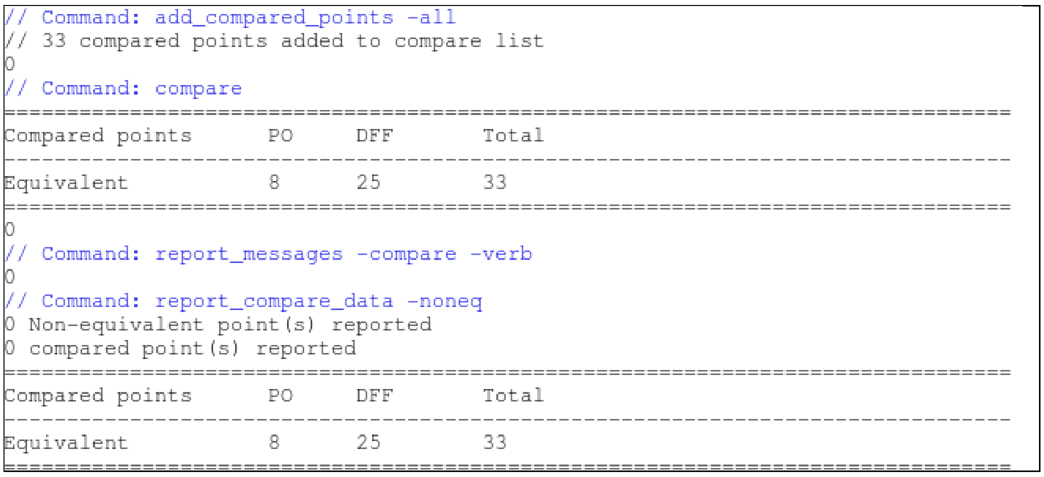
5.1.3 Equivalence checking of netlist generated for Intermediate Slack:-

❖ Similarly, the reports for intermediate slack netlist compared with golden netlist is shown below which shows that:
  - All the 58 points in golden netlist could be mapped into the revised netlist.
  - All the 33 points that have been compared between the two netlists have found to be equivalent.

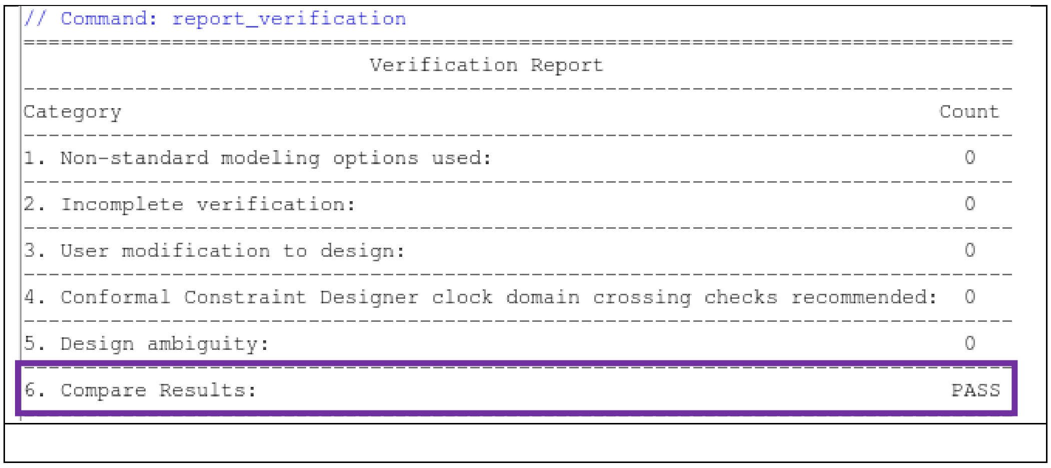
❖ Also, from the verification report we can see that generated netlist is equivalent to the golden netlist (RTL) and it has shown the PASS result.



```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points      PI      PO      DFF       Total
--------------------------------------------------------------------------------
Golden             25      8       25        58
--------------------------------------------------------------------------------
Revised            25      8       25        58
```



```
// Command: add_compared_points -all
// 33 compared points added to compare list
0
// Command: compare
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           8      25        33
================================================================================
0
// Command: report_messages -compare -verb
0
// Command: report_compare_data -noneq
0 Non-equivalent point(s) reported
0 compared point(s) reported
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           8      25        33
================================================================================
```



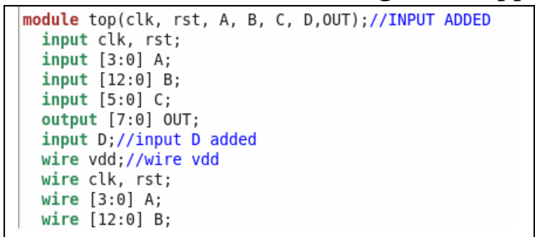
```
// Command: report_verification
================================================================================
                            Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                 0
--------------------------------------------------------------------------------
3. User modification to design:                                             0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                        0
--------------------------------------------------------------------------------
6. Compare Results:                                                      PASS
--------------------------------------------------------------------------------
```

From the above equivalence checking results and from the fact that all the three netlists have been synthesized from the same RTL, we can infer that all the designs are equivalent.

5.2 **Equivalence checking of Bad Netlist**

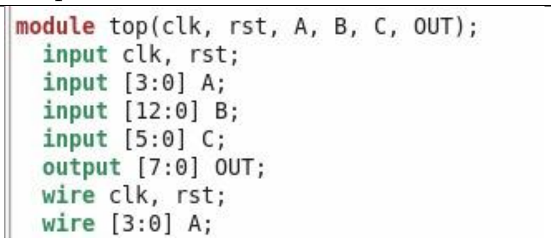
5.2.1 Netlist with extra wires added and connected to Output Ports/Pins:-

- ❖ We added an extra input D in the netlist.
- ❖ Also, we included extra wires like vdd, gnd in the top module and connected vdd to A_reg[3] through a DFF.
- ❖ As, a result of which we got unmapped components which has been shown below.



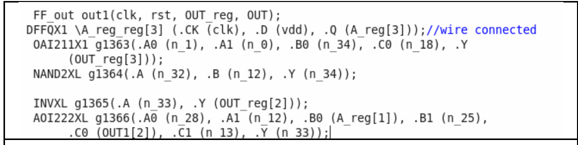
```
module top(clk, rst, A, B, C, D,OUT);//INPUT ADDED
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
  input D;//input D added
  wire vdd;//wire vdd
  wire clk, rst;
  wire [3:0] A;
  wire [12:0] B;
```

(a) Revised Netlist



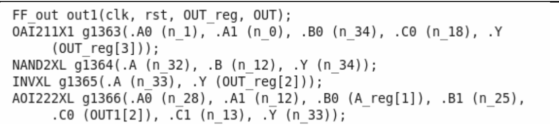
```
module top(clk, rst, A, B, C, OUT);
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
  wire clk, rst;
  wire [3:0] A;
```

(b) Golden Netlist



```
 FF_out out1(clk, rst, OUT_reg, OUT);
DFFQX1 \A_reg_reg[3] (.CK (clk), .D (vdd), .Q (A_reg[3]));//wire connected
 OAI211X1 g1363(.A0 (n_1), .A1 (n_0), .B0 (n_34), .C0 (n_18), .Y
      (OUT_reg[3]));
 NAND2XL g1364(.A (n_32), .B (n_12), .Y (n_34));

 INVXL g1365(.A (n_33), .Y (OUT_reg[2]));
 AOI222XL g1366(.A0 (n_28), .A1 (n_12), .B0 (A_reg[1]), .B1 (n_25),
      .C0 (OUT1[2]), .C1 (n_13), .Y (n_33));
```

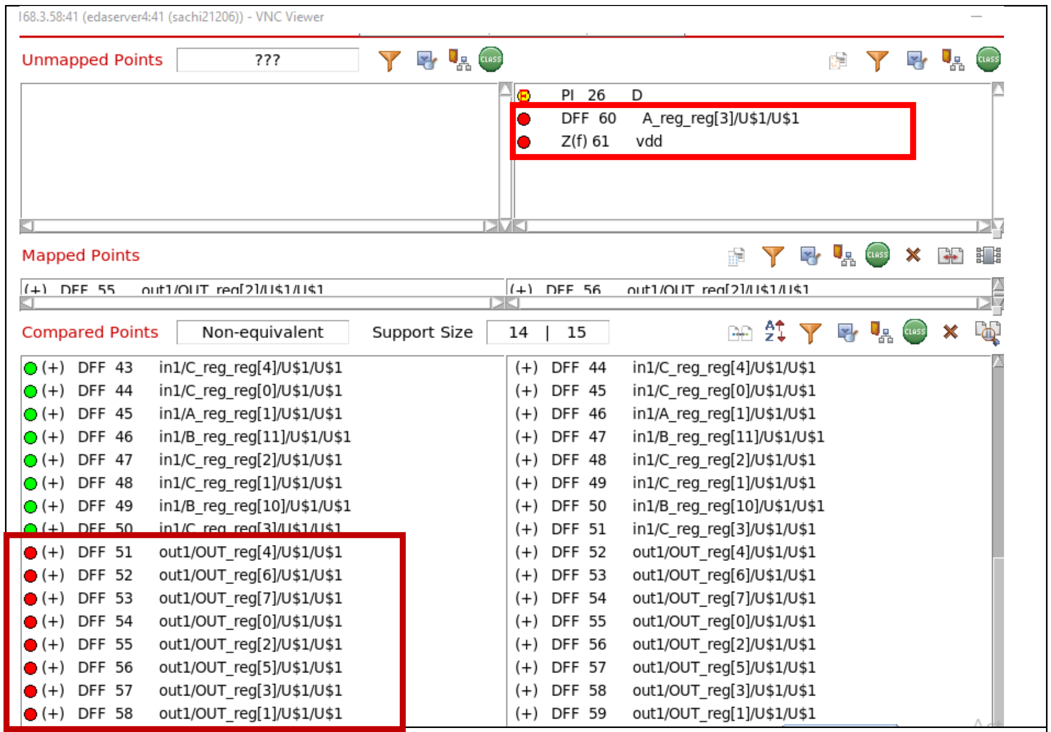
(a) Revised Netlist



```
FF_out out1(clk, rst, OUT_reg, OUT);
OAI211X1 g1363(.A0 (n_1), .A1 (n_0), .B0 (n_34), .C0 (n_18), .Y
     (OUT_reg[3]));
NAND2XL g1364(.A (n_32), .B (n_12), .Y (n_34));
INVXL g1365(.A (n_33), .Y (OUT_reg[2]));
AOI222XL g1366(.A0 (n_28), .A1 (n_12), .B0 (A_reg[1]), .B1 (n_25),
     .C0 (OUT1[2]), .C1 (n_13), .Y (n_33));
```

(b) Golden Netlist

- ❖ The mapping manager shows that:
  - The extra flipflop highlighted in revised netlist (***DFF \A_reg_reg[3]***) and ***wire vdd*** remains unmapped.
  - As the output of this unmapped ff has been connected to other nets therefore, some output ports have also become non-equivalent.
  - Due to above changes other FFs from OUT_reg[0] to OUT_reg[7] have also become nonequivalent.



```
168.3.58:41 (edaserver4:41 (sachi21206)) - VNC Viewer

Unmapped Points   ???

    PI   26    D
●   DFF  60    A_reg_reg[3]/U$1/U$1
●   Z(f) 61    vdd

Mapped Points
(+)  DFF  55    out1/OUT_reg[2]/U$1/U$1        (+)  DFF  56    out1/OUT_reg[2]/U$1/U$1

Compared Points   Non-equivalent   Support Size   14  |  15

● (+)  DFF  43   in1/C_reg_reg[4]/U$1/U$1       (+)  DFF  44   in1/C_reg_reg[4]/U$1/U$1
● (+)  DFF  44   in1/C_reg_reg[0]/U$1/U$1       (+)  DFF  45   in1/C_reg_reg[0]/U$1/U$1
● (+)  DFF  45   in1/A_reg_reg[1]/U$1/U$1       (+)  DFF  46   in1/A_reg_reg[1]/U$1/U$1
● (+)  DFF  46   in1/B_reg_reg[11]/U$1/U$1      (+)  DFF  47   in1/B_reg_reg[11]/U$1/U$1
● (+)  DFF  47   in1/C_reg_reg[2]/U$1/U$1       (+)  DFF  48   in1/C_reg_reg[2]/U$1/U$1
● (+)  DFF  48   in1/C_reg_reg[1]/U$1/U$1       (+)  DFF  49   in1/C_reg_reg[1]/U$1/U$1
● (+)  DFF  49   in1/B_reg_reg[10]/U$1/U$1      (+)  DFF  50   in1/B_reg_reg[10]/U$1/U$1
● (+)  DFF  50   in1/C_reg_reg[3]/U$1/U$1       (+)  DFF  51   in1/C_reg_reg[3]/U$1/U$1
● (+)  DFF  51   out1/OUT_reg[4]/U$1/U$1        (+)  DFF  52   out1/OUT_reg[4]/U$1/U$1
● (+)  DFF  52   out1/OUT_reg[6]/U$1/U$1        (+)  DFF  53   out1/OUT_reg[6]/U$1/U$1
● (+)  DFF  53   out1/OUT_reg[7]/U$1/U$1        (+)  DFF  54   out1/OUT_reg[7]/U$1/U$1
● (+)  DFF  54   out1/OUT_reg[0]/U$1/U$1        (+)  DFF  55   out1/OUT_reg[0]/U$1/U$1
● (+)  DFF  55   out1/OUT_reg[2]/U$1/U$1        (+)  DFF  56   out1/OUT_reg[2]/U$1/U$1
● (+)  DFF  56   out1/OUT_reg[5]/U$1/U$1        (+)  DFF  57   out1/OUT_reg[5]/U$1/U$1
● (+)  DFF  57   out1/OUT_reg[3]/U$1/U$1        (+)  DFF  58   out1/OUT_reg[3]/U$1/U$1
● (+)  DFF  58   out1/OUT_reg[1]/U$1/U$1        (+)  DFF  59   out1/OUT_reg[1]/U$1/U$1
```

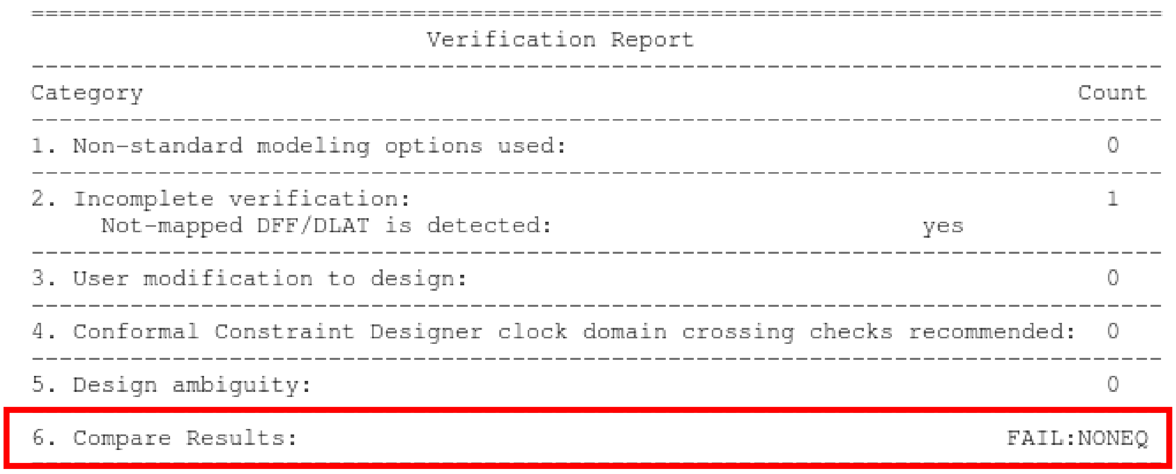
Mapping Manager

```
// Mapping key points ...
// Warning: Primary input 'D' in Revised has no correspondence in Golden
```

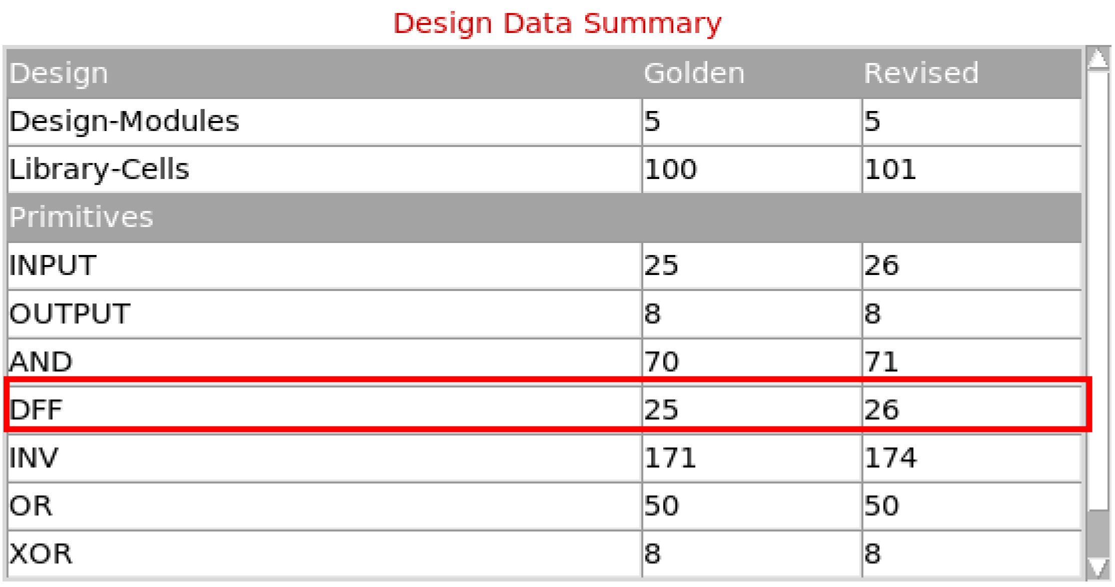
```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points     PI      PO      DFF       Total
--------------------------------------------------------------------------------
Golden            25      8       25        58
--------------------------------------------------------------------------------
Revised           25      8       25        58
================================================================================
Unmapped points:
================================================================================
Revised:
--------------------------------------------------------------------------------
Unmapped points   PI      DFF     Z         Total
--------------------------------------------------------------------------------
Extra             1       0       0         1
Not-mapped        0       1       1         2
================================================================================
// Warning: Key point mapping is incomplete
```

```
// Command: compare
================================================================================
Compared points       PO      DFF       Total
--------------------------------------------------------------------------------
Equivalent            8       17        25
--------------------------------------------------------------------------------
Non-equivalent        0       8         8
================================================================================
```

The image shown below shows that the two netlists are non-equivalent because of the above changes.



```
==============================================================================
                          Verification Report
------------------------------------------------------------------------------
Category                                                                 Count
------------------------------------------------------------------------------
1. Non-standard modeling options used:                                     0
------------------------------------------------------------------------------
2. Incomplete verification:                                                1
     Not-mapped DFF/DLAT is detected:                          yes
------------------------------------------------------------------------------
3. User modification to design:                                            0
------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended: 0
------------------------------------------------------------------------------
5. Design ambiguity:                                                       0
------------------------------------------------------------------------------
6. Compare Results:                                                FAIL:NONEQ
```



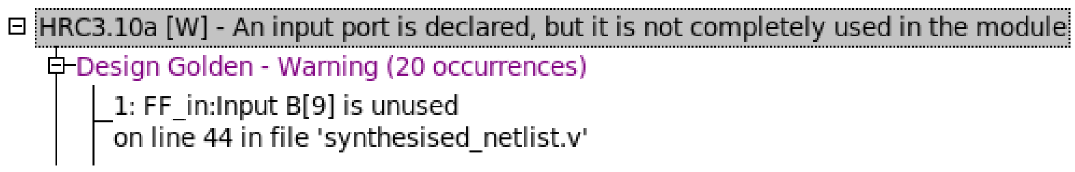
Design Data Summary

Design	Golden	Revised
Design-Modules	5	5
Library-Cells	100	101
Primitives		
INPUT	25	26
OUTPUT	8	8
AND	70	71
DFF	25	26
INV	171	174
OR	50	50
XOR	8	8

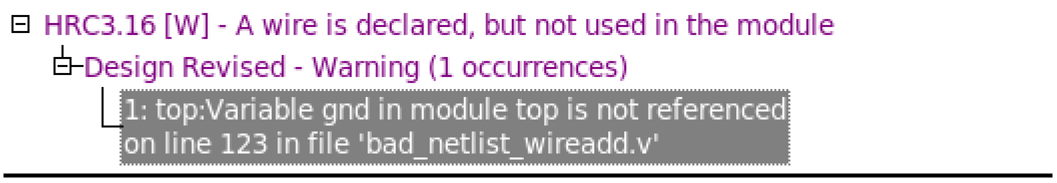
- From the above design data summary, we can observe that because of the changes we made in revised netlist the number of circuit components have changed.

- For example- As we added an extra FF in revised netlist so the number of DFFs has changed from 25 (in golden netlist) to 26 in revised netlist.

--ERROR MESSAGES---------------------------------



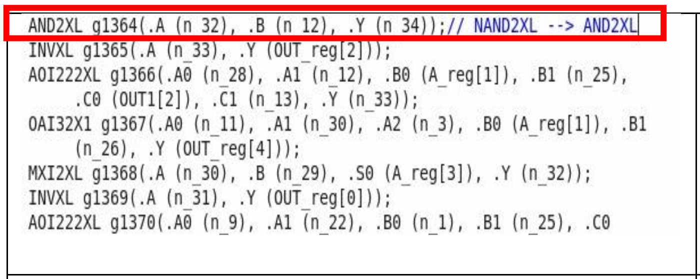
```
⊟ HRC3.10a [W] - An input port is declared, but it is not completely used in the module
   ⊟ Design Golden - Warning (20 occurrences)
        1: FF_in:Input B[9] is unused
        on line 44 in file 'synthesised_netlist.v'
```



```
HRC3.16 [W] - A wire is declared, but not used in the module
  Design Revised - Warning (1 occurrences)
    1: top:Variable gnd in module top is not referenced
    on line 123 in file 'bad_netlist_wireadd.v'
```

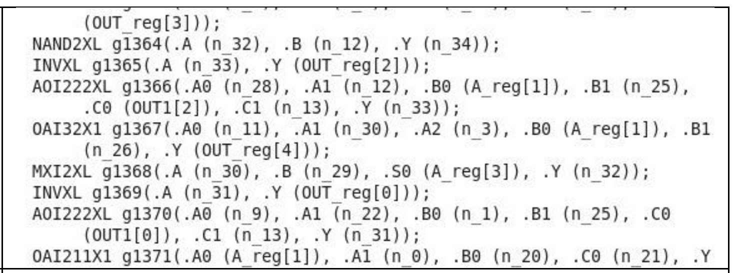
5.2.2 Netlist with cell changed: -

- Here, the NAND cell (NAND2XL) in golden netlist has been changed to AND cell (AND2XL) in revised netlist.
- the XNOR cell (XNOR2X1) in golden netlist has been changed to XOR cell (XOR2X1) in revised netlist.
- Due to the above changes the compared 2 netlists have become inequivalent.



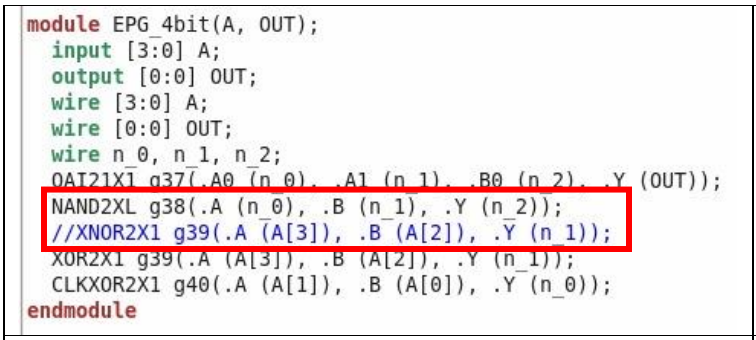
```
AND2XL g1364(.A (n_32), .B (n_12), .Y (n_34));// NAND2XL --> AND2XL
INVXL g1365(.A (n_33), .Y (OUT_reg[2]));
AOI222XL g1366(.A0 (n_28), .A1 (n_12), .B0 (A_reg[1]), .B1 (n_25),
     .C0 (OUT1[2]), .C1 (n_13), .Y (n_33));
OAI32X1 g1367(.A0 (n_11), .A1 (n_30), .A2 (n_3), .B0 (A_reg[1]), .B1
     (n_26), .Y (OUT_reg[4]));
MXI2XL g1368(.A (n_30), .B (n_29), .S0 (A_reg[3]), .Y (n_32));
INVXL g1369(.A (n_31), .Y (OUT_reg[0]));
AOI222XL g1370(.A0 (n_9), .A1 (n_22), .B0 (n_1), .B1 (n_25), .C0
```

(a) Revised Netlist



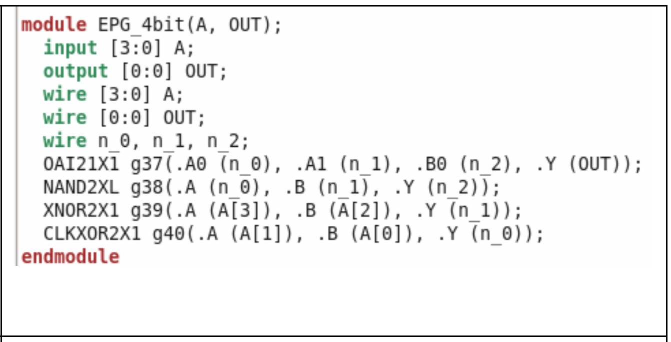
```
     (OUT_reg[3]));
NAND2XL g1364(.A (n_32), .B (n_12), .Y (n_34));
INVXL g1365(.A (n_33), .Y (OUT_reg[2]));
AOI222XL g1366(.A0 (n_28), .A1 (n_12), .B0 (A_reg[1]), .B1 (n_25),
     .C0 (OUT1[2]), .C1 (n_13), .Y (n_33));
OAI32X1 g1367(.A0 (n_11), .A1 (n_30), .A2 (n_3), .B0 (A_reg[1]), .B1
     (n_26), .Y (OUT_reg[4]));
MXI2XL g1368(.A (n_30), .B (n_29), .S0 (A_reg[3]), .Y (n_32));
INVXL g1369(.A (n_31), .Y (OUT_reg[0]));
AOI222XL g1370(.A0 (n_9), .A1 (n_22), .B0 (n_1), .B1 (n_25), .C0
     (OUT1[0]), .C1 (n_13), .Y (n_31));
OAI211X1 g1371(.A0 (A_reg[1]), .A1 (n_0), .B0 (n_20), .C0 (n_21), .Y
```

(b) Golden Netlist



```
module EPG_4bit(A, OUT);
  input [3:0] A;
  output [0:0] OUT;
  wire [3:0] A;
  wire [0:0] OUT;
  wire n_0, n_1, n_2;
  OAI21X1 g37(.A0 (n_0), .A1 (n_1), .B0 (n_2), .Y (OUT));
  NAND2XL g38(.A (n_0), .B (n_1), .Y (n_2));
  //XNOR2X1 g39(.A (A[3]), .B (A[2]), .Y (n_1));
  XOR2X1 g39(.A (A[3]), .B (A[2]), .Y (n_1));
  CLKXOR2X1 g40(.A (A[1]), .B (A[0]), .Y (n_0));
endmodule
```

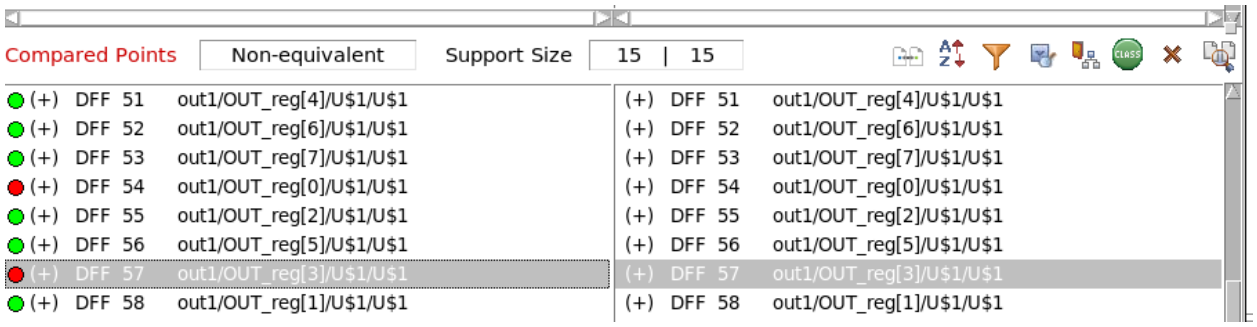
(a) Revised Netlist



```
module EPG_4bit(A, OUT);
  input [3:0] A;
  output [0:0] OUT;
  wire [3:0] A;
  wire [0:0] OUT;
  wire n_0, n_1, n_2;
  OAI21X1 g37(.A0 (n_0), .A1 (n_1), .B0 (n_2), .Y (OUT));
  NAND2XL g38(.A (n_0), .B (n_1), .Y (n_2));
  XNOR2X1 g39(.A (A[3]), .B (A[2]), .Y (n_1));
  CLKXOR2X1 g40(.A (A[1]), .B (A[0]), .Y (n_0));
endmodule
```

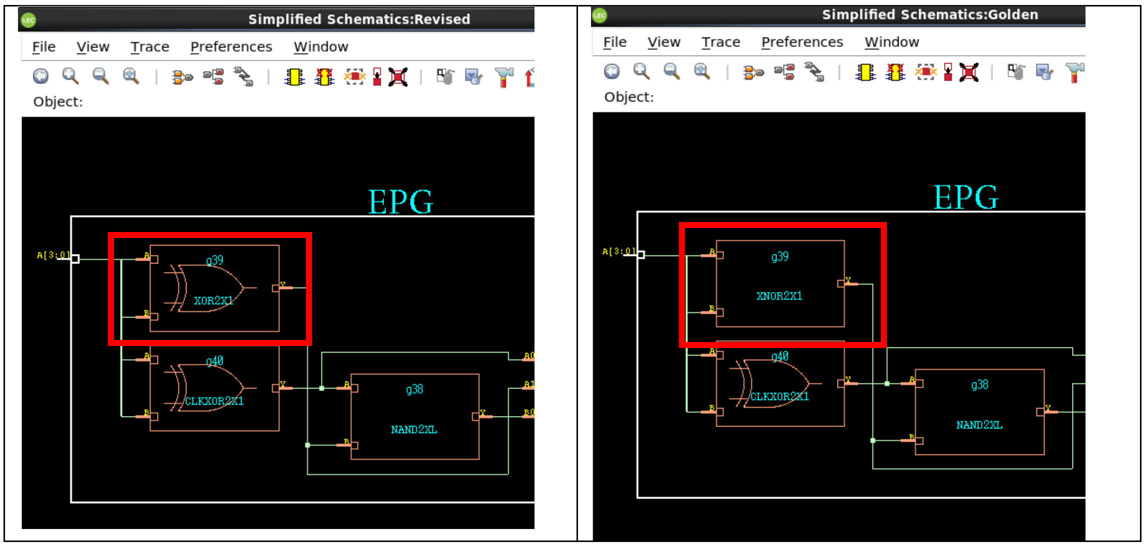
(b) Golden Netlist

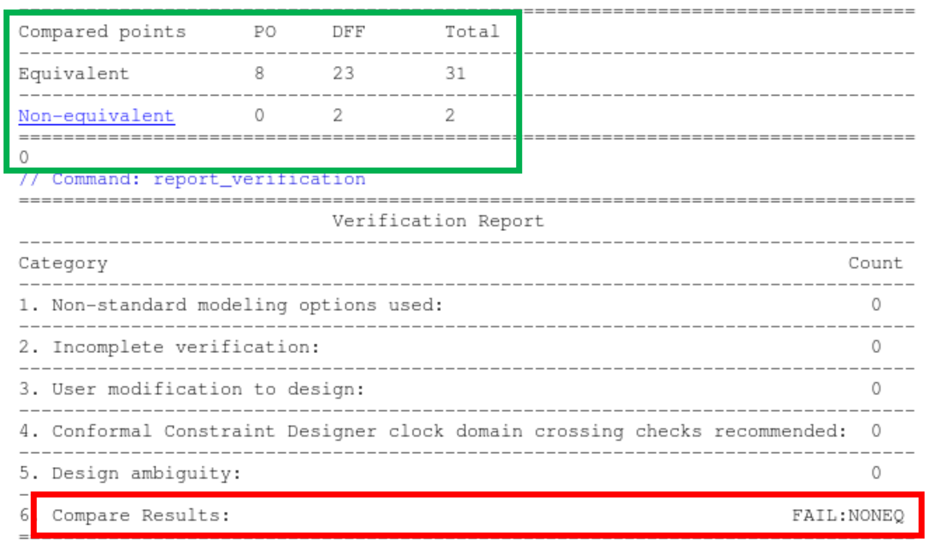
❖ The mapping manager clearly shows that there are 2 unmapped points generated due to above changes in the netlist which changes the entire functionality.



```
● (+)  DFF 51   out1/OUT_reg[4]/U$1/U$1     (+)  DFF 51   out1/OUT_reg[4]/U$1/U$1
● (+)  DFF 52   out1/OUT_reg[6]/U$1/U$1     (+)  DFF 52   out1/OUT_reg[6]/U$1/U$1
● (+)  DFF 53   out1/OUT_reg[7]/U$1/U$1     (+)  DFF 53   out1/OUT_reg[7]/U$1/U$1
● (+)  DFF 54   out1/OUT_reg[0]/U$1/U$1     (+)  DFF 54   out1/OUT_reg[0]/U$1/U$1
● (+)  DFF 55   out1/OUT_reg[2]/U$1/U$1     (+)  DFF 55   out1/OUT_reg[2]/U$1/U$1
● (+)  DFF 56   out1/OUT_reg[5]/U$1/U$1     (+)  DFF 56   out1/OUT_reg[5]/U$1/U$1
● (+)  DFF 57   out1/OUT_reg[3]/U$1/U$1     (+)  DFF 57   out1/OUT_reg[3]/U$1/U$1
● (+)  DFF 58   out1/OUT_reg[1]/U$1/U$1     (+)  DFF 58   out1/OUT_reg[1]/U$1/U$1
```

❖ The schematics shown in below image shows the non-equivalent point in golden and revised netlists.


Simplified Schematics:Revised
File View Trace Preferences Window
Object:
EPG
A[3:0]
g39
XOR2X1
g40
CLKXOR2X1
g38
NAND2XL
Simplified Schematics:Golden
File View Trace Preferences Window
Object:
EPG
A[3:0]
g39
XNOR2X1
g40
CLKXOR2X1
g38
NAND2XL



```
==============================================================================
Compared points      PO      DFF      Total
------------------------------------------------------------------------------
Equivalent           8       23       31
------------------------------------------------------------------------------
Non-equivalent       0       2        2
==============================================================================
0
// Command: report_verification
==============================================================================
                          Verification Report
------------------------------------------------------------------------------
Category                                                              Count
------------------------------------------------------------------------------
1. Non-standard modeling options used:                                  0
------------------------------------------------------------------------------
2. Incomplete verification:                                             0
------------------------------------------------------------------------------
3. User modification to design:                                         0
------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
------------------------------------------------------------------------------
5. Design ambiguity:                                                    0
------------------------------------------------------------------------------
6. Compare Results:                                             FAIL:NONEQ
==============================================================================
```

The image shown above shows that the two netlists are non-equivalent because of the above changes in cells.

5.2.3 Netlist with Extra Input

❖ An extra input port ***D*** has been added to the top module and connected it as the input of an inverter ***INVXL*** with input being B [5].

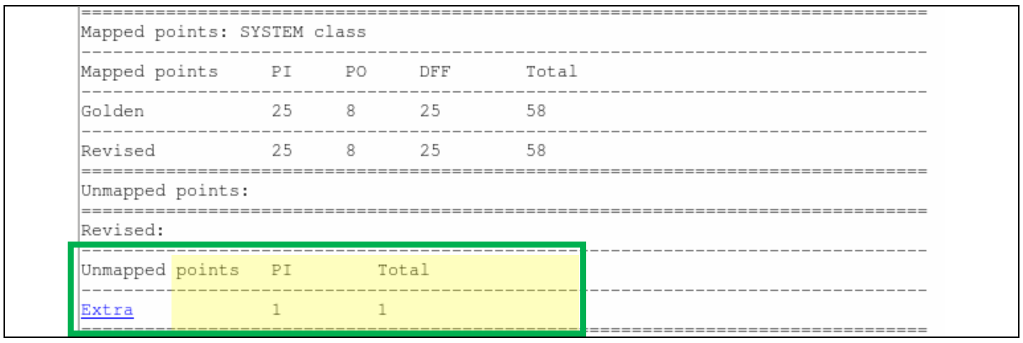
```
module top(clk, rst, A, B, C, D, OUT);
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;

  input D;//Input Port added
  INVXL instance1(.A(D),.Y(OUT[0]));
//Connected the input port D to the
//one of the output port through inverter
```

(c) Revised Netlist

```
module top(clk, rst, A, B, C, OUT);
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
```

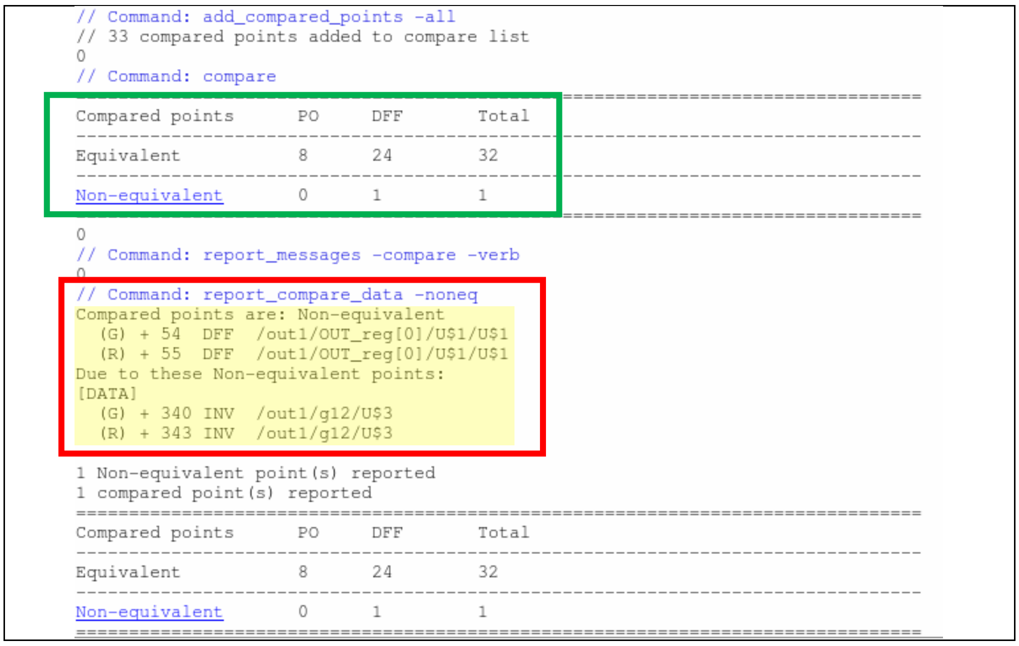
(d) Golden Netlist

Results:



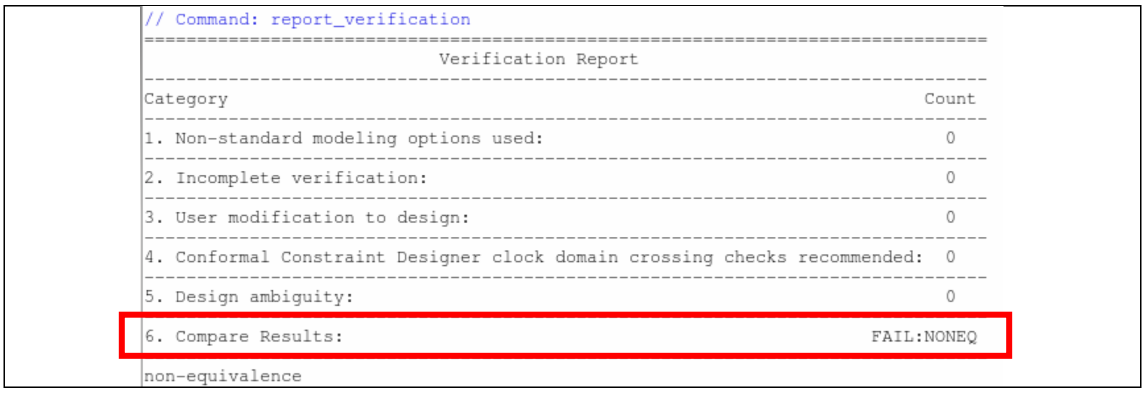
```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points       PI      PO      DFF        Total
--------------------------------------------------------------------------------
Golden              25      8       25         58
--------------------------------------------------------------------------------
Revised             25      8       25         58
================================================================================
Unmapped points:
================================================================================
Revised:
--------------------------------------------------------------------------------
Unmapped points     PI          Total
--------------------------------------------------------------------------------
Extra               1           1
================================================================================
```

- Here there is one unmapped point as there is inclusion of the extra input port in the revised netlist.



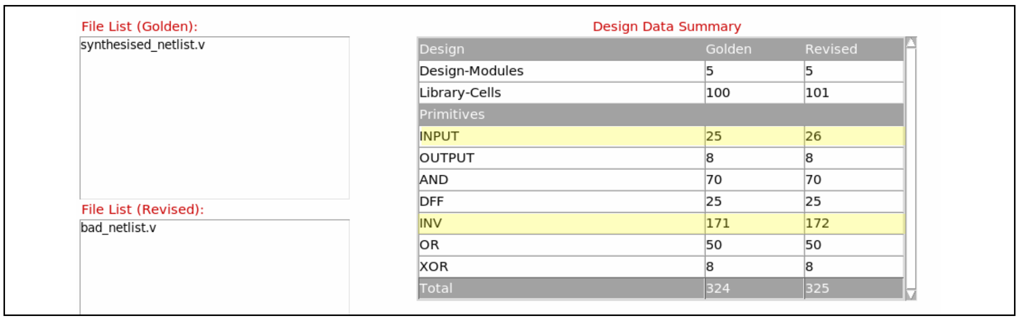
```
// Command: add_compared_points -all
// 33 compared points added to compare list
0
// Command: compare
================================================================================
Compared points      PO      DFF        Total
--------------------------------------------------------------------------------
Equivalent           8       24         32
--------------------------------------------------------------------------------
Non-equivalent       0       1          1
================================================================================
0
// Command: report_messages -compare -verb
0
// Command: report_compare_data -noneq
Compared points are: Non-equivalent
  (G) + 54   DFF   /out1/OUT_reg[0]/U$1/U$1
  (R) + 55   DFF   /out1/OUT_reg[0]/U$1/U$1
Due to these Non-equivalent points:
[DATA]
  (G) + 340 INV   /out1/g12/U$3
  (R) + 343 INV   /out1/g12/U$3

1 Non-equivalent point(s) reported
1 compared point(s) reported
================================================================================
Compared points      PO      DFF        Total
--------------------------------------------------------------------------------
Equivalent           8       24         32
--------------------------------------------------------------------------------
Non-equivalent       0       1          1
================================================================================
```

- 24 DFF are found to be equivalent and, one DFF has found to be nonequivalent with the golden netlist.



```
// Command: report_verification
===============================================================================
                          Verification Report
-------------------------------------------------------------------------------
Category                                                                  Count
-------------------------------------------------------------------------------
1. Non-standard modeling options used:                                      0
-------------------------------------------------------------------------------
2. Incomplete verification:                                                 0
-------------------------------------------------------------------------------
3. User modification to design:                                             0
-------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:  0
-------------------------------------------------------------------------------
5. Design ambiguity:                                                        0
-------------------------------------------------------------------------------
6. Compare Results:                                                FAIL:NONEQ
-------------------------------------------------------------------------------
non-equivalence
```

- The image shown above shows that the two netlists are non-equivalent because of the above changes in cells.



File List (Golden):
synthesised_netlist.v

File List (Revised):
bad_netlist.v

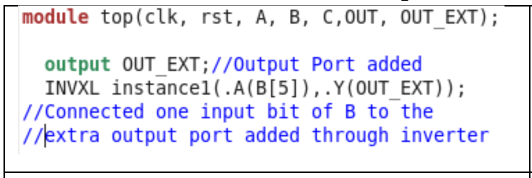
Design Data Summary

Design	Golden	Revised
Design-Modules	5	5
Library-Cells	100	101
Primitives		
INPUT	25	26
OUTPUT	8	8
AND	70	70
DFF	25	25
INV	171	172
OR	50	50
XOR	8	8
Total	324	325

- From the design data summary, it can be seen that the input port INPUT and the number of inverters INV has been added in the revised netlist.
- This information explains that the ports and the cells used in the two netlists aren’t logically equal.

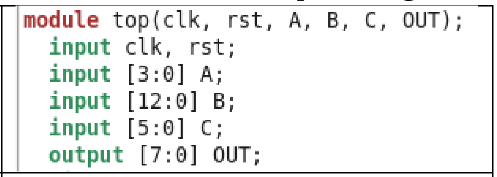
5.2.4 NETLIST with extra output port

- An extra output port ***OUT_EXT*** has been added to the top module and connected it as the output of an inverter ***INVXL*** with input being B [5].



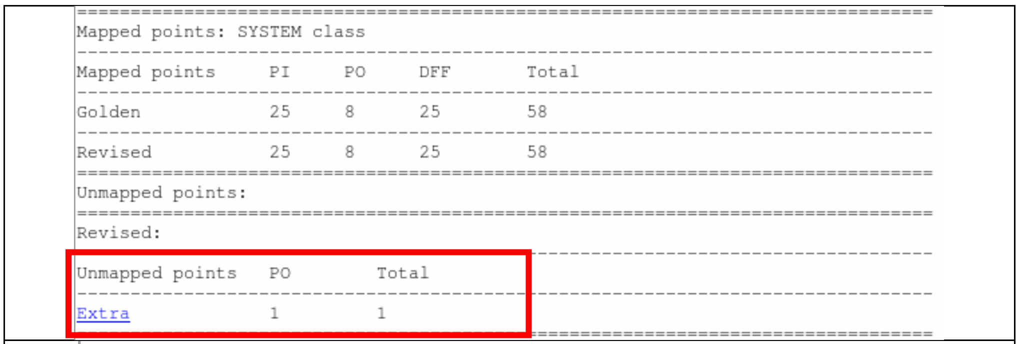
```
module top(clk, rst, A, B, C,OUT, OUT_EXT);

  output OUT_EXT;//Output Port added
  INVXL instance1(.A(B[5]),.Y(OUT_EXT));
//Connected one input bit of B to the
//extra output port added through inverter
```

(a) Revised Netlist

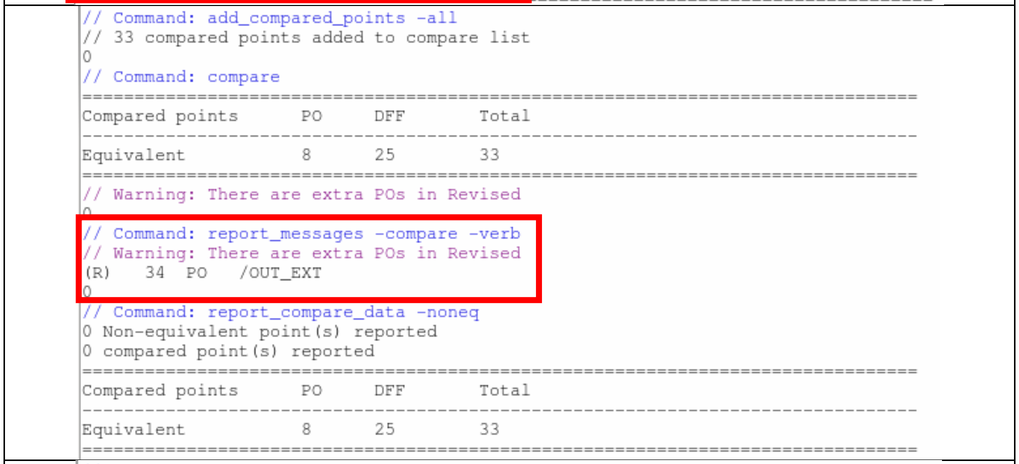


```
module top(clk, rst, A, B, C, OUT);
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
```

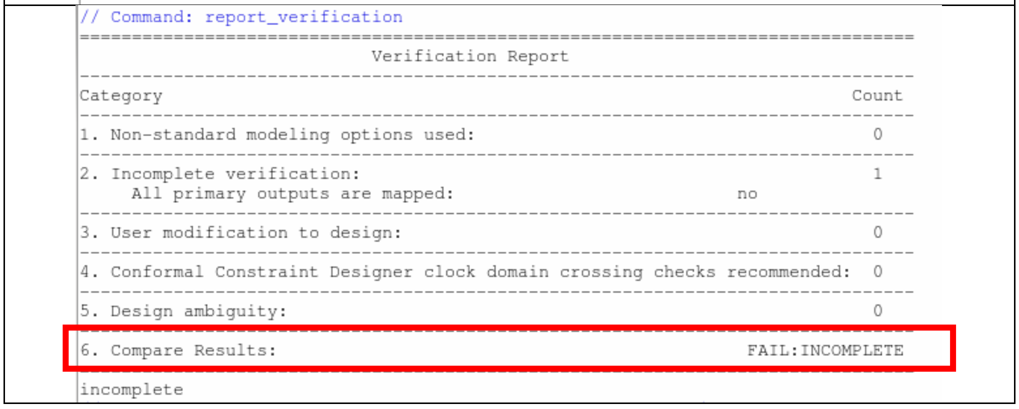
(b) Golden Netlist



```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points      PI      PO      DFF        Total
--------------------------------------------------------------------------------
Golden             25      8       25         58
--------------------------------------------------------------------------------
Revised            25      8       25         58
================================================================================
Unmapped points:
================================================================================
Revised:
--------------------------------------------------------------------------------
Unmapped points    PO         Total
--------------------------------------------------------------------------------
Extra              1          1
================================================================================
```

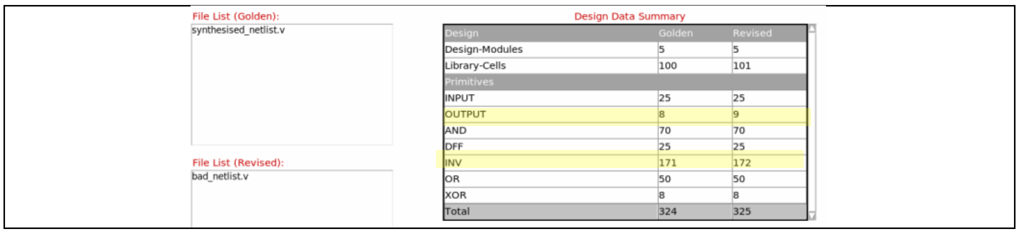


```
// Command: add_compared_points -all
// 33 compared points added to compare list
0
// Command: compare
================================================================================
Compared points      PO      DFF        Total
--------------------------------------------------------------------------------
Equivalent           8       25         33
================================================================================
// Warning: There are extra POs in Revised
0
// Command: report_messages -compare -verb
// Warning: There are extra POs in Revised
(R)    34   PO    /OUT_EXT
0
// Command: report_compare_data -noneq
0 Non-equivalent point(s) reported
0 compared point(s) reported
================================================================================
Compared points      PO      DFF        Total
--------------------------------------------------------------------------------
Equivalent           8       25         33
================================================================================
```



```
// Command: report_verification
================================================================================
                            Verification Report
--------------------------------------------------------------------------------
Category                                                                   Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                       0
--------------------------------------------------------------------------------
2. Incomplete verification:                                                  1
     All primary outputs are mapped:                            no
--------------------------------------------------------------------------------
3. User modification to design:                                              0
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:   0
--------------------------------------------------------------------------------
5. Design ambiguity:                                                         0
--------------------------------------------------------------------------------
6. Compare Results:                                              FAIL:INCOMPLETE
================================================================================
incomplete
```

- Here there is one unmapped point as there is inclusion of the extra output port PO in the revised netlist.
- There is a warning message as highlighted above, which indicates that there has been an extra output port has been added.



File List (Golden):
synthesised_netlist.v

File List (Revised):
bad_netlist.v

Design Data Summary

Design	Golden	Revised
Design-Modules	5	5
Library-Cells	100	101
Primitives		
INPUT	25	25
OUTPUT	8	9
AND	70	70
DFF	25	25
INV	171	172
OR	50	50
XOR	8	8
Total	324	325

- From the design data summary, it can be seen that the output ports OUTPUT and the number of inverters INV has been added in the revised netlist.
- This information explains that the ports and the cells used in the two netlists aren’t equal.

STATIC TIMING ANALYSIS (STA)

Tool Used: Tempus

Command Used to run the tool:

```
tempus -nowin
source script.tcl
```

Script:

```
file mkdir reports
read_lib slow.lib
read_verilog synthesised_netlist.v
set_top_module top
read_sdc constraints_btw.sdc
check_timing > reports/check_timing.rpt
report_timing > reports/timing_report.rpt
report_analysis_coverage > reports/analysis_coverage.rpt
report_analysis_summary > reports/analysis_summary.rpt
#report_annotated_parasitics > $report_dir/annotated.rpt
report_clocks > reports/clocks.rpt
report_case_analysis > reports/case_analysis.rpt
report_constraints -all_violators > reports/allviolations.rpt
```

SDC

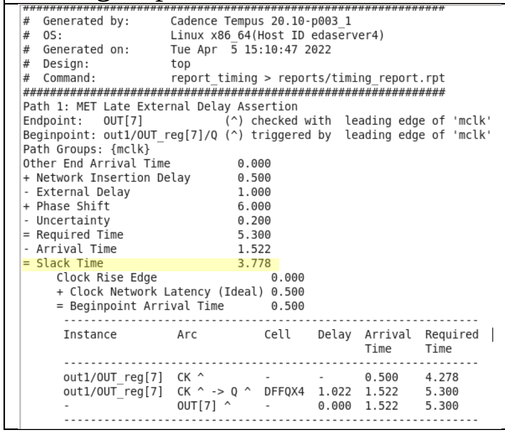
```
create_clock -name mclk -period 6 [get_ports clk]

set_clock_transition -rise 0.05 [get_clocks mclk]
set_clock_transition -fall 0.05 [get_clocks mclk]
set_clock_uncertainty 0.2 [get_clocks mclk]
set_clock_latency 0.5 [get_clocks mclk]

set_input_delay -clock [get_clocks mclk] 1 [get_ports A]
set_input_delay -clock [get_clocks mclk] 1 [get_ports B]
set_input_delay -clock [get_clocks mclk] 1 [get_ports C]
set_input_delay -clock [get_clocks mclk] 1 [get_ports rst]

set_input_transition 0.01 [get_ports A]
set_input_transition 0.01 [get_ports B]
set_input_transition 0.01 [get_ports C]
set_input_transition 0.01 [get_ports rst]

set_output_delay -clock [get_clocks mclk] 1 [get_ports OUT]

set_load 0.5 [get_ports OUT]
```

- ✓ Constraint file same as 3(c) is used for all three synthesised netlists for performing STA analysis.

6.1 Without Wire Load Model

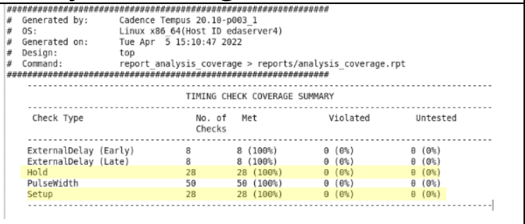
6.1.1 Minimum Area

Timing Report



```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:10:47 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
################################################################
Path 1: MET Late External Delay Assertion
Endpoint:   OUT[7]            (^) checked with  leading edge of 'mclk'
Beginpoint: out1/OUT_reg[7]/Q (^) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.000
+ Network Insertion Delay       0.500
- External Delay                1.000
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.300
- Arrival Time                  1.522
= Slack Time                    3.778
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      -------------------------------------------------------------
      Instance         Arc           Cell     Delay  Arrival  Required |
                                                     Time     Time
      -------------------------------------------------------------
      out1/OUT_reg[7]  CK ^          -        -      0.500    4.278
      out1/OUT_reg[7]  CK ^ -> Q ^   DFFQX4   1.022  1.522    5.300
      -                OUT[7] ^      -        0.000  1.522    5.300
      -------------------------------------------------------------
```

Analysis Coverage



```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:10:47 2022
#  Design:            top
#  Command:           report_analysis_coverage > reports/analysis_coverage.rpt
################################################################
    ------------------------------------------------------------------------------
                          TIMING CHECK COVERAGE SUMMARY
    ------------------------------------------------------------------------------
     Check Type                 No. of   Met          Violated      Untested
                                Checks
    ------------------------------------------------------------------------------
    ExternalDelay (Early)      8        8 (100%)     0 (0%)        0 (0%)
    ExternalDelay (Late)       8        8 (100%)     0 (0%)        0 (0%)
    Hold                       28       28 (100%)    0 (0%)        0 (0%)
    PulseWidth                 50       50 (100%)    0 (0%)        0 (0%)
    Setup                      28       28 (100%)    0 (0%)        0 (0%)
    ------------------------------------------------------------------------------|
```

- The slack obtained is 3.778. The slack got reduced from the reporting of timing report in the synthesis part because now the time period of the constraint file used in 3(c) has reduced to 6ns.

- The critical path from the STA analysis by the tool is from out1/OUT_reg[7]/Q to OUT[7].

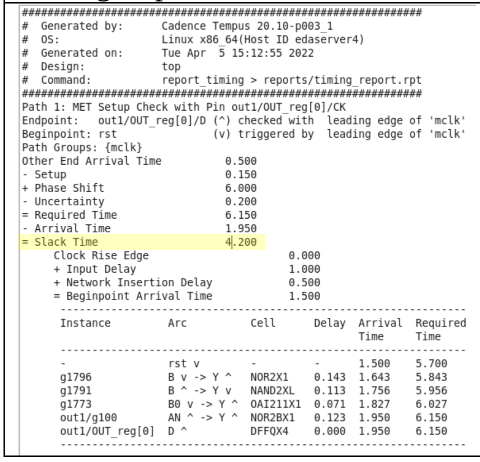
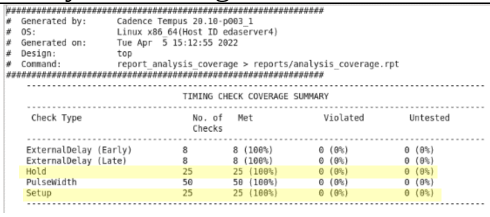
- Arrival Time (AT) is given by the time at which a signal that is generated at a given vertex would settle. The clock latency is 0.5 and the clock to q delay for 1.022. The Ck -- > Q delay is determined from the lookup table of the DFFQX4 cell in library, the value is computed by interpolating values accordingly of input slew and output load. The arrival time is then computed as (0.5+1.022) 1.522.

- Required Time (RT) is time by which a signal that is generated at a given vertex should settle to avoid setup/hold violation. Here the clock latency is 0.5 and external delay added for meeting timing constraint of next external FF is 1, the time period is 6, uncertainty modelled before the physical routing is 0.2. Then the RT is calculated (6+0.5-0.2-1) as 5.3.

- Setup slack is given by RT-AT as (5.3-1.522) 3.778.

- No Setup or hold violations are reported

6.1.2 Best Timing

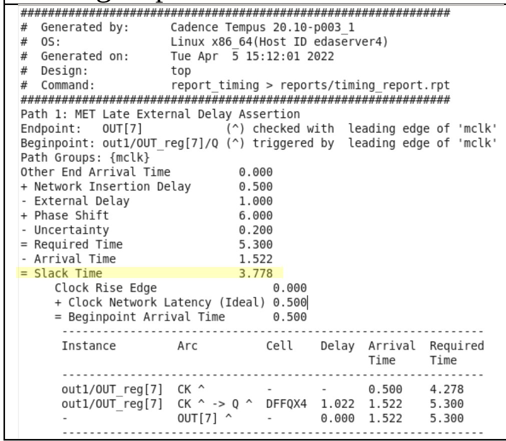
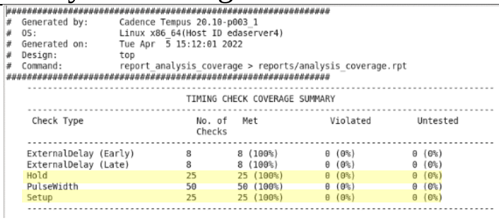
Timing Report	Analysis Coverage
	

```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:12:55 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.150
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.150
- Arrival Time                  1.950
= Slack Time                    4.200
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     + Network Insertion Delay            0.500
     = Beginpoint Arrival Time            1.500
      ---------------------------------------------------------------
      Instance         Arc          Cell      Delay  Arrival  Required
                                                     Time     Time
      ---------------------------------------------------------------
      -                rst v        -         -      1.500    5.700
      g1796            B v -> Y ^   NOR2X1    0.143  1.643    5.843
      g1791            B ^ -> Y v   NAND2XL   0.113  1.756    5.956
      g1773            B0 v -> Y ^  OAI211X1  0.071  1.827    6.027
      out1/g100        AN ^ -> Y ^  NOR2BX1   0.123  1.950    6.150
      out1/OUT_reg[0]  D ^          DFFQX4    0.000  1.950    6.150
      ---------------------------------------------------------------
```

```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:12:55 2022
#  Design:            top
#  Command:           report_analysis_coverage > reports/analysis_coverage.rpt
################################################################
    ------------------------------------------------------------------------------
                              TIMING CHECK COVERAGE SUMMARY
    ------------------------------------------------------------------------------
     Check Type                   No. of   Met            Violated       Untested
                                  Checks
    ------------------------------------------------------------------------------
    ExternalDelay (Early)        8        8 (100%)       0 (0%)         0 (0%)
    ExternalDelay (Late)         8        8 (100%)       0 (0%)         0 (0%)
    Hold                         25       25 (100%)      0 (0%)         0 (0%)
    PulseWidth                   50       50 (100%)      0 (0%)         0 (0%)
    Setup                        25       25 (100%)      0 (0%)         0 (0%)
    ------------------------------------------------------------------------------
```

- The critical path from the STA analysis by the tool is from rst to out1/OUT_reg[0]/D.
- The slack obtained is 4.2. This increase in slack is observed because of the increase in time period used in the constraint file 3(c).
- No Setup or hold violations are reported

6.1.3 Intermediate Slack

Timing Report	Analysis Coverage
	

```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:12:01 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
################################################################
Path 1: MET Late External Delay Assertion
Endpoint:   OUT[7]            (^) checked with  leading edge of 'mclk'
Beginpoint: out1/OUT_reg[7]/Q (^) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.000
+ Network Insertion Delay       0.500
- External Delay                1.000
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.300
- Arrival Time                  1.522
= Slack Time                    3.778
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      ---------------------------------------------------------------
      Instance         Arc          Cell      Delay  Arrival  Required
                                                     Time     Time
      ---------------------------------------------------------------
      out1/OUT_reg[7]  CK ^         -         -      0.500    4.278
      out1/OUT_reg[7]  CK ^ -> Q ^  DFFQX4    1.022  1.522    5.300
      -                OUT[7] ^     -         0.000  1.522    5.300
      ---------------------------------------------------------------
```

```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:12:01 2022
#  Design:            top
#  Command:           report_analysis_coverage > reports/analysis_coverage.rpt
################################################################
    ------------------------------------------------------------------------------
                              TIMING CHECK COVERAGE SUMMARY
    ------------------------------------------------------------------------------
     Check Type                   No. of   Met            Violated       Untested
                                  Checks
    ------------------------------------------------------------------------------
    ExternalDelay (Early)        8        8 (100%)       0 (0%)         0 (0%)
    ExternalDelay (Late)         8        8 (100%)       0 (0%)         0 (0%)
    Hold                         25       25 (100%)      0 (0%)         0 (0%)
    PulseWidth                   50       50 (100%)      0 (0%)         0 (0%)
    Setup                        25       25 (100%)      0 (0%)         0 (0%)
    ------------------------------------------------------------------------------
```

6.2 With Wire Load Model

Wire Load Model

```
  wire_load("WLM1") {
  resistance :     0.0006 ;
  capacitance :    0.0001 ;
  area:            0.1    ;
  slope  :         1.5    ;
  fanout_length(1, 0.002) ;

  fanout_length(2, 0.006) ;
  fanout_length(3, 0.009) ;
  fanout_length(4, 0.015) ;
  fanout_length(5, 0.020) ;

  fanout_length(7, 0.028) ;
  fanout_length(8, 0.030) ;
  fanout_length(9, 0.035) ;
  fanout_length(10, 0.040) ;
}
```

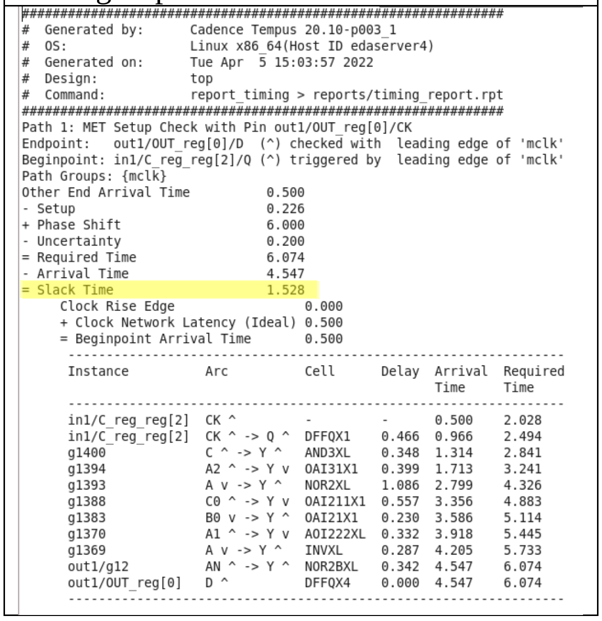
- Wire load model is named as WLM1. It defines the resistance per unit length, capacitance per unit length, slope and length of wire for various fanout from 1 to 10.

SDC:

```
create_clock -name mclk -period 6 [get_ports clk]
set_clock_transition -rise 0.05 [get_clocks mclk]
set_clock_transition -fall 0.05 [get_clocks mclk]
set_clock_uncertainty 0.2 [get_clocks mclk]
set_clock_latency 0.5 [get_clocks mclk]
set_input_delay -clock [get_clocks mclk] 1 [get_ports A]
set_input_delay -clock [get_clocks mclk] 1 [get_ports B]
set_input_delay -clock [get_clocks mclk] 1 [get_ports C]
set_input_delay -clock [get_clocks mclk] 1 [get_ports rst]
set_input_transition 0.01 [get_ports A]
set_input_transition 0.01 [get_ports B]
set_input_transition 0.01 [get_ports C]
set_input_transition 0.01 [get_ports rst]
set_output_delay -clock [get_clocks mclk] 1 [get_ports OUT]
set_load 0.5 [get_ports OUT]
set_wire_load_model -name "WLM"
```

6.2.1 Minimum Area

Timing Report



```
#################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:03:57 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
#################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D  (^) checked with  leading edge of 'mclk'
Beginpoint: in1/C_reg_reg[2]/Q (^) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.226
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.074
- Arrival Time                  4.547
= Slack Time                    1.528
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      ---------------------------------------------------------------
      Instance          Arc          Cell      Delay  Arrival  Required
                                                      Time     Time
      ---------------------------------------------------------------
      in1/C_reg_reg[2]  CK ^         -         -      0.500    2.028
      in1/C_reg_reg[2]  CK ^ -> Q ^  DFFQX1    0.466  0.966    2.494
      g1400             C ^ -> Y ^   AND3XL    0.348  1.314    2.841
      g1394             A2 ^ -> Y v  OAI31X1   0.399  1.713    3.241
      g1393             A v -> Y ^   NOR2XL    1.086  2.799    4.326
      g1388             C0 ^ -> Y v  OAI211X1  0.557  3.356    4.883
      g1383             B0 v -> Y ^  OAI21X1   0.230  3.586    5.114
      g1370             A1 ^ -> Y v  AOI222XL  0.332  3.918    5.445
      g1369             A v -> Y ^   INVXL     0.287  4.205    5.733
      out1/g12          AN ^ -> Y ^  NOR2BXL   0.342  4.547    6.074
      out1/OUT_reg[0]   D ^          DFFQX4    0.000  4.547    6.074
      ---------------------------------------------------------------
```

- After adding Wire Load model into the constraints of STA, the critical path has changed to in1/C_reg[2]/Q to out1/OUT_reg[0]/D.

- The slack obtained in this path is 1.528. The worst-case slack has significantly reduced after adding wire load model.

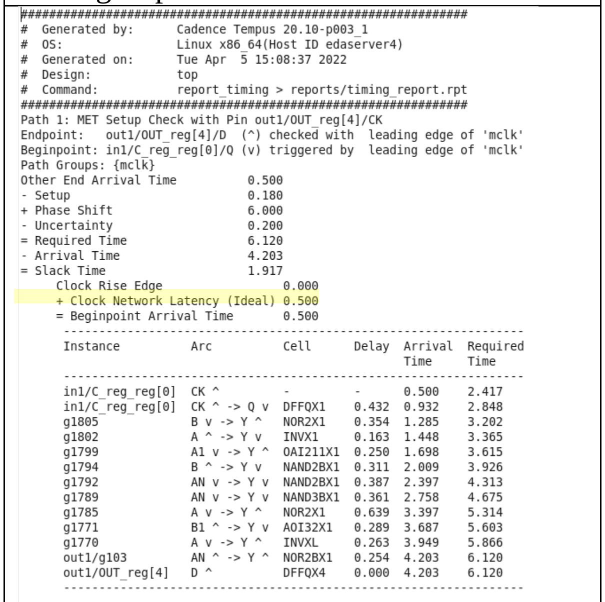
- Arrival time is computed by summation of all delay from CLK of launch FF here in1/C_reg[2] to D pin of capture FF here out1/OUT_reg[0].
  - The input clock has a network latency of 0.5, from the library delays of DFFQX1 is computed for data arriving at Q after the clock edge by 0.466.
  - The combinational delay constitutes of AND3XL gate is 0.348, delay of OAI31X1 gate as 0.399, delay of NOR2XL is 1.086, delay of OAI21X1 is 0.230, delay of AOI222Xl is 0.332, delay of INVXL is 0.287, delay of NOR2BXL is 0.342.
  - Summation of Ck-- > Q delay and combinational delay constitutes to the arrival time (AT) of 4.547.

- Required time is computed by setup time of the capture FF 0.226, time period of 6, uncertainty of 0.2. RT is determined by the Setup time + Time Period - Uncertainty (0.226+0.6-0.2) 6.074.

- Setup Slack time is computed by RT-AT as 1.528.

6.2.2 Best Timing

Timing Report



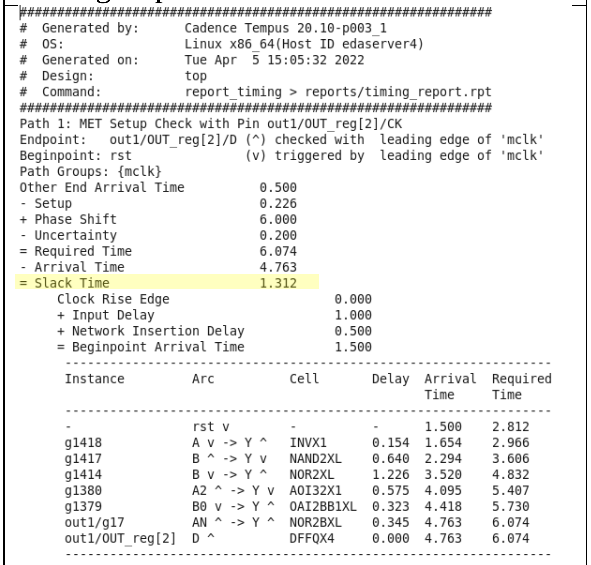
```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:08:37 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[4]/CK
Endpoint:   out1/OUT_reg[4]/D  (^) checked with  leading edge of 'mclk'
Beginpoint: in1/C_reg_reg[0]/Q (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.180
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.120
- Arrival Time                  4.203
= Slack Time                    1.917
     Clock Rise Edge                 0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      -----------------------------------------------------------------
      Instance          Arc          Cell      Delay  Arrival  Required
                                                      Time     Time
      -----------------------------------------------------------------
      in1/C_reg_reg[0]  CK ^         -         -      0.500    2.417
      in1/C_reg_reg[0]  CK ^ -> Q v  DFFQX1    0.432  0.932    2.848
      g1805             B v -> Y ^   NOR2X1    0.354  1.285    3.202
      g1802             A ^ -> Y v   INVX1     0.163  1.448    3.365
      g1799             A1 v -> Y ^  OAI211X1  0.250  1.698    3.615
      g1794             B ^ -> Y v   NAND2BX1  0.311  2.009    3.926
      g1792             AN v -> Y v  NAND2BX1  0.387  2.397    4.313
      g1789             AN v -> Y v  NAND3BX1  0.361  2.758    4.675
      g1785             A v -> Y ^   NOR2X1    0.639  3.397    5.314
      g1771             B1 ^ -> Y v  AOI32X1   0.289  3.687    5.603
      g1770             A v -> Y ^   INVXL     0.263  3.949    5.866
      out1/g103         AN ^ -> Y ^  NOR2BX1   0.254  4.203    6.120
      out1/OUT_reg[4]   D ^          DFFQX4    0.000  4.203    6.120
      -----------------------------------------------------------------
```

- After adding Wire Load model into the constraints of STA, the critical path has changed to in1/C_reg[0]/Q to out1/OUT_reg[4]/D.

- The slack obtained in this path is 1.917. The worst-case slack has significantly reduced after adding wire load model.

6.2.3 Intermediate Slack

Timing Report



```
################################################################
#  Generated by:      Cadence Tempus 20.10-p003_1
#  OS:                Linux x86_64(Host ID edaserver4)
#  Generated on:      Tue Apr  5 15:05:32 2022
#  Design:            top
#  Command:           report_timing > reports/timing_report.rpt
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.226
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.074
- Arrival Time                  4.763
= Slack Time                    1.312
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     + Network Insertion Delay            0.500
     = Beginpoint Arrival Time            1.500
      -----------------------------------------------------------------
      Instance         Arc          Cell       Delay  Arrival  Required
                                                      Time     Time
      -----------------------------------------------------------------
      -                rst v        -          -      1.500    2.812
      g1418            A v -> Y ^   INVX1      0.154  1.654    2.966
      g1417            B ^ -> Y v   NAND2XL    0.640  2.294    3.606
      g1414            B v -> Y ^   NOR2XL     1.226  3.520    4.832
      g1380            A2 ^ -> Y v  AOI32X1    0.575  4.095    5.407
      g1379            B0 v -> Y ^  OAI2BB1XL  0.323  4.418    5.730
      out1/g17         AN ^ -> Y ^  NOR2BXL    0.345  4.763    6.074
      out1/OUT_reg[2]  D ^          DFFQX4     0.000  4.763    6.074
      -----------------------------------------------------------------
```

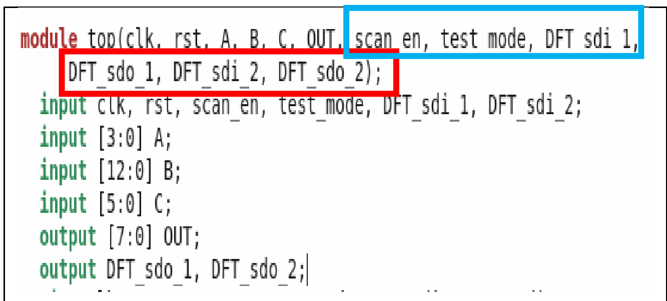
- After adding Wire Load model into the constraints of STA, the critical path has changed to rst to out1/OUT_reg[2]/D.

- The slack obtained in this path is 1.312. The worst-case slack has significantly reduced after adding wire load model.

TEST INSERTION

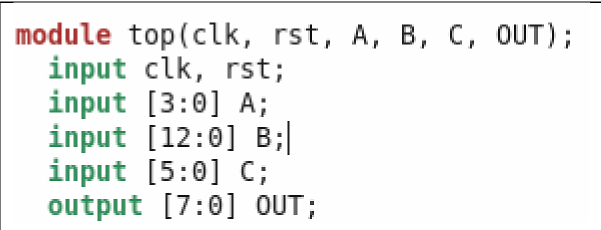
We have analyzed the netlist generated in step 3 by doing logical equivalence checking and Static Timing Analysis, now in this step we will be inserting scan chain in netlist and we will further analyze the difference it has with the previous netlist.

7.1 Differences in Original and Scan Chain Inserted Netlists:



```
module top(clk, rst, A, B, C, OUT, scan_en, test_mode, DFT_sdi_1,
    DFT_sdo_1, DFT_sdi_2, DFT_sdo_2);
  input clk, rst, scan_en, test_mode, DFT_sdi_1, DFT_sdi_2;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
  output DFT_sdo_1, DFT_sdo_2;
```

Scan Chain Inserted Netlist

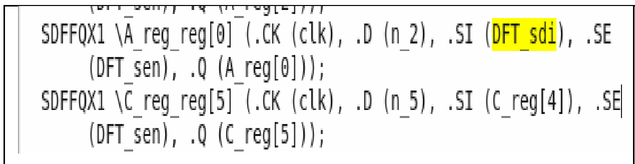


```
module top(clk, rst, A, B, C, OUT);
  input clk, rst;
  input [3:0] A;
  input [12:0] B;
  input [5:0] C;
  output [7:0] OUT;
```

Original Netlist

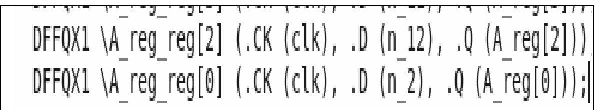
- For the first difference we can see that for enabling and assisting shift operation in the scan chain and selecting between normal operation and test mode operation extra inputs and outputs are added in the new netlist.

- These are **scan_en: scan enable, test mode, DFT_sdi_1, DFT_sdi_2 : scan inputs and DFT_sdo_1, DFT_sdo_2: scan outputs.**



```
SDFFQX1 \A_reg_reg[0] (.CK (clk), .D (n_2), .SI (DFT_sdi), .SE
    (DFT_sen), .Q (A_reg[0]));
SDFFQX1 \C_reg_reg[5] (.CK (clk), .D (n_5), .SI (C_reg[4]), .SE
    (DFT_sen), .Q (C_reg[5]));
```

Scan Chain Inserted Netlist



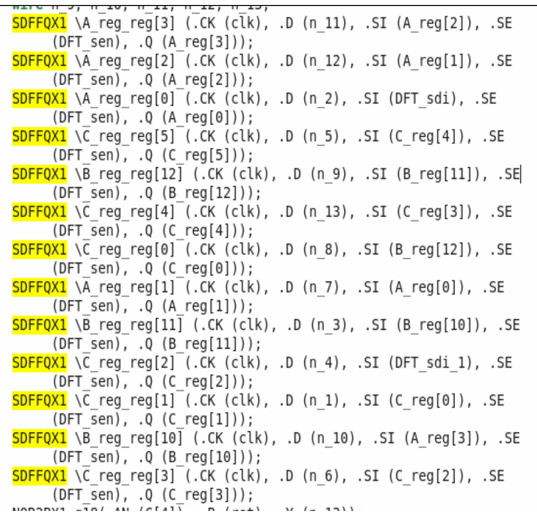
```
DFFQX1 \A_reg_reg[2] (.CK (clk), .D (n_12), .Q (A_reg[2]))
DFFQX1 \A_reg_reg[0] (.CK (clk), .D (n_2), .Q (A_reg[0]));
```

Original Netlist

- A scan chain with first scan cell input as DFT_sdi and output as A_reg[0] has been introduced by replacing the normal DFFs.

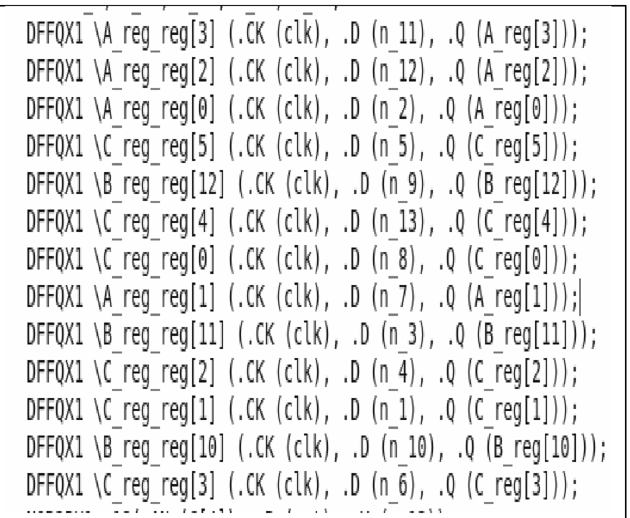
➢ One of the scan chain formed in our circuit is as follows: : DFT_sdi_1 ->A_reg[0]→ A_reg[1]→ A_reg[2]→ A_reg[3]→ B_reg[10]→ B_reg[11]→ B_reg[12]→ C_reg[0]→ C_reg[1]→ C_reg[2]→ C_reg[3]→ C_reg[4]→ C_reg[5]→DFT_sdo_1.

The scan chain formed is shown below.



```
SDFFQX1 \A_reg_reg[3] (.CK (clk), .D (n_11), .SI (A_reg[2]), .SE
      (DFT_sen), .Q (A_reg[3]));
SDFFQX1 \A_reg_reg[2] (.CK (clk), .D (n_12), .SI (A_reg[1]), .SE
      (DFT_sen), .Q (A_reg[2]));
SDFFQX1 \A_reg_reg[0] (.CK (clk), .D (n_2), .SI (DFT_sdi), .SE
      (DFT_sen), .Q (A_reg[0]));
SDFFQX1 \C_reg_reg[5] (.CK (clk), .D (n_5), .SI (C_reg[4]), .SE
      (DFT_sen), .Q (C_reg[5]));
SDFFQX1 \B_reg_reg[12] (.CK (clk), .D (n_9), .SI (B_reg[11]), .SE
      (DFT_sen), .Q (B_reg[12]));
SDFFQX1 \C_reg_reg[4] (.CK (clk), .D (n_13), .SI (C_reg[3]), .SE
      (DFT_sen), .Q (C_reg[4]));
SDFFQX1 \C_reg_reg[0] (.CK (clk), .D (n_8), .SI (B_reg[12]), .SE
      (DFT_sen), .Q (C_reg[0]));
SDFFQX1 \A_reg_reg[1] (.CK (clk), .D (n_7), .SI (A_reg[0]), .SE
      (DFT_sen), .Q (A_reg[1]));
SDFFQX1 \B_reg_reg[11] (.CK (clk), .D (n_3), .SI (B_reg[10]), .SE
      (DFT_sen), .Q (B_reg[11]));
SDFFQX1 \C_reg_reg[2] (.CK (clk), .D (n_4), .SI (DFT_sdi_1), .SE
      (DFT_sen), .Q (C_reg[2]));
SDFFQX1 \C_reg_reg[1] (.CK (clk), .D (n_1), .SI (C_reg[0]), .SE
      (DFT_sen), .Q (C_reg[1]));
SDFFQX1 \B_reg_reg[10] (.CK (clk), .D (n_10), .SI (A_reg[3]), .SE
      (DFT_sen), .Q (B_reg[10]));
SDFFQX1 \C_reg_reg[3] (.CK (clk), .D (n_6), .SI (C_reg[2]), .SE
      (DFT_sen), .Q (C_reg[3]));
```

Scan Chain Inserted Netlist



```
DFFQX1 \A_reg_reg[3] (.CK (clk), .D (n_11), .Q (A_reg[3]));
DFFQX1 \A_reg_reg[2] (.CK (clk), .D (n_12), .Q (A_reg[2]));
DFFQX1 \A_reg_reg[0] (.CK (clk), .D (n_2), .Q (A_reg[0]));
DFFQX1 \C_reg_reg[5] (.CK (clk), .D (n_5), .Q (C_reg[5]));
DFFQX1 \B_reg_reg[12] (.CK (clk), .D (n_9), .Q (B_reg[12]));
DFFQX1 \C_reg_reg[4] (.CK (clk), .D (n_13), .Q (C_reg[4]));
DFFQX1 \C_reg_reg[0] (.CK (clk), .D (n_8), .Q (C_reg[0]));
DFFQX1 \A_reg_reg[1] (.CK (clk), .D (n_7), .Q (A_reg[1]));
DFFQX1 \B_reg_reg[11] (.CK (clk), .D (n_3), .Q (B_reg[11]));
DFFQX1 \C_reg_reg[2] (.CK (clk), .D (n_4), .Q (C_reg[2]));
DFFQX1 \C_reg_reg[1] (.CK (clk), .D (n_1), .Q (C_reg[1]));
DFFQX1 \B_reg_reg[10] (.CK (clk), .D (n_10), .Q (B_reg[10]));
DFFQX1 \C_reg_reg[3] (.CK (clk), .D (n_6), .Q (C_reg[3]));
```

Original Netlist

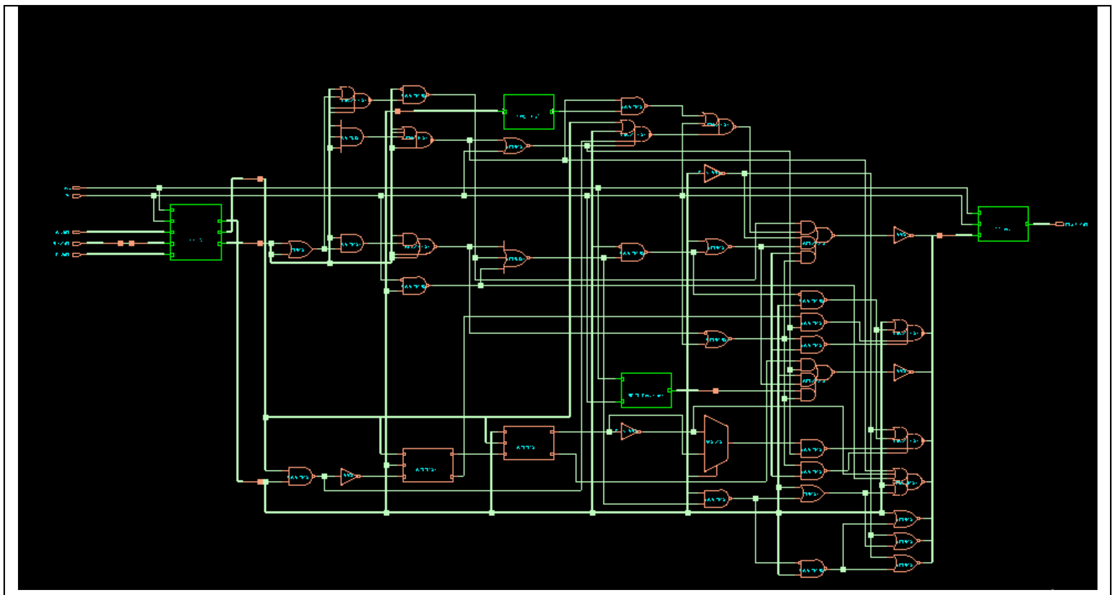


Fig7.1 Top module without scan chain

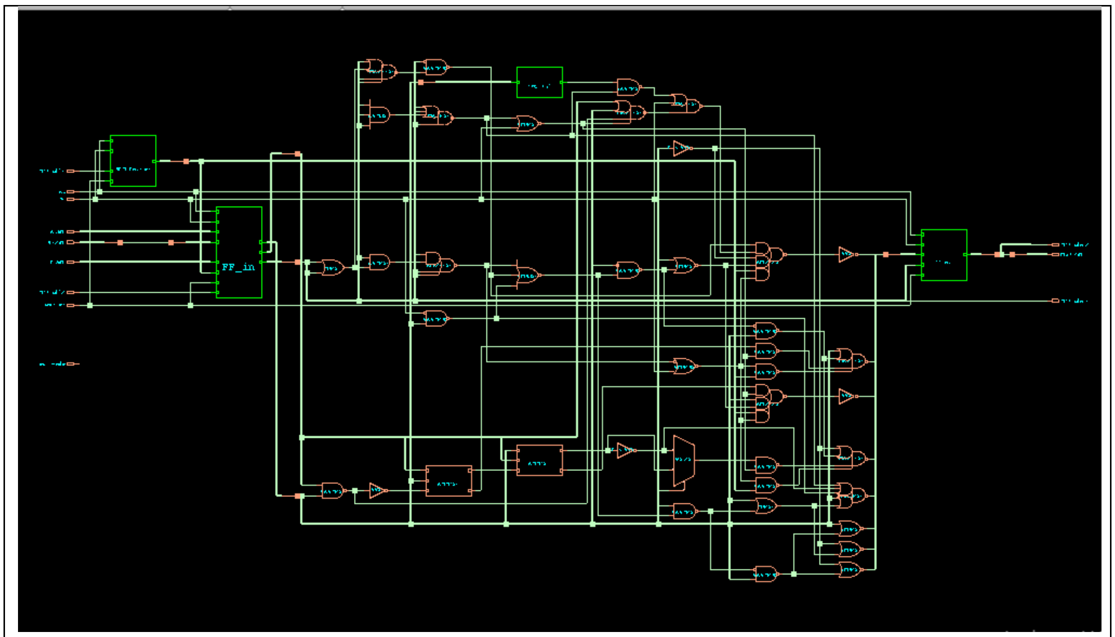


Fig7.2 Top module with scan chain:

- **Following are the scan chains formed in our circuit:-**

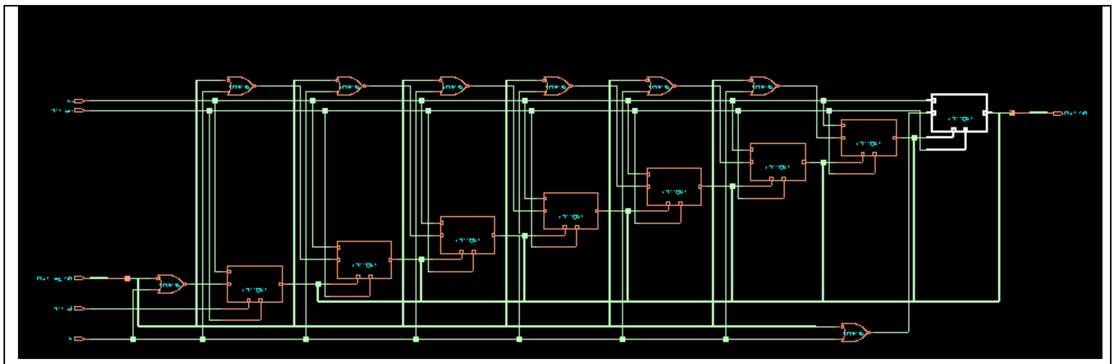


Fig7.3 FF_OUT

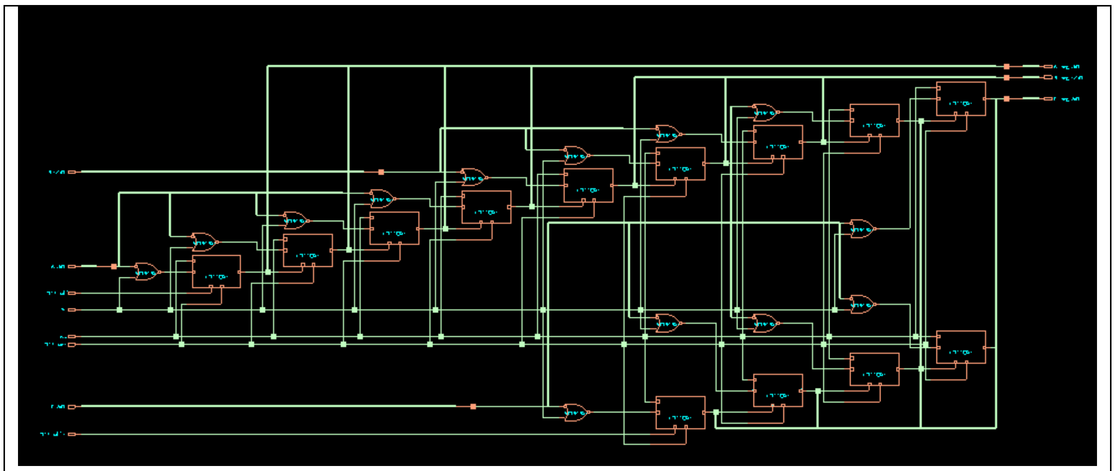


Fig7.4 FF_IN

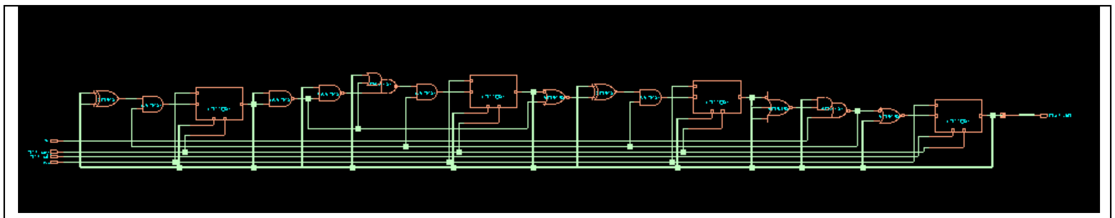


Fig7.5 BCD_Counter

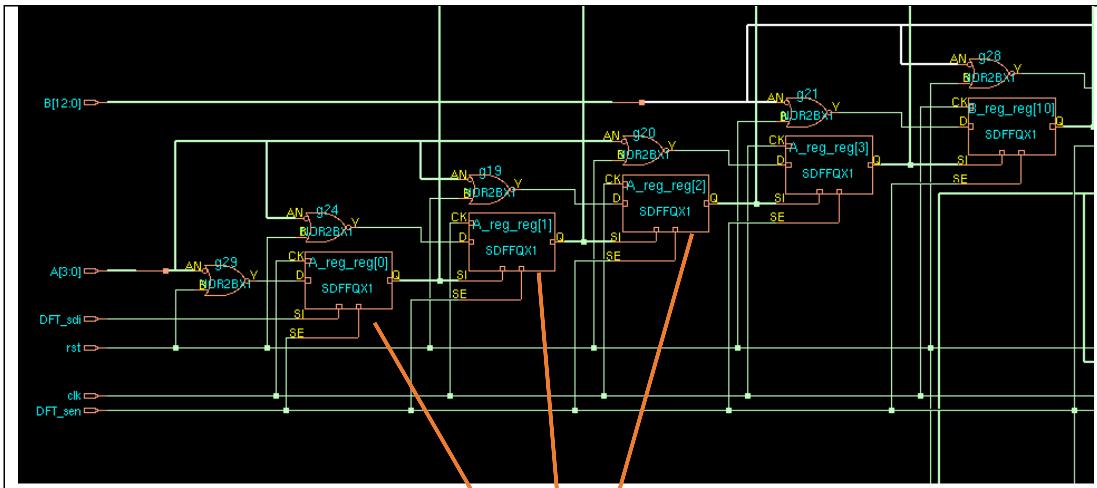

B[12:0]
A[3:0]
DFT_sdi
rst
clk
DFT_sen
AN g29 BOR2BX1 Y
AN g24 BOR2BX1 Y
CK A_reg_reg[0] D SDFFQX1 Q SI SE
AN g19 BOR2BX1 Y
CK A_reg_reg[1] D SDFFQX1 Q SI SE
AN g20 BOR2BX1 Y
CK A_reg_reg[2] D SDFFQX1 Q SI SE
AN g21 BOR2BX1 Y
CK A_reg_reg[3] D SDFFQX1 Q SI SE
AN g28 BOR2BX1 Y
CK B_reg_reg[10] D SDFFQX1 Q SI SE

Fig7.6 A Single Detailed Scan Chain View

These are some of the the Scan Cells (SDFFs).

7.2 Purpose of Scan Cells SDFFs and detection of failures:

- ***Scan chain design works in three modes:***
  1. Normal Mode
  2. Shift Mode
  3. Capture Mode

- The input port ***SE*** of the mux is used to select between Data Input(D) and Scan Input ***(SI).***
  - In Normal or Capture Mode, ***SE*** is set to 0 so the value present at D is latched by DFF.
  - In Shift Mode, ***SE*** is set to 1 ie. The value of SI is latched by DFF.

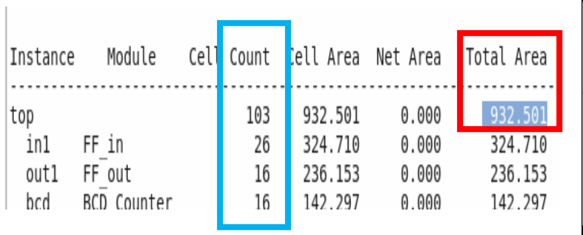
- In the Normal Mode***, scan_en and test_mode*** values are low (level 0) which indicate that SDFFs will work as normal DFFs having the same set of D and clock inputs and Q outputs.

- In the Shift Mode***, scan_en and test_mode*** values are high (level 1) and the test vectors are shifed into scan cells using port ***SI*** and results of computation are shifted to port ***DFT_sdo_1.*** This improves the Controllability of the design as the design does not have to go to all the transitions and complexity decreases.

- In Capture Mode the test vectors reach the desired point, they are provided to the cell to be tested and ***test_mode*** remains high but ***scan_en*** is turned low for one clock cycle. This captures the output which is the output of the cell to be tested. This increases the observability of the design.

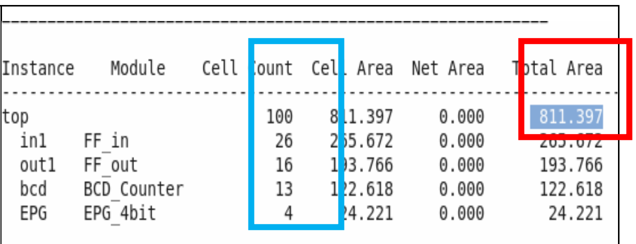
- Now, this output will travel to the scan chain output and then it’s being compared with the golden output. If there is a mismatch then **failure is detected.**

7.3.1 Comparison of Area Reports: -



```
Instance    Module     Cell Count  Cell Area  Net Area  Total Area
-------------------------------------------------------------------
top                       103     932.501    0.000     932.501
  in1     FF_in            26     324.710    0.000     324.710
  out1    FF_out           16     236.153    0.000     236.153
  bcd     BCD_Counter      16     142.297    0.000     142.297
```

(a) With Inclusion of Scan Chain



```
------------------------------------------------------------

Instance    Module     Cell Count  Cell Area  Net Area   Total Area
--------------------------------------------------------------------
top                       100     811.397     0.000     811.397
  in1     FF_in            26     265.672     0.000     265.672
  out1    FF_out           16     193.766     0.000     193.766
  bcd     BCD_Counter      13     122.618     0.000     122.618
  EPG     EPG_4bit          4      24.221     0.000      24.221
```

(a) Without Scan Chain

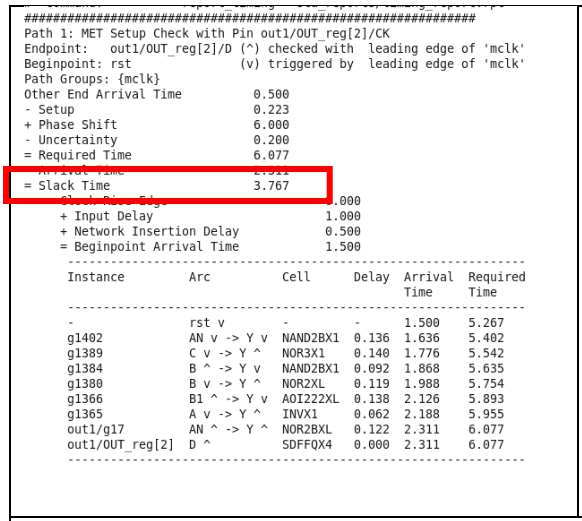
Area Reports

QoR Analysis:

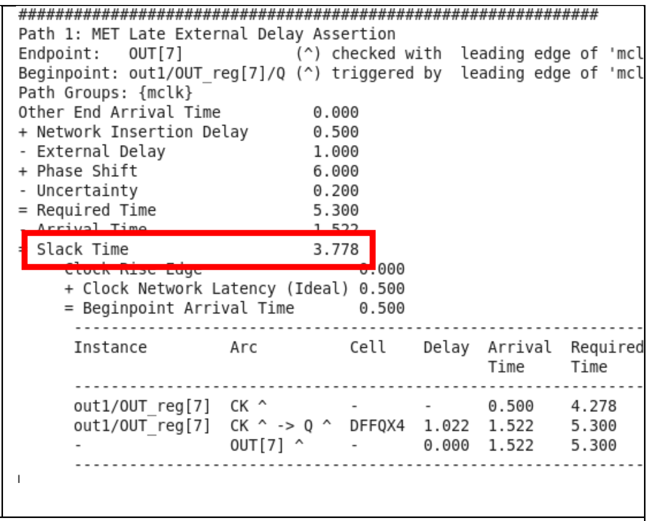
- From the ***Area Reports*** of both the netlists (with and without scan chain) we observe that,
  - After Scan Chain Insertion, the ***area of scan inserted netlist*** is bigger than original netlist with scan chain insertion.
    - With Scan Chain Insertion Area→932.501 units.
    - Without Scan Chain Insertion Area→811.397 units.
  - This is because SDFFs have more area than normal DFFs, because of additional mux circuitry and added testing functionality in SDFFs.

  - We can also observe that ***cell count*** has also increased in the scan chain insertion netlist. This can be due to additional functionality given by SDFFs given in the design as the extra cells are helpful for performing the two modes of operation i.e. Normal and the Testing mode.

7.3.2 Comparison and Detailed Analysis of Timing Reports: -



```
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[2]/CK
Endpoint:   out1/OUT_reg[2]/D (^) checked with  leading edge of 'mclk'
Beginpoint: rst               (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.223
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.077
- Arrival Time                  2.311
= Slack Time                    3.767
     Clock Rise Edge                      0.000
     + Input Delay                        1.000
     + Network Insertion Delay            0.500
     = Beginpoint Arrival Time            1.500
      ----------------------------------------------------------------
      Instance         Arc          Cell      Delay  Arrival  Required
                                                     Time     Time
      ----------------------------------------------------------------
      -                rst v        -         -      1.500    5.267
      g1402            AN v -> Y v  NAND2BX1  0.136  1.636    5.402
      g1389            C v -> Y ^   NOR3X1    0.140  1.776    5.542
      g1384            B ^ -> Y v   NAND2BX1  0.092  1.868    5.635
      g1380            B v -> Y ^   NOR2XL    0.119  1.988    5.754
      g1366            B1 ^ -> Y v  AOI222XL  0.138  2.126    5.893
      g1365            A v -> Y ^   INVX1     0.062  2.188    5.955
      out1/g17         AN ^ -> Y ^  NOR2BXL   0.122  2.311    6.077
      out1/OUT_reg[2]  D ^          SDFFQX4   0.000  2.311    6.077
      ----------------------------------------------------------------
```



```
################################################################
Path 1: MET Late External Delay Assertion
Endpoint:   OUT[7]            (^) checked with  leading edge of 'mcl
Beginpoint: out1/OUT_reg[7]/Q (^) triggered by  leading edge of 'mcl
Path Groups: {mclk}
Other End Arrival Time          0.000
+ Network Insertion Delay       0.500
- External Delay                1.000
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 5.300
- Arrival Time                  1.522
= Slack Time                    3.778
     Clock Rise Edge                      0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      ----------------------------------------------------------------
      Instance         Arc            Cell    Delay  Arrival  Required
                                                     Time     Time
      ----------------------------------------------------------------
      out1/OUT_reg[7]  CK ^           -       -      0.500    4.278
      out1/OUT_reg[7]  CK ^ -> Q ^    DFFQX4  1.022  1.522    5.300
      -                OUT[7] ^       -       0.000  1.522    5.300
      ----------------------------------------------------------------
```

Worst Path Timing Report (with and without scan chain insertion)

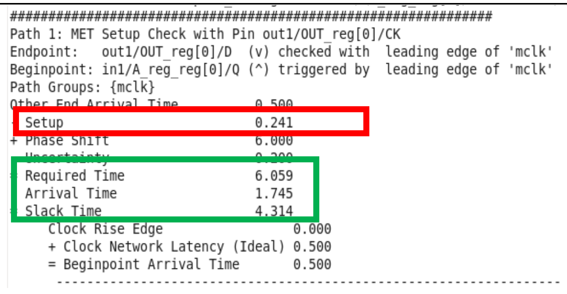
- While running the STA tool generally do the pessimistic analysis.

- Therefore we can see that after inserting the scan chain the critical path has been changed as earlier critical path was from *OUT_reg[7]/Q→OUT [7]* without inserting scan chain, Now it has changed to *rst→/OUT_reg[2]/D.*

- Also, we can see that after inserting the scan chain we have got the new slack value (3.767) which is lesser than the previous one which was (3.778). This is because critical path or worst path has changed after inserting scan chain.

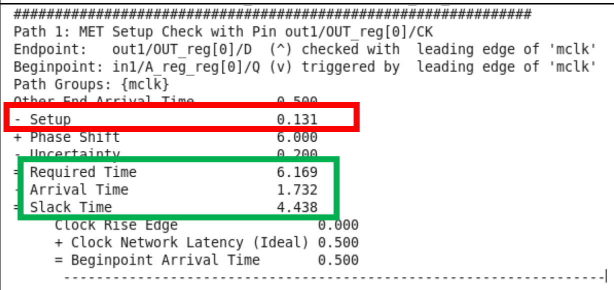
7.3 Timing Report (Same Path)

Path: A_reg_reg[0]/Q to OUT_reg[0]/D



```
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D  (v) checked with  leading edge of 'mclk'
Beginpoint: in1/A_reg_reg[0]/Q (^) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.241
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.059
- Arrival Time                  1.745
= Slack Time                    4.314
     Clock Rise Edge                     0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      -----------------------------------------------------------------
```

Path: A_reg_reg[0]/Q to OUT_reg[0]/D



```
################################################################
Path 1: MET Setup Check with Pin out1/OUT_reg[0]/CK
Endpoint:   out1/OUT_reg[0]/D  (^) checked with  leading edge of 'mclk'
Beginpoint: in1/A_reg_reg[0]/Q (v) triggered by  leading edge of 'mclk'
Path Groups: {mclk}
Other End Arrival Time          0.500
- Setup                         0.131
+ Phase Shift                   6.000
- Uncertainty                   0.200
= Required Time                 6.169
- Arrival Time                  1.732
= Slack Time                    4.438
     Clock Rise Edge                     0.000
     + Clock Network Latency (Ideal) 0.500
     = Beginpoint Arrival Time       0.500
      -------------------------------------------------------------------|
```

Timing Analysis of Same Path (with and without scan chain insertion)

- ❖ Analysis of the original netlist and scan chain inserted netlist timing report has been done with respect to the same path.

- ❖ **Following are the Difference in <u>QoR</u> by observations on different fields of timing report:**

  - ➢ Due to increase in the delays of path after scan chain insertion, Arrival Time has been increased from 1.732 to 1. 745.This increment in delay is because of the extra mux circuitry added, additional ports i.e., bigger cells (SDFFs) inserted.

  - ➢ The Required Time has decreased because of the increase in the setup time from 0.131 to 0. 241.This is because of the SDFFs which demands more setup time than DFFs.

  - ➢ Due to the decrement in RT and increment in AT, overall Slack has been reduced (as Slack=RT-AT) from 4.438 to 4.314.

  - ➢ Due to the reduction in slack of scan chain insertion circuit it has got more prone to violations.