A CMOS-VLSI RATE CONVERSION DIGITAL FILTER FOR DIGITAL AUDIO SIGNAL PROCESSING

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ABSTRACT

This paper describes CMOS-VLSI architecture for a rate conversion digital filter which interpolates an input discrete-time audio signal at the twice times higher sampling rate. In the proposed architecture, two discrete-time audio signals with 16-bit word length are multiplexed into a serial bit stream and are simultaneously interpolated through parallel table look up array multiplications.

Based on the architecture study, the VLSI interpolator which contains 34,000 transistors has been fabricated with 3 μm CMOS technologies. Its power consumption is less than 100 mW and the maximum input sampling rate is 50 kHz. The interpolator quality is specified in terms of in-band amplitude ripple and out-band attenuation each of which is ± 0.13 dB or 80 dB, respectively.

INTRODUCTION

Rate conversion or interpolation is often required in a variety of digital signal processing systems. For example, the speech signal stored or transmitted with a reduced rate should be converted back into the original signal with the much higher samlpling rate. In another aspect, the interpolation technique is used to make it easy to remove the undesirable sampling image by leaving it far apart from the desired signal spectrum as is shown in Fig.1.

The interpolation problem has been studied by many authors from the viewpoint of digital signal processing. Among them, Shafer and Rabiner revealed that the optimally designed linear phase FIR digital filter, as an interpolator, enjoys its advantage over not only IIR digital filters but also classical polynomial interpolators [1].

The FIR interpolator can in general be decomposed into L parallel FIR subfilters provided that the rate conversion factor is L, and each subfilter operates on the input discrete-time sequence once in an input sampling period. Recognizing the parallelism, it is natural to combine the L-channel multiplexing function with the interpolating process. Upon this consideration this paper first presents the FIR interpolator architecture which combines two-channel multiplexing and twice times interpolation efficiently. In the proposed architecture, two discrete-time sequences are multiplexed into a single stream and are simultaneously interpolated through the table look up array multiplications [2].

Since the two-subfilter arrangement is symmetric in the two-dimensional space and each subfilter retains symmetry in the coefficient array, the FIR interpolator can be compactly integrated on a VLSI chip. Furthermore, pipelining the table look up array multiplications assures the high speed operation of the interpolator even when CMOS technologies are exploited to fabricate the VLSI.

FILTER DESIGN

Consider a band limited continuous-time signal $\hat{x}(t)$ with the Fourier transform $\hat{X}(w)$. The signal $\hat{x}(t)$ is sampled to provide the discrete-time sequence

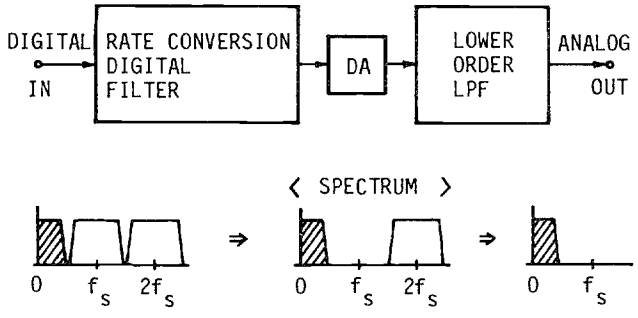

Fig.1. Application of a rate conversion digital filter.

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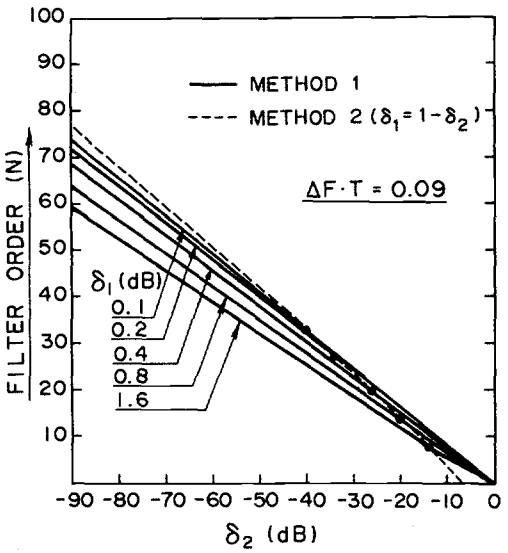

Fig.2. Required order of optimal FIR interpolator.

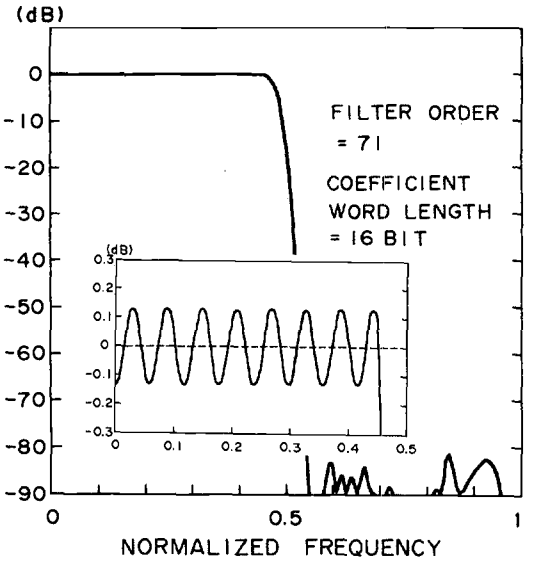

Fig.3. Optimally designed FIR interpolator frequency response.

$x(n) = \hat{x}(nT)$

with the sampling rate T^{-1} which is slightly higher than 2B, where B is the frequency band of $\hat{X}(w)$. Our purpose is to produce an interpolated sequence y(n) from the original sequence x(n) so that the mean-squared error

$$< |y(n) - \hat{x}(nT/2)|^2 >$$

is minimized.

Let z^{-1} be the unit delay of T/2, then the z-transform of the sequences x(n) and y(n) are

$$X(z^2) = \sum_n x(n)\, z^{-2n}$$

$$Y(z) = \sum_n y(n)\, z^{-n}$$

respectively. The interpolated sequence Y(z) is now related to the sequence $X(z^2)$ through a linear phase FIR interpolator H(z) as

$$Y(z) = X(z^2)\, H(z).$$

Since the original signal is band-limited within 1/2T, the ideal interpolator is the ideal low-pass filter with the cut-off frequency 1/2T.

There are two methods to optimize the linear phase FIR interpolator that approximates the ideal low-pass filter. The first method is to directly optimize H(z) so as to minimize in-band ripple and to maximize out-band attenuation. The second method is basd on the following subfilter decomposition.

$$H(z) = H_1(z^2) + H_2(z^2)\, z^{-1}$$

Oetken et al. showed that each subfilter can be optimized independently [3]. It can easily be shown that the optimal subfilter $H_1(z^2)$ is unity, and hence, optimizing the second subfilter $H_2(z^2)$ is equivalent to optimizing H(z) under the constraint that it meets the Nyquist I criterion [4].

Figure 2 shows the comparison of the required filter order between two methods. The evaluation is based on the formula derived by Rabiner and Gold [5]. In the figure, δ_1 and δ_2 denote in-band ripple and out-band attenuation respectively. The in-band edge and the out-band edge normalized by T^{-1} are assumed to be 0.455 and 0.545 respectively. At first glance, the second method seems to be more efficient because the optimized first subfilter $H_1(z^2)$ does not bring any computational complexity. However, as is recognized from Fig. 2, this cannot be true when the out-band attenuation more than 40 dB is required.

Taking the comparison results into account, the direct optimization method was exploited to design the high performance interpolator with δ_1 and δ_2 specified by 0.15 dB and 80 dB respectively. The optimization was performed through the Remez exchange algorithm [5] which provides the equiripple chebyshev approximation. The resultant interpolator is the 71st order linear phase FIR filter with 16-bit coefficient word length. Figure 3 shows the designed FIR interpolator performance.

ARCHITECTURE STUDY

As was mentioned previously, the FIR interpolator $H(z)$ can be decomposed into two subfilters $H_1(z^2)$ and $H_2(z^2)$. By multiplexing two input sequences, these subfilters are fully accessed without any idle time. Let $X_1(z^2)$ and $X_2(z^2)$ be two independent discrete-time sequences to be interpolated with the twice times higher sampling rate. The two-channel multiplexed sequence $S(z)$ is then

$$S(z) = X_1(z^2) + X_2(z^2)z^{-1}.$$

By applying the sequence $S(z)$ to $H_1(z^2)$ and $H_2(z^2)$ independently, we obtain

$$S(z)H_1(z^2) = X_1(z^2)H_1(z^2) + X_2(z^2)H_1(z^2)z^{-1}$$

$$S(z)H_2(z^2)z^{-1} = X_1(z^2)H_2(z^2)z^{-1} + X_2(z^2)H_1(z^2)z^{-2}.$$

Hence the interpolated sequences are derived by alternating individual even and odd sequences as

$$X_1(z^2)H(z) = [S(z)H_1(z^2)]_E + [S(z)H_2(z^2)z^{-1}]_O$$

$$X_2(z^2)H(z)z^{-1} = [S(z)H_1(z^2)]_O + [S(z)H_2(z^2)z^{-1})]_E,$$

where $[.]_E$ and $[.]_O$ denote the even numbered sequence and the odd numbered sequence respectively. The structure of the FIR interpolator which combines the multiplexing function is depicted in Fig. 4.

Besides the structural symmetry as in Fig. 4, each subfilter retains its coefficient array symmetry since the original filter is an odd order linear phase FIR filter. Therefore the effective number of multiply-and-add operations per output sample to execute the 71st order FIR filtering reduces to eighteen.

In order to fully reflect the symmetrical natures on the VLSI design, the table look up array multiplication technology [2] is exploited for the multiply-and-add operations. The ROM tables are divided into two groups, one for the first subfilter and the other for the second subfilter. Each group contains four parallelly divided ROM tables whose total capacity is 1536 bits. Figure 5 shows the designed interpolator architecture suitable for CMOS-VLSI implementation.

VLSI SYSTEM DESIGN

Based upon the architecture study, the VLSI system is designed. Generally speaking, parallel processing is not suitable for LSI implementation, since the wiring area may become wider as compared to that in serial processing. However, with the aid of the two-dimensional symmetry in the derived architecture, each block can be located closely to its predecessor and successor. The dynamic shift register is arranged in the center of the chip in order to minimize the tap-off wiring area for the ROM array which locates symmetrically around the center. Surrounding the ROM array, pre full adders and final full adders occupy their

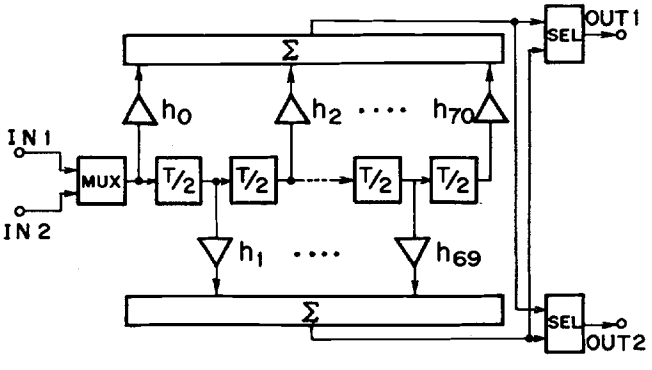

Fig.4. FIR interpolator configuration with multiplexing function.

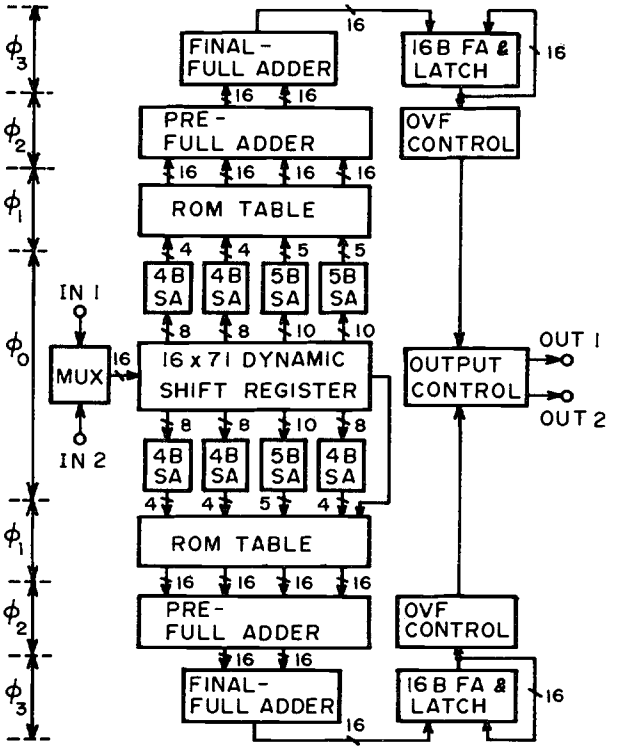

Fig.5. Interpolator architecture for CMOS-VLSI implementation.

positions in this order. Finally, an input block, an output block, a timing generator and test circuits are arranged in the peripheral area.

In addition to the topological innovation, each block is designed so that it provides minimized chip area and maximized timing margin. Along this line, the dynamic shift register is modified to the 16-bit wide dynamic shift register excited by nine different phase shift clocks. The table look up array multiplications are pipelined into four stages, denoted by ϕ_0, ϕ_1, ϕ_2 and ϕ_3 in Fig.5, which guarantees the high speed interpolating operation even when CMOS technologies are applied to the VLSI fabrication.

The VLSI interpolator which contains 34,000 transistors was fabricated through 3μm CMOS technology. The 3μm gate CMOS technology is believed to be the good compromise between integration density and production yield. The LSI chip size is about 48 mm^2, and its power consumption is less than 100 mW. The maximum available input sampling rate is 50 kHz which is enough to cope with the highest rate audio signal existing at present.

The designed VLSI chip is mounted on a 42-pin shrink DIP package and is operating with 2 MHz system clock under +5V power supply. Figure 6 shows the VLSI chip photograph and Table 1 summarizes the VLSI specifications.

CONCLUSION

The architecture study and design for a rate conversion digital filter which multiplexes two input discrete-time sequences and interpolates them with the twice times higher sampling rate have been presented from the veiwpoint of CMOS-VLSI implementation. Enjoying full advantage of symmetric structure, the rate conversion digital filter has been fabricated on a VLSI chip through 3 μm CMOS technologies. Its power consumption is 100 mW and the available input sampling rate is up to 50 kHz which covers the highest rate audio signal at present.

The designed rate conversion digital filter passes the desired signal with the in-band ripple within ± 0.13 dB and attenuates the out-band signal more than 80 dB without introducing any delay distortion or nonlinear distortion. Because of its qualified performance, the VLSI chip thus obtained will find extensive application areas with the advent of new digital media.

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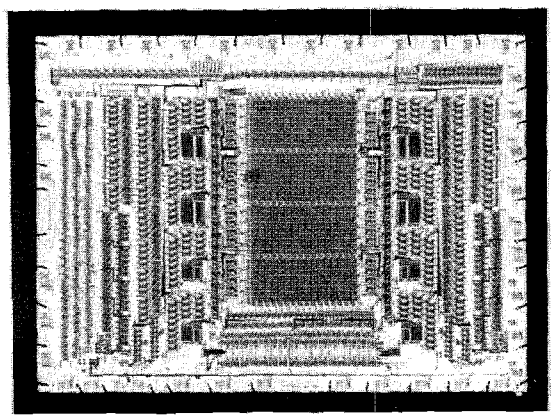

Fig.6. VLSI interpolator chip photograph.

design rule	3 μm gate CMOS
power consumption	100 mW
I/O data word length	16 bits
input sample rate	50 KHz max.
in-band ripple	±0.13 dB ($0 < f < 0.455$)
out-band loss	80 dB ($0.545 < f$)

Table 1. VLSI interpolator specifications.

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