MP 4.4 A Digital 80Mb/s OFDM Transceiver IC for Wireless LAN in the 5GHz Band

Wolfgang Eberle, Mustafa Badaroglu, Veerle Derudder, Steven Thoen[1], Patrick Vandenameele[1], Liesbet Van der Perre, Mario Vergara, Bert Gyselinckx, Marc Engels, Ivo Bolsens

IMEC, Leuven, Belgium
[1]Also PhD student at KU Leuven.

Emerging standards for broadband wireless LANs (WLANs) such as IEEE802.11a, Hiperlan-II and MMAC require orthogonal frequency division multiplex (OFDM) modulation for the physical layer (PHY) interface. OFDM modems are previously realized in the context of very high speed digital subscriber lines (VDSL) [1] and digital audio broadcast (DAB) [2]. However, the WLAN application puts different constraints on the OFDM transceiver presented here because the terminals are portable. Therefore, an adaptive frequency domain equalizer is integrated to mitigate the variations of the indoor wireless channel. Fast programmable on-chip acquisition hardware supports burst mode communications.

The monolithic transceiver IC encompasses all the digital signal processing required by an OFDM WLAN physical layer, except for forward error correction (FEC) (Figure 4.4.1). It can be used both in the gateway and in the terminal. The IC communicates with off-chip FIFO memories on the host side and to a pair of 8b DACs and 8b ADCs on the front-end side.

The first block in the transmit path, the mapper, maps the payload bits, which are input 2b parallel through the TX_data port, onto the subcarriers using BPSK or QPSK modulation. To facilitate the filtering in the front-end, a programmable number of carriers is not modulated, both on the low and high side of the spectrum. The mapper optionally achieves frequency diversity by spreading the data over the carriers with a programmable code. Spreading uses a local RAM to reduce off-chip memory accesses.

The IFFT performs the OFDM modulation. Its architecture is based on recursive decomposition (Figure 4.4.2) [3]. The implementation calculates 64, 128, and 256 point complex IFFTs in less than 1.28, 2.56, and 5.12µs with a latency of 64+11, 128+13, and 256+14 clock cycles, respectively. The optimum wordlength for each butterfly and multiplier/rotator is derived from a bit-true C++ model. The FFT delivers output samples in bit-reversed order.

Symbol reordering consists of two single-port 256x16b RAMs and a set of address generators. These transform the (I)FFT output to linear order. During transmission, they also perform the addressing to insert the guard interval and to introduce the acquisition training sequence. During reception, they interleave the FFT output to align all data carriers in an OFDM symbol to a single contiguous block of data suitable for an integrate & dump despreading operation in the demapper.

Since the WLAN standards require half-duplex operation only, the hardware of the (I)FFT and symbol reordering unit is shared between reception and transmission modes. This leads to 98% of the datapath memory being centralized and reused.

The coarse time synchronizer determines the received signal power, the carrier frequency offset and the start of the FFT-frames. Furthermore, it produces an automatic gain control signal and performs frequency correction. Importantly, it powers on the succeeding receiving circuitry upon successful detection of the frame start based on the acquisition sequence, leading to power saving during sleep mode.

The adaptive equalizer (Figure 4.4.3) consists of a single complex operator that sequentially processes the different carriers, and removes residual phase errors due to group delay and CFO. The equalizer performs channel estimation, per carrier, based on an initially or periodically transmitted BPSK modulated OFDM training symbol. Equalization is in one of three ways: feed forward based on the channel estimate, based on decision feedback per carrier (SC-FB), or averaged over all carriers (AC-FB). AC-FB introduces an additional delay of 1 OFDM symbol that is compensated by operating the equalizer for 1 symbol in SC-FB mode before switching to the AC-FB mode. Calculation of the equalizer coefficients makes use of matched filtering requiring a gain control unit instead of dividers. Finally, the demapper despreads the modulated symbols and delivers a 2x3b soft output signal suitable for a convolutional decoder.

Distributed control, based on token flow semantics, facilitates on-chip communication (Figure 4.4.4). Token flow greatly simplifies the global timing constraints and thus parallel designing. It is compatible with distributed local clock gating which is applied here to reduce the power consumption and implement power-efficient multi-rate signal processing.

The OFDM transceiver is flexible and programmable with respect to the symbol and burst structure (Figure 4.4.5). Thus, the modem operates efficiently under various channel conditions and service requirements. The IC is programmed through an asynchronous microprocessor interface. A test port allows an off-chip DSP full-speed access to all on-chip datapaths between different units.

The IC design started from an end-to-end dataflow simulation based on in-house C++ based OCAPI design environment [4]. Special C++ support libraries automated hierarchy issues, library management and synthesis scripting to produce input for a commercial HDL/standard cell methodology including layout and verification. Figure 4.4.6 summarizes the key IC figures including power consumption for the chip programmed similar to IEEE 802.11a QPSK mode. Figure 4.4.7 shows the die micrograph.

Acknowledgements:
The authors thank G. Vanwijnsberghe for contributions to design and test, and acknowledge IWT for funding part of this work.

References:
[1] Veithen, D. et.al., "A 70Mb/s Variable-Rate DMT-based Modem for VDSL," IEEE International Solid State Circuits Conference, vol. 42, pp. 248-249, Feb. 1999.
[2] Huisken, J.A. et.al., "A Power-Efficient Single-Chip OFDM Demodulator and Channel Decoder for Multimedia Broadcasting," IEEE-Journal-of-Solid-State-Circuits, vol.33, no.11; pp.1793-8, Nov. 1998.
[3] Despain A.M., "Very Fast Fourier Transform Algorithms for Hardware Implementation," IEEE Transactions on Computers, vol. C-28, pp. 333-341, May 1979.
[4] S. Vernalde, P. Schaumont, I. Bolsens, "An Object Oriented Programming Approach for Hardware Design", IEEE Computer Society Workshop on VLSI" 1999, Orlando/FL, April 1999.

Technology	3.3V CMOS 0.35µm 5LM
Maximum clock	50MHz
Package	144 PQFP
Transistor count	846000
Die size	16.4mm^2

Power consumption in "IEEE mode" at 20MHz	
-Transmission mode	270mW
-Reception mode	230mW
-Programming mode	160mW
-Sleep mode	50mW

Figure 4.4.6: IC key figures.

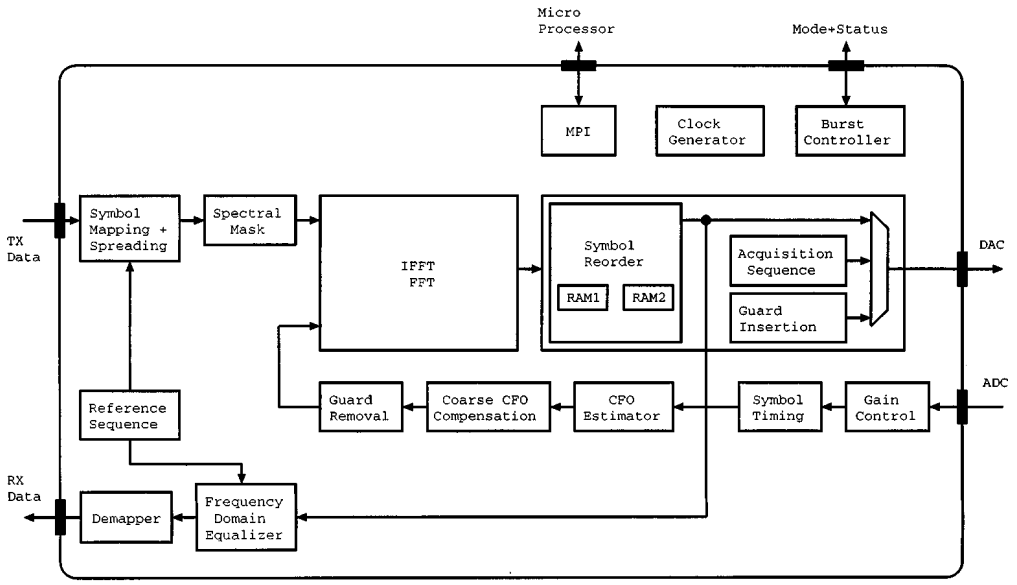


Figure 4.4.1: The OFDM transceiver core takes advantage of hardware sharing of half-duplex operation.

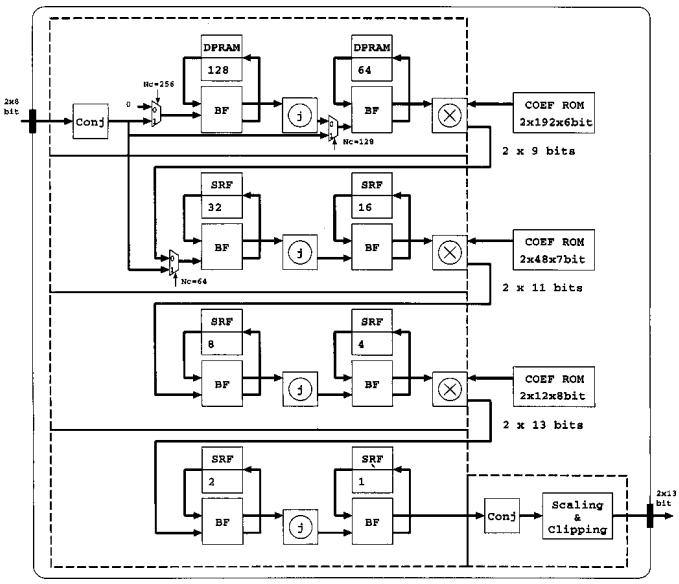


Figure 4.4.2: Recursive decomposition leads to good trade-off between IFFT/FFT latency and operator complexity.

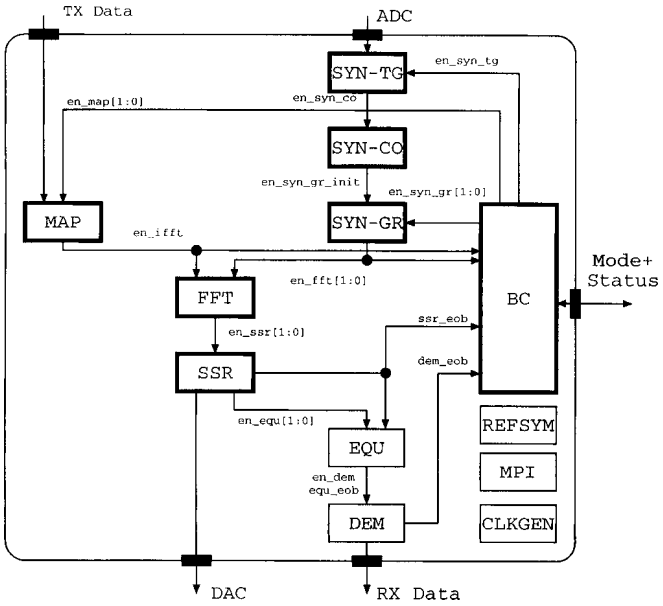


Figure 4.4.4: Distributed control compatible with clock gating applied to reduce average power consumption.

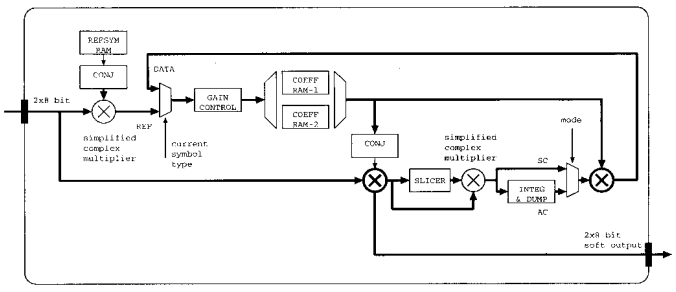


Figure 4.4.3: The frequency domain equalizer supports periodic channel estimation and tracking in three modes.

Parameter	Options
Number of carriers	64, 128, 256
Length of the guard interval	0:4:28
Modulation on the carriers	QPSK (BPSK)
Equalizer modes	REF-FF, SC-FS, AC-FB
Spreading	1, 2, 4, 8
Number of zero carriers	
-near DC	0:1:3, left and right
-near NYQUIST	0:2:30, left and right

Figure 4.4.5: Programmability allows transceiver core to adapt to channel conditions and service requirements.

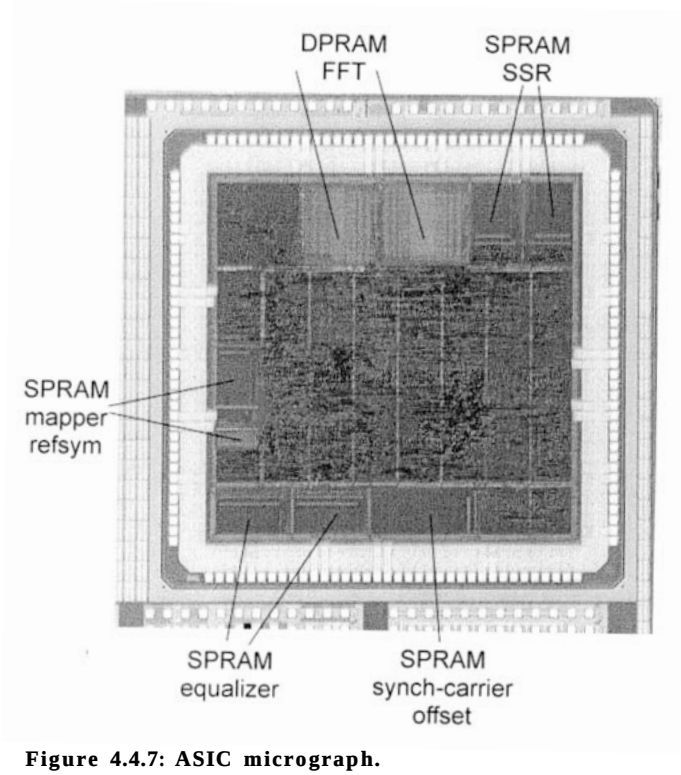
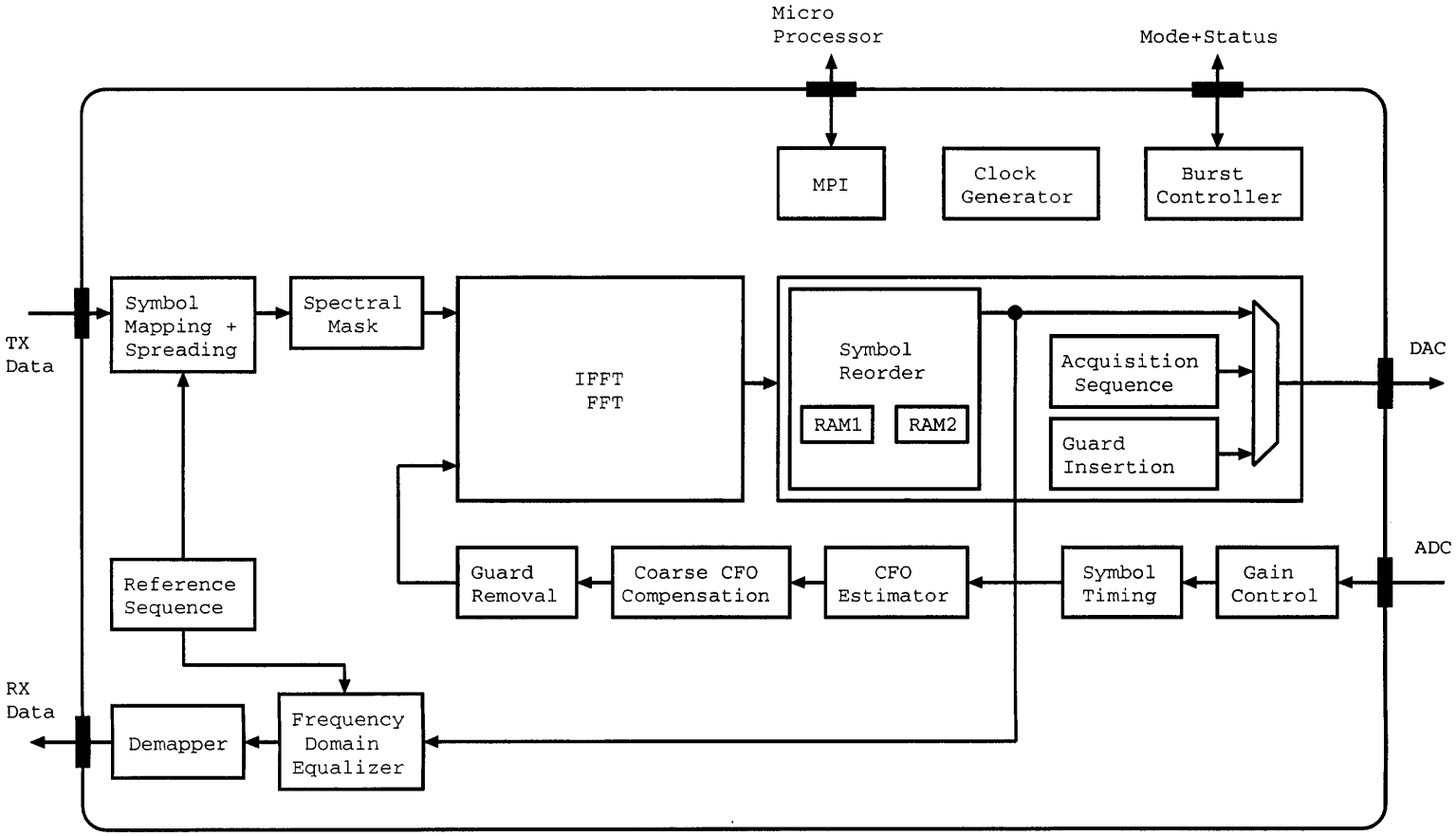


Figure 4.4.7: ASIC micrograph.



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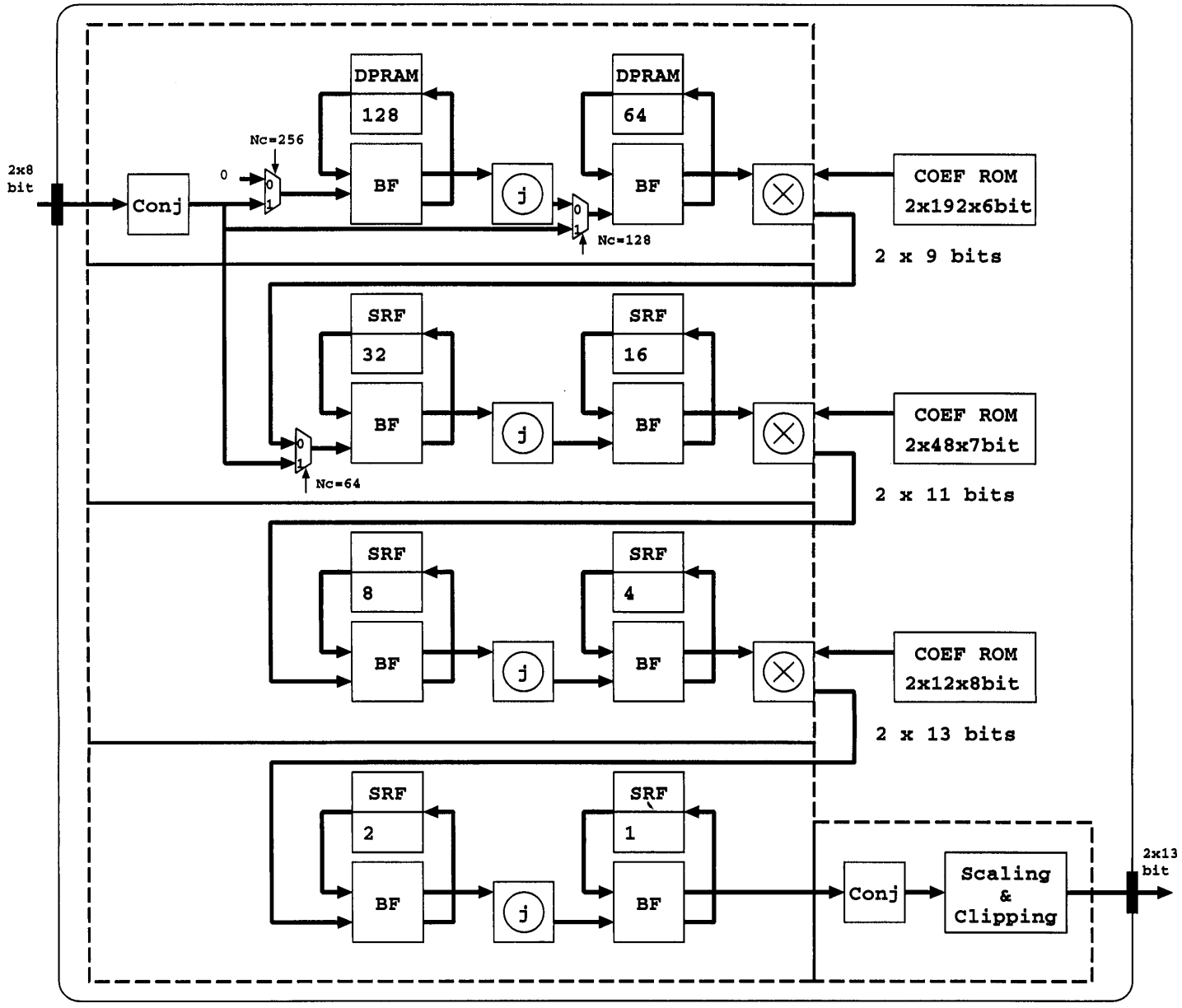

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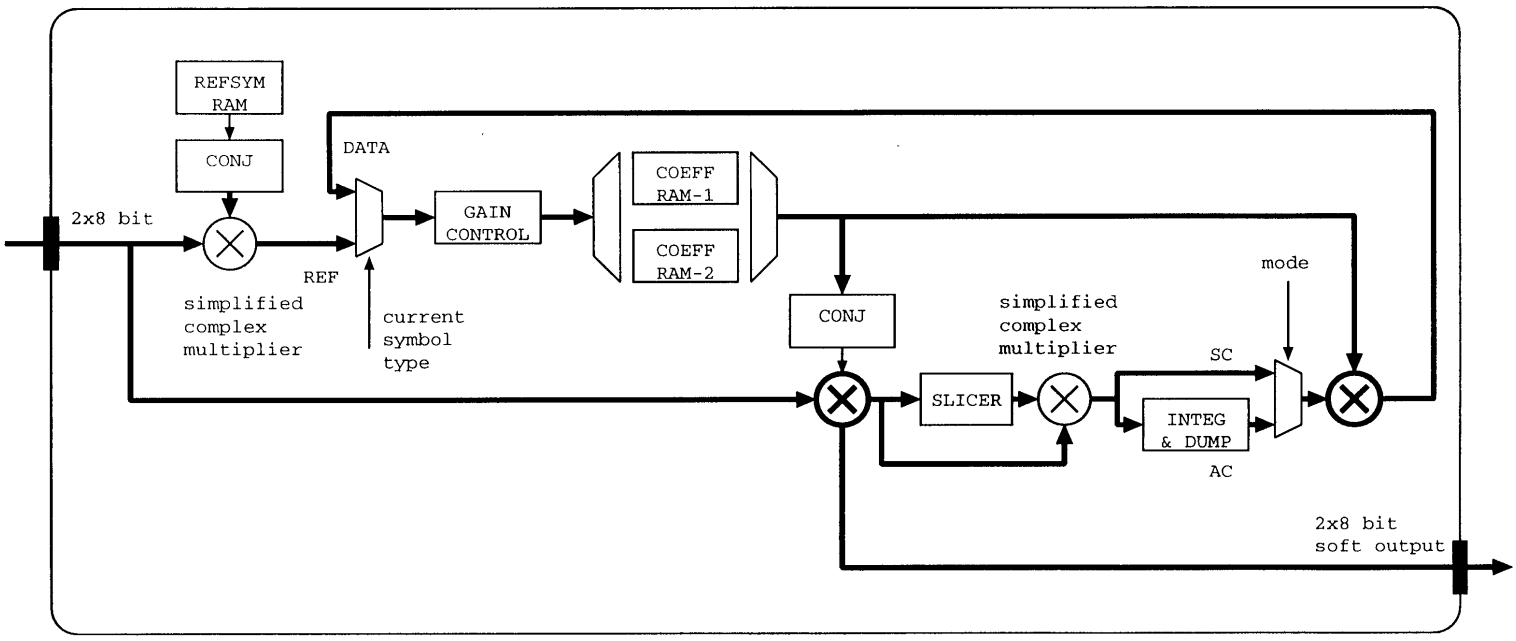

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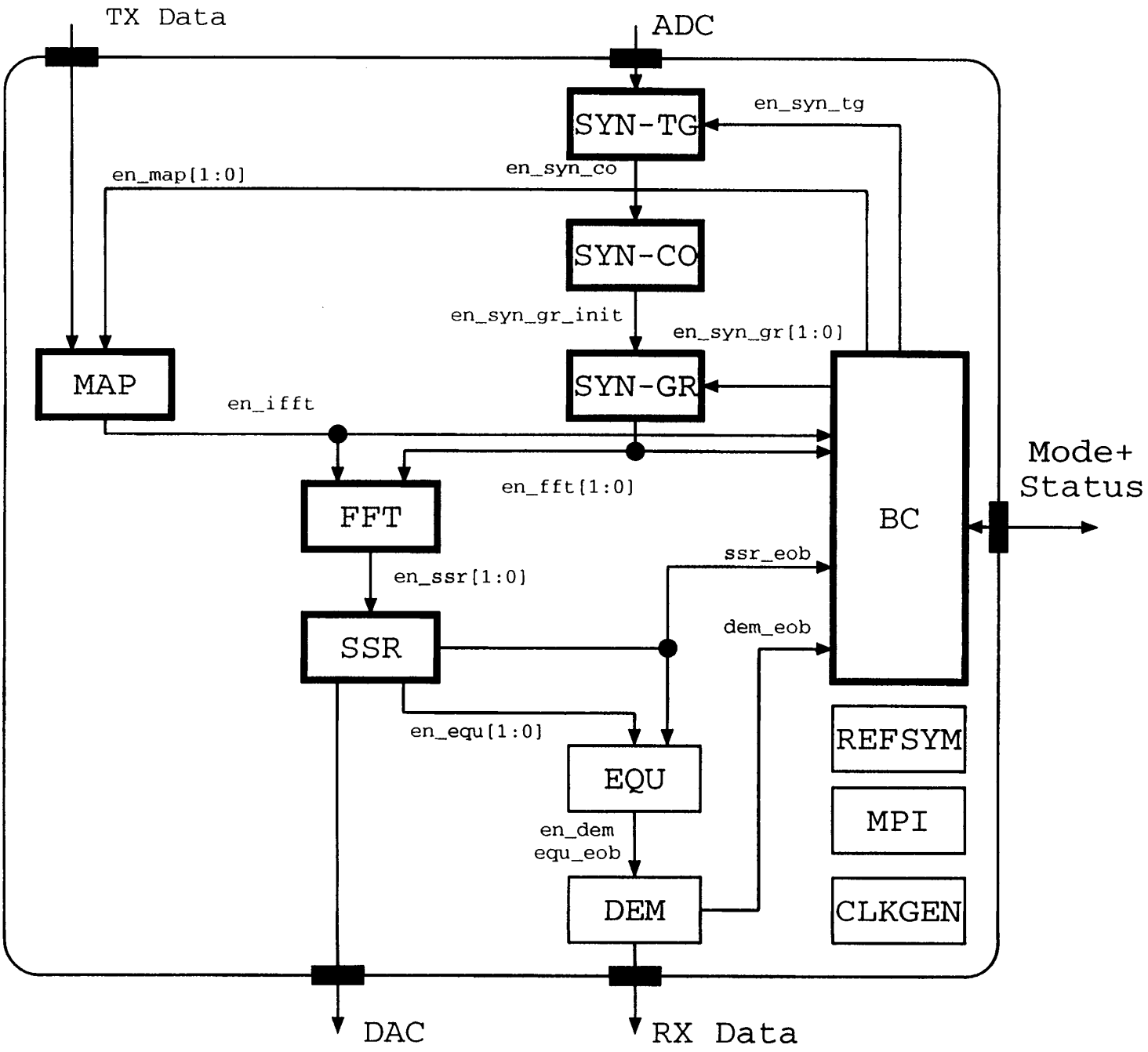

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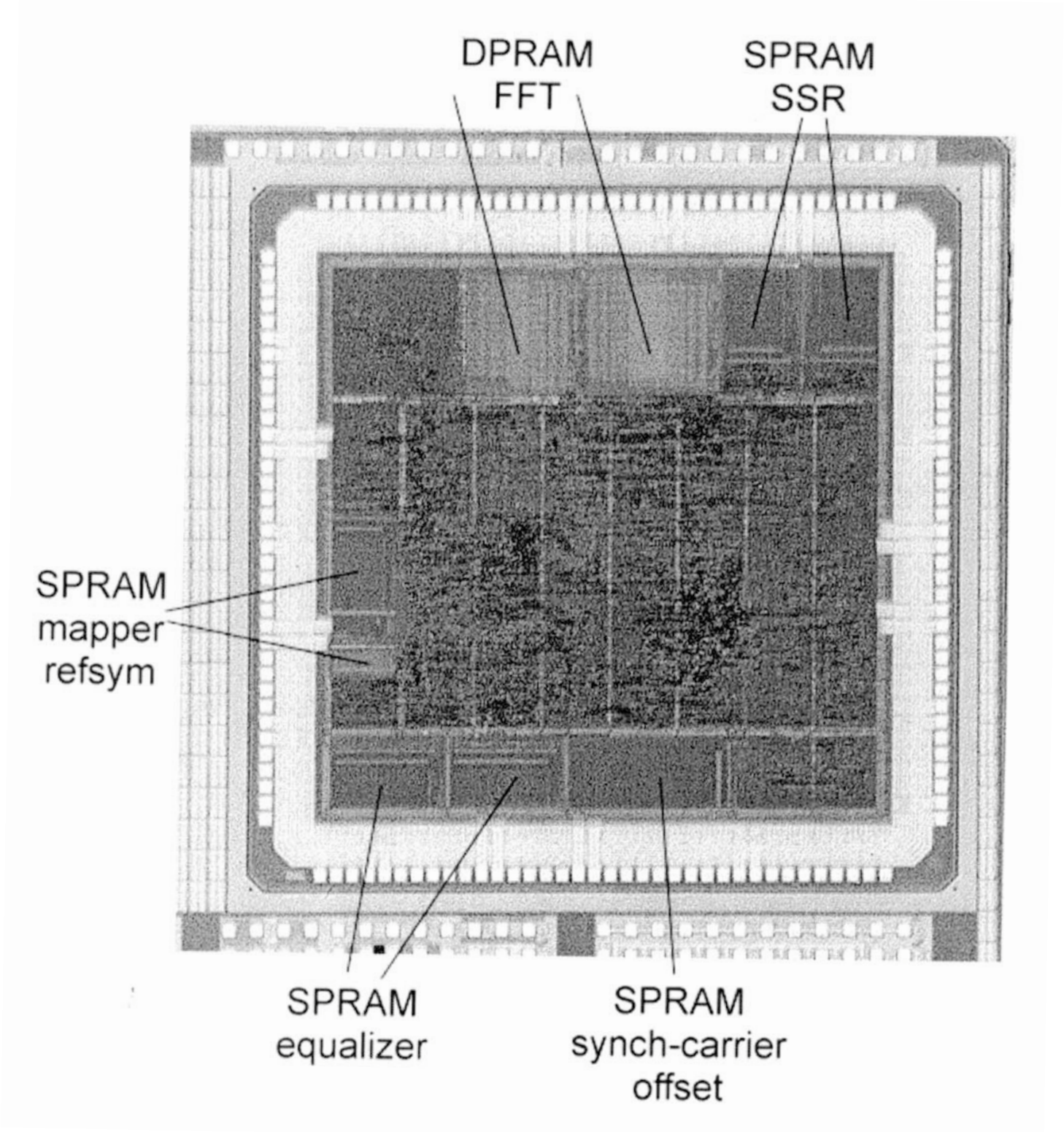

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