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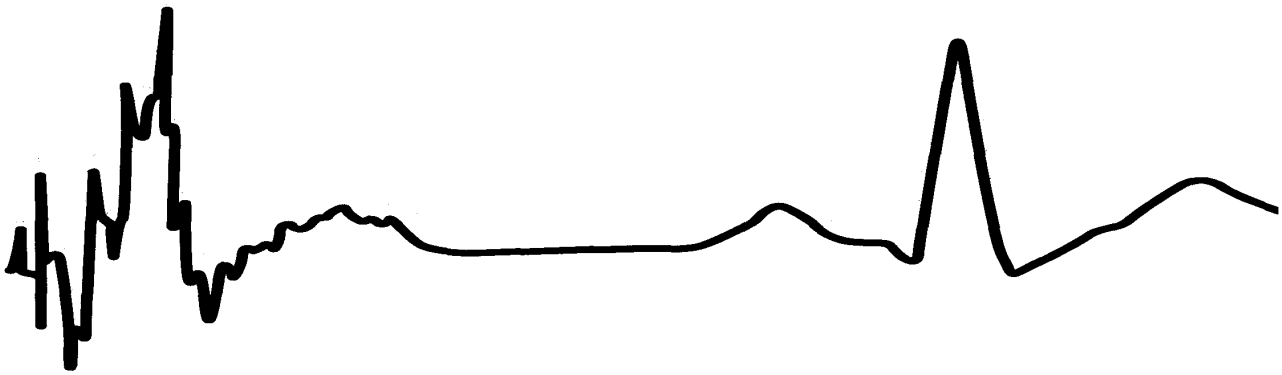

Merging Data Converters and DSPs for Mixed-Signal Processors

Sigma-Delta technology for analog-to-digital and digital-to-analog converters has existed for more than 10 years. Until recently, however, the process technology needed to make these devices commercially viable was not available. We can now manufacture 1-micrometer (or submicrometer), double polysilicon, CMOS (complementary metal-oxide semiconductor) geometries with high-quality capacitors. This approach supports widespread use of Sigma-Delta converters.

More significantly, these converters can integrate with complex digital signal processors (DSPs) on one chip. Our Sigma-Delta conversion produces high resolution without the analog components such as precise resistors in an A/D or a D/A converter. The precision moves from the analog domain to the digital domain and from analog circuitry to digital circuitry. These factors allow the manufacture of a monolithic, mixed-signal IC without involving new or costly processes or performance compromises.

Designers often refer to the Sigma-Delta converter as an "oversampling converter," although oversampling (sampling above the Nyquist rate) is just one of the techniques contributing to the performance of a Sigma-Delta converter. With this in mind, we characterize a Sigma-Delta converter for voice-band signals as one that quantizes an analog signal with a very low resolution (1 bit) and a very high sampling rate (about 2 MHz). Oversampling techniques and digital filtering reduce the sampling rate to about 8 kHz and increase the resolution to 16 bits.

Figure 1 on the next page shows this process. The main components are the Sigma-Delta modulator and the digital decimation filter, which selects one out of every m samples. This particular example describes a voice-band converter in which a DC input signal with approximately a 4-kHz bandwidth feeds into the converter. The modulator samples this waveform at a 2-MHz rate with a 1-bit resolution. The 1-bit output of the modulator feeds into a digital decimation filter that provides an averaging effect over a large number of these 1-bit samples, yielding a higher resolution, 16-bit digital sample at a lower rate (8 kHz) than that of the modulator.

The noise levels injected into the silicon substrate during digital switching limited the integration of both analog and digital circuitry on one VLSI chip. Our Sigma-Delta technology, which moves the precision to the digital realm, solved this problem and allowed the implementation of the ADSP-21MSP50, the first mixed-signal processor.

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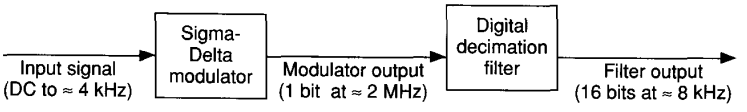

Figure 1. Sigma-Delta process in a voice-band converter.

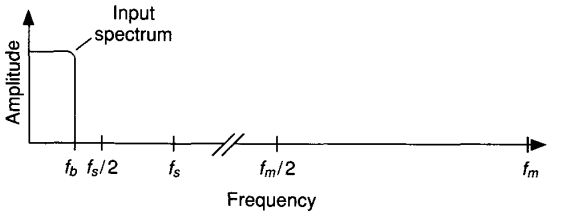

Figure 2. Relationships between sampling rates and the analog signal bandwidth.

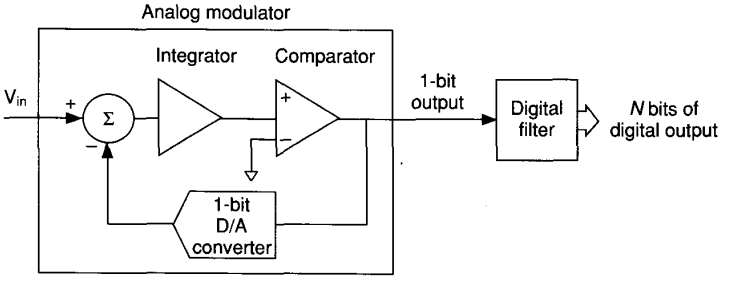

Figure 3. Block diagram of a Sigma-Delta A/D converter.

A Sigma-Delta converter samples an analog signal at one rate—producing digital data—and resamples the digital data at another rate. Figure 2 demonstrates the relationships between the different sampling rates involved and the analog signal bandwidth.

The input signal is contained in the frequency area below f_b, the input signal bandwidth. The modulator sampling frequency f_m is 512 times higher than the upper band edge of the input spectrum. The other two frequency references in the diagram are f_s, the rate of the data at the output of the digital filter (the rate at which resampling occurs), and $f_s/2$, the upper frequency limit of the signal entering the digital resampler (implemented within the digital filter).

Converter elements

Figure 3 shows the basic elements of the Sigma-Delta A/D converter. The analog modulator consists of an integrator and a comparator with a feedback loop containing a 1-bit D/A converter (a switch connecting to either positive or negative reference levels). A digital filter follows the modulator. Also, a clock circuit (not shown) provides timing for the modulator and digital filter.

This topology, although it is not new, greatly resembles some traditional, widely used A/D converters, namely the dual-slope, integrating converter and the synchronous voltage-to-frequency converter (SVFC). The Sigma-Delta converter provides the resolution typical of the former type, but with the higher clock rate typical of the latter.

The dual-slope integrating A/D converter in Figure 4a includes the same basic elements (integrator, comparator, feedback with a switch, and clock) found in the Sigma-Delta converter. The basic operation of the dual-slope, integrating A/D converter consists of the integration of the input voltage over a given time period followed by integration back to zero ("deintegration") using the reference voltage level. The counter determines how many clock cycles it takes for the voltage to reach the reference during the deintegration stage. This time is proportional to the input voltage level V_{in} and, therefore, the counter provides a binary number representation of the input voltage. The counter operation over this deintegration period is comparable to the digital filtering of the Sigma-Delta converter.

The integration and deintegration operations employ the same components. This circumstance leads to advantages in practice, such as no differential nonlinearity and an integral linearity that is not limited by component mismatches.

Because the frequency response of the dual-slope integrating A/D converter is limited, this type of device appears mainly in low-frequency measurement applications.

The SVFC in Figure 4b also includes the same basic elements (integrator, comparator, feedback with a switch, and clock) found in the Sigma-Delta converter. The output of the SVFC is a 1-bit value produced by the output of the comparator in response to the voltage level at the output of the integrator. A counter (not shown) uses the 1-bit value to determine the number of cycles between zero logic levels. The resultant binary number (relative to the output period) is proportional to

the input voltage level. The SVFC, also well-suited to lower frequency input signals, has the same performance benefits as the dual-slope, integrating A/D converter.

Data versus signal

The encoding principles of the dual-slope converter and the SVFC consider each measurement to be independent. In fact, the key to obtaining high precision at high sampling rates in the Sigma-Delta method is that only small changes between adjacent samples need be encoded in an actual "band-limited" signal. The Delta technology comes from this approach. The term *signal acquisition* better suits this scenario because the signal is being acquired as opposed to only a single data sample being taken.

Because signal acquisition must satisfy a certain bandwidth requirement, it requires a different type of converter from the type used for single-data sampling. Until recently, designers usually employed successive-approximation or flash-type A/D converters for this purpose. The Sigma-Delta architecture offers good signal acquisition due to:

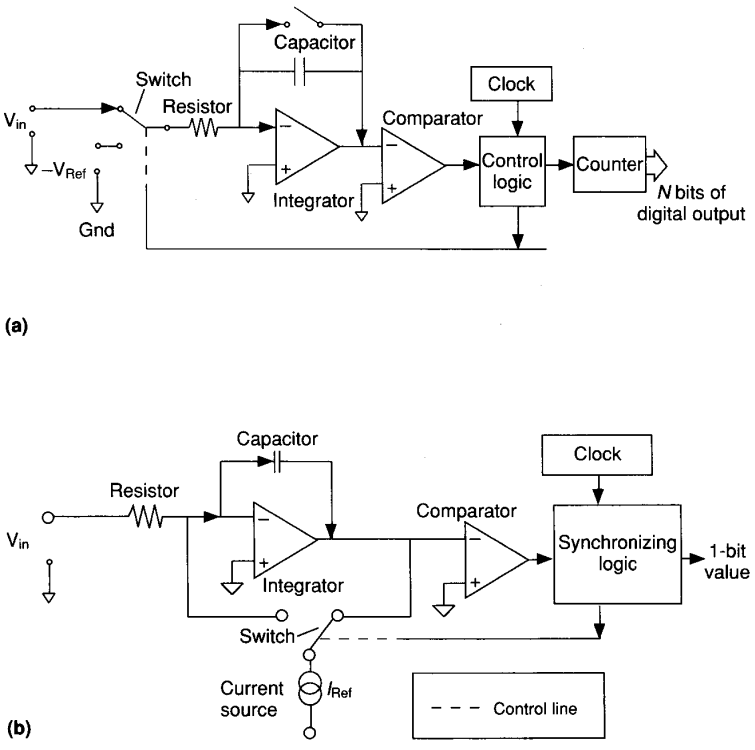

Figure 4. Comparison of a dual-slope integrating A/D converter (a) to a synchronous voltage-to-frequency converter (b).

- a complete conversion and filtering system;
- low-cost, high-performance conversion;
- integral digital filtering;
- system-level filter response, antialiasing, and noise rejection;
- freedom from differential nonlinearity errors; and
- good low-level, signal-to-noise performance.

We examine the advantages and drawbacks of the Sigma-Delta A/D converter, as well as the implications for expanded DSP applications.

DSPs and converters

Effective use of DSPs for implementing algorithms—such as the ubiquitous FFT (fast Fourier transform)—for real-world signals requires an architecture that is optimized for the inherent, looping, repetitive nature of these algorithms. (The sum-of-products operation is typical.) This architecture, which is implemented in Analog Devices' ADSP-2100 family,[1] must include

- fast and flexible arithmetic,
- an extended dynamic range on sum-of-products terms,
- a single-cycle fetch of two operands,
- circular buffering in hardware to simplify address generation, and
- looping and branching operations without overhead.

In short, fast multiplication capability alone does not provide an effective signal-processing architecture. The arithmetic core of the ADSP-2100 series consists of an ALU, a multiply-accumulate unit (Mac), and a barrel shifter. A result bus connects all units so that during the next cycle the output of any unit may be used as its own input or as input for any other unit (see Figure 5 on the next page). The ALU and Mac directly connect to both the program bus (not shown) and the data-memory bus. Operands for the ALU and Mac can come from on- and off-chip memories or from data registers within the processor.

When an A/D converter functions as an integral part of the monolithic DSP, the DSP becomes more techni-

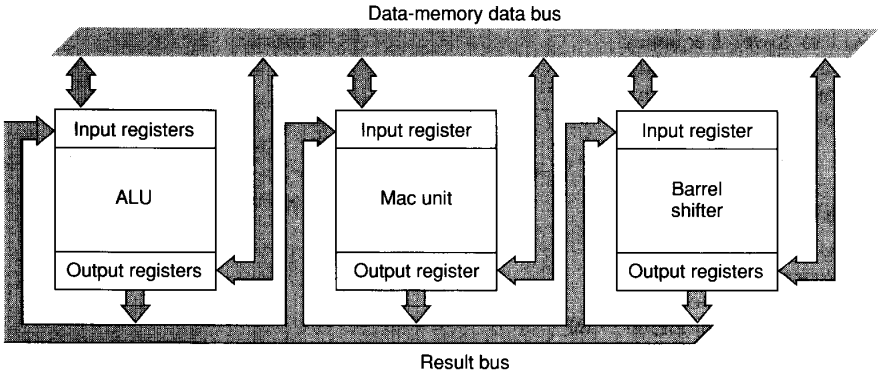

Figure 5. Arithmetic architecture.

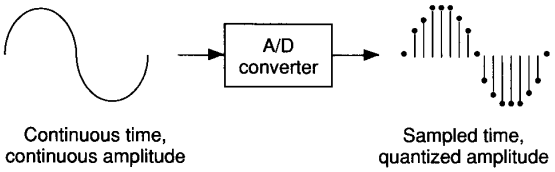

Figure 6. A continuous signal sampled in time and quantized in amplitude.

cally and economically feasible for use as an embedded mixed-signal processor. The DSP could function in a similar fashion to microcontrollers (microprocessors with significant digital I/O, on-board memory, and other critical support functions). These devices appear in products such as security alarms, thermostats, and videocassette recorders.

This mixed-signal processor could function in 9,600-bps, full-duplex modems; acoustic noise-cancellation systems; voice compression; and digital cellular phones.

Unfortunately, major difficulties occur when one tries to combine the data-conversion circuitry with the DSP core. High-performance conversion circuitry usually requires IC processes that are very different from the digital CMOS processes used for a DSP. Even if both could be combined by a common process into a monolithic IC, the digital noise of the DSP would severely compromise the converter performance.

An alternative strategy is to develop architectures such as Sigma-Delta converters that are compatible with digital processes and provide techniques for minimizing the effects of noise. The Sigma-Delta converter scheme does not electrically isolate the converter from the DSP noise. Instead, the scheme moves the need for precision from the analog circuitry of the converter to digital circuitry of the IC. This digital circuitry, of course, is far less noise sensitive than the analog circuitry. In fact, one can design digital circuitry specifically to minimize, via its algorithm, the effect of noise.

Sampling, quantization noise

Figure 6 represents the conversion of a signal that is continuous in both time and amplitude to one that is sampled in time and quantized in amplitude.

The quantization of the amplitude contributes noise into the system. This quantization noise leads to a function of the Sigma-Delta modulator known as *noise-shaping* (see section on frequency domain analysis). In the voltage range from – 1/2 least significant bit to + 1/2 LSB, the quantized value remains the same. Since the converter output is the same for the range of analog voltages, the quantization introduces an error.

For dynamic signals encountered in signal processing applications, the error probability density is evenly distributed over this voltage range of –1/2 LSB to + 1/2 LSB. In the frequency domain, this uncertainty appears as white noise. The level of this white noise is inversely proportional to the number of bits in the quantization and to the sampling rate, as shown by

$$1\ \text{LSB} / \sqrt{12 f_s}.$$

We increased the number of bits used for quantization to yield better signal-to-noise performance.

A dramatic increase in the sampling rate makes the denominator of this spectral density amplitude very large and thus the quantization noise level small. Also, with the sampling rate substantially increased, the band of interest for the input signal is well below half of the sampling rate. As shown in Figure 7, the noise between the upper band edge of the input signal spectrum and half of the sampling rate can be filtered out. The figure

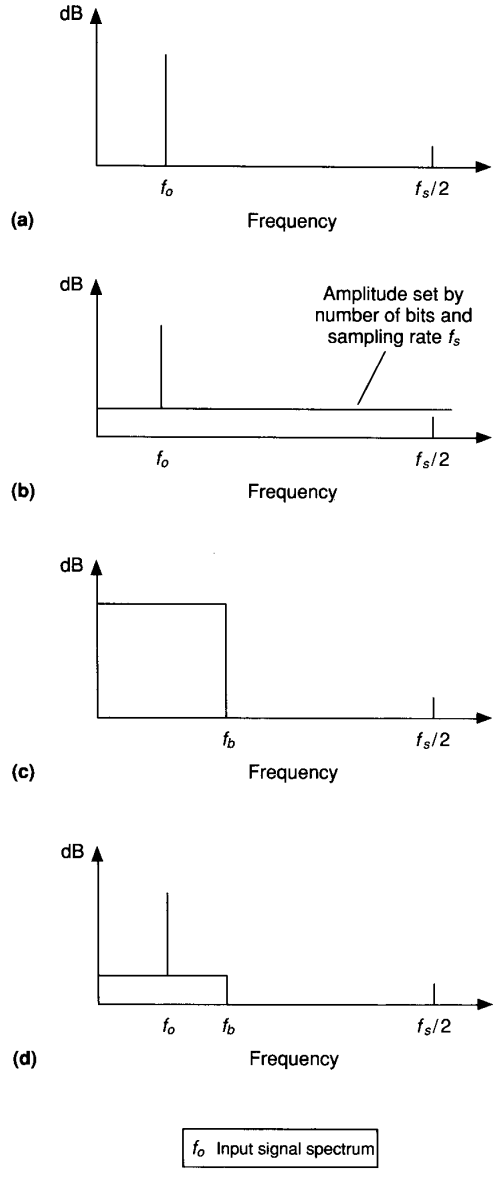

Figure 7. Quantization noise-shaping: input signal spectrum (a), output spectrum of an *n*-bit A/D converter (b), digital filter response (c), and filter output spectrum (d).

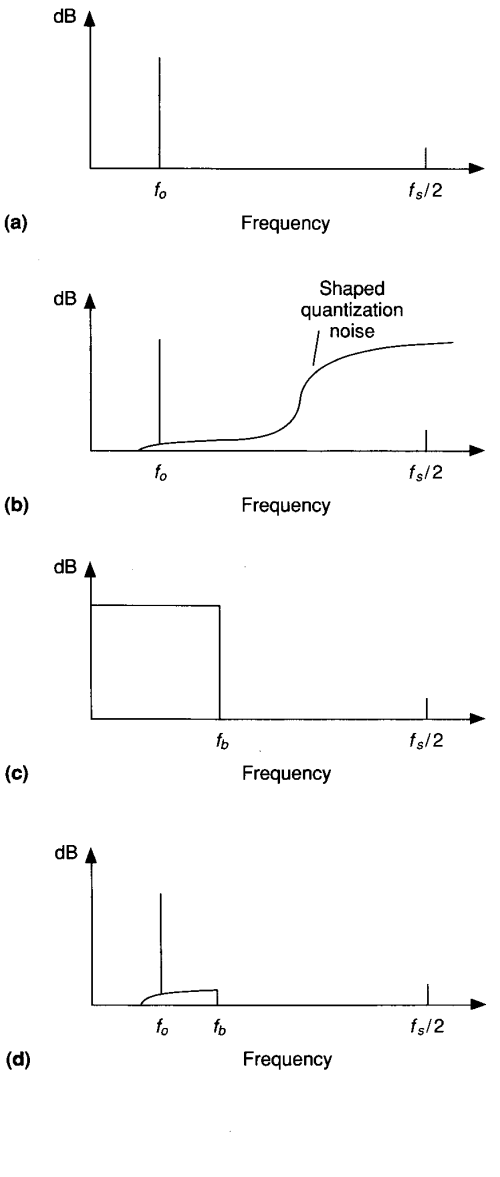

Figure 8. Sigma-Delta noise-shaping: input signal spectrum (a), modular output spectrum (b), digital filter response (c), and filter output spectrum (d).

shows the resultant output after a quantized signal passes through the digital filter.

One of the major differences of the Sigma-Delta converter comes into play at this point. If the noise can be shaped so that the overall noise energy is still the same but the noise is pushed out to the area above the signal spectrum of interest, practically no noise will occur in the signal band of interest. Also, the noise in the out-of-band area can be filtered out without affecting the input signal spectrum (see Figure 8). Figure 8 demonstrates the same process as Figure 7, except for Figure 8b, which shows the shaped quantization noise.

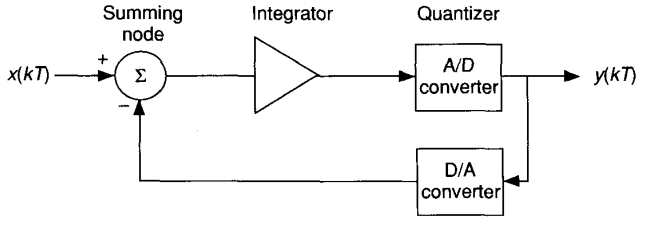

Figure 9. Block diagram of a Sigma-Delta modulator.

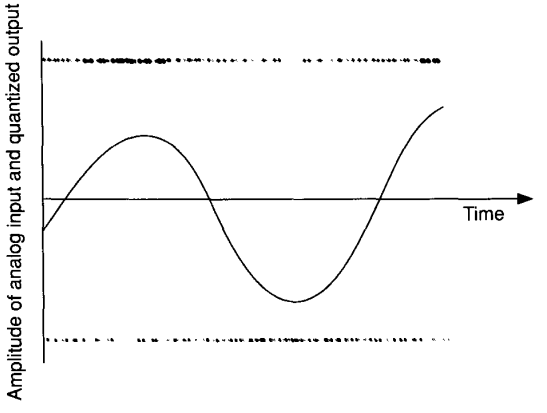

Figure 10. Sigma-Delta modulator output for a sine wave input.

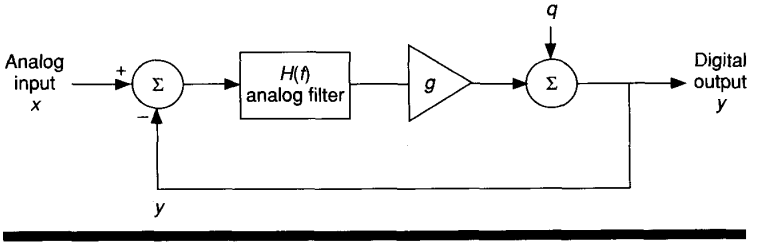

Figure 11. Detailed Sigma-Delta modulator in the frequency domain.

The modulator of the Sigma-Delta converter performs this noise-shaping function. Noise-shaping can dramatically reduce quantization noise effects in the signal band. The combination of noise-shaping and a very high sampling rate allows for a 1-bit conversion with noise performance equivalent to 16 bits or higher of quantization (at a much lower sampling rate).

Modulator design

Figure 9 illustrates a generalized block diagram of the Sigma-Delta modulator. The modulator consists of a summing node, an integrator, a comparator that functions as an A/D converter, and a feedback loop with a D/A converter that can be built with a 1-bit switch.

For a "perfect" conversion, the output sample $y(kT)$ "perfectly" represents the input $x(kT)$, in which (kT) is a time-varying function at any given sampling interval. Since the conversion is quantized, a quantization error occurs. The D/A converter changes the erroneous output back into an analog signal and feeds it to the summing node where it is subtracted from the input signal to yield the quantization error value. The node integrates the error and subsequently feeds it to the quantizer. This process keeps the output equal to the input over an average of sampling intervals.

The Sigma-Delta modulator is very difficult to analyze in the time domain because of the apparent randomness of the output 1-bit data value. Figure 10 shows the output of a first-order Sigma-Delta modulator for a sine wave input. The output is either 1 or 0. When the signal is near plus, full scale, the output is positive during most of the clock cycles. The opposite is true for near-minus, full-scale signals.

When a digital filter that can perform sophisticated averaging functions (see Figure 1) follows the modulator, the 1-bit sequence becomes a more meaningful signal by virtue of the filter algorithm.

Frequency domain analysis

Figure 11 shows the frequency domain linearized model of the Sigma-Delta modulator in which the integrator is represented as an analog filter with a given transfer function. For an integrator, the transfer function has an amplitude that is inversely proportional to the input frequency ($1/f$ relationship).

Figure 11 models the quantizer as a gain stage g followed by the addition of quantization noise q. One of the advantages of analysis in the frequency domain is that one can use algebra to describe the signals. If, for the moment, the gain is set to 1 and the transfer function $H(f)$ is represented as $1/f$, the blocks of Figure 11 are

$$y = (x - y)/f + q.$$

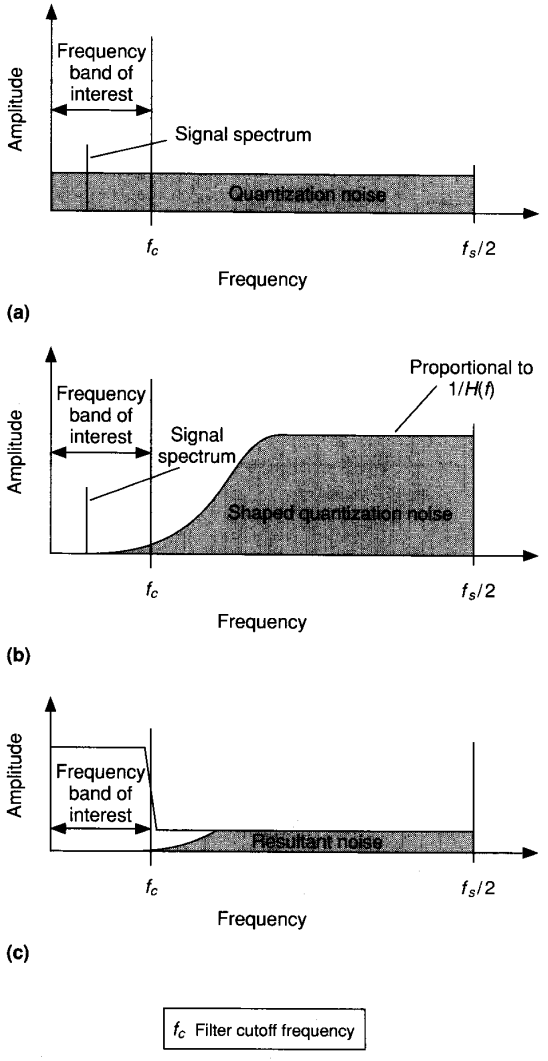

Figure 12. Noise-shaping in the frequency domain: noise distribution without shaping (a), with shaping (b), and resultant noise after filtering (c).

Applying algebraic rearrangement to place the y terms on the left of the equation yields

$$(1 + 1/f)\, y = x/f + q$$
$$y = x/(f+1) + qf/(f+1).$$

Note that at a frequency $f = 0$, the output equals x with no noise element q. At higher frequencies, the value of x is reduced and the value of q is increased. At a frequency $f = \infty$, the output equals only noise. The analog filter has a low-pass effect on the signal and a high-pass effect on the noise.

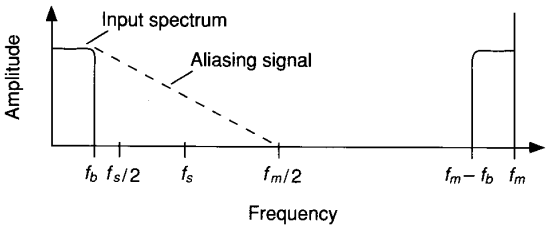

Figure 13. Aliasing in the signal bandwidth.

Because of this fact, one can think of the analog filter of the modulator as a noise-shaping filter (see Figures 12a and 12b) that reduces the effects of quantization noise in the frequency band of interest.

Filtering

After the noise has been shaped and pushed into the frequencies above the band of interest, digital filtering techniques minimize this shaped quantization noise as shown in Figures 12b and 12c. In addition to quantization noise removal, the digital filter reduces the sampling rate by decimation.

In an oversampled A/D converter, the unit samples the continuous input signal $x(t)$ at a frequency f_s and feeds it to a modulator that provides 1-bit quantization at the rate f_s. The digital output from the modulator then feeds into a decimation filter that computes a more "accurate" (less noisy) representation of the input signal at a reduced rate f_n. In essence, the A/D converter is filtering the digital signal from the output of the modulator and then digitally resampling it at a lower rate. The bandwidth of the input signal must be band-limited to a frequency less than one half of the sampling rate to avoid aliasing.

When this band-limiting is not properly performed, aliasing occurs. Aliasing transposes frequencies above the value $f_s/2$ into frequencies that fall below $f_s/2$. This transposition is symmetrical around $f_s/2$. For example, when $f_s/2$ equals 50 kHz, a 70-kHz input signal aliases to 30 kHz.

When the frequency value $f_s/2$ is well above the upper edge of the usable bandwidth, some aliasing can occur as long as the aliased frequencies do not fold back into the band of interest. Figure 13 shows that quite a large amount of aliasing can occur with no effect on the input signal within the signal band f_b.

The modulator sampling rate f_m places a limitation on the bandwidth of the input signal so it is less than $f_m/2$. Since the upper edge of the bandwidth of the

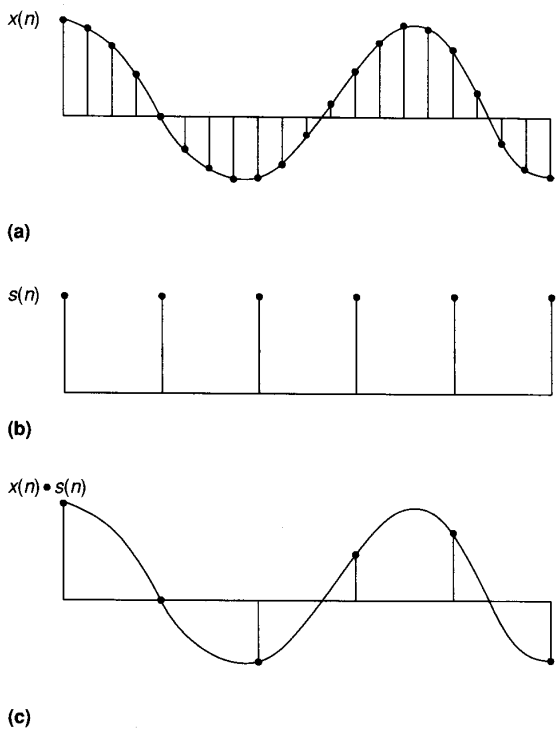

Figure 14. Reduced sampling rate: input signal with a sampling rate of W_s (a), decimation rate (b), and output waveform (c).

input signal is only f_b, aliased frequencies can fall in the region from f_b to $f_m / 2$ without affecting the signal range f_b. For example, a Sigma-Delta modulator sampling at 2 MHz with an input signal bandwidth of 4 kHz allows for input frequencies just over 1.9 MHz with no aliased frequencies corrupting the input signal. Consequently, most systems employing a Sigma-Delta A/D converter do not need an antialiasing filter in front of the converter, as with a traditional A/D converter.

However, when the A/D converter resamples the digital signal and further reduces the rate to f_s (the rate of data output by the last stage of the Sigma-Delta converter), it must properly band-limit the signal to $f_s / 2$. Before the digital signal is resampled, a digital antialiasing filter must process it to eliminate the frequencies that exist above $f_s / 2$.

A low-pass digital filter removes the noise produced by the aliasing, the noise-shaping process of the Sigma-Delta modulator, and the antialiasing before digital resampling can occur. The low-pass filter function can also combine with decimation.

In Figure 14, decimation reduces the sampling rate W_s of the input signal $x(n)$ by a factor of 4. The digital filter resamples this signal at the lower rate (the decimation rate) $s(n)$. The output produced is simply the multiplication of $x(n)$ and $s(n)$. This resampling process can combine with the low-pass filter functions as shown in Figure 15.

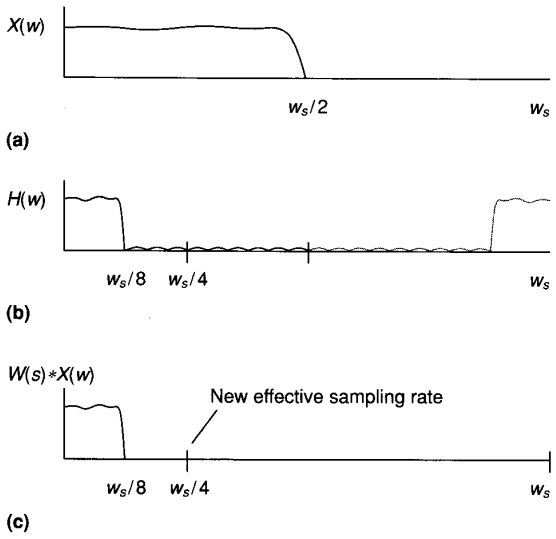

Figure 15. Resampling and low-pass filtering: spectrum of input waveform (a), transfer function of band-limiting filter (b), and spectrum of resultant output waveform (c).

$X(w)$ in Figure 15a represents the spectrum of the arbitrary waveform at the input of the decimation filter and is the spectrum of the signal coming out of the Sigma-Delta modulator. The reduction of the data rate by digital resampling requires proper band-limiting to one half the new sampling rate shown in Figure 15b by $H(w)$. This low-pass function also results in the elimination of higher frequency noise produced by aliasing in the modulator and the noise-shaping of the modulator. The spectrum of the resultant output waveform in Figure 15c is limited to one half the rate of the decimation filter, as shown by the convolution $W(s) * X(w)$. The filter transfer function can also be further modified to include system-level filtering such as rejection of very low frequencies. (For further discussion of filter design and trade-offs, including FIR (finite-length impulse response) versus IIR (infinite impulse response) filters, see Higgins.[2])

Integration

The combination of a Sigma-Delta converter with a complex signal processor offers many of the traditional advantages delivered by higher levels of integration. These advantages include an increased system reliability, a simplified design task, a reduced board space, re-

duced power requirements, and a reduced system cost.

One must weigh these benefits, though, against specific trade-offs associated with the selection of a Sigma-Delta converter. Before investigating application trade-offs, one must understand why Sigma-Delta converters facilitate integration with a DSP core.

We have understood the benefits of integrating both analog and digital circuitry on a one silicon substrate for years. However, the noise levels injected into the silicon substrate during digital switching have limited researchers' desire to integrate analog functions alongside complex, digital, very large scale integration processors.

Traditional converter technologies, such as those used in successive approximation converters and flash converters, consist mostly of analog circuitry. They require very high performance comparators with as much as a 16-bit accuracy.

The digital noise and the high-frequency digital clocks in current DSPs adversely affect these converters. In addition, we need significant silicon "real estate" to implement precision analog components. However, as stated, the Sigma-Delta method moves the precision to the digital realm and therefore reduces the analog design and implementation requirements.

The digital filters that follow the 1-bit conversion determine a significant portion of the performance achieved with Sigma-Delta converters. These converters use more digital circuitry per percentage of silicon area than alternate technologies. The analog section of these converters performs conversions to only 1 bit of accuracy, although with high linearity. Sigma-Delta converter technology is therefore compatible with a DSP manufacturing process that also produces capacitors with very good linearity properties.

Although the Sigma-Delta converter has advantages over the successive approximation or flash converter, system trade-offs exist. The decimation filters, for example, require many consecutive input samples to produce an output value. This stream of input values cannot be disrupted. In applications requiring many input channels (in which a front-end multiplexer would normally be used), the Sigma-Delta converter therefore cannot function in the conventional way. Figure 16 shows how multiplexing occurs for a conventional conversion system and for a Sigma-Delta system.

The conventional system consists of an antialiasing filter for each channel, with all channels routed to the inputs of a multiplexer. The output of the multiplexer proceeds to one A/D converter. This system requires only one A/D converter but uses an antialiasing filter for each channel. Each antialiasing filter can reach the complexity of an 8-pole filter. The Sigma-Delta conversion system, on the other hand, does not require the same level of antialiasing for each channel but does require a converter for each channel.

The system then multiplexes the digital outputs of the converters. This seemingly expensive limitation

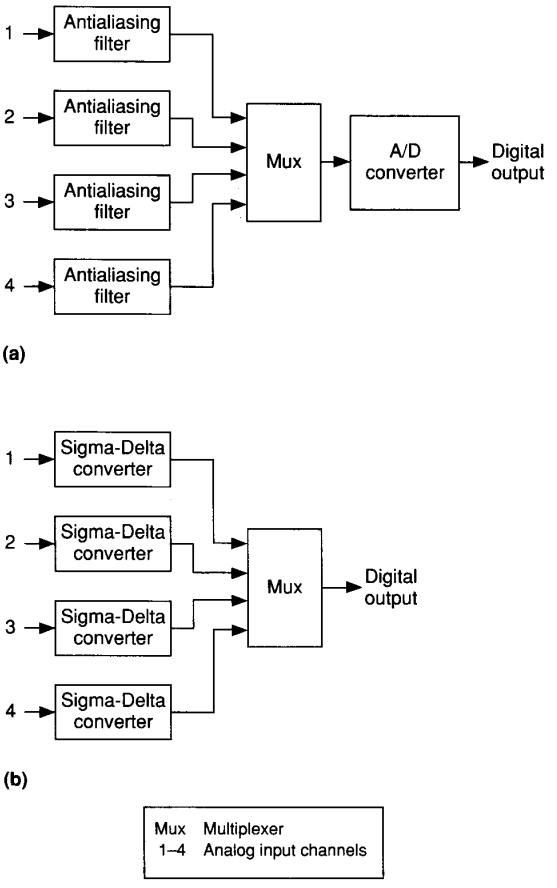

Figure 16. Multiplexed, front-end conversion: conventional system (a) and Sigma-Delta system (b).

can actually be more cost effective than the many high-performance antialiasing filters of the conventional system. The system multiplexes digital data instead of the analog signal, which can offer better performance in terms of less stray capacitance and channel-to-channel "feedthrough."

As shown in Figure 17 on the next page, the Analog Devices ADSP-21MSP50 integrates the A/D converter, the D/A converter, and the processor functions on one chip. (The converters appear here as modulators.) The 21MSP50 incorporates 2 Kwords × 24 bits of program-memory static RAM and 1 Kword × 16 bits of data-memory SRAM. The machine can access internal program memory twice per instruction cycle and supports one-cycle, dual-operand fetches from on-chip memory.

The 21MSP50 integrates a programmable 16-bit timer with an 8-bit prescaler for generating software

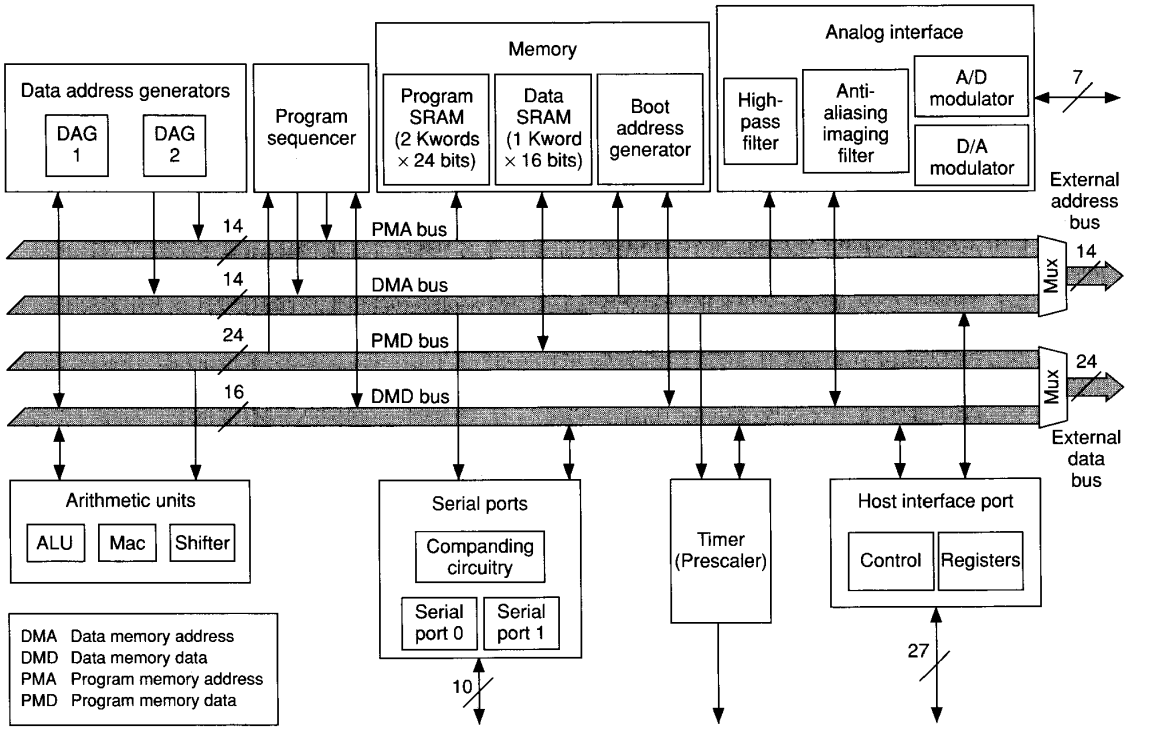

Figure 17. Block diagram of the ADSP-21MSP50 digital signal processor.

interrupts over a range of user-defined time bases. The system can read from or write to the timer, which makes the processor suitable for control tasks. A parallel host-interface port directly transfers 8-bit or 16-bit data to and from any standard host processor. Consequently, users can configure the 21MSP50 as a memory-mapped peripheral to a host microcomputer.

The 21MSP50 integrates Sigma-Delta A/D and D/A converters. These converters produce 8-kHz samples with a minimum of 65 decibels of signal-to-noise ratio. The converters are well suited for voice-band applications. Preprogrammed digital filters generate sampled results over voice-band frequencies only. A user can select a high-pass filter with software for a high-frequency cutoff between 300 Hz and 4 kHz.

Sigma-Delta technology best suits the integration of converters with complex digital signal processors. The fixed-function nature of the converters, however, limits the results. Users must work with the preprogrammed filter response as defined by the device filter architecture and implementation. User systems must also provide specific master-clock frequencies specified by the processors. These limitations restrict mixed- signal processors to application-specific environments. As the technology for these mixed-signal processors evolves, greater user programmability of the filter function will become necessary.

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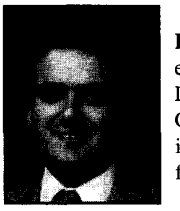

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