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Features

- Factors square or rectangular matrices from 3 to 64 rows and columns
- Fixed-point arithmetic for high-performance with up to 53 bits of precision
- Based on the triangular-orthogonal (QR) factorization of the input matrix
- Implementation based on Givens Rotations in conventional form using CORDIC rotations
- Includes reference MATLAB model and self-checking RTL testbench
- Core can be imported into Xilinx System Generator for DSP

Applications

- Kalman filtering
- Space-Time Adaptive Processing (STAP)
- Wireless signal processing
- Beamforming
- Software Defined Radio (SDR)
- Radar / Sonar
- Guidance, navigation and control
- Geo-/Astrophysical exploration
- Biomedical signal processing

Core Facts

Provided with Core	
Documentation	Users Guide
Design File Formats	VHDL
Constraints Files	NA
Verification	Testbench generated from MATLAB, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	NA
Additional Items	NA
Simulation Tools Used	
MATLAB (The MathWorks), ModelSim (Mentor Graphics)	
Support	
Provided by AccelChip Inc.	

Table 1: Core Implementation Statistics

Supported Family	Devices	Fmax (MHz)	Slices[1]	IOB[2]	Throughput	BRAM	MULT/ DSP48	Design Tools
Virtex-II Pro™	XC2VP30-7	96.1	1522	616	459 KSPS	0	8	ISE 6.3.03i
Virtex-4™	XC4VSX55-11	135.0	1521	616	645 KSPS	0	8	ISE 6.3.03i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

3) Fmax and throughput can be increased with greater use of device resources.

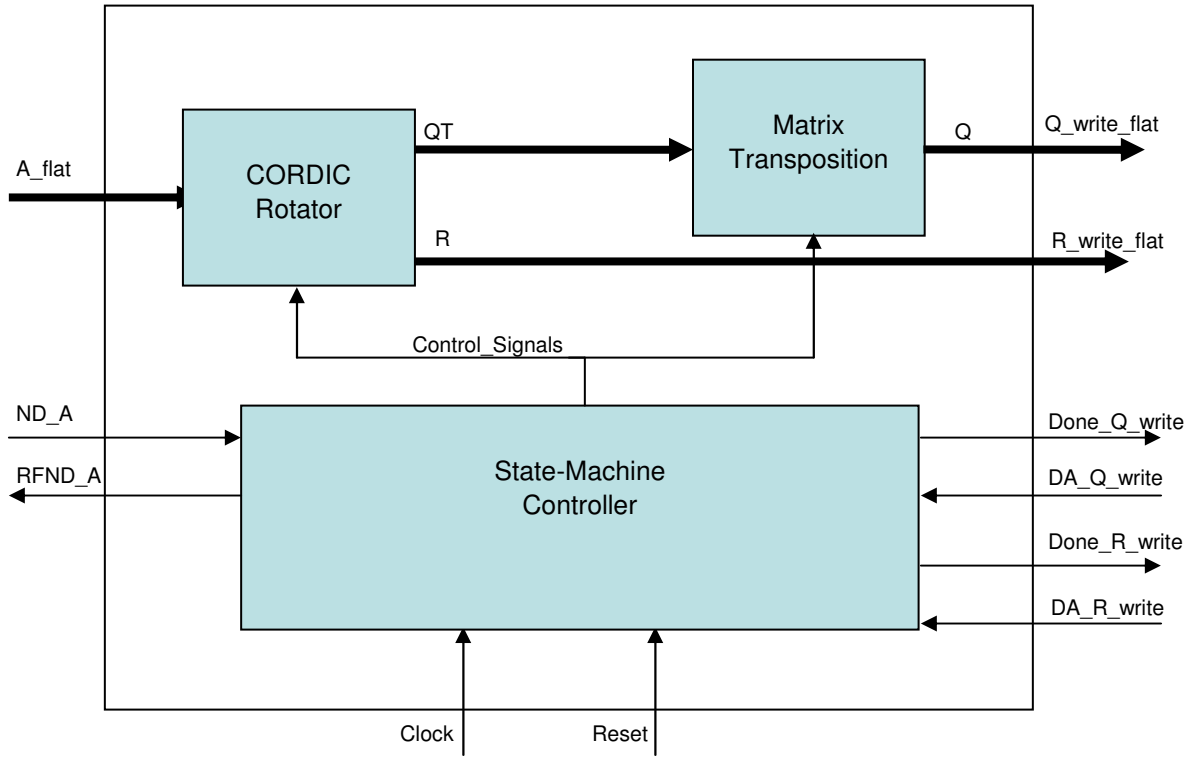

Figure 1: QR Matrix Factorization Core Block Diagram.

General Description

The QR Matrix Factorization core factors a real-valued, input matrix A into an upper triangular matrix R and a lower triangular matrix Q such that Q • R = A. (For applications where where an explicit matrix inverse is required, see the data sheet for the Matrix Inverse – QR method.)

Functional Description

The QR Matrix Factorization core uses an algorithm based on Givens Rotations (GR) to produce the triangular (R) and orthogonal (Q) factors. The Givens Rotations are implemented in their 'conventional' form using a COordinate Rotation DIgital Computer (CORDIC) for the vector rotations required to null elements below the diagonal and produce the upper triangular matrix R [for further information, see ***Advanced Digital Signal Processing***, John G. Proakis et al., Macmillan Publishing Company, New York, New York, 1992]. The resulting R and Q factors are then returned as outputs.

Core Modifications

There are two levels of core modifications possible with AccelCore IP. First, there are implementation parameters specific to each type of core – these parameters are listed in the table below. Additionally, AccelChip can perform further optimizations based on customer speed and area requirements, such as rolling/unrolling of algorithmic loops or parallel implementations of matrix operations.

Parameter Name	Parameter Description	Range
A quantizer	Input matrix quantization	2 to 24 bits
Implementation Algorithm	Algorithm used for factorization implementation	Conventional Givens rotation
Input Data Type	Input matrix data type	Real
Matrix Rows	Input matrix number of rows	Integer between 3 and 64
Matrix Columns	Input matrix number of columns	Integer between 3 and 64
Input/Output type	Input/output matrix dimension representation	1-D or 2-D
Rotation Angle Precision	Number of bits for Givens rotations angle computation	Integer between 4 and 24 – "auto" sets value to input matrix wordlength
Q Matrix Precision	Number of bits for Q matrix quantization	Integer between 4 and 24 – "auto" sets value based on input matrix wordlength
R Matrix Precision	Number of bits for R matrix quantization	Integer between 4 and 24 – "auto" sets value based on input matrix wordlength
Resource Sharing	Resource-shared implementation option	Yes / No

Input Matrix Quantization

The number representation of the input is defined by the input matrix quantization. The QR Matrix Factorization core accepts real-valued, fixed-point input data with quantization parameters defined by this quantization.

Implementation Algorithm

The implementation algorithm used for matrix factorization is based on conventional Givens Rotations with CORDIC.

Input Data Type

The input matrix must be real-valued.

Matrix Rows / Matrix Columns

The QR Matrix Factorization core can operate on a square or rectangular matrix. These two parameters set the number of rows and columns, respectively, of the input matrix.

Input/Output Data Type

The QR Matrix Factorization core can be generated to accept input and generate output matrices as 1-D or 2-D arrays.

Rotation Angle Precision

This parameter defines the precision, in number of bits, used in the calculation of the rotation angle in Givens Rotations.

Q Matrix Precision

This parameter defines the numerical precision of the inverse output matrix Q in terms of the number of bits and is automatically computed during the generation of the QR Matrix Factorization core. The output precision can be constrained as required.

R Matrix Precision

This parameter defines the numerical precision of the inverse output matrix R in terms of the number of bits and is automatically computed during the generation of the QR Matrix Factorization core. The output precision can be constrained as required.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock	Input	Clock Input
Reset	Input	Reset Input
A_flat	Input	Input matrix data
RFND_A	Output	Ready for new data
ND_A	Input	New input data valid
Q_write_flat	Output	Q Output matrix data
Done_Q_write	Output	Q Done indication
DA_Q_write	Input	Q Data accepted indication
R_write_flat	Output	R Output matrix data
Done_R_write	Output	R Done indication
DA_R_write	Input	R Data accepted indication

Core Assumptions

All implementations of matrix factorization can be sensitive to the condition number of the input matrix. This core is designed to operate on well-conditioned matrices, so the designer should take steps to ensure that that the input matrix is not ill-conditioned.

Verification Methods

The AccelCore QR Matrix Factorization core has a complete verification flow to ensure a bit-true implementation. The core is specfied using a fixed-point MATLAB model along with a set of stimulus and results. Based on the user's specifications, AccelChip produces an RTL model for the core, which is verified against the MATLAB model to ensure it is bit-true. AccelChip can also produce bit-true, cycle-accurate verification models for use with Simulink® from The MathWorks or Xilinx® System Generator for DSP.

Recommended Design Experience

The user should have some familiarity with linear algebra techniques and with HDL design methodologies.

Available Support Products

Customers may request that AccelChip provide versions of the AccelCore IP cores that can be imported into Xilinx System Generator for DSP. This allows the customer to verify the core using System Generator's system-level simulation facilities and libraries.

AccelChip Inc. uses proprietary algorithmic synthesis tools in the development of AccelCore IP cores. To obtain the AccelChip DSP Synthesis tool directly, contact your local AccelChip sales representative or send email to sales@accelchip.com.

Ordering Information

This product is available directly from AccelChip Inc. under the terms of the SignOnce IP License. The AccelCore QR Matrix Factorization core is available under the following AccelChip part numbers

AccelChip Part Number	Description
QRF08	AccelCore QR Matrix Factorization Core – up to 8x8 matrix
QRF16	AccelCore QR Matrix Factorization Core – up to 16x16 matrix
QRFXX	AccelCore QR Matrix Factorization Core – larger than 16x16 matrix

Please contact your local AccelChip sales representative or send email to sales@accelchip.com.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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