C29116A
16-bit Microprocessor Megafunction

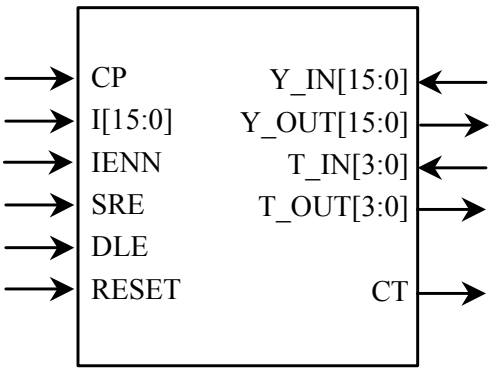
General Description

The C29116A is a microprogrammable 16-bit bipolar microprocessor megafunction whose architecture and instruction set is optimized for high-performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applications. In addition to its complete arithmetic and logic instruction set, the C29116A instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundance-check (CRC) generation.

Features

- 8 or 16 bit data width
- Powerful Field Insertion/Extraction and Bit Manipulation Instructions
  Rotate and Merge, Rotate and Compare, and Bit Manipulation Instructions provided for complex bit control.
- 32 Working 16 bit Registers
- 16 bit Barrel Shifter
- Immediate Instruction Capability
  May be used for storing constants in microcode or for configuring a second data port
- The C29116A is also available in VHDL or Verilog and synthesizes to approximately 3,800 gates (excluding RAM) depending on the process used
- Functionality based on the Advanced Micro Devices AM29116A

Symbol

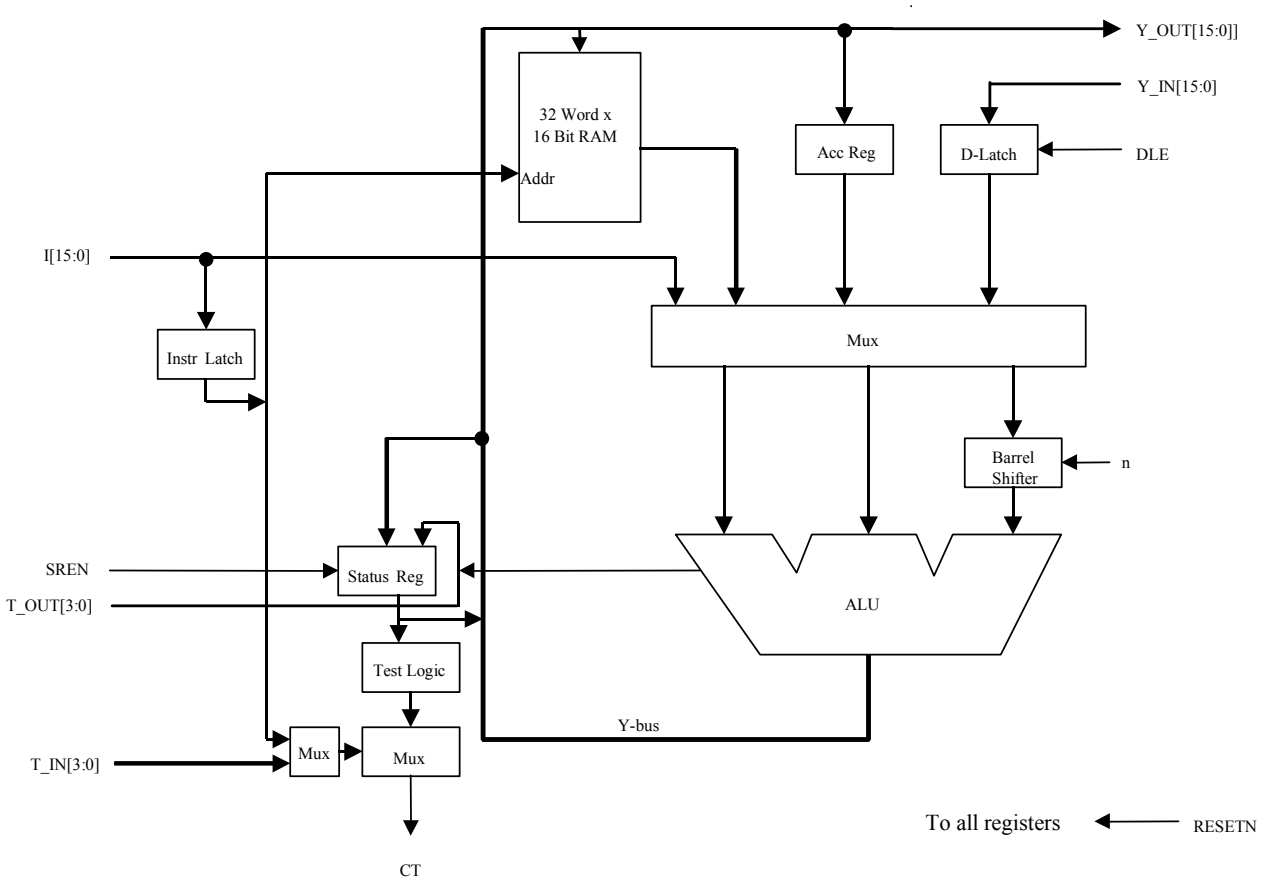


Pin Description

Name	Type	Polarity	Description
CP	In	Low/High/Rising *	Clock
RESETN	In	Low	Resets all registers
I	In	-	Instruction (or immediate data)
IENN	In	Low	Instruction Enable
SREN	In	Low	Status Register Enable
DLE	In	High	Data Latched Enable
Y_IN	In	-	Data Input Lines
Y_OUT	Out	-	Data Output Lines
T_IN	In	-	Conditional Test select inputs
T_OUT	Out	-	Status outputs
CT	Out	High	Conditional Test

* Ram latch is transparent when clock is high; Data is written to Ram when clock is low; Accumulator and Status registers are updated with rising clock.

Block Diagram



Functional Description

The C29116A megafunction is partitioned into modules as shown above and described below:

RAM

The 32-word by 16-bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock (CP) input is high and latched when the clock is low. Data is written into the RAM while the clock is low if the IENN input is also low and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into.

Accumulator

The 16-bit accumulator is an edge-triggered register. The accumulator accepts data on the low-to-high transition of the clock input if IENN input is low and if the instruction being executed defines the accumulator as the destination of the operation. For byte instructions, only the lower eight bits are written into; for word instructions, all 16 bits are written into.

Data Latch

The 1t-bit data latch holds the data input to the C29116A on the bi-directional Y bus. The latch is transparent when the DLE input is high and latched when the DLE input is low.

Barrel Shifter

The 16-bit barrel shifter is used as one of the ALU inputs. This permits rotating data from the RAM, the accumulator or the data latch up to 15 positions. In the word mode, the barrel shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

ALU

The C29116A contains a 16-bit ALU with full carry look-ahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two’s complement, add, subtract, AND, NAND, OR, NOR, XOR, and XNOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge, and rotate and compare with mask. All ALU operation can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the carry multiplexer which can select an input of zero, one, or the stored carry bit from the status register, QC. Using QS as the carry input allows execution of multi-precision addition and subtractions.

Priority Encoder

The priority encoder produces a binary-weighted code to indicate the locations of the highest order one at its input. The input to the priority encoder is generated by the ALU which performs

an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization.

Status Register

The status register holds the 8-bit status word. With the status register enable, SREN input low and the IENN input low, the status register is updated at the end of all instructions, except NO-OP. The lower four bits of the status register contain the ALU status bits of zero (Z), carry (C), negative (N), and overflow (O). The upper four bits contain a link bit and three user-definable status bits (Flag1, Flag2, and Flag3).

Instruction Latch and Decode

The 16-bit instruction latch is normally transparent to allow decoding of the instruction inputs by the instruction decoder into the internal control signals. All instructions except immediate instructions are executed in a single clock cycle.

Megafunction Assumptions

The C29116A was modeled with two single port rams with the following specifications:

Interface:

```
WENABLE : boolean; -- write enable
RamAddress : std_logic_vector(4 downto 0); -- address
datain : std_logic_vector(15 downto 0); -- data in
dataout : out std_logic_vector(15 downto 0) -- data out
```

Description:

- Single port ram
- 32 words, with 8 bits per word
- Transparent Write from datain when WENABLE is Low
- Transparent Read at all times to dataout

Device Utilization & Performance

Target Device	Speed Grade	Utilization		Performance	Availability
		LCs	EABs	F_{max}	
EPF10K30E	-1	1060	2	21 MHz	**Now**
EP1K30	-1	1002	2	17 MHz	**Now**

Deliverables

Encrypted Netlist License

- Post synthesis EDIF netlist
- Assignment & Configuration
- Symbol & Include files
- Testbench
- Vectors for testing the functionality of the megafunction
- Place & Route Scripts
- Documentation

VHDL Source License

- VHDL RTL source code
- Testbenches
- Vectors for testing functionality
- Expected results
- Synthesis scripts
- Simulation scripts
- Documentation

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