

Modifiable Coefficient, Single-Channel FIR Filters



Cascadable FIR Filters - Data Sheet



Executive Summary 8-tap, 8-bit Benchmark Results

Modules	FIR1 - Rate 1	FIR2 - Rate 4	FIR3 - Rate 8
Device	QuickDSP QL7180		
Speed Grade	-7 (Worst Case)		
Unbuffered Logic Cell Utilization	193 / 4,032	218 / 4,032	190 / 4,032
Buffered Logic Cell Utilization	198 / 4,032	234 / 4,032	216 / 4,032
ECU Utilization	8 / 18	2 / 18	1 / 18
Maximal Clock Frequency	84 MHz	67 MHz	68 MHz

Device Highlights

- High performance 8-Tap and 2-Tap cascadable FIR filter cores with QuickDSP ECU block
- Number of taps ranging from 8 to 128
- Two's complement input, output and coefficients
- Includes data clock and coefficient clock
- Input word length 8 or 12 bits
- Coefficient word length 8 or 12 bits
- Parameterised option of On-line programmable coefficients or on-the fly modifiable coefficient
- Support for cascading multiple cores to create a larger filter
- Parameterised data rate - 1, 4, 8 times clock rate
- Optimised for QuickLogic FPGA technologies

General Description

FIR (Finite Impulse Response) filters are one of the most basic building blocks used in digital signal processing. The output Y of an 8-tap FIR filter is given by the equation below..

[1]

$$Y_t = Y_0 + a_0 X_t + a_1 X_{t-1} + \dots + a_{N-2} X_{t-6} + a_{N-1} X_{t-7}$$

Here X is the input to the filter; Y0 is offset for the cascading purpose, and a0, a1... a7 are the filter's coefficients. The FIR filter represented by equation [1] is called a cascadable filter.

The FIR filter core is designed to perform the filtering function defined by equation [1] and can be used to create a filter for different data rate (**rate selection RS**) and two coefficient modification modes (coefficient (**A**) modification **selection AMS**). It is also designed to perform part of the filtering function and can be used to create a large filter whose number of taps is 8 times.

The core processes bit-parallel two's complement input data and the data rate can be selected by a parameter RS.



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I/O Descriptions

There are two generic parameters that specify the FIR filter cores, as listed in Table 1.

Name	Range	Description
RS	1, 4, 8	Data rate selection
AMS(RS = 1) only	0, 1	Coefficient modification mode 0: on line modification 1: on the fly modification
X	8 or 12	Data Bit Width
A0	8 or 12	Coefficient Bit Width

TABLE 1 : Generic parameters

Unless otherwise stated all signals are active high and bit (0) is the least significant bit.

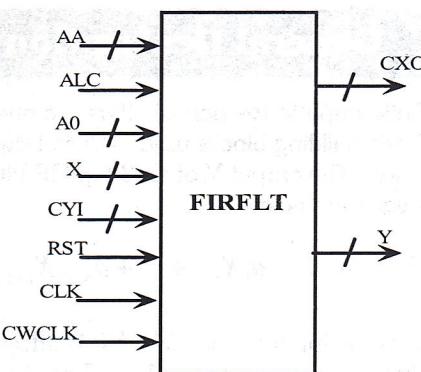


FIGURE 1: Symbol of FIR filter core (Rate 1)

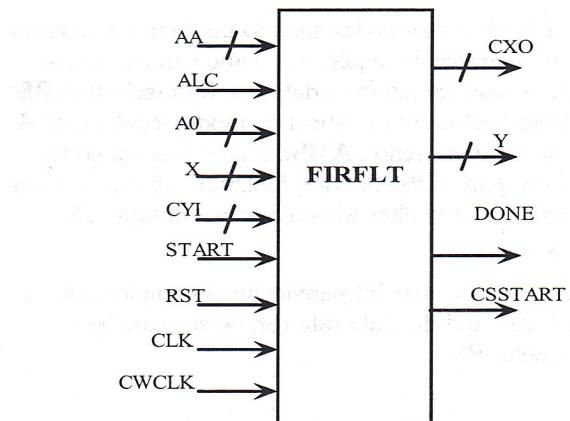


FIGURE 2: Symbol of FIR filter core (Rate 4 and Rate 8)

Pin	I/O	Width (Bits)	Description
RST	I	1	Global reset signal
CLK	I	1	Clock signal, rising edge active
CWCLK	I	1	Coefficient Write Clock signal, rising edge active
START	I	1	Input data indicator for data rate 4 and 8
CYI	I	21 ~ 31	Cascade Y input, connected to Y of the preceding core
X	I	8 or 12	Input data to the filter core, in two's complement format
A0, A1, etc.	I	8 or 12	Filter coefficient data, in two's complement format
ALC	I	1	Filter coefficient loading control, active HIGH, indicating that the coefficient data on port A should be loaded to the location addressed by AA
AA	I	3 ~ 7	Filter coefficient address, in unsigned binary format with the value indicating the subscript of the coefficient data on port A
CXO	O	8 or 12	Cascade X output, connected to X of the successive core
Y	O	21 ~ 31	Output data from the filter core, in two's complement format
DONE	O	1	Output data flag for data rate 4 and 8. Result is only valid when DONE = 1
CSSTART	O	1	Output START signal for cascaded filters

TABLE 2 : I/O Descriptions

Functional Description

Coefficient Loading

In on-line mode, the filter coefficients are loaded serially through port A0 under the control of signal AA and ALC, with AA indicating the address of the coefficient being loaded and ALC indicating that loading should be performed.

In on-the-fly mode (Rate 1 only), the filter coefficients are loaded into the core through ports A0 to A7 under the control of signal ALC.

The coefficients are in two's complement format and can be either 8 or 12 bits depending upon the FIR chosen.

Data Loading

Two's complement format is used for the data inputs for the filter and can be either 8 or 12 bits depending upon the FIR chosen.

For Rate 4 and Rate 8 filters the input data is only valid when START is high. All other inputs will be ignored. For a Rate 4 FIR data should be loaded every 4 clock cycles and for a Rate 8 FIR data should be loaded every 8 clock cycles.

Filter Outputs

The filter outputs are in two's complement format and they maintain full precision throughout the processing (i.e. no bits are rounded off and there are no overflows).

For Rate 4 and Rate 8 filters the outputs are only valid when DONE is high. All other outputs should be ignored. For a Rate 4 FIR the DONE signal will be high every 4 clock cycles and for a Rate 8 FIR the DONE signal will be high every 8 clock cycles.

Rate 4 and Rate 8 filters also have a CSSTART output, which is connected to the START input of another FIR if the FIR's are cascaded.

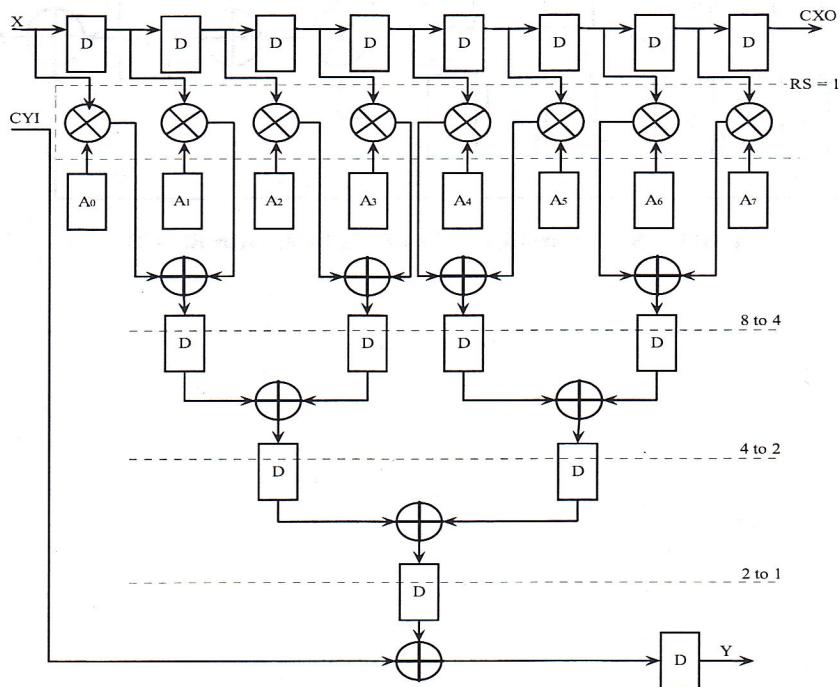


FIGURE 3: The architecture of FIR filter with RS = 1

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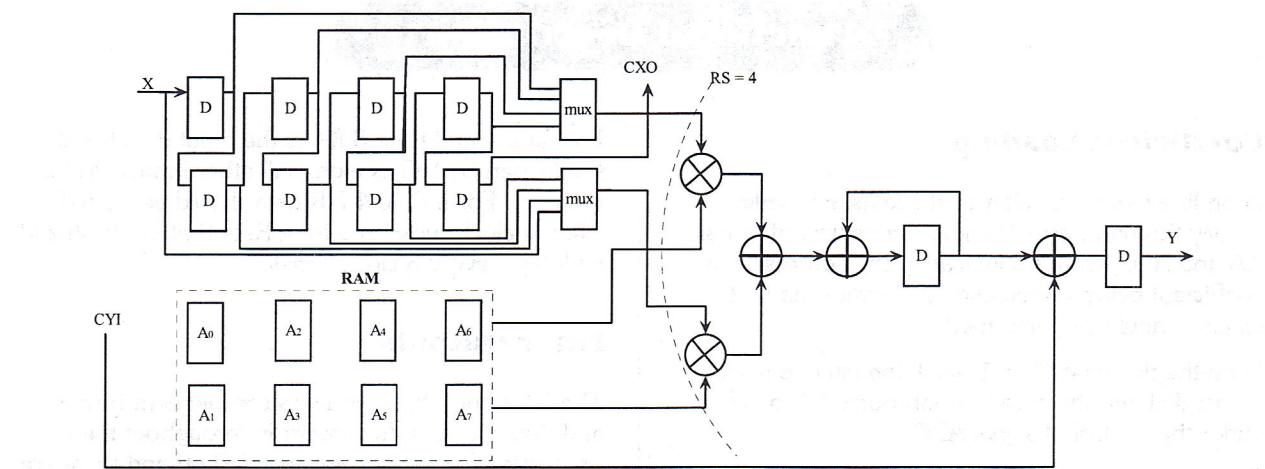


FIGURE 4: The architecture of FIR filter with RS = 4

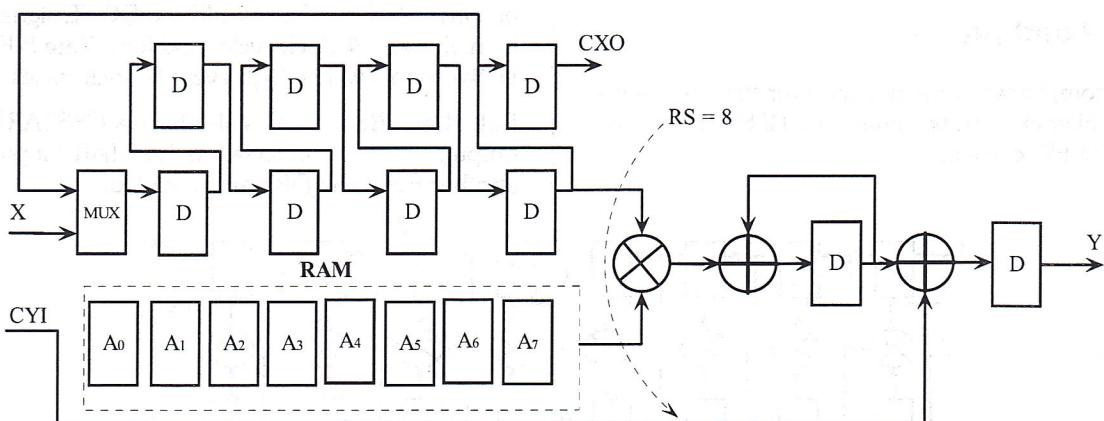


FIGURE 5: The architecture of FIR filter with RS = 8

When AMS = 1 and RS = 1, the filter core works under on-the fly mode, which means that all the coefficients are updated at the same time. Figure 6 shows the on-the-fly modification architecture of the FIR filter.

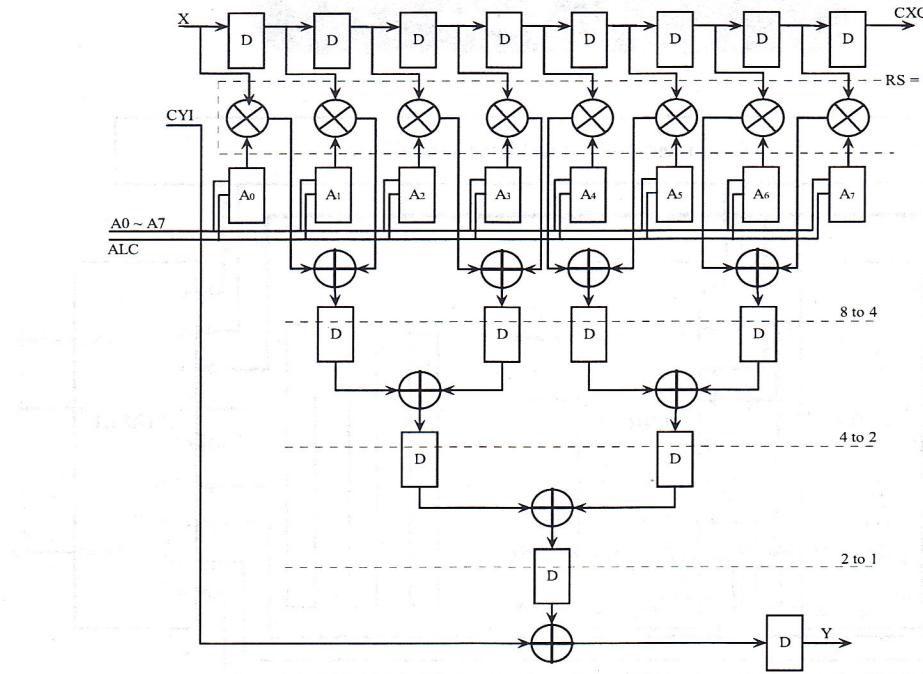


FIGURE 6: The architecture of FIR filter with RS = 1 and AMS = 1

Cascading Multiple FIR Filter Cores

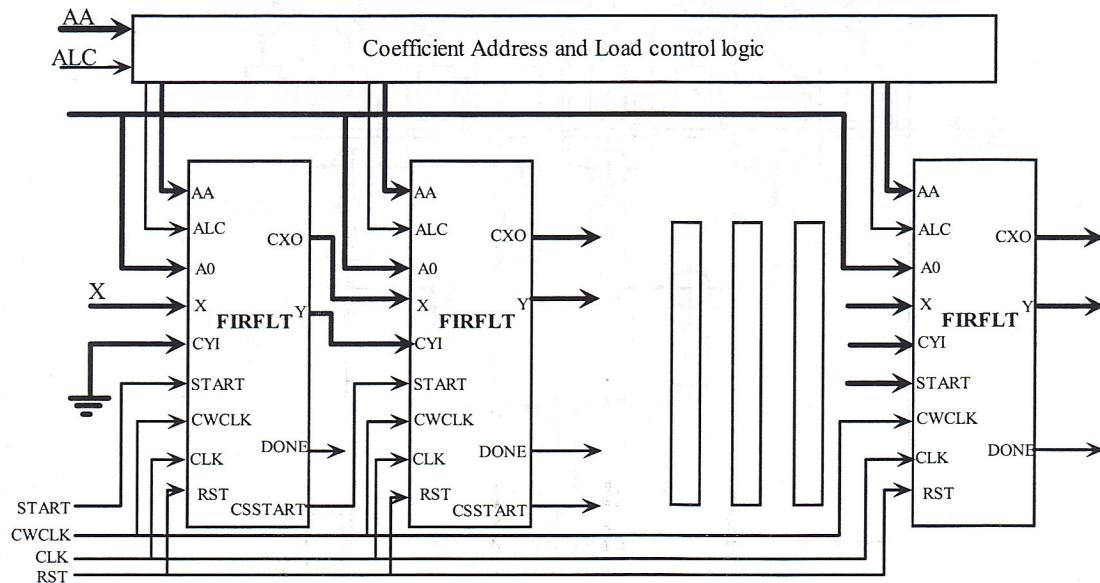


FIGURE 7: Cascading Multiple FIR Filters

Multiple FIR filter cores may be cascaded together to build filters with large numbers of taps, as shown in Figure 7. There is no requirement for additional logic on the data path of the cascaded cores. A small portion of control logic is needed to generate the coefficient loading address and control signals for each of the cascaded cores.

Note: Rate 1 FIR Filters do not have the START input port, or the DONE and CSSTART output ports.

The coefficient address AA and loading control signal ALC of the cascaded cores are obtained by decoding the address AA and loading control ALC of the large filter. For example, when four FIR filter cores, each having eight taps, are used to create a 32-tap filter, the address of the large filter has 5 bits. Let AA_i and ALC_i be the address and loading control signal of the cascaded cores, where i = 0, 1, 2, 3, then the

address and loading control logic can be expressed in Verilog as:

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Wire [2:0] AA0 = AA[2 :0];
Wire [2:0] AA1 = AA[2 :0];
Wire [2:0] AA2 = AA[2 :0];
Wire [2:0] AA3 = AA[2 :0];
Wire ALC0 = !(AA[4]) & !(AA[3]) & ALC;
Wire ALC1 = !(AA[4]) & AA[3] & ALC;
Wire ALC2 = AA[4] & !(AA[3]) & ALC;
Wire ALC3 = AA[4] & AA[3] & ALC;
```

Notes on Cascading FIR Filters:

Rate 1 FIR's

Rate 1 FIR's are 2-tap and 8-tap cascadable
(range from 8 taps to a maximum of 18)

The output port for 8-bit FIR's is 21 bits

The output port for 12-bit FIR's is 29 bits

Rate 4 FIR's

Rate 4 FIR's are 8-tap cascadable
(maximum of 64 taps)

The output port for 8-bit FIR's is 22 bits

The output port for 12-bit FIR's is 30 bits

Rate 8 FIR's

Rate 8 FIR's are 8-tap cascadable
(maximum of 128 taps)

The output port for 8-bit FIR's is 23 bits

The output port for 12-bit FIR's is 31 bits

Timing Diagrams

It should be noted that the following timing diagrams provide only the functional timing for the FIR filter operation, since the actual timing depends on the target implementation technology. These details can be provided upon request.

The FIR filter cores are a synchronous design with all the flip-flops being triggered at the rising edge of the clock signal CLK. The functional timing diagrams are shown in following figures.

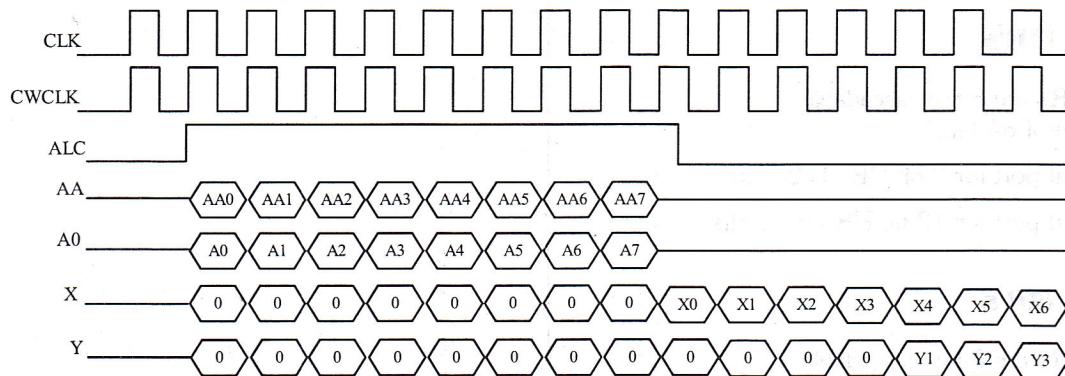


FIGURE 8: The Timing Diagram of FIR filter with RS = 1 and on line coefficient modification

The X signal in figure 7 is the input and the output 4 clock cycles later is Y. The first Y output is during the fifth clock cycle since there are 4 pipeline delays in the FIR filter for data selection rate (RS) 1.

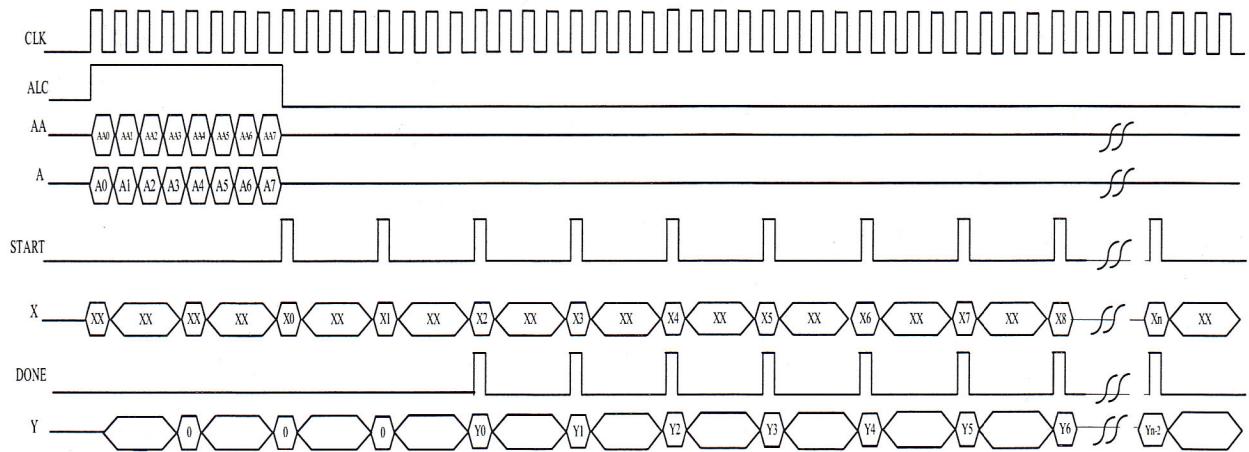


FIGURE 9: The Timing Diagram of FIR filter with RS = 4 and on line coefficient modification

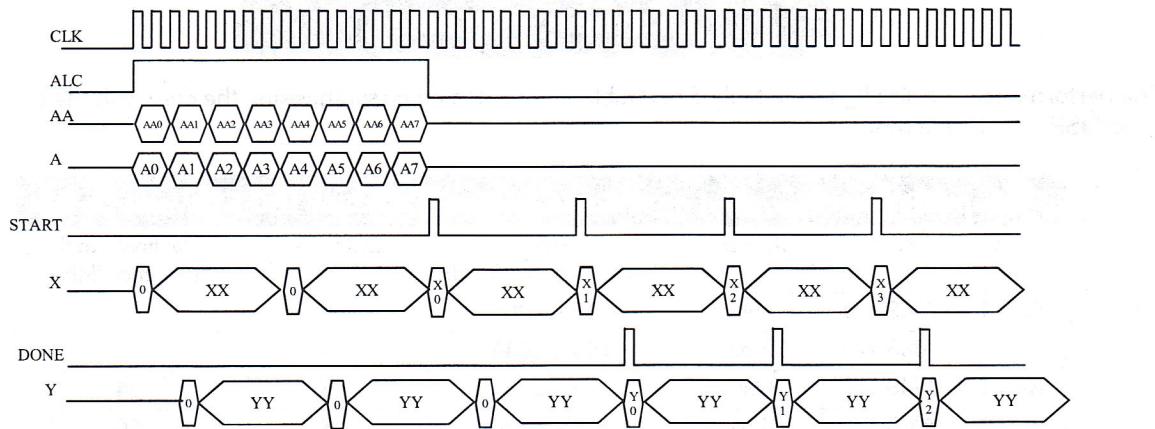


FIGURE 10: The Timing Diagram of FIR filter with RS = 8 and on line coefficient modification

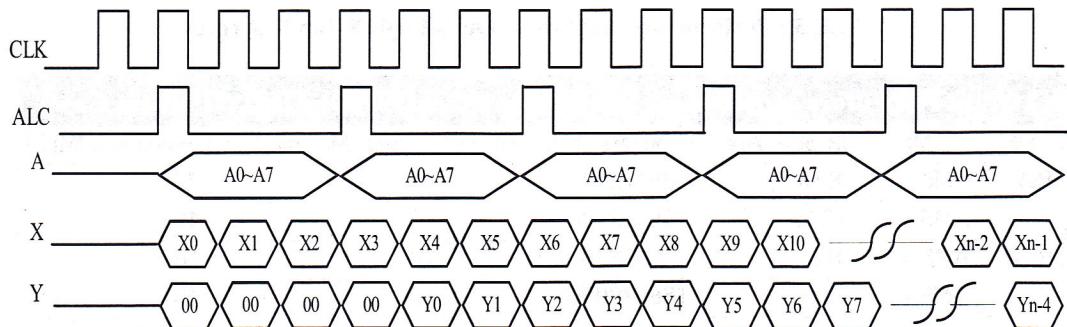


FIGURE 11: The Timing Diagram of FIR filter with RS = 1 and on the fly coefficient modification

Example Metrics

The performance and size figures in table 3 and table 4 are obtained by synthesising the core with the QuickLogic QuickDSP QL7180 library.

8 Tap FIR Filters targeted on QuickLogic QuickDSP QL7180 (-7 Worst Case)					
FIR	AMS	FIR Size	Area (no buffers /buffered)	ECU's used	Maximal Clock Frequency (MHz)
Rate 1	AMS = 0	8 bit	193/198	8	84
	AMS = 0	12 bit	1482/1644	8	49
Rate 1	AMS = 1	8 bit	187/205	8	84
	AMS = 1	12 bit	1483/1720	8	46
Rate 4	N/A	8 bit	218/234	2	67
	N/A	12 bit	536/648	2	45
Rate 8	N/A	8 bit	190/216	1	68
	N/A	12 bit	298/498	1	48

TABLE 3 : Performance and Size of QuickLogic 8-Tap FIR cores

10 Tap FIR Filters targeted on QuickLogic QuickDSP QL7180 (-7 Worst Case)					
FIR	AMS	FIR Size	Area (no buffers /buffered)	ECU's used	Maximal Clock Frequency (MHz)
Rate 1	AMS = 0	8 bit	281/297	10	77
	AMS = 0	12 bit	1866/2106	10	45
Rate 1	AMS = 1	8 bit	285/296	10	76
	AMS = 1	12 bit	1868/2096	10	48

TABLE 4 : Performance and Size of QuickLogic 10-Tap FIR cores

The 2-Tap 8-bit FIR Filters (Rate 1 only) use approximately 100 logic cells.

The 2-Tap 12-bit FIR Filters (Rate 1 only) use approximately 400 logic cells.

Support Contact Details**QuickLogic Corp.**

1277 Orleans Dr.
Sunnyvale, CA 94089
USA

Tel:408-990-4100

Fax:408-990-4040

Email:support@quicklogic.com

URL: <http://www.quicklogic.com>