SESSION II: HIGH SPEED MICROPROCESSORS

WAM 2.5: A NMOS LSI 16x16 Multiplier

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A 1.5μ NMOS 16x16 PARALLEL MULTIPLIER designed for a throughput time of less than 40ns will be described. Preliminary measurements suggest a best-case throughput time of 16ns. The pipelined architecture of the multiplier (Figure 1) gives a throughput time of one clock cycle and a total multiply time of two clock cycles. The chip draws 1W at 4V, has 7500 transistors, and dimensions of 2800μ x 2500μ. It was designed to accept and deliver TTL logic levels. A photograph of the chip appears in Figure 2.

This chip was fabricated in an advanced NMOS process[1-2] with 1.5μ design rules. X-ray lithography was used on all levels. A layer of tantalum silicide was deposited on the polysilicon to reduce the sheet resistance to 2.5$\Omega/\square$, affording maximum poly runner delays of about 3ns.

The chip performs the multiplication of two 16bit 2's complement binary numbers with a modified Booth's algorithm. The multiplier x and the multiplicand y are clocked into two input registers, each consisting of 16 master-slave flip-flops: Figure 1. Next, they are processed by a recoder circuit that views the multiplier as a radix-4 number with coefficients 0, 1, 2, -1, and -2. This recoding reduces the number of adder stages in a column of the carry-save adder tree by one-half relative to a fully parallel approach, and another reduction of one-half is obtained by using a modified Wallace scheme; as a result, the maximum number of adders encountered through any path of the adder tree is just four. Additional speed is obtained by using a carry-lookahead adder to assimilate carries. The master-slave pipeline register is placed halfway through the carry-save adder tree. The 31bit 2's complement output is multiplexed to a 16-cell output register to reduce pinout. Eventually, the multiplier will be used as a major subcircuit of a larger chip; the multiplexer will then be eliminated.

Proper functionality of the chip was verified by running a static test consisting of over 5000 test vectors. These give more than 99% single stuck-at fault coverage. The chip was tested dynamically on a probe station by feeding the sign bit of the output back to the sign bit of the y input, and setting $x = -1$ and $y = 1$ (except for the sign bit of y). In this configuration, the circuit acts as a divide-by-three counter, and providing a test of a signal path that consists of 14 gate delays in the circuitry following the pipeline register; Figure 1). The shortest clock period at which this circuit could be clocked was 12.5ns; Figure 3. There is a signal delay of about 5ns through the master-slave latches due to the requirement of non-overlapping master and slave clock waveforms; thus, the 14 gates have a total delay of 12.5ns–5ns = 7.5ns. This gives an average gate delay of about 0.5ns per gate. The longest logic path through which a signal has to propagate in one clock cycle is 21 gates, so it is estimated that the throughput time for this particular chip will be (21 x 0.5 + 5)ns $\approx$ 16ns.

To obtain optimum performance, the chip layout was carefully hand-packed using a computer-aided layout system. Parasitic fringing capacitances for various structures were calculated with a two-dimensional numerical solution of the field equations; the parasitic nodal capacitances were then extracted directly from the encoded layout information using an automatic layout analysis program. These values were used to equalize the delay times through the critical paths of the circuit.

Acknowledgments

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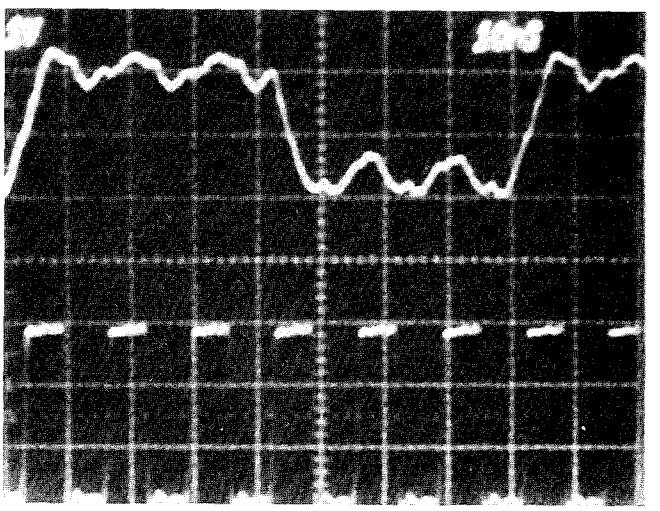

FIGURE 3—Waveforms from the dynamic test of the multiplier. The feedback sign bit is shown on top, and the external clock is shown on the bottom.

[1] Kushner, R.A., "A One-Micron NMOS Technology with High Conduction Gates," *Semicon/West '82 Technical Program Proceedings,* May 26-28; 1982.

[2] Fraser, D.L., Jr., Boll, H.J., Bayruns, R.J., Wittwer, N.C., and Fuls, E.N., "Gigabit Logic Circuits with Scaled nMOS," *ESSCIRC Digest of Technical Papers,* p. 202-204; Sept., 1981

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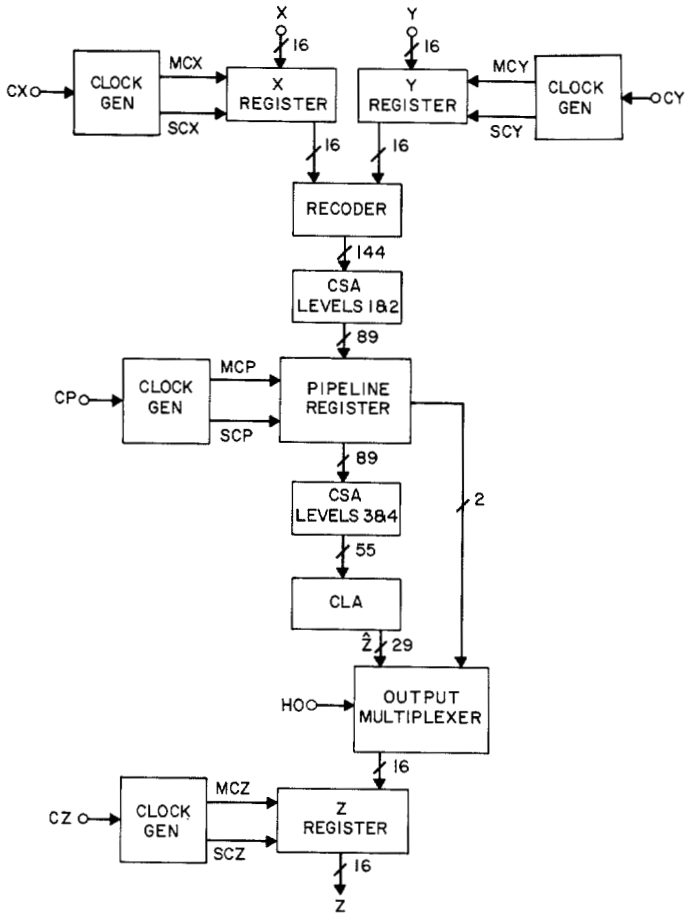

FIGURE 1—Block diagram of the 16 x 16 multiplier.

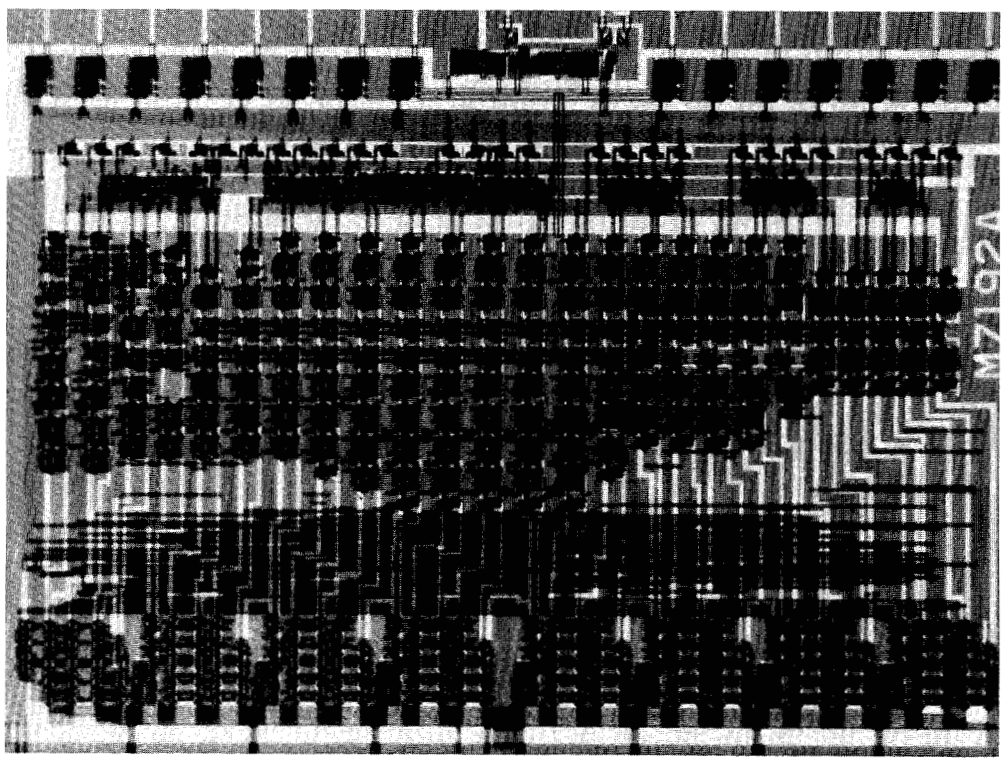

FIGURE 2—Photograph of the multiplier chip.