SESSION III: SPECIAL APPLICATION MEMORIES

WAM 3.3: An 8Kb Content-Addressable and Reentrant Memory

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MEMORY DEVICES providing several functions in addition to that of merely storing the data (functional memories) are not frequently encountered, because their bit-density is poor and they are not as general-purpose as conventional memories. This paper proposes a functional memory and Content-Addressable and Reentrant Memory (CARM) that minimizes these drawbacks by adopting a small-size associative memory cell and a PLA for easy programming of the various functions.

The primary application of this memory is as a high-speed matching unit in the dynamic data-flow computer[1], where the following functions are required: (*1*) the incoming data are associatively checked with the stored data in the memory (search for partner); (*2*) if a match occurs, the stored data (the partner) are extracted. Otherwise the incoming data are stored. In case of matching, the vacant memory site should be stuffed (garbage-collection) soon after the extraction, so that the used memory area would be consecutive at any time. These functions are realized in the CARM as reentrant mode operations.

The block diagram of the device is shown in Figure 1. Four phase internal clock pulses are distributed to each block for synchronous operation. The maximum clock rate is 10MHz, typically. The memory size is 256 word x 32b, and the width of internal buses (bidirectional) are 32b for data and 8b for address.

The circuit diagram of the cell is shown in Figure 2. It consists of a conventional static RAM cell (6 transistors), exclusive NOR (4 transistors) and one horizontal sense line. The cell size is 30 x 36μ^2. Each sense line has a matching sense amplifier (MSA) at its horizontal edge. Associative operation is accomplished by applying complementary voltages to the bit lines as is the case with the write-operation in SRAMs, but no word line is accessed and the sense lines are precharged to the high level. If a match occurs between the reference data on the bit lines and the stored data in the memory cells, the voltage of the sense line stays at the high level, otherwise it is discharged to the low level. The response of this transition is less then 25ns.

A Sequential Address Encoder (SAE) generates the sequential address outputs of the matched words according to their priority. The SAE has a hierachical structure of three levels: section, group and cell. Eight cells make a group, eight groups make a section and four sections make the SAE block. The propagation of INHIBIT signal plays an important role in this structure. It is generated at the matched word and inhibits the address-encoding at the words of lower priority. After the address output, the INHIBIT of that word is cleared. The circuit diagram of the SAE cell is shown in Figure 3. This is the Manchester-chain type circuit. On the other hand, look-ahead type circuits are placed at each group and each section. The total propagation time of INHIBIT signal is less then 15ns. Typical waveforms of I/O pulses in a matching operation are shown in Figure 4.

The delayed-write technique for Reentrant operations is another feature. Reentrant operation is a conditional one, and an instantaneous on-chip garbage collection is accomplished. In the Reentrant CAM mode, for example, if a match occurs at the address X, then X is outputed to the address bus. If the data are at the pointer (N−1) which has been pre-decremented, is read out, it is written into the address X. If a match doesn't occur, the reference data are written into the word at the pointer (N) which is post-incremented. The pointer always indicates the boundary of the free storage area in the chip. In the former case, two-cycle execution is possible, if both the reading-out and the writing-in are executed in one machine cycle. This is realized by the delayed-write technique where the two words are accessed in one cycle sequentially. The second word is accessed 25ns (△) after the first access, and the data of the first word are copied to the second word. The timing diagram is illustrated in Figure 5.

The device was fabricated by the 2μ CMOS process. Because both the vertical (bit) lines and horizontal (sense or word) lines in the associative memory cells should be low resistive, a double layer metalization structure is indispensable. The etch-back technology permits fine patterning of the double layer metalization. The CARM chip has 99,000-transistors on a die area of 4.8 x 7.1mm^2. Several LSI characteristics are summarized in Table 1.

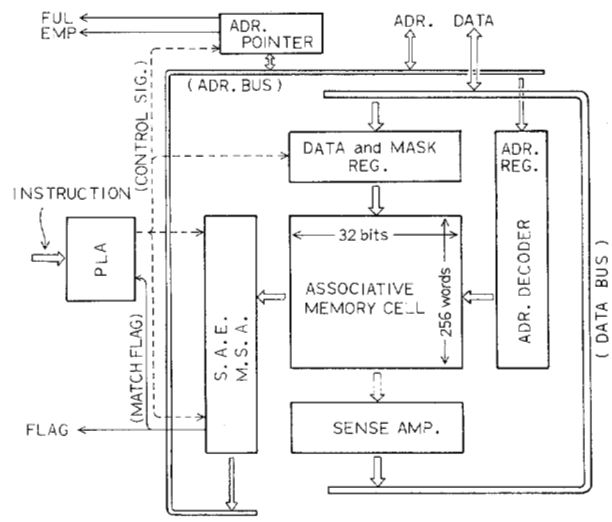

FIGURE 1—Block diagram of the CARM.

[1] e.g. Watson, I. and Gurd, J., "A Practical Data Flow Computer", *IEEE Computer*, Vol. 15, No. 2, p. 51-57; Feb., 1982.

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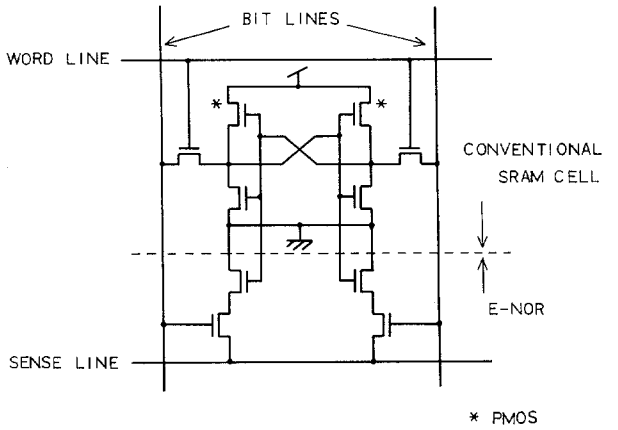

FIGURE 2—Circuit diagram of associative memory cell.

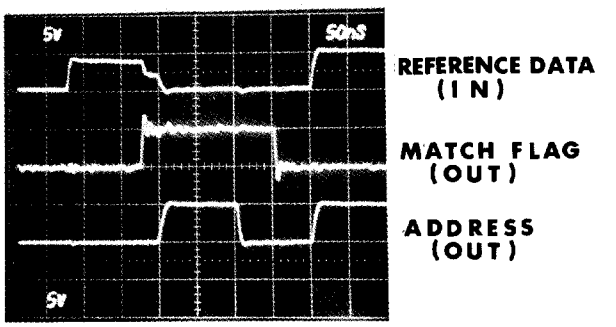

FIGURE 4—I/O pulse waveforms in the matching operation. Matches occur at two words.

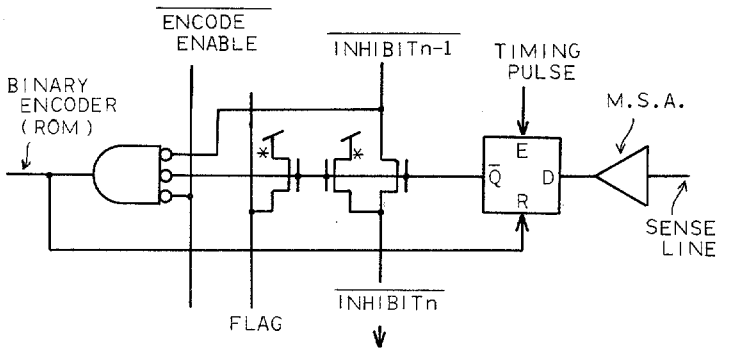

FIGURE 3—Circuit diagram of the SAE cell.

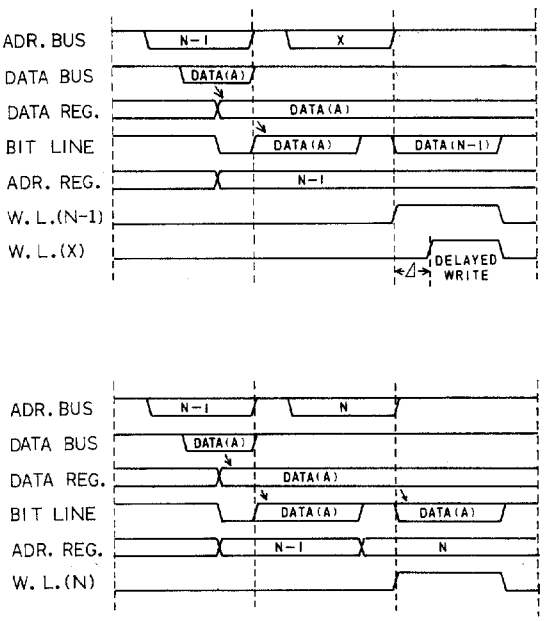

FIGURE 5—Timing diagram of Reentrant CAM Mode (*a*) match occurs; (*b*) match doesn't occur.

Memory structure	256w x 32b
Number of instructions	12
Cycle time	100ns
Supply voltage	5V
Power dissipation	500mW (10MHz)
Number of devices	99,000
Die size	4.8 x 7.1mm
Process technology	2μ CMOS 2-layer metal

TABLE 1—Characteristics of the CARM.