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Isn't It Time You Got Faster, Quicker?

AltiVec™ Technology
At-a-Glance

OVERVIEW

Motorola's advanced AltiVec™ technology is designed to enable host processors compatible with the PowerPC instruction-set architecture (ISA) to perform with significantly more general-purpose processing power. At the same time, this leading-edge technology is engineered to support high bandwidth data processing and algorithmic-intensive computations, all in a single chip solution. With its ease-of-use software environment, AltiVec technology is engineered to bring exceptional power to applications such as telecom switches, IP telephony gateways, speech processing systems, image and video processing systems, virtual private network servers, high-resolution 3-D graphics and more.

AltiVec technology has proven itself to be a leader in enabling high performance: Motorola's MPC7455 was named 2001 Embedded Processor of the Year by In-Stat MDR, and according to the EEMBC®, a consortium of semiconductor, compiler and RTOS vendors, the MPC7455 has the highest certified performance rating of any microprocessor in production the consortium has ever published.

AltiVec technology offers a programmable solution designed to easily migrate via software upgrades to follow changing standards and customer requirements. The bottom line? With AltiVec technology and host processors compatible with the PowerPC ISA, your technology investment is protected well into the future.

MICROPROCESSOR REPORT ANALYSTS' CHOICE
Best High-Performance Embedded Processor Chip
MPC7455

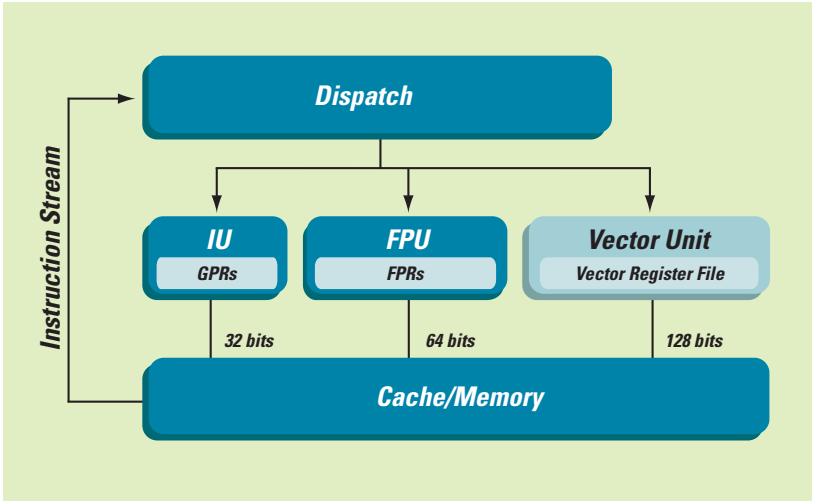
This at-a-glance guide to AltiVec technology is designed to give you the information you need to make the right choices about processors and performance. This guide includes a roadmap, features and benefits, benchmarks and URLs to help you find more information.

AltiVec technology has proven itself to be a leader in enabling high performance.

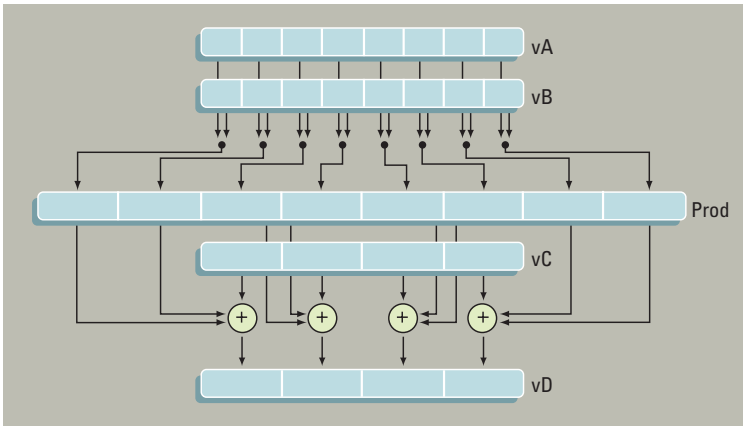
THE SOLUTION FOR EMBEDDED COMPUTING CHALLENGES

With its high performance and ease-of-use software environment, AltiVec technology offers a single-chip solution to many common embedded computing challenges. AltiVec technology enables:

- High-bandwidth data communications
- Packet data processing
- Image and video processing
- Access concentrators/DSLAMs
  - ADSL and digital data concentrators
- Speech recognition
- Voice/sound processing
- Array numeric processing
- Basestation processing
- Real-time continuous speech I/O
  - HMM, Viterbi acceleration, neural algorithms
- 3-D graphics
  - Games, entertainment
  - High-precision CAD
- Virtual reality
- Motion video
  - MPEG2, MPEG4
  - H.234
- High-fidelity audio
  - 3-D audio, AC-3, MP3
- Machine intelligence



ALTIVEC EXECUTION OF MULTIPLY-ACCUMULATE



ALTIVEC TECHNOLOGY'S VECTOR EXECUTION UNIT

- Vector execution unit is concurrent with integer and floating point units (FPUs)
- 32 separate, dedicated 128-bit vector registers
  - Large namespace for low register pressure/spillage
  - Long vector length enables more data-level parallelism
  - Separate files are accessible by execution units in parallel
  - Deep register files allow for sophisticated software optimizations
- No penalty for mingling integer, FPU and AltiVec technology operations

ALTIVEC TECHNOLOGY FEATURES AND BENEFITS

ALTIVEC TECHNOLOGY BENEFITS

- Designed to provide a single, high-performance RISC microprocessor with DSP-like computing power for controller and signal processing functions
  - Supplements performance-leading host processors compatible with the PowerPC ISA with an advanced, best-in-class execution unit
  - Vector processing engine designed to provide for highly parallel operations, which can allow for the simultaneous execution of up to 16 operations in a single clock cycle
  - Designed to accelerate many traditional computing and embedded processing operations with its wide data paths and field operations
- Designed to provide product designers and customers with an innovative "one part/one code" integrated approach engineered to converge system control functionality with specialized functionality typically resident on off-chip devices
- Offers a programmable solution designed to easily migrate via software upgrades to follow changing standards and customer requirements
  - Simplifies design and support—programmable in flexible extensions to C language
  - Designed to allow customers to leverage PowerPC compatibility and legacy code, and add AltiVec performance as they need it

ALTIVEC TECHNOLOGY FEATURES

- SIMD functionality for embedded applications with massive data processing needs
- Key features:
  - 128-bit vector execution unit with 32-entry, 128-bit register file
  - Parallel processing with vector permute unit and vector arithmetic logical unit
  - 162 additional instructions
  - Advanced data types such as packed byte, halfword and word integers, and packed IEEE single-precision floats
  - Saturation arithmetic
- Simplified architecture
  - Virtually no interrupts other than data storage interrupt on loads and stores
  - Allows hardware unaligned access support
  - Virtually no penalty for running AltiVec and standard PowerPC instructions simultaneously
  - Streamlined architecture to facilitate efficient implementation
- Maintains PowerPC ISA's RISC register-to-register programming model
- Supports parallel operation on byte, halfword, word and 128-bit operands
  - Intra and inter-element arithmetic instructions
  - Intra and inter-element conditional instructions
  - Powerful permute, shift and rotate instructions
- Vector integer and floating-point arithmetic
  - Data types
    - 8-, 16- and 32-bit signed and unsigned integer data types
    - 32-bit IEEE single-precision floating-point data type
    - 8-, 16- and 32-bit Boolean data types (e.g., OxFFFF= 16-bit TRUE)
  - Modulo and saturation integer arithmetic
  - 32-bit "IEEE-default" single-precision floating point arithmetic
    - IEEE-default exception handling
    - IEEE-default "round-to-nearest"
    - Fast non-IEEE mode (e.g., denorms flushed to zero)
- Control flow with highly flexible bit manipulation engine
  - Compare creates field mask used by select function
  - Compare RC bit enables setting Condition Register
    - Trivial accept/reject in 3-D graphics
    - Exception detection via software polling
    - Available library

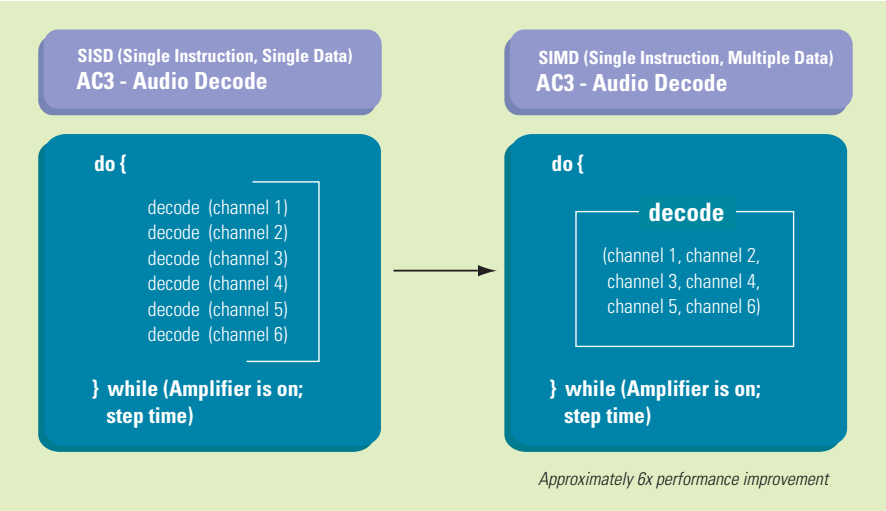
ABOUT 128-BIT SIMD VECTOR ARCHITECTURE

128-BIT VECTOR ARCHITECTURE FEATURES

- 128-bit wide data paths between L1 cache, L2 cache, load/store units and registers
  - Wider data paths speed save and restore operations
- Offers SIMD processing support for the following:
  - 16-way parallelism for 8-bit signed and unsigned bytes and characters
  - 8-way parallelism for 16-bit signed and unsigned halfword
  - 4-way parallelism for 32-bit signed and unsigned integers and IEEE floating point numbers
- Four fully pipelined independent execution units
  - Vector permute unit is a highly flexible byte manipulation engine
    - Vector simple fixed-point, vector complex fixed-point, and vector floating-point execution engines
  - Dual AltiVec instruction issue

Without the power of AltiVec technology, the code may have to call a routine six times to perform the same operation on multiple pieces of data. With AltiVec technology, the routine may be run only once, on all six sections of data simultaneously.

SAMPLE-BASED PROCESSING



ALTIVEC INSTRUCTION SET

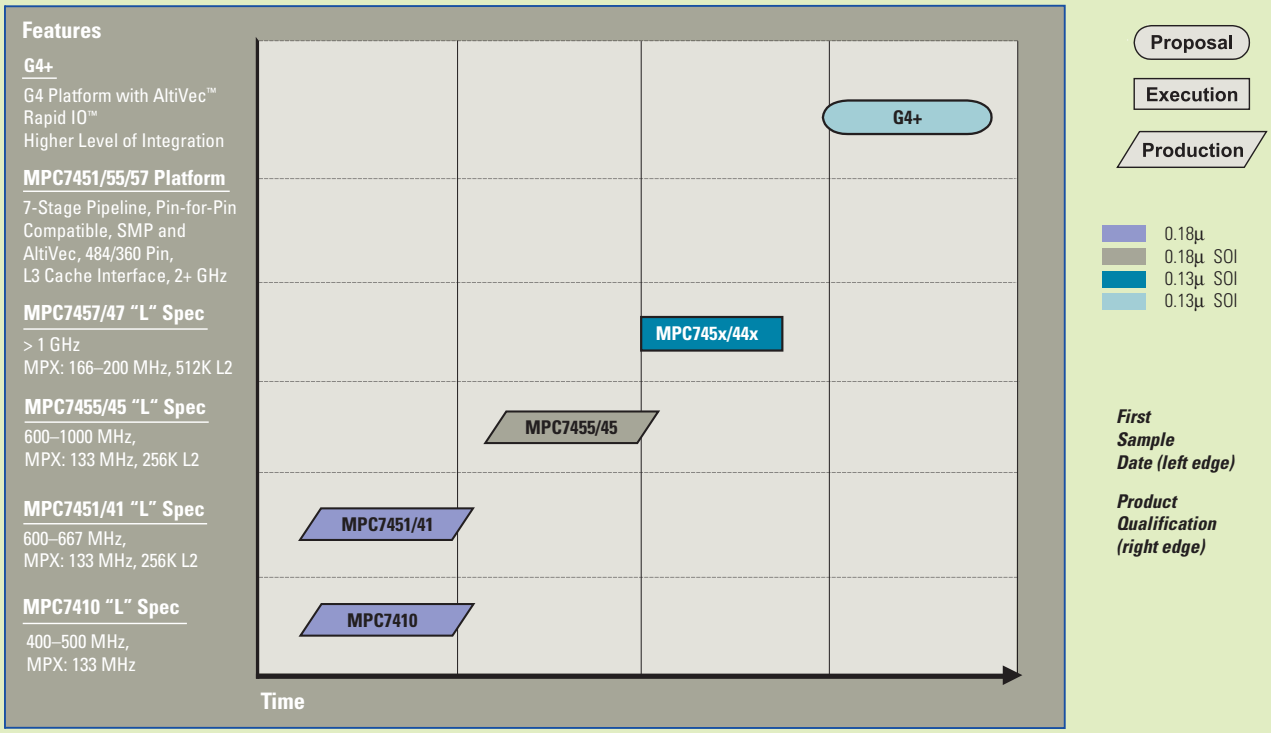
- 162 instructions added to the PowerPC ISA
- 4 operand, non-destructive instructions
  - Up to three source operands and a single destination operand
  - Supports advanced "multiply-add/sum" and permute primitives
- Instructions fully pipelined with single-cycle throughput
  - Simple ops: 1 cycle latency
  - Compound ops: 3–4 cycle latency
  - No restriction on issue with scalar instructions
- Enhanced cache/memory interface
  - Software hints for data re-use probability
  - Prefetch support (stride-N access)
- Simplified load/store architecture
  - Simple byte, halfword, word and quadword loads and stores
  - Virtually no unaligned accesses—software-managed via permute instruction

ALL ABOUT ALTIVEC TECHNOLOGY

WHAT IS A VECTOR ARCHITECTURE, ANYWAY?

- Designed to allow the simultaneous processing of many data items in parallel
- Has roots in supercomputing, which attempted to extract large amounts of parallelism from software
- Performs operations on multiple data elements by a single instruction, called Single Instruction, Multiple Data (SIMD) parallel processing
- AltiVec technology is a short SIMD vector architecture
  - Uses 128-bit wide registers to provide 4-, 8- or 16-way parallelism
  - Supports a wide variety of data types
- SIMD extension to host processors compatible with the PowerPC ISA
  - Processes multiple data streams/blocks in a single cycle
  - Common approach to accelerate processing of next-generation data types (audio, video, packet data)

MOTOROLA'S HIGH-PERFORMANCE EMBEDDED MICROPROCESSOR PRODUCTS

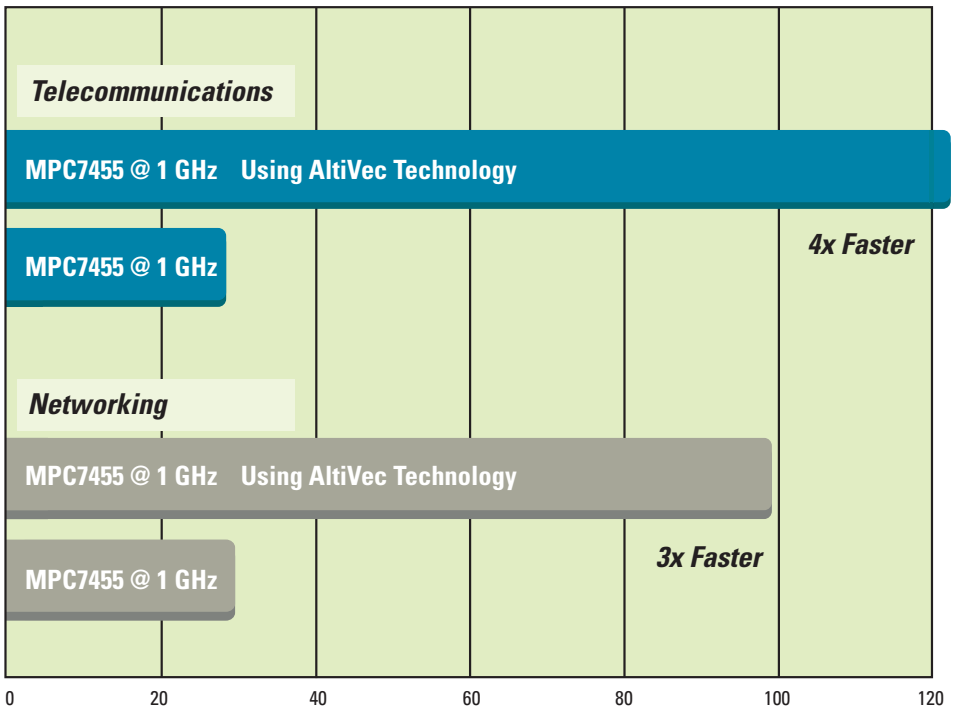


Except for historical information, all of the expectations and assumptions contained in the foregoing are forward-looking statements involving risk and uncertainties. Important factors that could cause actual results to differ materially from such forward-looking statements include, but are not limited to, the competitive environment for our products, changes of rates of all related services and legislation that may affect the industry. For additional information regarding these and other risks associated with Company's business, refer to the Company's reports with the SEC.

BENCHMARKING DATA

EEMBC RESULTS: TELECOMMUNICATIONS AND NETWORKING WITH ALTIVEC™ TECHNOLOGY

MPC7455 @ 1 GHz



EEMBC Telemark™
MPC7455 with AltiVec: 121.6
MPC7455 without AltiVec: 28.3

EEMBC Netmark™
MPC7455 with AltiVec: 98.4
MPC7455 without AltiVec: 29.4

www.eembc.org

www.ebenchmarks.com

The EEMBC Certification Laboratories, LLC (ECL) has certified these scores according to the rules established by the EEMBC Board of Directors and ECL. These scores are repeatable and the disclosure information on the EEMBC Web site has all been verified.

FOR MORE INFORMATION

Find more information about AltiVec technology embedded in Motorola's G4 processors at ***www.motorola.com/AltiVec***

- Libraries
  - May be linked via standard third-party compilers
  - Contain elements that have been shown to be effective by EEMBC's networking and telecom benchmark suites
- Application notes
  - Software code may be incorporated into customer's specific code, i.e., Fft, dct, Invert, etc.
- Customer code
  - Motorola's software engineers are available to help customers take advantage of the power of AltiVec technology in their code.

For more information about Motorola's products:
www.motorola.com/semiconductors

For additional tech questions:
www.motorola.com/semiconductors/support

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