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Features

- Factors symmetric positive definite matrices from 3 to 64 rows and columns
- Fixed-point arithmetic for high-performance with up to 53 bits of precision
- Based on Cholesky factorization (decomposition) of the input matrix
- Includes reference MATLAB model and self-checking RTL testbench
- Core can be imported into Xilinx System Generator for DSP

Applications

- Kalman filtering
- Space-Time Adaptive Processing (STAP)
- Wireless signal processing
- Beamforming
- Software Defined Radio (SDR)
- Radar / Sonar
- Guidance, navigation and control
- Geo-/Astrophysical exploration
- Biomedical signal processing

Core Facts

Provided with Core	
Documentation	Users Guide
Design File Formats	VHDL
Constraints Files	NA
Verification	Testbench generated from MATLAB, Test Vectors
Instantiation templates	VHDL, Verilog
Reference designs & application notes	NA
Additional Items	NA
Simulation Tools Used	
MATLAB (The MathWorks), ModelSim (Mentor Graphics)	
Support	
Provided by AccelChip Inc.	

Table 1: Core Implementation Statistics.

Supported Family	Devices	Fmax (MHz)	Slices[1]	IOB[2]	Throughput	BRAM	MULT/ DSP48	Design Tools
Virtex-II Pro™	XC2VP30-7	TBD	TBD	TBD	TBD	TBD	TBD	ISE 6.3.03i
Virtex-4™	XC4VSX55-11	TBD	TBD	TBD	TBD	TBD	TBD	ISE 6.3.03i

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

2) Assuming all core I/Os and clocks are routed off-chip

3) Fmax and throughput can be increased with greater use of device resources.

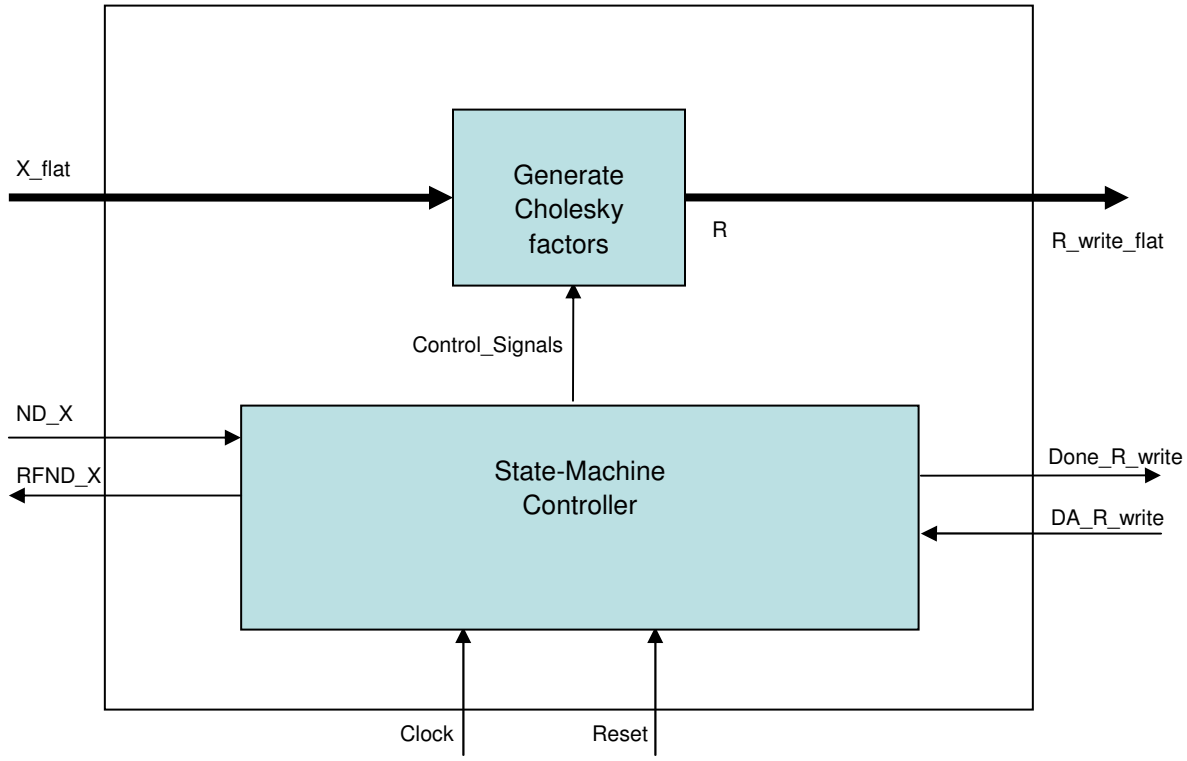

Figure 1: Cholesky Matrix Factorization Core Block Diagram.

General Description

The Cholesky Matrix Factorization core factors a real-valued, input matrix A into triangular matrices for special classes of symmetric matrices. (For applications where where an explicit matrix inverse is required, see the data sheet for the Cholesky Matrix Inverse.)

Functional Description

The AccelCore Cholesky Matrix Factorization core operates on a symmetric, positive definite input matrix X to produce an upper triangular output matrix R such that R' * R = X. The output matrix R is called a Cholesky factor of X. The Cholesky Matrix Factorization model uses a factorization algorithm based on a column-wise version of the Cholesky factorization algorithm described in ***Matrix Computations***, G. H. Golub and C. F. Van Loan, The Johns Hopkins University Press, Baltimore, Maryland, 1996.

Core Modifications

There are two levels of core modifications possible with AccelCore IP. First, there are implementation parameters specific to each type of core – these parameters are listed in the table below. Additionally, AccelChip can perform further optimizations based on customer speed and area requirements, such as rolling/unrolling of algorithmic loops or parallel implementations of matrix operations.

Parameter Name	Parameter Description	Range
X quantizer	Input matrix quantization	2 to 24 bits
Input Data Type	Input matrix data type	Real
Matrix Rows	Input matrix number of rows	Integer between 3 and 64
Matrix Columns	Input matrix number of columns	Integer between 3 and 64
Input/Output type	Input/output matrix dimension representation	1-D or 2-D
Output Matrix Precision	Number of bits for output matrix	Up to 32 bits when used as standalone core
Resource Sharing	Resource-shared implementation option	Yes / No

Input Matrix Quantization

The number representation of the input is defined by the input matrix quantization. The Cholesky Matrix Factorization core accepts real-valued, fixed-point input data with quantization parameters defined by this quantization.

Input Data Type

The input matrix must be real-valued.

Matrix Rows / Matrix Columns

The Cholesky Matrix Factorization core can operate on a square or rectangular matrix. These two parameters set the number of rows and columns, respectively, of the input matrix.

Input/Output Data Type

The Cholesky Matrix Factorization core can be generated to accept input and generate output matrices as 1-D or 2-D arrays.

Output Matrix Precision

This parameter defines the numerical precision of the factorized matrix R in terms of the number of bits and is automatically computed during the generation of the Cholesky Matrix Factorization core. The output precision can be constrained as required.

Core I/O Signals

The core I/O signals have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Clock	Input	Clock Input
Reset	Input	Reset Input
X_flat	Input	Input matrix data
RFND_X	Output	Ready for new data
ND_X	Input	New input data valid
R_write_flat	Output	Output matrix data
Done_R_write	Output	Output done indication
DA_R_write	Input	Output accepted indication

Core Assumptions

All implementations of matrix factorization can be sensitive to the condition number of the input matrix. This core is designed to operate on well-conditioned matrices, so the designer should take steps to ensure that that the input matrix is not ill-conditioned.

Verification Methods

The AccelCore Cholesky Matrix Factorization core has a complete verification flow to ensure a bit-true implementation. The core is specfied using a fixed-point MATLAB model along with a set of stimulus and results. Based on the user's specifications, AccelChip produces an RTL model for the core, which is verified against the MATLAB model to ensure it is bit-true. AccelChip can also produce bit-true, cycle-accurate verification models for use with Simulink® from The MathWorks or Xilinx® System Generator for DSP.

Recommended Design Experience

The user should have some familiarity with linear algebra techniques and with HDL design methodologies.

Available Support Products

Customers may request that AccelChip provide versions of the AccelCore IP cores that can be imported into Xilinx System Generator for DSP. This allows the customer to verify the core using System Generator's system-level simulation facilities and libraries.

AccelChip Inc. uses proprietary algorithmic synthesis tools in the development of AccelCore IP cores. To obtain the AccelChip DSP Synthesis tool directly, contact your local AccelChip sales representative or send email to sales@accelchip.com.

Ordering Information

This product is available directly from AccelChip Inc. under the terms of the SignOnce IP License. The AccelCore Cholesky Matrix Factorization core is available under the following AccelChip part numbers

AccelChip Part Number	Description
CHF08	AccelCore Cholesky Matrix Factorization Core – up to 8x8 matrix
CHF16	AccelCore Cholesky Matrix Factorization Core – up to 16x16 matrix
CHFXX	AccelCore Cholesky Matrix Factorization Core – larger than 16x16 matrix

Please contact your local AccelChip sales representative or send email to sales@accelchip.com.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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