32-BIT FLOATING-POINT MULTIPLICATION TWOS COMPLEMENT (MIL-STD 1750A)

The ADSP-1024A is a useful building block for high-speed floating-point multipliers. The implementation described here accepts normalized 24-bit twos-complement mantissas and 8-bit twos-complement exponents as inputs. The product will be normalized to the same format. Pipelined throughput will be at the clocked multiply rate of the ADSP-1024A, e.g. 95ns for the ADSP-1024AK. This design exhibits very low latency as well.

The ADSP-1024A performs the mantissa multiplication. It also normalizes the mantissa product with its output shifter. The NORM and OVF flags determine the number of bits to be shifted on output and also provide the control lines to the external adders to denormalize the exponent as the mantissa is normalized.

In this implementation, a single clock drives the ADSP-1024A's CLKX, CLKY, and CLKP as well as the exponent circuitry. On the clock's rising edge, the pair of mantissas is loaded into the ADSP-1024A's input registers. At the same time, the two exponents are clocked into their respective 'LS273 octal D flip-flops.

During the clock cycle, the ADSP-1024A will compute the product of the mantissas. In parallel, the exponents will be added in the 'LS283 4-bit full adders. Their sum will be valid well before the clock goes high again, when it will be latched into a 'F273 octal D flip-flop. At this same rising edge, the mantissa product is clocked into the output register within the ADSP-1024A. New floating-point inputs can also be clocked into the circuit at the same time, making possible floating-point throughput at the ADSP-1024A's clocked multiply time.

NORM and OVF from the ADSP-1024A will be valid t_{DNRM} and t_{DOVF} after this second rising clock edge, respectively. When valid, these (decoded) flags normalize the mantissa using the 1024A's output shifter and denormalize the exponent using a pair of 'F382 4-bit ALUs. Output can be enabled as soon as NORM and OVF are valid. The ADSP-1024A already offers three-state control; an octal 'F244 buffers the ALUs to the output bus.

If OVF is LOW and NORM is HI, then we shift the mantissa product left one bit on output to eliminate the redundant sign bit. Since we are simply formattting the mantissa, the value at the 'F273 flip-flop is already the correct exponent, and we leave it alone. If OVF is HI (and NORM is LO), then we shift the mantissa product zero bits (because the product register's MSP is already normalized in this singular case of full-scale negative times full-scale negative). The exponent is incremented by one. If OVF and NORM are both LO, we shift the mantissa product left two bits on output to eliminate two redundant sign bits and produce a normalized result. The exponent is decremented by one.

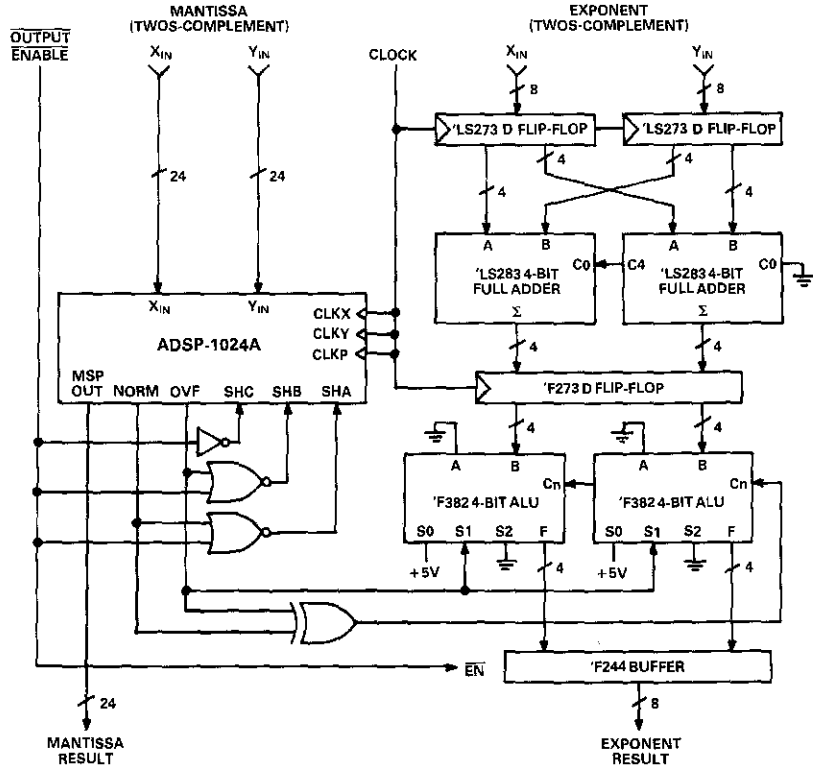

Figure 10. 32-Bit Floating-Point Multiplier Circuit