SP 25.4: A 4.1ns Compact 54x54b Multiplier Utilizing Sign Select Booth Encoders

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A sign select Booth encoder reduces transistor count of multipliers. This encoder is applied in a 54x54b multiplier in 0.25µm CMOS technology. Because of the rapid progress in VLSI design technologies, consecutive improvements in operational speed and design integration are made. As a result of these improvements, interactive real-time 3D graphics applications have become available even in personal computers. A 3D graphics application typically consists of two operational stages: geometric conversion and rendering. In the geometric conversion process, a large number of arithmetic operations are required. The volume of these arithmetic operations in real-time 3D graphics applications depends on the quality of the 3D objects and the frame rate. For example, in the case of a screen with a 1600x1280 resolution and 60Frame/s, if 3D objects are formed with small polygons (25-pixels/polygon) and 80% of the entire screen is constantly processed by 3D objects, approximately 4Mp/s (million polygons per second) are processed. To achieve 1Mp/s 3D geometric conversion performance, 250 to 300MFLOPS floating point arithmetic is required. To achieve 4Mp/s operation, more than 1GFLOPS of floating computation power is needed.

In most of the 3D graphics applications running on PCs, all geometric conversions are performed by the host CPU. Although CPU performance is improving, the feasible floating point performance of CPUs in the '98 to '99 time period are likely be in the range of 300 to 500MFLOPS. This means the host CPUs floating-point performance will not be sufficient for real-time 3D graphics operations. Such 3D graphics operations would be possible using dedicated high-end workstations, but high-end systems are too expensive for most PC users. In such circumstances as above, a cost effective, high-speed floating point computational core takes on greater importance. This compact high-speed multiplier core meets these requirements.

Figure 1 shows the configuration of a conventional 54x54b multiplier used for mantissa multiplier of two double-precision numbers, consisting of three parts: a second-order Booth encoder, a carry-save adder tree (CSA) with Booth selectors, and final carry propagation adder (CPA). In the conventional design, nearly 90% of the total transistor count consists of Booth selectors and CSA tree because a large number of components are required. Specifically, about 1,500 Booth selectors and about 900 adders are used. The proportion of Booth encoders is just 1.2%. Therefore, the key to establishing a compact multiplier lies in minimizing the volume of CSA tree and Booth selectors. In a conventional second-order Booth encoder, three signals are generated from the three adjacent multiplier bits for selecting a partial product, that is, one of 0, +X, -X, +2X and -2X. Here, X represents the multiplicand value. In this case, the logic in the Booth selector includes exclusive OR circuit and requires 18 transistors for static CMOS logic. A sign select Booth encoder with four output signals is used as shown in Figure 2. In the conventional encoder, only Mj, representing the negative partial product, is generated. Conversely, in this sign-select encoder, signals for both the negative and positive partial products are generated. PLj and Mj become active when the partial product is positive and negative respectively. The Xj and 2Xj signals show whether or not the partial product is doubled. Using these encoded signals, simplified the partial-product generation logic. For example, when +2X is necessary for the partial product, the PLj and 2Xj signals are active, and the logical product of PLj and 2Xj chooses +2X as the partial product, and when -X is necessary, the logical product of Mj and Xj chooses the correct partial product, and so on. Thus in this Booth selector, exclusive OR logic is no longer necessary. Also, by utilizing pass transistor logic, the Booth selector circuit is formed with fewer transistors. The Booth selector transistor count can be reduced by about half when 2b Booth selectors are combined in a single module, as shown in Figure 3. Although four more transistors are needed for each bit in the Booth encoder, eight transistors are eliminated from each bit in the Booth selector. As described before, the transistor count of Booth selectors occupies 35% of the space in 54x54b multiplier compared to only 1.2% for Booth encoders. The reduction of transistors in Booth selectors thus has a greater impact on the total transistor count.The transistor count for the 4:2 compressors is reduced from 60 to 48 by using pass transistor logic [1]. Total transistor count for the new 54x54b multiplier is shown in Figure 4 compared with that of the conventional regularly structured tree (RST) multiplier [2]. By adopting RST, the complicated Wallace tree wiring scheme is simplified and less design time is required. The transmission gate type of adder used previously for the final propagation adder is used [2, 3]. The sign select Booth encoder enables us to reduce the transistor count by about 44% in the Booth selectors and about 24% in the whole multiplier. A total of 60,797 transistors in a 54x54b multiplier is the minimum count reported to date [2, 4 - 8]. When this method is applied to a 26x26b multiplier, used for mantissa multiplier of two single precision numbers, 23% reduction of transistor count is obtained, showing that the logic used is effective in reducing transistor count for a smaller multiplier.

This multiplier is fabricated using 0.25µm CMOS technology. The major process parameters are summarized in Table 1. The thickness of the gate oxide is 5.5nm and CoSi2 salicidation process is forms source/drain area to reduce parasitic resistance. A three-metal-layer process is used with the CMP planarization technique. A micrograph of the chip is shown in Figure 5. The chip integrates 60,797 transistors in an active area of 1.27mm² except testing circuits. This is a 21% reduction of area compared to a conventional RST multiplier made using the same fabrication technology.

Figure 6 shows measured waveforms along critical path using electron beam probing. A critical path delay is 4.1ns at room temperature with a 2.5V supply. This speed is a little faster than those of the multipliers fabricated with the equivalent technology [4 - 5]. Measured power dissipation is 2.23mW/MHz at 2.5V supply.

Acknowledgments:

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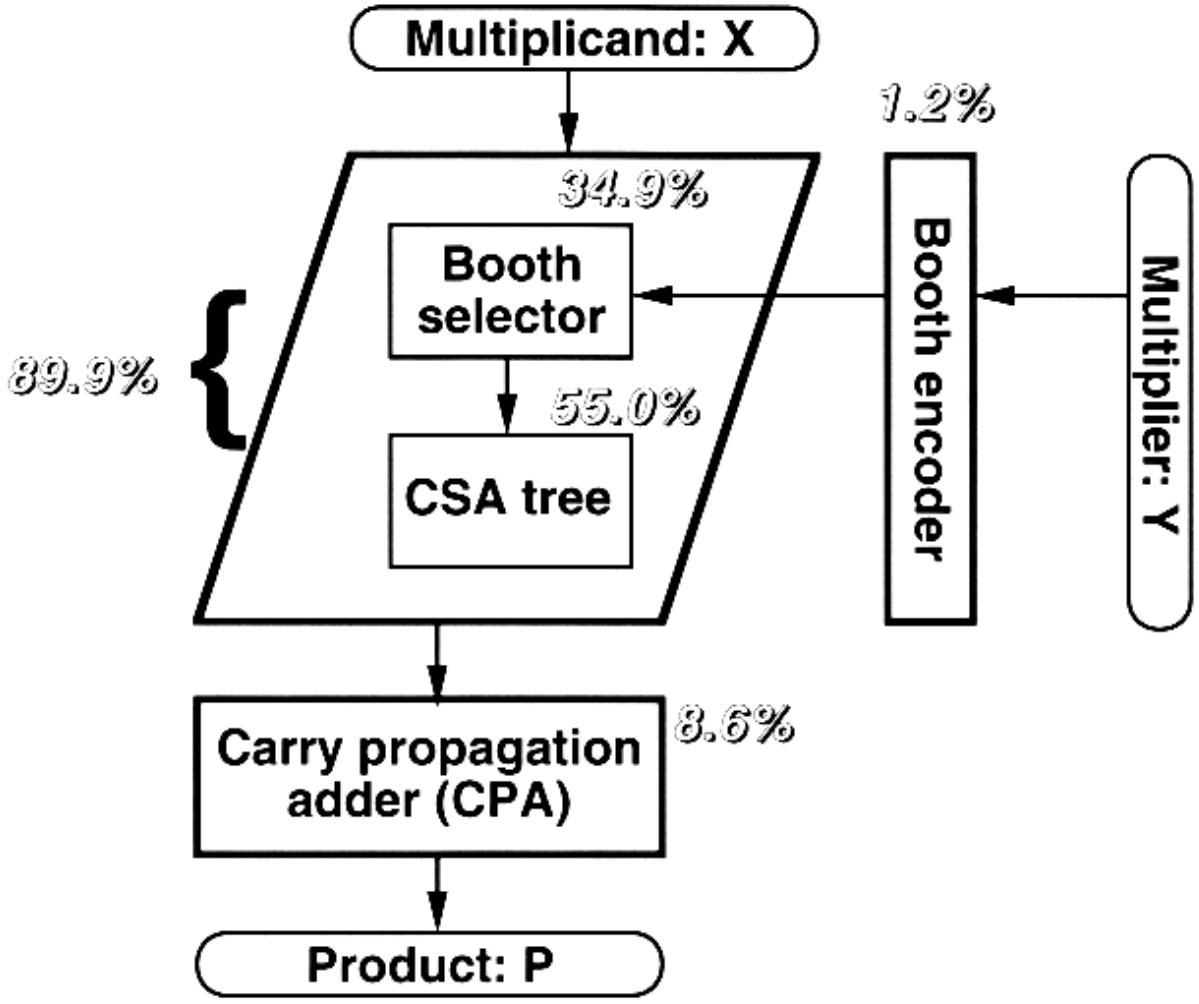


25-4-1: Block diagram of multiplier.

$$P = \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} a_i b_j * 2^{i+j} \qquad X = \sum_{i=0}^{n-1} a_i * 2^i$$

$$= \sum_{i=0}^{n-1} \sum_{j=0,2,-,n-2} a_i 2^i \left(b_{j-1} + b_j - 2b_{j+1} \right) 2^j \qquad Y = \sum_{i=0}^{n-1} b_i * 2^i$$

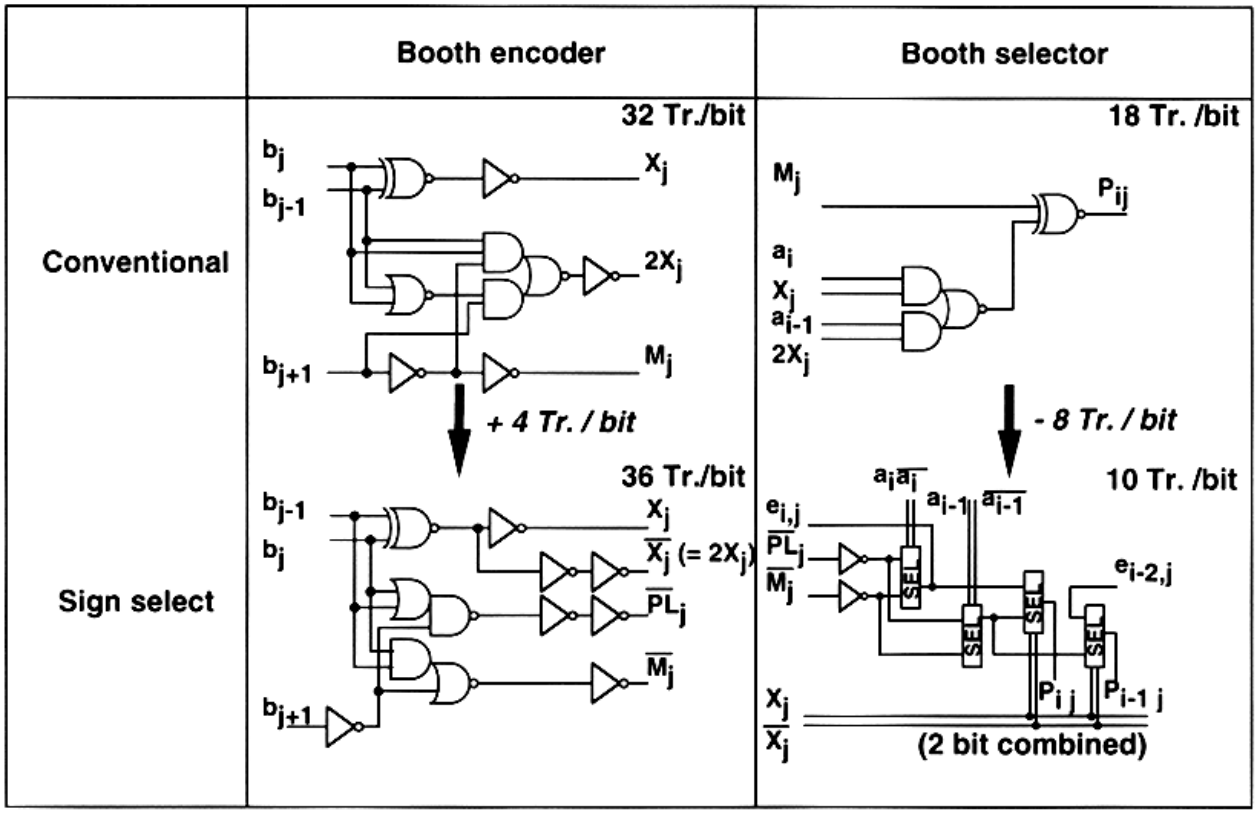
$$= \sum_{i=0}^{n-1}\sum_{j=0}^{n-1} P_{i,j}$$

b_{j+1}	b_j	b_{j-1}	Func.	Coventional encoding	Signed encoding
0	0	0	0	0	0
0	0	1	+X	$X_j \oplus M_j$	$PL_j * X_j$
0	1	0	+X	$X_j \oplus M_j$	$PL_j * X_j$
0	1	1	+2X	$2X_j \oplus M_j$	$PL_j * 2X_j$
1	0	0	-2X	$2X_j \oplus M_j$	$M_j * 2X_j$
1	0	1	-X	$X_j \oplus M_j$	$M_j * X_j$
1	1	0	-X	$X_j \oplus M_j$	$M_j * X_j$
1	1	1	0	0	0

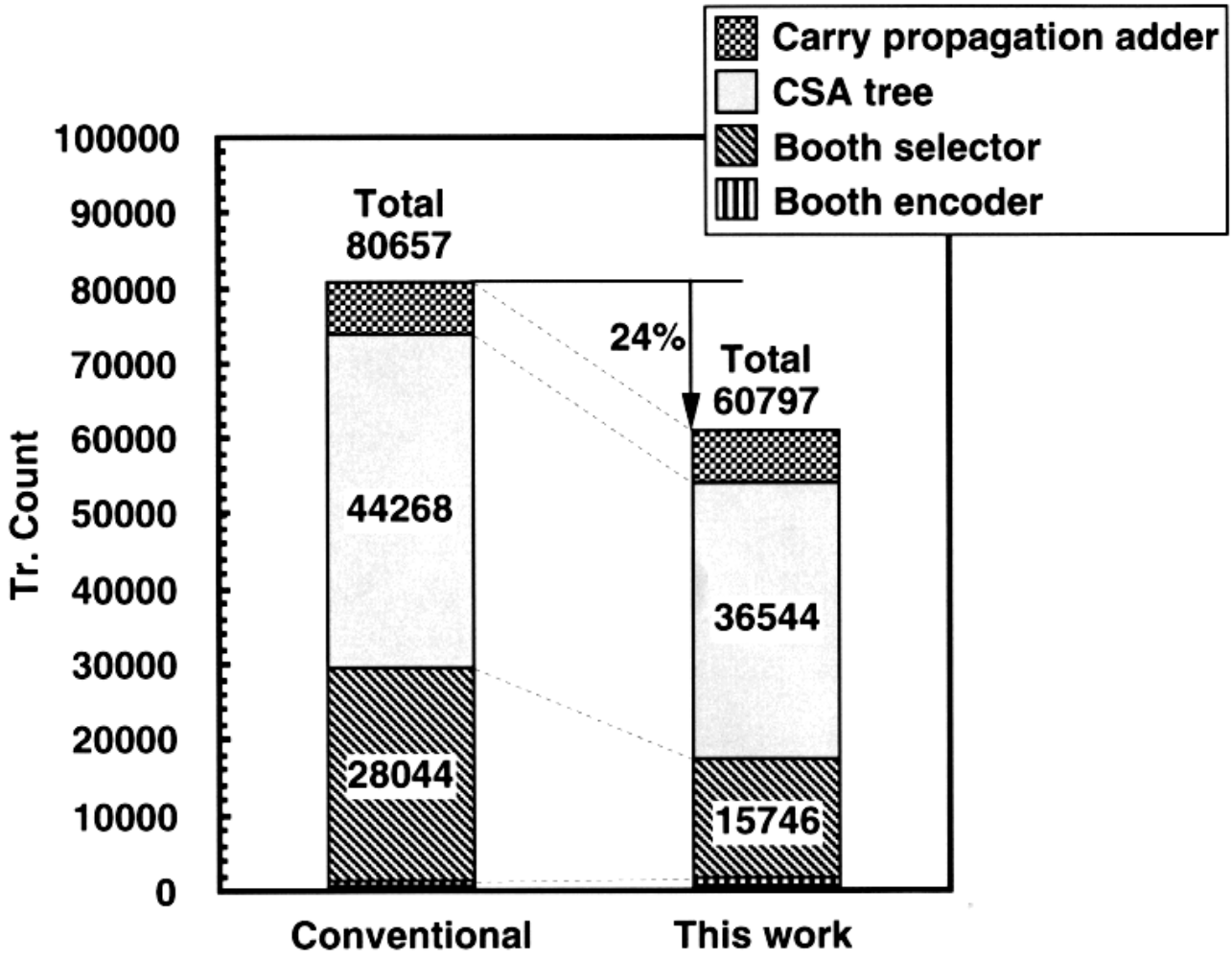
PL_j : Positive partial product X_j : Not doubled

M_j : Negative partial product $2X_j$: Doubled

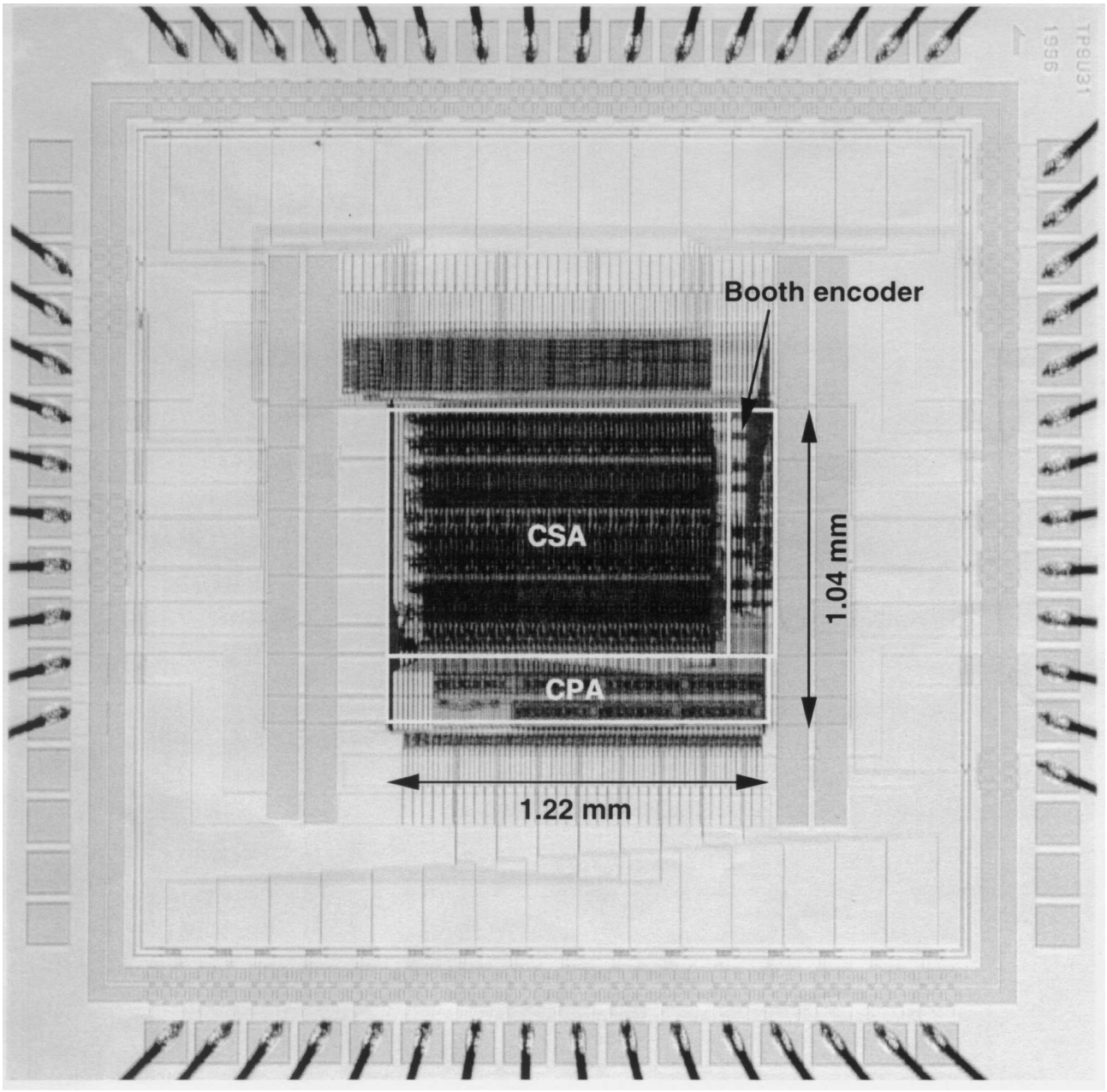
25-4-2: Booth encoding algorithm.



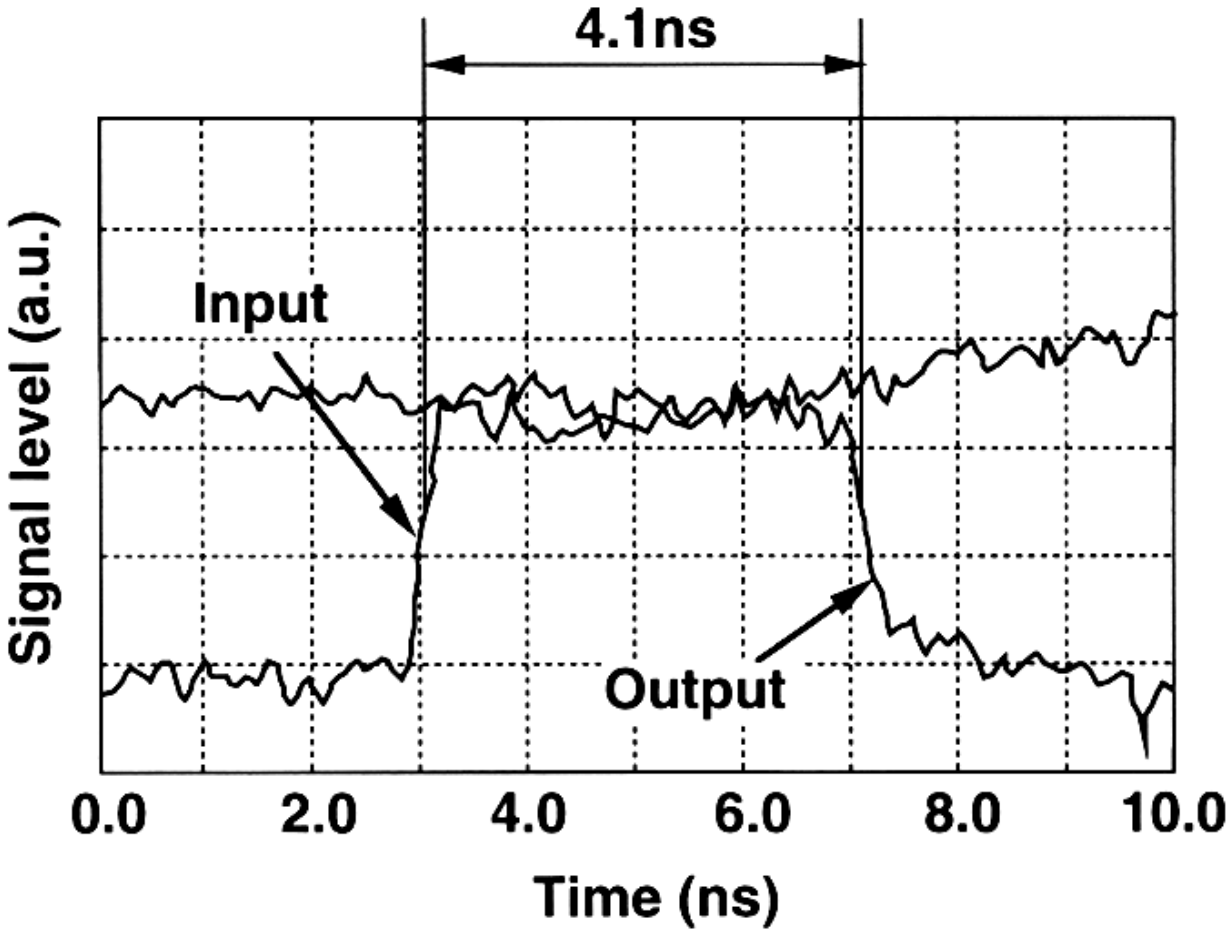
25-4-3: Circuit diagram for Booth encoder and selector.



25-4-4: Total transistor count compared with conventional multiplier.



25-4-5: Micrograph of 54x54b multiplier.



25-4-6: Signal waveform for critical path.

Technology	0.25µm CMOS 3-metal layer Co-Salicide
Gate length	0.25µm
Gate oxide	5.5nm
1st metal (line/space)	0.44µm/0.46µm
2nd metal (line/space)	0.44µm/0.46µm
3rd metal (line/space)	0.44µm/0.46µm
Planarization	CMP
Supply voltage	2.5V

25-4-Table 1: Process technology.