DESIGN FOR LOW-POWER, LOW-COST, AND HIGH-RELIABILITY PRECOMPUTATION-BASED CONTENT-ADDRESSABLE MEMORY

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ABSTRACT

This paper presents a novel VLSI architecture for a fully parallel precomputation-based content addressable memory (PB-CAM) with low-power, low-cost, low-voltage, and high-reliability features. This design is based on a precomputation skill that saves not only power consumption of the PB-CAM system, but also reduces transistor count and operating voltage of the PB-CAM cell. In addition, the proposed CAM word structure adopts the static pseudo nMOS circuit design to improve system reliability. The whole design was fabricated with the TSMC 0.35 μm SPQM CMOS process parameters under 3.3 V supply voltage. With a 128 words by 30 bits CAM size, the measurement results indicate that the proposed circuit works up to 100 MHz with the power consumption less than 33 mW. Furthermore, by the low voltage measurement results, the proposed circuit works up to 30 MHz under 1.5 V supply voltage.

1. INTRODUCTION

A content addressable memory (CAM), especially fully parallel CAM, provides the high efficient hardware architecture for high-speed data searching topic. CAM is a functional memory that contains large amounts of stored data for simultaneous comparison with the input data, and an address from among those matches of comparison is sent to the output. CAM function is used in wide range of applications such as lookup tables, databases, associative computing, data compression, and so forth [1] – [2]. Recently in high-speed networks, such as gigabit Ethernet and asynchronous transfer mode (ATM) switch, the high-speed lookup tables are necessary to satisfy the requirements of these leading-edge applications [3] – [4].

In order to achieve powerful data searching function, the data comparison of CAM architecture is implemented in parallel operation. In the parallel comparison, all valid data stored in CAM are compared with the input data simultaneously. The large amounts of parallel comparisons not only consume large amounts of comparison power but they also require more hardware cost. To overcome this problem, the dynamic CMOS circuit design is one of the best choices in the fully parallel CAM [5] – [7]. Although dynamic CMOS circuit design achieves low-power and low-cost requirements, however, this design remains having some reliable problems, such as noise margin, clock skew, charge sharing, and others [8].

In general, CAM architecture is achieved by large amounts of CAM cells, each CAM cell is implemented by comparison circuit along with bit storage. In the standard CMOS technology, the transistor count of traditional CAM cell requires nine-transistor [5] – [6]. More transistors take more hardware cost. Hence, the CAM cell has relatively low memory density compared with standard memory cells such as DRAMs and SRAMs [8]. The low memory density limits the circuit capacity for CAM's applications. Although some researches propose less than nine-transistor CAM cells, however, these circuit designs require special manufacturing technology [9]. In addition, comparison circuit in traditional CAM cell adopts pass-transistor logic (PTL) type XOR gate. Since XOR gate demands more power consumption than other standard gates such as NAND gate and NOR gate, the power consumption plays one of the key issues in CAM cell circuit design.

In portable system designs, the low-voltage operation is one of the key design factors. In the traditional CAM cell design, as a result of the comparison circuit adopting PTL type XOR gate, the operating voltage of CAM cell cannot be reduced efficiently. In the previous literatures, some low-voltage CAM integrated circuits have been proposed [7]. However, most of them require more hardware cost. Consequently, they are not suitable for low-power and low-cost system designs.

This paper presents a precomputation-based content addressable memory (PB-CAM) that achieves low-power, low-cost, low-voltage, and high-reliability features. The concept of the proposed PB-CAM architecture will first be introduced, and followed by the whole circuit design. Based on the precomputation skill, the proposed PB-CAM architecture avoids most of the comparisons to reduce majority parts of power consumption in the parallel comparison process. In addition, the PB-CAM cell requires only seven-transistor including NAND type comparison circuit. In the standard CMOS technology, the proposed PB-CAM cell is the simplest circuit and is without XOR gate compared to the previous literatures [5] – [7]. Therefore, the hardware cost and power consumption for the proposed PB-CAM cell is reduced efficiently. Moreover, the operating voltage of PB-CAM cell is lower than traditional CAM cell due to the comparison circuit in PB-CAM cell that adopts CMOS type NAND gate to replace PTL type XOR gate [8]. In order to improve overall system reliability, the proposed CAM word structure adopts the static pseudo nMOS circuit design to replace the traditional dynamic CMOS

0-7803-7690-0/02/$17.00 ©2002 IEEE

circuit design. The static pseudo nMOS circuit avoids some system reliable problems such as noise margin and charge sharing compared to dynamic CMOS circuit. This feature helps the PB-CAM circuit to be well combined with its applications.

2. THE DESIGN CONCEPT OF THE PB-CAM

A general CAM architecture usually consists of the follows: data memory with valid bit field, address decoder, bitline precharger, word match circuit, and address priority encoder, as shown in Fig. 1. The memory organization of the traditional CAM architecture is composed of the data memory and the valid bit field, where the valid bit field indicates the availability of stored data. In the data searching operation, the input data is sent into CAM to compare with all valid data stored in CAM simultaneously, and an address from among those matches of comparison is sent to the output. In this architecture, the CAM circuit performs massive comparisons to identify all valid data stored in CAM per data searching operation. The massive comparisons consume most of the power dissipation. To minimize the comparison power, one of the best skills is to reduce most of the comparisons. Based on this idea, a novel architecture is developed for low-power CAM circuit design called precomputation-based CAM (PB-CAM).

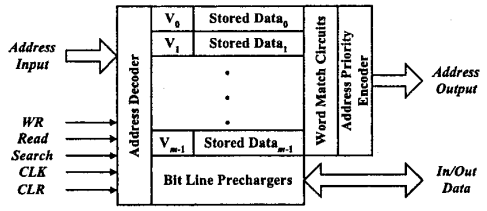

Fig. 1. Functional block diagram of CAM.

To address the proposed low-power PB-CAM architecture, the design concept for this architecture is introduced. Unlike the traditional CAM architecture, the memory organization of the PB-CAM architecture is composed of the data memory, the parameter memory, and the parameter extractor. Fig. 2 shows the memory organization of the proposed PB-CAM architecture. In the data writing operation, the parameter extractor extracts the parameterof the input data, and then stores the input data and its parameter into the data memory and the parameter memory respectively. In the data searching operation, in order to reduce massive comparisons, the operation is separated into two comparison processes. In the first comparison process, the parameter extractor extracts the parameter of the input data, and the parameter comparison circuits then compare the parameter of the input data with all parameters stored in parameter memory in parallel. If the stored parameter mismatches the parameter of the input data, then the data related to this stored parameter mismatches the input data at the same time; otherwise, the data related to this stored parameter is yet to be unidentified. Using the first comparison process results, in the second comparison process, the CAM word circuits are only compared the input data with those unidentified data to identify any match. Based on the two comparison processes, if majority parts of stored parameter mismatch the parameter of the input data, then the number of comparison of the second comparison process is largely reduced. This parameter comparison process as a simple filter, it filters majority parts of unmatched data in the first comparison process and then reduce most of the comparisons in the second comparison process. In this paper, the parameter comparison process is also known as precomputation process. Although the data searching operation uses two comparison processes to identify any match, however, both two comparison processes performed in parallel to improve the data searching performance.

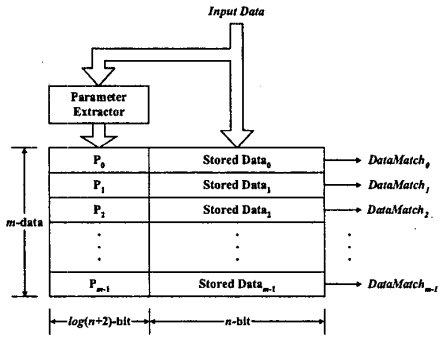

Fig. 2. The memory organization of the proposed PB-CAM architecture.

In the proposed PB-CAM architecture, the parameter extractor dominates majority parts of comparison power, since this circuit decides the number of unidentified data remaining after the parameter comparison process. In addition, both parameter memory and parameter comparison circuit of the PB-CAM architecture expend extra hardware cost and power dissipation compared to traditional CAM architecture. Therefore, the design principle of the parameter extractor is to filter as many unmatched data in the parameter comparison process with the possible shortest bit length of the parameter. In this paper, the PB-CAM architecture adopts 1's count function to perform the parameter extraction. With an n-bit data length, the kinds of 1's count are $n + 1$ (from zero 1's count to n 1's count). Furthermore, adding an extra kind of 1's count to indicate the availability of stored data is necessary. Therefore, based on this parameter extraction function, the minimal bit length of parameter is equal to $\lceil \log(n+2) \rceil$. The required bit length of the parameter is shown in Fig. 2. In the PB-CAM architecture design, with an m words by n bits CAM size, the average data comparison of the second comparison process equals to $m / (n + 1)$, since the kinds of 1's count are $n + 1$, and only one kind of 1's count (matches with the 1's count of the input data) is unidentified in the parameter comparison

process. For example, with a 128 words by 30 bits CAM size, if the input data is 01234567_{16}, then the parameter of the input data equals to 12. Therefore, the stored data mismatches the input data when its parameter is unequaled to 12. Since the range of parameter value is from 0 to 31 and onlyon e is unidentified in which parameter value equals to 12, the average data comparison of the second comparison process equals to $128 / 31 \cong 4$.

To summarize the two comparison processes in the PB-CAM architecture, with an m words by n bits CAM size, the first comparison process takes $m \times \lceil \log(n+2) \rceil$ CAM cell comparisons and the second comparison process takes $(m \times n)/(n+1)$ CAM cell comparisons. Therefore, the total number of CAM cell comparison equals to $m \times \lceil \log(n+2) \rceil + (m \times n)/(n+1) < m \times (\lceil \log(n+2) \rceil + 1)$. As a result of the traditional CAM architecture taking $m \times n$ CAM cell comparisons and $m \times (\lceil \log(n+2) \rceil + 1) < m \times n$, the proposed PB-CAM architecture saves most of the comparison power more than traditional CAM architecture.

3. THE CIRCUIT DESIGN OF THE PB-CAM

In the traditional CAM architecture, the circuit design of CAM word structure adopts dynamic CMOS circuit to improve overall system performance and hardware cost. Fig. 3 shows the traditional dynamic circuit design of CAM word circuit. In the dynamic circuit design, the output node (*Match Sense Node*) is precharged to V_{dd} by the PM1 (precharge phase) and conditionally discharged by both NM1 and NM2 connected to V_{ss} (evaluate phase). Compare with the static CMOS circuit design,th e dynamic circuit design improves circuit performance and hardware cost. However, using dynamic circuit to perform CAM word function has the following drawbacks:

- Extra precharge time. In the dynamic circuit design, the operation is separated into the precharge phase and the evaluate phase. In the precharge phase, the dynamic circuit charges the output node to V_{dd}, and then enters the evaluate phase to execute comparison operation. Therefore, the CAM word circuit needs an extra precharge time per data searching operation.
- Low reliability. In the dynamic circuit design, since the output voltage level is kept by the loading capacitance, the dynamic circuit has some reliable problems, such as charge sharing, noise margin, and leakage current problems. These problems easily affect the output voltage level.
- Heavy clock loading. In the dynamic circuit design, a clock signal is necessary to dominate the operation phase. In the traditional CAM circuit design, the clock signal not only drives all CAM word circuits, but also controls some peripheral circuits. Therefore, the loading capacitance of clock signal is extremely heavy. To overcome this problem, the circuit design of the clock driver usually adopts tree structure to improve circuit performance. The heavy clock loading consumes most of the power dissipation. In addition, to satisfy timing requirements, careful circuit design of the clock driver is necessary.
- High power dissipation. In the traditional CAM architecture, with m CAM word circuits, these circuits take $(m - 1)$ charge-discharge operations per data searching operation. Large amount of charge-discharge operations cause massive dynamic power dissipation.
- Low noise margin. In the dynamic circuit design, the output voltage level is kept by the loading capacitance. As a result of the output voltage level discharged by both NM1 and NM2 connected to V_{ss}, the noise margin of dynamic circuit is less than V_{tn}.

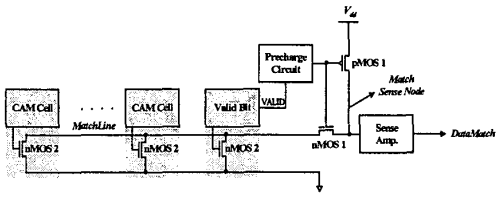

Fig. 3. Traditional dynamic CAM word circuit.

In order to eliminate these drawbacks in the traditional CAM word structure, a static pseudo nMOS circuit design for CAM word structure is proposed as shown in Fig. 4. The proposed CAM word circuit works as follows. In the data searching operation, if the valid bit is invalid ($V = 1$), then the PM1 is turned off and the NM1 is turned on. In this situation, the output signal (*MatchLine*) equals to 0 to indicate that the stored data mismatches the input data. Otherwise ($V = 0$), PM1 is turned on and NM1 is turned off. In this situation, the circuit behaves likes a static pseudo nMOS structure. Therefore, the output signal (*MatchLine*) depends on the comparison results of CAM cells.

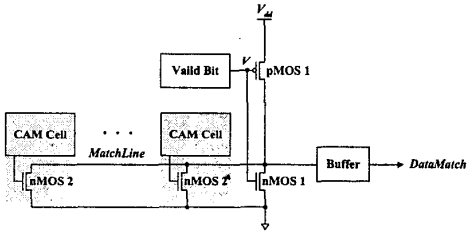

Fig. 4. The proposed static pseudo nMOS CAM word circuit.

In the proposed CAM word circuit, although the static pseudo nMOS circuit design avoids some problems occurred in the dynamic circuit design, however, the main problem with the pseudo nMOS circuit is the static power dissipation that occurs whenever the pull-down NM2 is turned on. In the proposed static pseudo nMOS CAM word circuit, if the input data mismatches the stored data, then the static power dissipation occurs in the CAM word circuit as a result of at least one pull-down NM2 turning on in the CAM cells. In general, with m words CAM size,

the input data only matches one stored data per data searching operation. Therefore, there are $(m - 1)$ stored data mismatching the input data per data searching operation. If the CAM word circuit is performed by the static pseudo nMOS structure, then static power dissipation is one of the critical issues in the CAM circuit design.

To reduce the static power dissipation in the static pseudo nMOS CAM word circuit, a novel staticpseudo nMOS CAM word circuit based on the PB-CAM architecture is proposed as shown in Fig. 5. In order to reduce static power dissipation occurring in the static pseudo nMOS CAM word circuit, the parameter comparison circuit is used to control the pull-upPM 1. Recalling the design concept of the PB-CAM architecture, based on the two comparison processes, with an m words by n bits CAM size, the average data comparison of the second comparison process equals to $m / (n + 1)$. Using the proposed precomputation skill, only $m / (n + 1)$ static pseudo nMOS CAM word circuits turn on its pull-up PM1 by its parameter comparison circuit. In addition, one stored data amount these $m / (n + 1)$ static pseudo nMOS CAM word circuits matches the input data. Therefore, the number of static power consuming CAM word circuits are reduced to $(m / (n + 1)) - 1$. For example, with a 128 words by 30 bits CAM size, the average static power consuming CAM word circuits are equal to (128 / 31) -1 ≅ 3, the static pseudo nMOS CAM word circuits reduce much of static power dissipation.

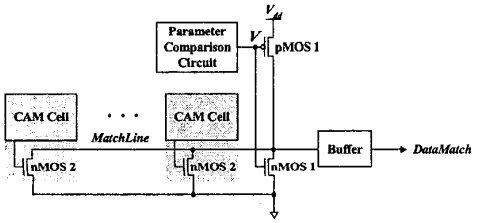

Fig. 5.The proposed static pseudo nMOS CAM word circuit based on the PB-CAM architecture.

In the previous CAM circuit design, the CAM cell is constructed by typical nine-transistor architecture as shown in Fig. 6. The CAM cell consists of an ordinary six-transistor SRAM cell to store a data bit, an XOR type comparison circuit containing two nMOSs, and an nMOS pull-down device to drive the word match line. The traditional CAM cell structure has following drawbacks:

- Low memory density. In the traditional nine-transistor CAM cell, the memory density is lower than standard memory cells such as DRAMs and SRAMs.
- High power dissipation. In the traditional CAM cell design, XOR gate realizes the comparison circuit. As a result of XOR gate having higher power dissipation than other standard gates such as NAND gate and NOR gate, the power consumption is one of the key issues.
- High operating voltage. In the traditional CAM circuit, the input voltage of the XOR gate needs larger than 2 V_m to turn on the pull-down MN2, that is due to the comparison circuit having performed by the PTL type XOR gate. Therefore, the operating voltage of traditional CAM cell cannot be reduced efficiently.
- More heavy lines. In order to improve circuit performance and hardware cost, the traditional CAM cell design adopts two complementary heavy bitlines structure. More heavy line takes more power dissipation. In addition, if both complementary heavy lines occur "phase skew" (two heavy lines not complementary completely), then the CAM circuit consumes massive static power dissipation.

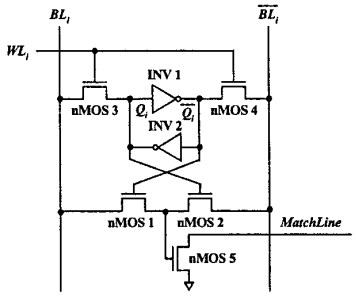

Fig. 6. Traditional nine-transistor CAM cell.

Unlike the traditional CAM cell design, the proposed PB-CAM cell is a seven-transistor cell structure as shown in Fig. 7. This cell incorporates a standard five-transistor D-latch device to store a data bit and a NAND type comparison circuit containing two nMOSs to drive the word match line. In the traditional CAM cell design as shown in Fig. 6, the CAM cell works in two operations. In the data writing operation, the WL signal rises to 1 to allow the input data BL_i be stored in the SRAM device. In the data searching operation, if the input data BL_i mismatches the stored data Q_i, then the word match line is pull-down to ground; otherwise, the word match line is floating. Compare with traditional CAM cell circuit, the proposed PB-CAM cell circuit has an incorrect case accrued in the data searching operation. The incorrect case is that when the input data BL_i equals to 0 and the stored data Q_i equals to 1 ($\overline{Q_i}$ equals to 0), both signals$\overline{Q}_i$ and BL_i will turn off the MN2 and MN3 respectively. In this case, the input data BL_i mismatches the stored data Q_i, however, the word match line is floating. This result does not meet the requirement of the traditional CAM cell design.

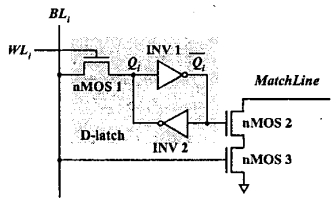

Fig. 7. The proposed seven-transistor PB-CAM cell.

Although the PB-CAM cell has an incorrect case accrued in the data searching operation, however, based on the proposed PB-CAM word structure as shown in Fig. 5, the incorrect case of the PB-CAM cell is ignored. To explain how this incorrect case is ignored, the proposed PB-CAM word circuit is introduced as follows. The PB-CAM word circuit has three situations for the data searching operation. In the first situation, the input data BL equals to stored data Q. Since $BL_i = Q_i$, for all i, the incorrect case is not accrued in all PB-CAM cells. In the second situation, the parameter of the input data is unequaled to the parameter of stored data ($V = 1$). Since PM1 is turned off and MN1 is turned on by signal V, the output of the PB-CAM word circuit equals to 0 disregarding the comparison results of PB-CAM cells. In the last situation, the input data BL is unequaled to stored data Q but the parameter of the input data equals to the parameter of stored data ($V = 0$). As a result of $BL \neq Q$ and $V = 0$, this situation exists at least two bit positions i, j, where $n-1 \leq i, j \leq 0$, such that $(BL_i, Q_i) = (1, 0)$ and $(BL_j, Q_j) = (0, 1)$ respectively. Therefore, the unmatched pattern $(BL_i, Q_i) = (1, 0)$ is detected by the PB-CAM cell, then the output of the PB-CAM word becomes equal to 0. Therefore, another unmatched pattern $(BL_i, Q_i) = (0, 1)$ (the incorrect case occurred in PB-CAM cell) isi gnored. To summarize these three situations, the incorrect case of the proposed PB-CAM cell does not affect the PB-CAM word match function. The proposed PB-CAM word structure with seven-transistor CAM cell is shown in Fig. 8.

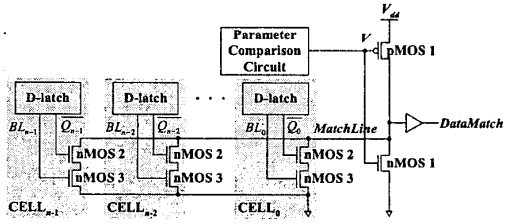

Fig. 8. The proposed PB-CAM word structure with seven-transistor PB-CAM cell.

In portable system designs, the low-voltage operation is one of the key design factors. In the traditional CAM cell design as shown in Fig. 6, the input voltage of the XOR gate needs larger than $2V_m$ to turn on the pull-down MN2, since the comparison circuit is performed by the PTL type XOR gate. However, in the proposed PB-CAM cell as shown in Fig. 7, the required turned on voltage of both pull-down NM2 and NM3 is reduced to V_m, as a result of the proposed circuit adopting CMOS type NAND gate to replace traditional PTL type XOR gate. Therefore, The proposed PB-CAM cell not only simplifies hardware design, but also reduces operating voltage.

Based on the proposed PB-CAM word structure and PB-CAM cell circuit design, the PB-CAM architecture achieves low-power, low-cost, low-voltage, and high-reliability features. However, the parameter comparison circuit is not yet mentioned in this paper. The parameter comparison circuit acts like the traditional CAM word function, it compares the parameter of the input data with the parameter of stored data, and then controls the PM1 of its related PB-CAM cell as shown in Fig. 5. In order to achieve low-power, low-voltage, and high-reliability features, the parameter comparison circuit avoids dynamic CMOS circuit and nine-transistor CAM cell designs. In this paper, since the bit length of parameter is short enough (equals to $\lceil \log(n+2) \rceil$), the parameter comparison function is realized by the static CMOS structure as shown in Fig. 9. The proposed parameter comparison circuit is composed of the 10-T CAM cell with clear function and the comparison detector used to identify comparison result. This circuit works in three operations. In the parameter setting operation, the stored parameter is set to the maximum value (each bit of parameter equals to 1) by the CLR signal falling to 0. Due to the bit length of parameter equaling to $\lceil \log(n+2) \rceil$, the set value of parameter then equals to $2 \wedge (\lceil \log(n+2) \rceil) - 1 \geqq n + 1$. In the previous definition of this paper, with an n-bit data length, the parameter of the input data is smaller then $n + 1$, therefore, the related stored data of the set parameter is invalid.In the parameter writing operation, the$W L$ signal rises to 1 to allow the input parameter P stored in the parameter storage. In the parameter comparing operation, if the input parameter P mismatches the stored parameter Q, then the output of comparison detector V equals to 1 to disable its related PB-CAM word circuit; otherwise, the output of parameter detector V equals to 0 to enable its related PB-CAM word circuit. Due to the PB-CAM word match circuit and the parameter comparison circuit work in parallel, the high searching speed of the PB-CAM architecture is achieved.

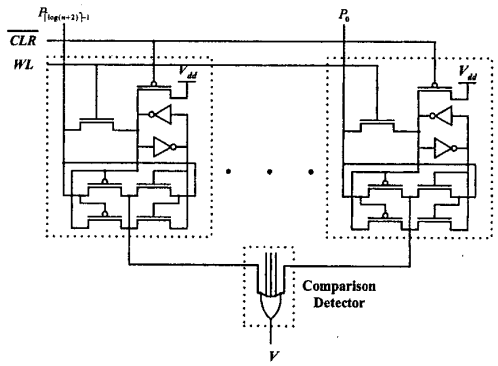

Fig. 9. The proposed static parameter comparison circuit.

4. EXPERIMENTAL RESULTS

The proposed PB-CAM circuit was fabricated with the TSMC 0.35 μm single poly quadruple metal (SPQM) CMOS process parameters under 3.3 V supply voltage without any special transistors such as low-V_{th} transistors. The microphotograph of this chip is shown in Fig. 10. The

memory capacity of this chip is 128 words by 30 bits and the area of the core is 0.66 mm × 0.8 mm. This chip composes of the data memory, the parameter memory, the address decoder, the word matchci rcuit, the parameter comparison circuit, and the address priority encoder. The layout of the seven-transistor PB-CAM cell is 5.6 μm × 7.5 μm. No special layout rules are used for the cell physical design. Based on the proposed parameter extraction circuit, the bit length of the parameter is 5 bits. To point out any invalid data stored in the PB-CAM, the "11111" pattern for data parameter is defined to mask all invalid data, since the 1's count of each data is always smaller than "11111". This chip was measured using the Integrated Measurement Systems (IMS) and the measured results show that this chip works well.

In the proposed PB-CM architecture, the PB-CAM word match circuit and parameter comparison circuit are both static type circuit designs, therefore, the test chip do not need clock signal to perform precharge phase. To measure the maximum speed, all input data stored in the PB-CAM are as similar as possible. The typical search speed includes address decoding and priority address encoding. The measured results indicate that this chip works up to 100 MHz under the 3.3 V supply voltage. Moreover, the measured results show that the minimum operating voltage of this chip is scaled down to 1.5 V. The typical searching operation power consumption at 100 MHzi n this chip is 33 mW under 3.3V supply voltage. The power-performance metric is 86 fJ/bit/search, compared with 131 fJ/bit/search of a dynamic CMOS CAM word structure with nine-transistor pMOS pull-down CAM cell [5] and 270 fJ/bit/search for a dynamic CMOS CAM word structure with nine-transistor nMOS pull-down CAM cell structure [1].

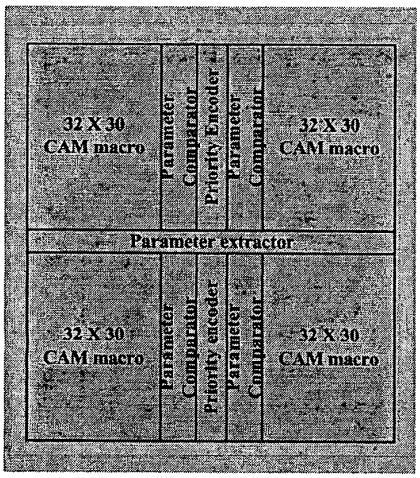

Fig. 10. Microphotograph of 128 × 30 PB-CAM chip.

5. CONCLUSIONS

In this paper, a low-power, low-cost, low-voltage, and high-reliability circuit design for precomputation-based content addressable memory (PB-CAM) has been proposed. Based on the precomputation skill, the circuit reduces most of the comparisons and transistors to achieve low-power, low-cost, and low-voltage features. Moreover, the CAM word structure design is based on static pseudo nMOS structure that improves overall system reliability and helps the PB-CAM circuit to be finely embedded in its applications. The experimental results showed that the data searching speed of the chip achieves 100 MHz with power consumption less than 33 mW at 3.3 V. Moreover, the experimental results indicate that the minimum operating voltage of this chip is scaled down to 1.5 V. The power-performance metric of the chip is 86 fJ/bit/search. This circuit is appropriate for VLSI implementation and suitable to be embedded in its applications.

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