

Modifiable Coefficient, Multi-Channel FIR Filters



Ref. QLPh6a Version 1.2



Executive Summary

Module	ONE BLOCK
Device	QuickDSP QL7180
Speed Grade	-4 (Worst Case)
Area (no buffers/buffered)	332/455 of 4032
ECU Cells	4 of 18
RAM Modules	8 of 36
Maximal Clock Frequency	32 MHz
Module	TWO BLOCK'S
Device	QuickDSP QL7180
Speed Grade	-4 (Worst Case)
Area (no buffers/buffered)	662/913 of 4032
ECU Cells	8 of 18
RAM Modules	16 of 36
Maximal Clock Frequency	30 MHz
Module	THREE BLOCK'S
Device	QuickDSP QL7180
Speed Grade	-4 (Worst Case)
Area (no buffers/buffered)	992/1324 of 4032
ECU Cells	12 of 18
RAM Modules	24 of 36
Maximal Clock Frequency	28 MHz
Module	FOUR BLOCK'S
Device	QuickDSP QL7180
Speed Grade	-4 (Worst Case)
Area (no buffers/buffered)	1324/1722 of 4032
ECU Cells	16 of 18
RAM Modules	32 of 36
Maximal Clock Frequency	21 MHz



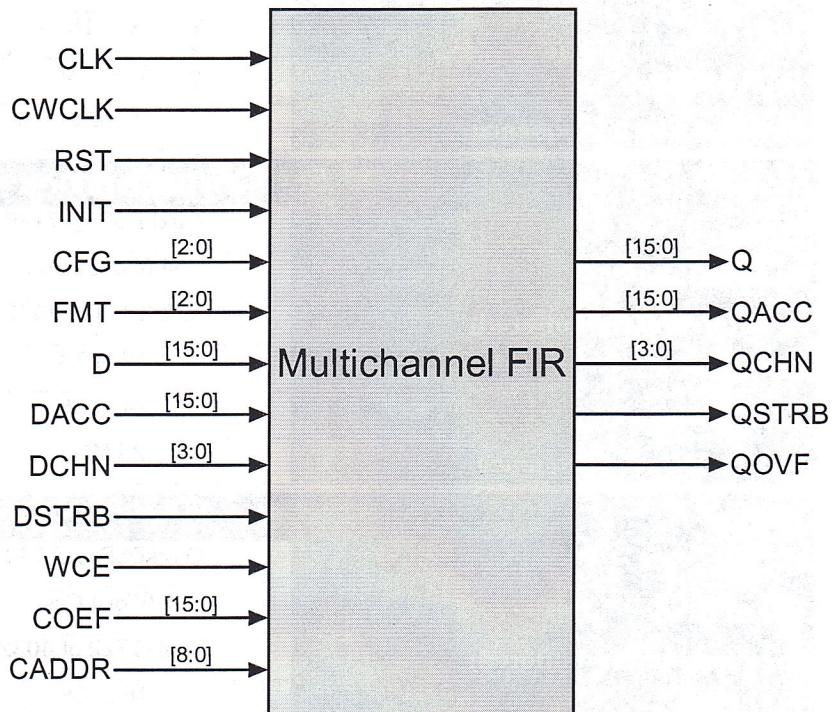
QUICKLOGIC

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Features

Features of the Amphion Multi-Channel FIR (Finite Impulse Response) Filter

- Supports up to 16 Channels per block
- Can be configured for 512 Taps per block
- 2 blocks can be designed into QL7100
- 3 blocks can be designed into QL7120
- 4 blocks can be designed into QL7160 and QL7180
- Input word length 16-bits
- Coefficient word length 16-bits
- Output word length 16-bits
- 40-bit internal accumulator
- FIR units can be cascaded
- Number of Channels and Taps can be programmed on-line
- Format of outputs can be programmed on-line
- Coefficients can be updated on-line
- Overflow detection and saturation
- Optimized for QuickLogic FPGA technologies
- Potential applications include:
 - Anti-Aliasing
 - Adaptive Filtering
 - Echo-Cancellation



General Description

FIR (Finite Impulse Response) filters are one of the most basic building blocks used in digital signal processing. The FIR filter difference equation is shown below.

$$y(n) = \sum_{k=0}^{N-1} h(k) x(n-k)$$

where $y(n)$ is the filter output

$h(k)$ are the filter coefficients

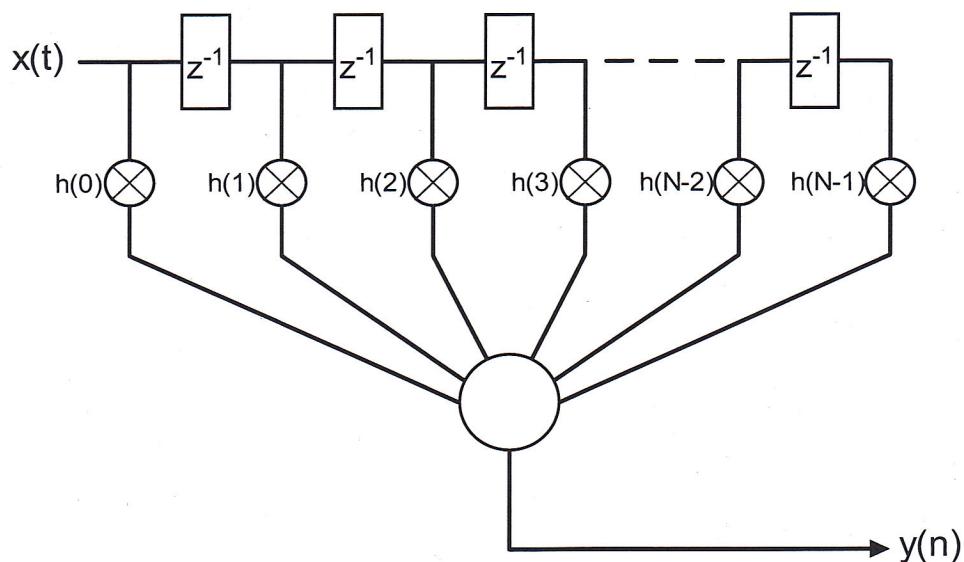
$x(n-k)$ are the past and present samples of the signal to be filtered

N is the length of the filter (number of taps)

This FIR is multi-channel; i.e. The FIR can support more than one channel of input data and coefficients. The number of channels and the number of taps per channel can be configured on-line.

For this FIR the number of channels multiplied by the number of taps per channel will always be 512.

No. of Channels x No. of Taps per Channel = 512



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The FIR is configured according to the CFG signals.

CFG [2:0]	No. of Channels	Taps per Channel
000	1	512
001	2	256
010	4	128
011	8	64
100	16	32

It is not possible to have a number of channels or a number of taps per channel other than defined above, e.g. It is not possible to have a 5 channel 100 tap FIR.

The minimal operating frequency of the FIR filter can be found using the following equation.

$$\begin{aligned}\text{Minimal Operating Frequency} &= \text{No. of Channels} \times \text{No. of Taps} \times \text{Sample Rate} \\ &= 512 \times 8\text{kHz} \\ &= 4,096,000 \text{ Hz} \approx 4\text{MHz}\end{aligned}$$

Functional Description

A functional description of the multi-channel FIR is given in the following sections.

Clock and Reset

All flipflops in the multi-channel FIR core operate on the rising edge of the input clock CLK. All flipflops in the multi-channel FIR core are reset on the rising edge of the input reset RST.

RAM Initialization

There are two sections of RAM within the multi-channel FIR filter. The coefficients are stored in synchronous RAM and the data is stored in asynchronous RAM. The input signal INIT is used to initialize all values in the RAM block to zero. If the INIT signal is asserted high for one clock cycle this will start an internal counter which runs for 512 clock cycles while the RAM is initialized. During these 512 initialization cycles all input data loading will be ignored, i.e. The FIR unit cannot be used for the next 512 clock cycles after an INIT signal.

It is not necessary to use the INIT signal, but it means that the RAM will be available for use after 512 clock cycles. If the RAM is not initialized it will require many operations on each channel before the results are valid.

FIR Configuration and Result Format

The configuration signal CFG determines the number of channels and number of taps per channel for the multi-channel FIR filter. This is explained in detail in the General Description section.

The format of the 16-bit result from the multi-channel FIR filter is determined by the FMT signal. This is explained in detail in the Data Format for Amphion Multi-Channel FIR Filter section.

Both of these signals must be kept at the required value for the entire FIR operation.

Coefficient Loading

There are 4 inputs to the multi-channel FIR filter which control coefficient loading,

CWCLK	--> Coefficient write clock
WCE	--> Write coefficient enable
COEF	--> 16-bit coefficient value
CADDR	--> Coefficient channel

New coefficients should only be loaded into a channel while that channel is not being used. Only when WCE is asserted high will the coefficient COEF be stored in the FIR RAM.

During coefficient loading the coefficient address must also be assigned. The format of this address depends on the configuration of the FIR.

The Coefficient Address (CADDR) is a 9-bit signal.

- If the configuration is 1 channel with 512 taps the coefficient address is composed from the tap number only.
- If the configuration is 2 channel with 256 taps per channel the coefficient address is composed from the channel number and tap number.
 - Bit 8 of CADDR is used to determine the channel and bits 7 to 0 are used to determine the tap number.
- If the configuration is 4 channel with 128 taps per channel the coefficient address is composed from the channel number and tap number.
 - Bits 8 and 7 of CADDR are used to determine the channel and bits 6 to 0 are used to determine the tap number.

- If the configuration is 8 channel with 64 taps per channel the coefficient address is composed from the channel number and tap number.
- Bits 8 to 6 of CADDR are used to determine the channel and bits 5 to 0 are used to determine the tap number.
- If the configuration is 16 channel with 32 taps per channel the coefficient address is composed from the channel number and tap number.
- Bits 8 to 5 of CADDR are used to determine the channel and bits 4 to 0 are used to determine the tap number.

CFG [2:0]	No. of Channels	Taps per Channel	CADDR [8:0]
000	1	512	Tap No. [8:0]
001	2	256	Ch No. [8] + Tap No. [7:0]
010	4	128	Ch No. [8:7] + Tap No. [6:0]
011	8	64	Ch No. [8:6] + Tap No. [5:0]
100	16	32	Ch No. [8:5] + Tap No. [4:0]

Data Loading

There are 4 inputs to the multi-channel FIR filter which control data loading,

- D -->16-bit data value
- DACC -->16-bit result from preceding FIR (cascade only)
- DCHN --> Data channel
- DSTRB --> Data load signal

Only when DSTRB is asserted high will input data D be loaded into the FIR. The input channel must also be assigned while DSTRB is asserted high.

The number of clock cycles required per operation is equal to the tap number so for successful operation of the FIR data should only be loaded every "number of taps per channel" cycles.

E.g. For configuration 2 there are 4 channels each with 128 taps. On this occasion data should only be loaded every 128 clock cycles.

If the FIR units are cascaded then the result from the preceding FIR unit must also be included during accumulation. This value must also be present while the DSTRB signal is asserted high.

Outputs

There are five outputs for the multi-channel FIR filter.

- Q Input data which has passed through the delay chain. This will be the input data for a cascaded FIR unit.
- QACC This is the result from the FIR.
- QCHN This signal denotes the output channel.
- QSRTB Outputs are only valid while this signal is asserted high. Any outputs that occur while QSRTB is asserted low should be ignored.
- QOVF This is asserted high if an overflow occurs during the filter operation. The output will be saturated accordingly if the overflow is positive or negative.

Each FIR unit has a 6-cycle latency. The number of clock cycles between the loading of input data and the result will be 6 plus the number of taps per channel.

Using the Multi-channel FIR Filter Generator

The Multi-channel FIR filter design files are generated by configuring the DSP Wizard Multi-channel FIR Filter GUI. The GUI requires a coefficient file (*.cof) and a input data file (*.dat) to generate the design files and testbenches.

Coefficient file (*.cof) is a coefficient test vectors file by the testbenches for simulating the filter. The user has to provide this file or else a default coefficient file will be generated. The Coefficient file format should follow the example as described below:

Channel 0

001E

001F

Channel 1

0021

0022

Channel2

0025

0026

Input Data file (*.dat) is a data test vectors file that are used by the testbenches for simulating the filter. If the user wishes to use his own input data file, the user should follow the format of this file as described below. Otherwise, the configured GUI will generate it's own input data file randomly.

DataSampsPerChan = 512

Channel 0

01F8

01F9

Channel 1

03F9

03FA

Channel 2

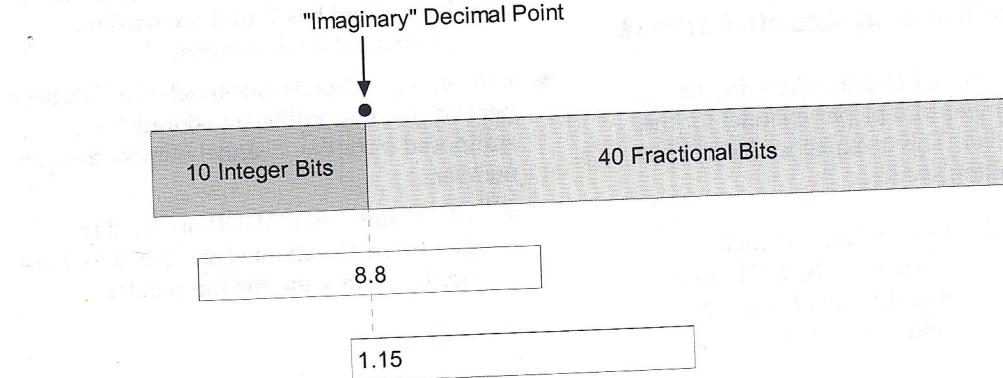
0006

0007

Channel 3

The products from the 16-bit, signed multiplier are then sign extended and added to the accumulator. The accumulator data format is 10.30 but only 16 bits of this result can actually be used for the output. The FMT signal decides which 16 are chosen, and the user determines this signal.

Accumulator Format



16-bit Result can range from 8.8 to 1.15