A MULTICHANNEL INPUT SUBSYSTEM

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ABSTRACT

A large amount of technical literature describing digital filter implementations has been aimed at approaches that have utilized fully custom VLSI chip designs or semi-custom designs using commercial DSP chip sets. This paper describes a high performance, multichannel analog acquisition subsystem that utilizes a common timing-control structure to drive multiple digital filters that are implemented with standard TTL components. The digital filter operates at a 262 kHz sample rate, has a passband ripple of ±.08 dB, stopband attenuation of greater than 80 dB and is constructed with only 36 IC's. The filter uses a technique that needs no hardware multipliers known as the Peled-Liu ROM-ACCUMULATOR architecture (1).

INTRODUCTION

Analog input system anti-alias (A-A) filters are the heart of most sampled data systems. Digital designs are replacing the older analog active-filter methods that were used to provide an appropriate low-pass filter for a desired sampling rate. Current input system designs utilize one fixed analog A-A filter preceeding the digitizing circuitry with digital filtering following the A/D to provide low-pass filtering and sample rate reduction simultaneously. Various sampling rates and bandwidths are obtained by selecting an output from a stage in a multi-stage digital low-pass filter. Digital filtering also provides the necessary increase in processing accuracy (gain, phase match of filters) to implement a frequency translation scheme ("ZOOM") with relative ease as compared to analog techniques.

The input subsystem is used in conjunction with signal processing hardware (Fig. 1) consisting of a high speed microprocessor and a host system based on a minicomputer. The microprocessor executes many of the speed-critical signal processing routines such as FFT's, auto-cross spectral estimations, control of the input subsystem, etc.

INPUT SUBSYSTEM

The input subsystem consists of one "Channel Control" card and from 1 to 4 "25 kHz Input" cards each of which is capable of acquiring four analog inputs. The system can acquire/process up to 16 inputs each with a sample rate of 65.536 kHz for a total throughput of 1.048 Megasamples per second. The digital filter hardware is time shared between the four input channels on a card giving an effective processing rate of 262 kHz.

The Channel Control card (Fig. 1) contains the circuitry necessary to control up to four 25 kHz Input cards and the interface to both the microprocessor and memory. This card also provides the following:

1) State sequencing signals for the digital filters
2) Sine, cosine generation for modulation of the A/D output
3) Channel/Bandwidth "sieve" that selects data from the digital filter outputs for:
   a) Output to memory (DMA)
   b) Input to digital trigger circuitry

Each input card consists of 4 programmable analog pre-amps followed by ninth-order, active elliptic filters and monolithic sample-and-hold units. The sampled inputs are converted by a time-multiplexed, 2 μS, 12-bit hybrid A/D. The digitized outputs (Fig. 2) are multiplied by a constant (A=2861/4096) for baseband analysis or by a complex exponential ($A \cdot COS(\theta c \cdot n)$, $j \cdot A \cdot SIN(\theta c \cdot n)$) for narrowband "ZOOM" analysis, where θc is the normalized center frequency in radians and n is the sample number. The multiplier output is passed through a cascade of halfband IIR decimating digital filters to obtain progressively lower bandwidths and sample rates. The above processes are all taking place concurrently in a pipelined fashion. When performing a narrowband (ZOOM) analysis, the A/D output from one channel is processed twice through the filtering chain. The "Real" component generated by the multiplication by the cosine term and the "Imaginary" component generated by the sine term are processed to generate a set of complex output points. Typically, a complex-to-complex FFT is performed on these points to provide the narrowband analysis around the selected center frequency.

DIGITAL FILTER DESIGN

The design (generation of filter coeficients) of the band-halving filter (Fig. 3) was directed at minimizing hardware complexity while attaining a reasonably flat (±.08 dB) passband and a high level of stopband attenuation (>80 dB). Minimizing the coefficient word length and the number of coefficients involved in the filter structure were of primary importance in generating a design that was economical as well as suitable for a fixed-point hardware implementation.

Another objective was to maximize the passband width over the interval 0 to B while maintaining the stopband over the interval (0.5-B) to 0.5 (B=normalized bandwidth=frequency/sampling frequency), where .5 is the Nyquist or "folding" frequency.

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A simple approach was taken where the zero's of the numerator polynomial were placed in the stopband of the filter on the unit circle and the denominator polynomial was chosen to flatten the passband while being constrained to utilize only even powers of Z. Constraining the denominator polynomial in this manner means that one need only calculate every other output point (2), a very desireable feature for a filter whose output is decimated by 2!

The numerator polynomial was constructed by convolving (polynomial multiplication) simple second order sequences that were composed of coefficients that could be expressed with at most 3 bits.

Figure 3 depicts the final pole-zero placement that was arrived at by an empirical procedure with the aid of a filter design program (written in Fortran) used to modify and evaluate various "prototypes". The normalized bandwidth "B" in this design is .15625 which means that 62.5% of the output band contains virtually unaliased data (aliases at least 80 dB down).

The numerator was constructed from the following polynomials:

$$PA(Z) = Z^{-2} + 2 \cdot Z^{-1} + 1$$
$$PB(Z) = 7 \cdot Z^{-2} + 8 \cdot Z^{-1} + 7$$
$$PC(Z) = 2 \cdot Z^{-2} + 3 \cdot Z^{-1} + 2$$

$P(Z)=PA(Z) \cdot PB(Z) \cdot PC(Z) \cdot PC(Z)$ = Overall numerator

The set of numerator coefficients after the above multiplication is:

28, 172, 503, 906, 1094, 906, 503, 172, 28

The denominator polynomial Q(Z) is

$$Q(Z) = 8 \cdot (87 \cdot Z^{-4} + 196 \cdot Z^{-2} + 256)$$

This set of coefficients possesses the feature that the filter gain at Z=1.0 (dc) is precisely unity. . . an important consideration when cascading up to 14 of these structures.

The main result here, however, is that the numerator and denominator polynomial coefficients can be expressed exactly with word lengths of 11 bits. From the Peled-Liu approach all possible sums of coefficients need to be computed and stored in a ROM. Exploiting the symmetry of the numerator, one needs a total of merely 13 bits to accomplish this.

FILTER ARITHMETIC

A decimate-by-two filter can be viewed as a device that requires two input points in order to generate one output point. Figure 4 is a simplified diagram of the structure of the filter with an implicit decimation of two by virtue of the organization of the shift registers (delay elements). The inputs to the device are the previous and current samples, i.e., x(n), x(n-1), and the output is y(n). The recursive terms are the previous outpus of the filter, i.e., y(n-2). The symmetry of the numerator is utilized by using serial adders to generate the sequences p(n), q(n), etc. and these sequences are operated on by the ROM/ACCUMULATOR elements. The superscript "j" in the figure indicates the j^{th} bit in the word. The subtraction required on the last cycle of the filter computation is implemented by storing the two's complement of the sums in ROM hence the +/- input bit on the coefficient ROM.

It should be stressed that the y(n) computation is exact except for a final rounding back to a 16-bit word which is the internal data bus width. Careful attention to rounding throughout the design is necessary to minimize the dc bias through the system which, when doing "ZOOM" analysis, ends up exactly at the center frequency of the analysis band. In this design the dc component is greater than 90 dB down from full scale.

HARDWARE IMPLEMENTATION

Figure 5 is a simplified block diagram of the hardware used to construct the overall digital filter. The internal states of the filters are stored in RAM. All timing and control signals are generated by the Control board along with the signals for the digital mixer. Approximately 36 IC's are needed to implement the filter/mixer combination with a power dissipation of less than 8 watts. The hardware is time-multiplexed between the four input channels and all 14 of the cascaded stages for each channel. The filter clock period is approximately 160 ns and 24 cycles, including all intermediate data movements, are required to complete the filter computation. The 256 x 8 RAM is used to store input/output data and the 1K x 8 RAM is used to create the serial in/out shift registers.

CONCLUSION

The design of a 16-channel, 25 kHz front-end subsystem has been presented. A high quality, multistage, decimating digital lowpass filter has been successfully implemented using the technique of Peled-Liu. By utilizing a common control architecture and time sharing the filter hardware, only about 9 IC's per channel are needed for the signal processing. The filter design was constrained so that a negligible degradation would be incurred with a fixed point hardware implementation.

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REFERENCES

(1) A. Peled and Bede Liu, "A New Hardware Realization of Digital Filters", IEEE Transactions ASSP Vol. 22, December 1974, pp. 456-462.

(2) H.G. Martinez and T.W. Parks "A Class of Infinite Duration Impulse Response Digital Filters for Sample Rate Reduction", IEEE Transactions ASSP Vol. 27, April 1979, pp. 154-162.

(3) T. Thong, "Finite Word Length Effects in the ROM Digital Filter", IEEE Transactions ASSP, October 1976, pp. 436-437.

(4) D.J. Goodman and M.J. Carey, "Nine Digital Filters for Decimation and Interpolation", IEEE Transactions ASSP Vol. 25, April 1977, pp.121-126.

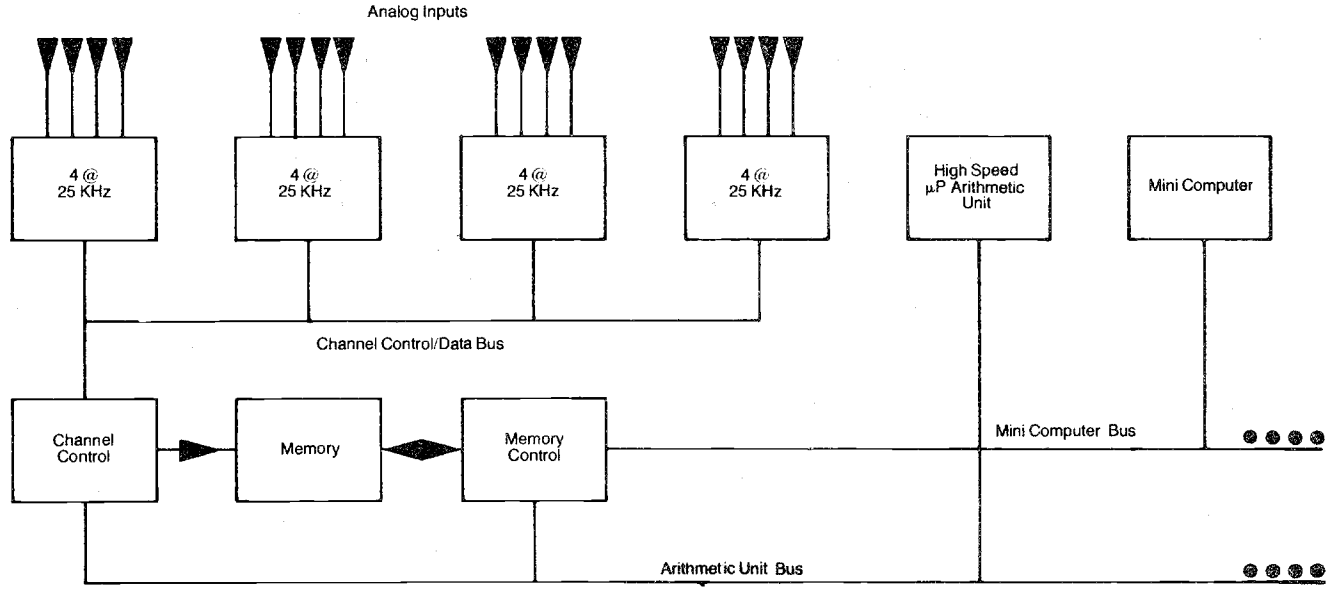


Fig. 1 **System Architecture**

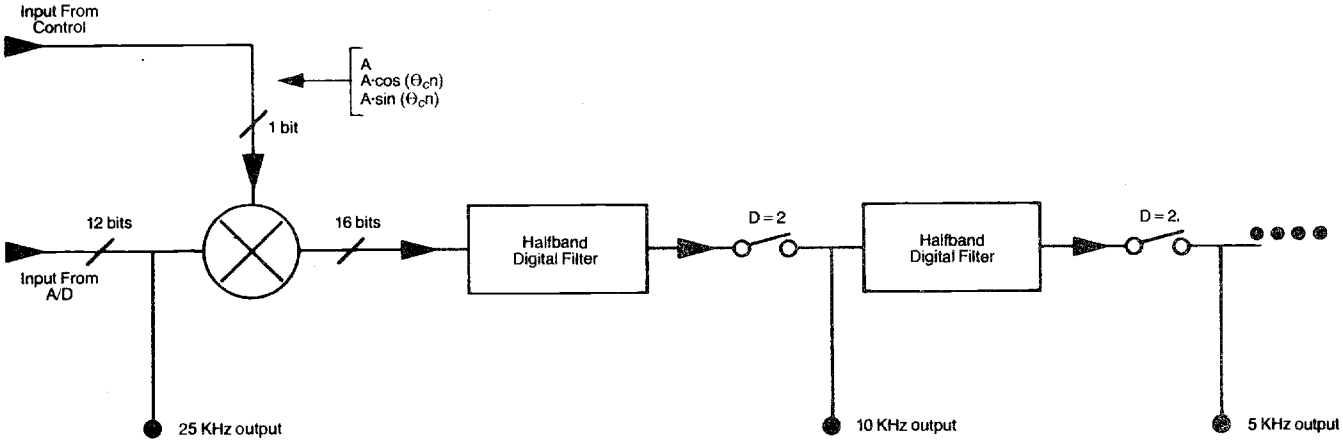


Fig. 2 **Digital Filtering Structure**

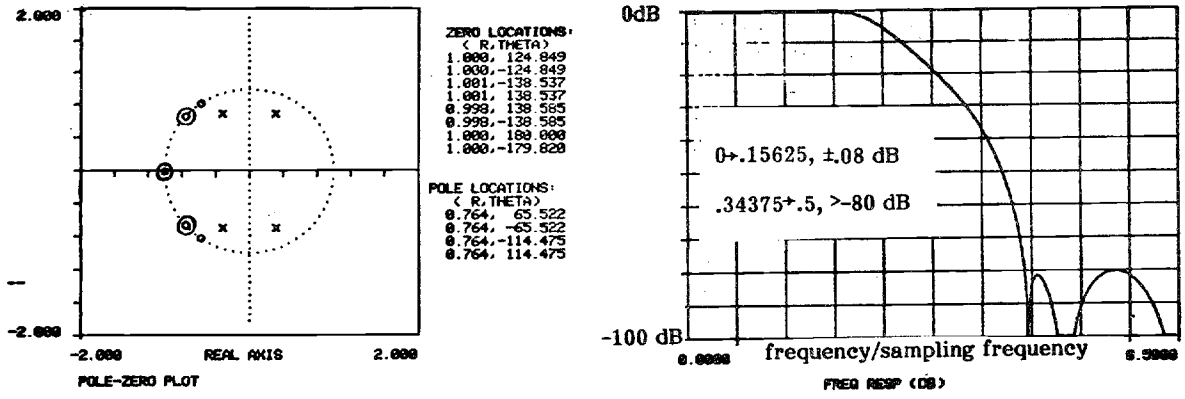
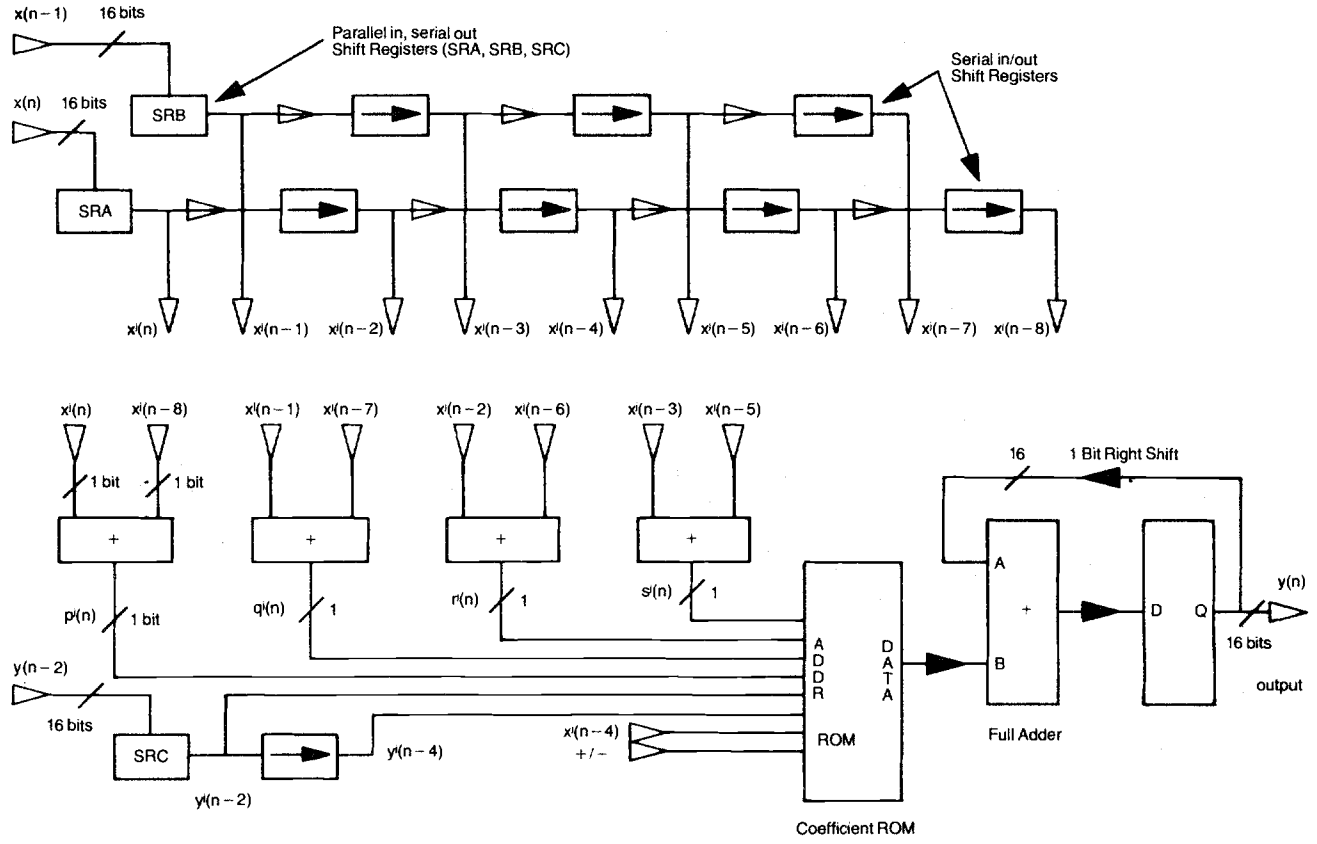


Fig. 3 **Filter Characteristics**



$$y(n) = (28 \cdot p(n) + 172 \cdot q(n) + 503 \cdot r(n) + 906 \cdot s(n) + 1094 \cdot (n-4) - 1568 \cdot y(n-2) - 696 \cdot y(n-4))/8 \cdot 256$$

$$p(n) = x(n) + x(n-8) \quad q(n) = x(n-1) + x(n-7) \quad r(n) = x(n-2) + x(n-6) \quad s(n) = x(n-3) + x(n-5)$$

Fig. 4 Digital Filter Arithmetic

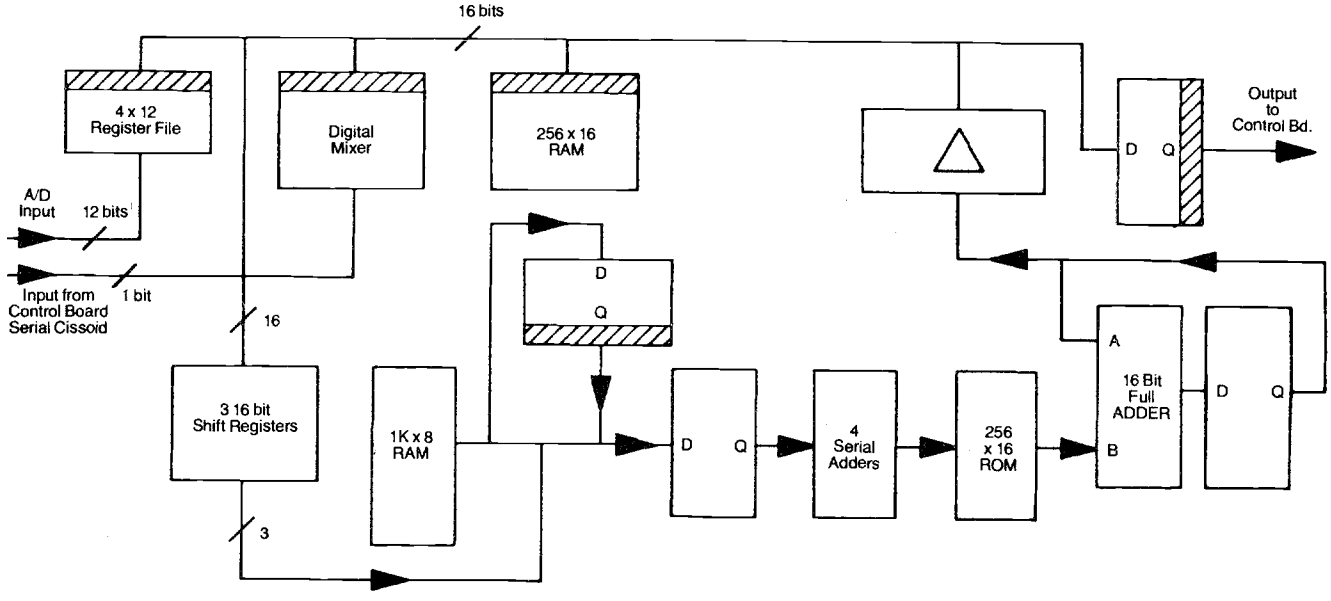


Fig. 5 Filter Architecture