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FILU-50HC11 ⇨ 60 MIPS 13000 gate MCU + DSP Core

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Features

- Verilog core combines 68HC11 functionality with DSP in a single core
- Instruction set compatible with the Motorola® MC68HC11
- Cycle by cycle instruction timing is identical to Motorola® M68HC11
- Fully synthesizable Verilog – single clock design
- Scan testable – high test coverage
- Enables DSP development and implementation in C
- Evaluation board available for system development

Microcoded DSP Functions

Basic set of DSP functions include:

- FIR filters
- 1st, 2nd & Nth order IIR filters
- 256 point real FFT
- Correlation
- Matrix & Vector operations
- Taylor series

A library of advanced DSP functions is available.

Performance

- 40 MHz clock in 0.35 μm.
- DSP core has 16-bit architecture with 40-bit accumulator

Applications

- Medical Applications
- Engine Management / Knock Detection
- AC / DC Motor Control
- Disk Drive Servo Control
- Communication Systems

Introduction

The FILU-50HC11 is an integrated 8-bit microcontroller core and a 16-bit fixed-point DSP coprocessor core. The microcontroller core is instruction set compatible with the Motorola® MC68HC11 (including 16-bit multiply and divide operations). The DSP coprocessor core has a set of pre-programmed DSP functions are accessed through a C function call from the 68HC11. This core provides 40 MIPS for the MCU and 20 MIPS for DSP in parallel.

The FILU-50HC11 is available in fully synthesizable Verilog and facilitates the development of custom systems in silicon that required DSP capability while retaining the advantages of industry standard development tools such as compilers, linkers and assemblers. At 13000 gates the FILU-50HC11 is a very cost effective, minimum area, microcontroller and DSP solution.

The FILU DSP coprocessor core is capable of implementing various DSP functions which are microcoded and are invoked by the microcontroller core via a shared RAM. The microcontroller core has Master control of the shared RAM via control / status bits. The microcoded kernel includes FIR and IIR filters, FFT, correlation, matrix operations and Taylor series. Extra DSP functions can be microcoded to suit particular applications.

The basic set of DSP functions are hardwired but RAM based functions can extend the DSP functionality after production. A library of advanced DSP functions is available.

It is expected that the user will develop their application entirely in C using an API to invoke DSP functions. To aid in the development process C and Verilog models are provided to allow system simulation. An evaluation board is available to allow the user to develop their own system applications.

The FILU-50 can be configured for integration with other microcontroller cores

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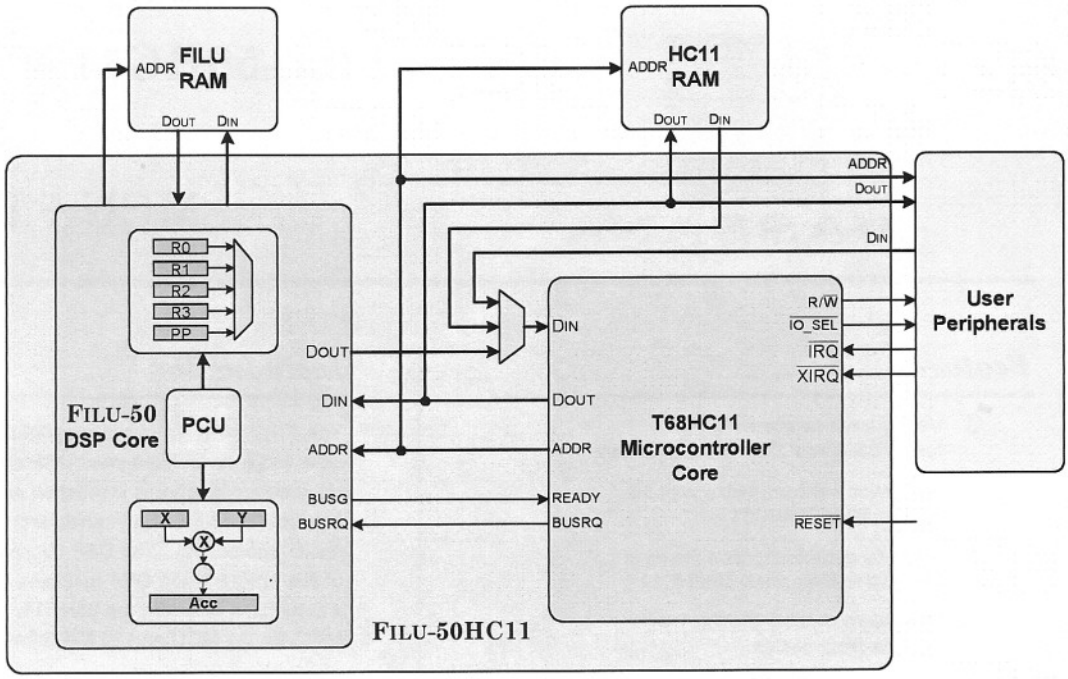

Figure 1 FILU-50HC11 *block diagram including RAMs and on chip peripherals.*

DSP Benchmarks

Function	Data Points	Num of Coeff	Num of Cycles	Exec Time µs
Correlation	N =200	-	2N+8	**5 µs**
FIR	N =100	n = 20	N(2n+7)+5	**59 µs**
2nd Order IIR	N =100	4	12N+8	**15 µs**
M 2nd Order IIR	N = 100	M = 3	N(4+8M)+8	**35 µs**
Real FFT	N = 256	-	10368	**130 µs**

The FILU-50HC11 has a DSP MIPS capability competitive to standard 16-bit DSPs such as the TI 320C50, the DSP Group Oak DSP Core and the Motorola® 56116.

Technical Specification

- Fully synthesizable – library independent
- 8-bit Microcontrollor with 16-bit addressing and 16-bit DSP architecture
- 13000 gates
- 0.65 mm^2 in 0.35 µm TLM.

Hardware & Software Interface

Complete hardware and software interface provided for the microcontroller and DSP cores. An API is provided that enables the microcontroller to use C function calls to invoke the pre-programmed DSP functions. All of the microcontroller signals including address and data bus are available to interface to the user designed peripherals.

- Microcontroller and DSP cores already integrated and tested
- FPGA implementation available
- API provided to access DSP functions.
- User designed peripherals easily added
- Evaluation board available
- ISS and Assembler for DSP available

For More Information

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