

APPLICATION NOTE

ADAPTIVE FIR FILTER

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Digital Filter Implementation on MB86975

The adaptive FIR filter in MB86975 adaptive filter processor (AFP) is based on the following difference equation.

$$y(n) = \sum_{i=0}^M a_i x(n-i)$$

The realization of a Mth-order adaptive FIR filter is shown in Figure 1. The AFP is using the Least-Mean-Square (LMS) algorithm to update the FIR coefficients. The coefficient is also called weight. For each incoming signal $x(n)$ and reference signal $d(n)$, the AFP will calculate a set of error term. The error term is based on the following equation.

$$\epsilon(n) = d(n) - \sum_{k=0}^M W(k)x(n-k)$$

The multiplier of AFP takes 16 most significant bits of coefficient times the 16 bit input signal to get a 26 bit product. The product will be shifted then truncated (or rounded) according to the specification in configuration registers. This result will be subtracted by the reference signal to get a 16 bit error term.

This error term will be used to update coefficients. The updated coefficients are based on the following equation.

$$W(k+1) = W(k) + \mu \epsilon(n-k) + \text{Leakage}$$

The multiplier will multiply the 16 bit error term with the 16 bit μ and 16 bit input signal to get a 26 bit product. This product will be truncated (or rounded) to 24 bit result, then added to the existing 24 bit coefficient and leakage constant to get an updated coefficient.

Setting up MB86975 for adaptive FIR filters

There are four steps to set up the MB86975 for adaptive FIR filters.

1. Set up the configuration registers to lead the coefficients and μ 's.
2. Input the initial coefficients and μ 's for each channel.
3. Set up the configuration registers
4. Turn the MB86975 to the RUN mode.

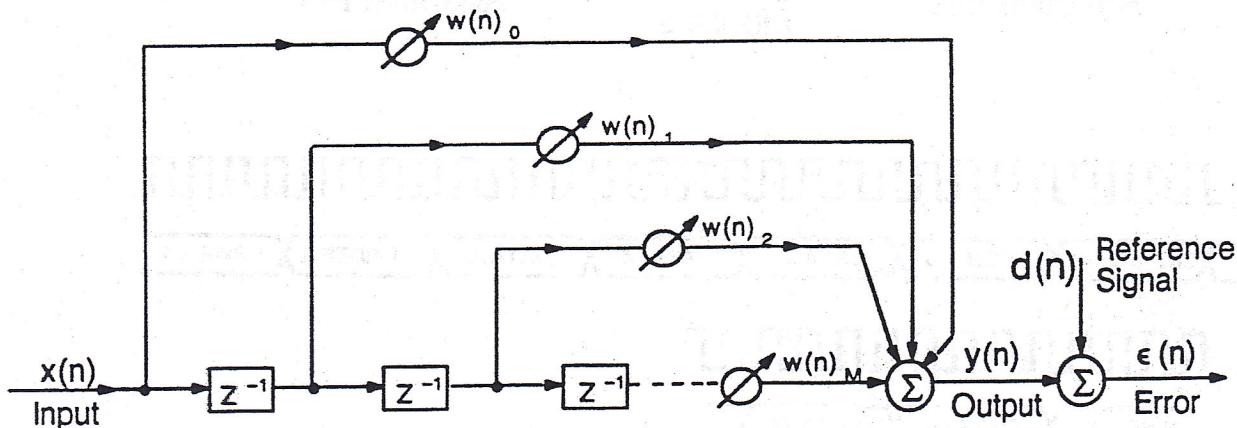
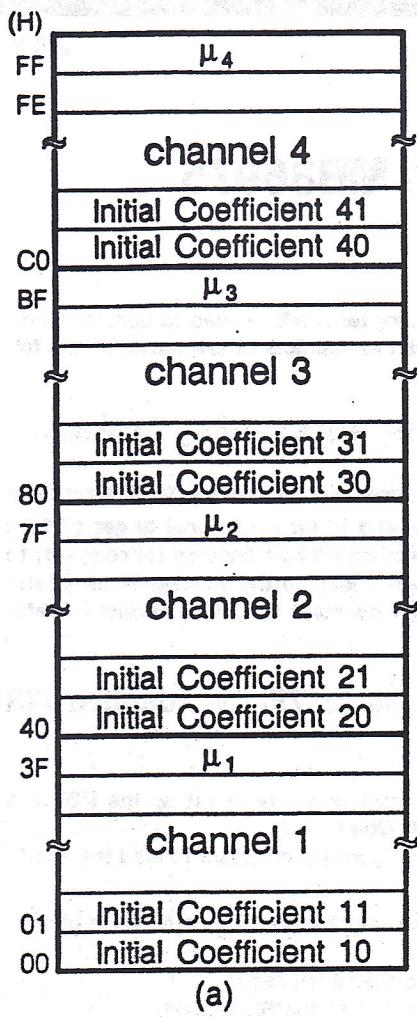
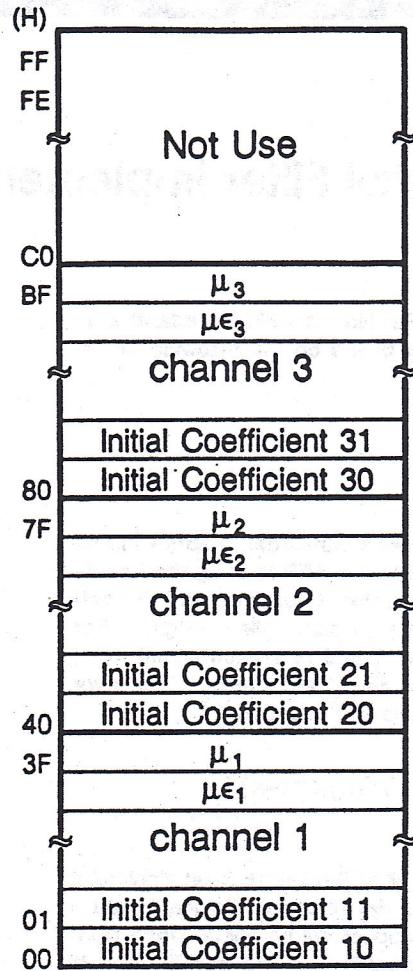


Figure 1

COEFFICIENT RAM (24 x 256) (Initial Condition)



(a)
4 channels
Adaptive FIR



(b)
3 channels
Adaptive FIR

Figure 2

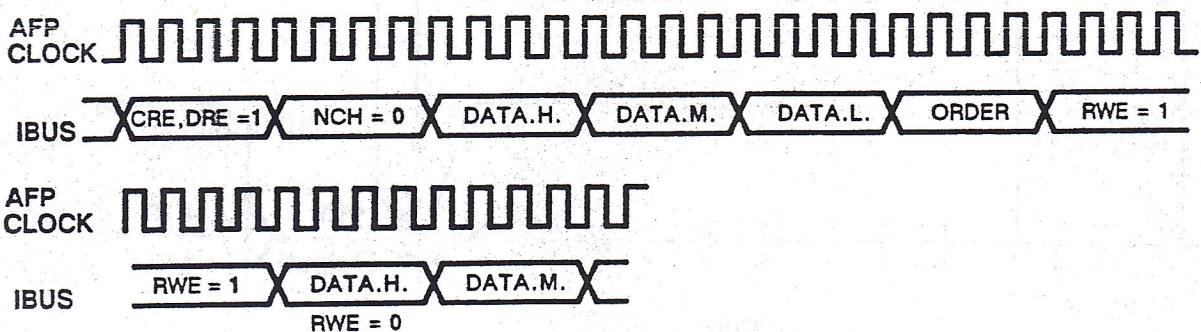


Figure 3

Set up The Configuration Registers to Load Coefficients and μ 's:

Before loading coefficients, SR bit in the MODE register, IOMODE, ALGCTRL, SCNCH, LKGRPSZ, NBGRP, and RECTRL registers must be set to zero for proper coefficient loading.

Input the FIR Coefficients:

The MB86975 contains a hardware implemented Least - Mean - Square (LMS) algorithm for adaptive FIR filters. Designers need only to input the initial coefficients and the μ factors to specify the characteristics of the adaptive filters. To load coefficients and μ 's into the proper coefficient RAM locations, designers use the Order Register to specify the coefficient RAM address and load the initial coefficients and μ 's into three Coefficient Read/Write registers(addr.=8,9,A). For single channel operations, the initial coefficient must be stored in coefficient RAM consecutively from the smallest address up. The μ

must be stored in coefficient RAM location FF. The product of $\mu\epsilon$ will be stored in coefficient RAM location FE (see Figure 2, b). See Figure 3 for coefficient loading consequence. Note that the RWE bit in the STATUS register will be set to 0 by AFP during the following DATA.H. loading. The coefficients must be stored in coefficient RAM consecutively from the smallest address up.

For multichannel operations, each channel shares a common filter type and length but have separate initial coefficients and μ 's. The 256 coefficient RAM will be divided into 2, 4, 8, 16, or 32 equal size blocks according to the number of channels. If the number of channels does not equal to 2, 4, 8, 16, or 32, the remainder blocks of RAM, that are not used should be left toward the highest coefficient RAM location (see Figure 2, b). The initial coefficient must be stored consecutively. The μ must be stored in the highest coefficient location at each RAM block. The $\mu\epsilon$ will be stored in the second highest coefficient RAM location at each RAM block. After MB86975 start run-

I = Information field U = user defined field IG = Ignored in this case

| REGISTER | ADDRESS | BIT POSITION | | | | | | | |
|----------------|---------|--------------------|----|----|---|----|----|-----|-----|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STATUS (read) | 0 | I | | IG | | I | I | I | I |
| STATUS (write) | 0 | | | IG | | | 1 | IG | IG |
| IOMODE | 1 | 0 | | U | U | | U | 0 | U |
| IOTIME | 2 | | | U | | | | U | |
| ALGCTRL | 3 | 0 | 0 | 0 | 0 | U | U | 0 | 1 |
| ORDER | 4 | VALUE | | | | | | | |
| SCNCH | 5 | U | | 1 | 1 | 1 | 1 | 1 | 1 |
| LKGRPSZ | 6 | U | | 0 | 0 | 0 | 0 | 0 | 0 |
| NBGRP | 7 | IG | | 1 | 1 | 1 | 1 | 1 | 1 |
| DATA | 8 | COEFFICIENT HIGH | | | | | | | |
| DATA | 9 | COEFFICIENT MIDDLE | | | | | | | |
| DATA | A | COEFFICIENT LOW | | | | | | | |
| RESERVED | B | IG | | | | | | | |
| RWCTRL | C | U | U | IG | | IG | IG | 1,0 | 0,1 |
| RESERVED | D | IG | | | | | | | |
| RESERVED | E | IG | | | | | | | |
| MODE | F | I | IG | | | | | 0 | 0,1 |

REGISTER ASSIGNMENTS

Figure 4

ning, the coefficient blocks will contain the updated coefficient for each tap. See Figure 5 for illustration.

Set up The Configuration Registers:

To make the MB86975 run properly, designers need to set up the configuration registers to serve their specific applications. Designers use the Register Address lines and Host Bus to write into any particular configuration registers. Figure 4 is one of the possible register configurations for a single chip adaptive FIR filter without the leakage control. This configuration contains 32 channels, 1 channel per group, and 32 groups total. Each channel processes a unique input data stream, and outputs a unique data stream. In Figure 4, the I stands for Information field. The MB86975 will provide certain information only if those situations ever occurred. The U stands for user define field. Designers can use these fields to define their specific applications. The IG stands for user can ignore these fields in the adaptive FIR filter operations. See the MB86975 data sheet for detail information about these registers. The next step is to turn the Mb86975 to the Run mode.

Turn MB86975 to the RUN mode:

After the configuration registers have been set up, designers need to write the filter order into the Order Register to specify the proper FIR filter order, write number of channels in NCH field (In our case it is 32 channels) in SCNCH register, set the CRE bit in the RWCTRL register to 0, and set the DRE bit in the RWCTRL register to 1 to accept input data. Lastly, designers need to turn the SR bit in the MODE register to 1, to start the MB86975.

References

The following is a representative of the common reference available for adaptive FIR digital filters.
Widrow B., and Stearns S. D., Adaptive Signal Processing. Englewood Cliffs, N.J.: Prentice-Hall, Inc., 1985.

For further information about the MB86975, please refer to

1. Adaptive Filter Processor data sheet.
2. Adaptive Filter Processor Support Tool data sheet.