A High-Speed LSI GaAs 8 × 8 Bit Parallel Multiplier

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Abstract—**Multiplication is frequently the speed-limiting function in digital signal processing systems. High-speed hardware multiplier IC's can therefore greatly enhance the throughput and bandwidth of many digital systems. In this paper, the design, fabrication, and performance of GaAs parallel multipliers are discussed. The largest of these circuits, an 8 × 8 bit multiplier, has 1008 gates, and is by far the most complex GaAs IC demonstrated today. This multiplier forms the 16 bit product of two 8 bit input numbers in 5.25 ns. This corresponds to an equivalent gate propagation delay of 150 ps/gate. The power dissipation ranges between 0.6–2 mW/gate.**

I. Introduction

GALLIUM arsenide has been utilized extensively over the last several years for low noise microwave amplification. Metal-semiconductor field-effect transistors (MESFET's) with 0.5–1.0 μm gate lengths have become available from several sources in manufacturing quantities, and the GaAs FET has virtually replaced all competing small-signal amplifier devices in the upper microwave region (8–18 GHz).

During the last four years, there has been a growing interest in the use of GaAs for digital integrated circuits. This is due largely to the high electron mobility and drift velocity of GaAs at room temperature and to the high resistivity (10^8 $\Omega \cdot$ cm) exhibited by GaAs when compensated with Cr or other deep level acceptors. This semi-insulating GaAs is available as a suitable substrate which can be used for direct ion implantation of active devices. The high resistivity of Si GaAs is also helpful in minimizing interconnect capacitance in an IC. The high mobility and drift velocity of electrons yield FET's with high f_τ (current gain-bandwidth products) which is directly related to switching speed ($\tau_d \geqslant N/\pi f_\tau$ where N is the number of identical devices being driven). Very high switching speeds, approaching those of Josephson junction devices, have been demonstrated for GaAs logic employing short channel (L_g = 0.6 μm) Schottky gate MESFET's, with τ_d = 17 ps at 77 K or τ_d = 30 ps at room temperature being reported [1]. Maximum clock frequencies as high as 5.5 GHz have also been observed on GaAs binary frequency divider circuits [2].

The Schottky-barrier gate field effect transistor (MESFET) is the main active device used in most GaAs integrated circuits to provide current gain and inversion. The f_τ of a FET ($f_\tau = g_m/(2\pi C_{gs})$) is dependent on the transconductance g_m, which is proportional to either the electron mobility μ_n or the saturated drift velocity v_s. C_{gs}, the gate-source capacitance, is approximately equal for Si and GaAs MESFET's. The performance margin to be expected over silicon FET's (MESFET or NMOS) depends critically upon which model is believed to correctly apply to a large or very large scale (LSI or VLSI) integrated circuit composed of large numbers of GaAs or Si devices. The mobility model predicts about six times higher g_m for GaAs than silicon for equivalent device geometries, while the velocity saturation model implies only a factor of 1.5–2 difference in g_m at high electric fields [3]. The mobility model certainly applies to very low pinchoff (threshold) voltage devices ($V_p < 0.5$ V), while the velocity saturation model is applicable to high pinchoff voltage (>2 V) devices such as discrete microwave MESFET's operating as Class A amplifiers. The switching FET used for low power GaAs logic has a pinchoff (threshold) voltage of ~1 V intermediate between the values that assure pure mobility and pure saturation regimes. Since the device switches between on and off states, it operates in a mobility-controlled regime for a fraction of a cycle and in saturation for another fraction. Velocity overshoot of electrons accelerated in the high mobility conduction band central valley before they transfer to the lower satellite valleys tend to increase switching speeds, the effect being more appreciable for short gate (~0.5 μm) devices

In view of the complexity of the models, it becomes attractive to compare GaAs and Si FET devices in a practical manner. Fig. 1 shows experimental curves of saturated drain current versus gate voltage at fixed drain voltage for GaAs MESFET's of 0.5 μm and 1.0 μm gate length [4], and for Si MESFET's [5], [6] (1 μm) and n-channel MOSFET's (NMOS) [7], [8] of 0.7 and 1.3 μm channel length.

All the curves in Fig. 1 start being nearly parabolic at the origin, and tend to become linear only at high gate voltage due to current saturation. However, logic devices for VLSI circuits are or will be required to operate at moderate voltage swing (<1 V) between "off" and "on" states. In this region of the characteristics (between 0 and 1 V), the curves show that mag-

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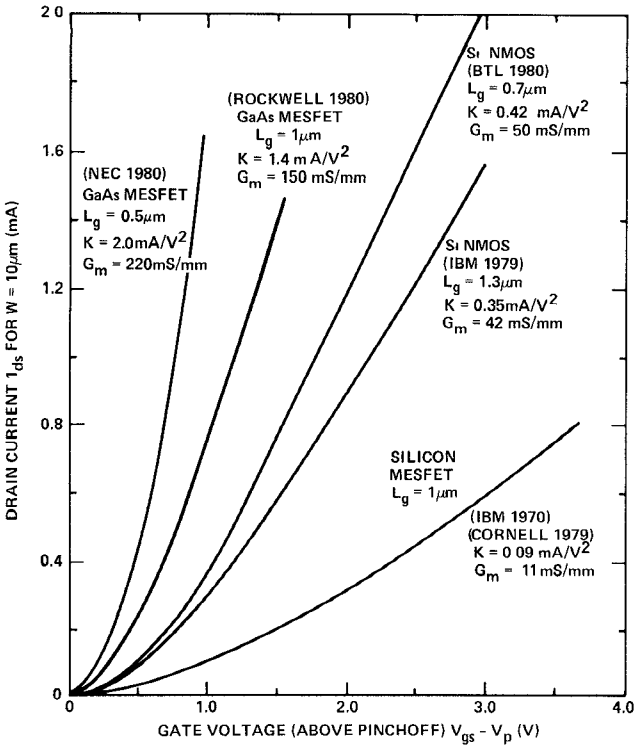


Fig. 1. Drain current versus gate voltage (at fixed drain voltage) for a number of GaAs and Si FET devices (MESFET's and MOSFET's). The gate voltages are measured from pinchoff (threshold).

nitude of the drain current is mainly determined by the semiconductor mobility, while the onset of velocity saturation has only a small corrective effect.

Comparing MESFET's in Fig. 1, GaAs and Si devices both approximately exhibit a square law dependence for drain current as a function of gate voltage ($I_{ds} = K(V_{gs} - V_p)^2$), but with greatly differing K values as would be predicted from the higher GaAs mobility. Drain currents also differ by about a factor of six. Silicon NMOS devices outperform Si MESFET's of equal gate length because the gate oxide can be made quite thin (200-300 Å), and thus the capacitive coupling of the gate to the channel is more effective for the MOSFET than is the MESFET. However, the K factor of the 0.7 μm NMOS device is still nearly two times smaller than the 1 μm GaAs MESFET, and over three times smaller than the 0.5 μm GaAs MESFET.

These performance margins favor GaAs, justifying continued development of GaAs MESFET devices for high-speed LSI integrated circuit applications and exploration of other GaAs-based high-speed device types to exploit even further potential performance advantages. The application of GaAs IC's to high-speed circuit requirements (digital multipliers, frequency synthesizers, A/D and D/A conversion, etc.) will provide the driving force for this continuing development.

The following section in this paper describes the IC material and fabrication technology and circuit design approaches used to build a GaAs high-speed parallel multiplier chip. Section III covers circuit design. The measurement techniques are discussed in Section IV, followed by a discussion of results in Section V. The data from both the 5 bit and 8 bit versions of the multiplier circuit show significantly improved performance over comparable silicon-based multipliers. The 8 bit version, containing over 3000 transistors and 3000 diodes, gave the 16 bit product in approximately 5 ns, while dissipating about 2.5 W of power.

II. GaAs Material Requirements and Fabrication Approach

The circuit fabrication utilizes localized implantation of Se and Si ions directly into semi-insulating GaAs substrates. In comparison with the use of epitaxial layers, this doping technique has lower cost and allows greater circuit flexibility. Also, isolation between adjacent devices is automatically obtained with the unimplanted regions of the substrate. As in Si technology, ion implantation in GaAs is advantageous from the standpoint of control over the doping characteristics in the device active layers. In Schottky diode-FET logic (SDFL) LSI circuits [9], a high degree of control is required over the gate threshold voltage, and consequently, over the doping concentration and thickness of the FET channel layers, which directly influences the pinchoff voltage of the transistors. It has been found at our laboratory that with ion implantation, the required doping control may be obtained uniformly over entire wafers and reproducibly over extended periods of time. In the development of this high yield implantation process, it has been found important to: 1) utilize GaAs substrates with low concentration of residual impurities incorporated during growth, and 2) maintain the purity and stoichiometry of the GaAs during the postimplant anneal (850°C). The first of these objectives may be met with Cr-doped Bridgman-grown substrates, provided attention is given to selection of ingots which have the desired purity; alternately, substrates grown by the liquid encapsulated Czochralski (LEC) techniques may be used. It has recently been shown that the LEC process can lead reproducibly to ingots with very low concentrations of background impurities (for example, residual Si concentrations can be reproducibly below 2×10^{15} cm^{-3}). At the same time, the process yields round wafers with large and well-controlled diameters up to 3 in. LEC GaAs substrates which are semi-insulating may be reproducibly produced with or without the addition of Cr or other deep acceptor impurity to the melt. Bridgman and LEC (both Cr-doped and undoped) substrates were used in this work, with excellent results for all three types of material.

In order to maintain the GaAs surface stoichiometry during the postimplant anneal, a thin layer of reactively sputtered Si_3N_4 is used as an encapsulant. This layer is deposited prior to the implant, immediately after chemical cleaning of the GaAs surface, and is maintained throughout all high temperature processing, so that surface impurity contamination is minimized.

The uniformity (over a wafer) and reproducibility (run-to-run) of the implantation process are evident in the statistics of pinchoff voltage of test FET's. An array of 72 uniformly distributed test FET's has been incorporated into each wafer processed for SDFL logic circuits (of dimensions 1 X 1 in), and automatically probed for process monitoring [10]. Fig. 2 shows a histogram of pinchoff voltage V_p obtained across a

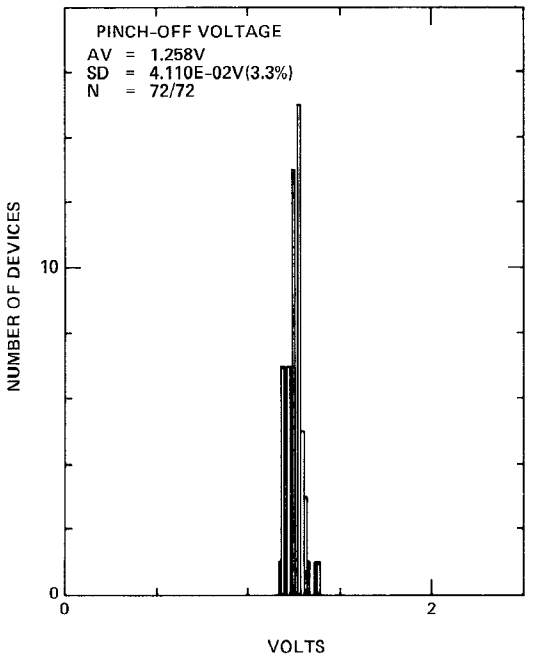


Fig. 2. Histogram of pinchoff voltages for 72 test MESFET's distributed over a 1 × 1 in wafer. This histogram highlights the uniformity of the implanted channel layers.

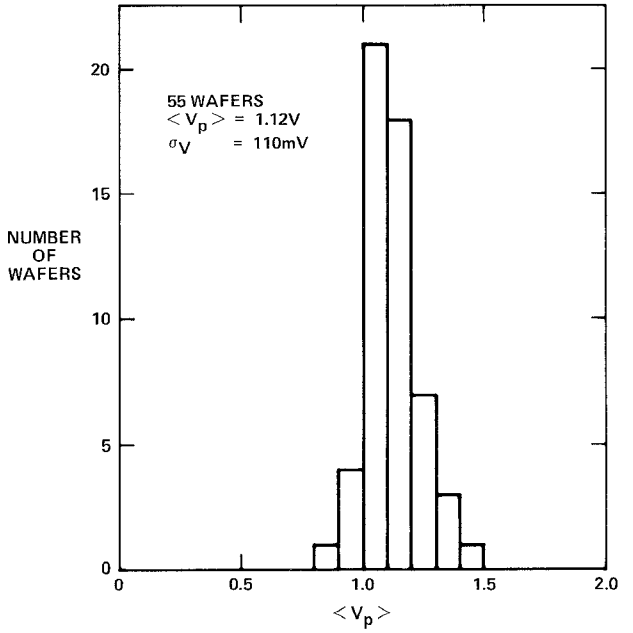


Fig. 3. Histogram of average values of MESFET pinchoff voltage for 55 wafers representing 14 separate runs on material from eight different ingots processed over a six month period. This histogram documents the reproducibility of the ion implantation process.

typical wafer, indicating the high degree of uniformity. The standard deviation of V_p for this wafer is 41 mV.

LEC wafers have been found to provide more uniform behavior than Bridgman substrates; for the LEC substrates, a standard deviation of pinchoff voltage as low as 34 mV has been observed, while the median standard deviation (over a sample of 24 processed wafers from three different ingots) was found to be 54 mV. By comparison, using Bridgman-grown substrates, the standard deviations of pinchoff voltage have been as low as 40 mV, but the median standard deviation has been 85 mV (over a distribution of 31 processed wafers from five ingots). In both cases, however, the uniformity is more than sufficient to permit high yields of LSI SDFL circuits.

The run-to-run reproducibility of the channel doping process is evident in the distribution of FET pinchoff voltage (averaged over entire wafers) obtained over a period of time. Fig. 3 shows a histogram of pinchoff voltage for 55 SDFL wafers processed in 14 separate runs over a period of approximately six months. Wafers from five Bridgman ingots and three LEC ingots are represented. The standard deviation of this distribution is 110 mV, again well within the limits required for high yield manufacturing. To obtain this reproducibility of V_p using numerous GaAs ingots, the channel implant fluences were selected (over the range of $2.1\text{-}2.6 \times 10^{12}$ cm^{-2}) for each lot, using information obtained from samples of the GaAs substrate under process.

Fabrication of the SDFL circuit is accomplished by a planar technique [11] which employs two different implants in order to optimize the doping profiles for both the low capacitance (deep implant) switching diode and the low pinchoff voltage (shallow implant) MESFET. The implantation into the substrate is carried out through a thin Si_3N_4 dielectric layer which protects the semi-insulating GaAs substrate throughout the entire process. The 1 μm MESFET gate length is achieved optically using 4× projection lithography. Two levels of metallization are used. The first-level metal, utilized for Schottky barriers as well as first layer interconnects, is defined by a photoresist liftoff procedure. The second level metal is fabricated using ion milling. Isolation between the upper and lower metal layers is provided by plasma-deposited Si_3N_4.

III. GaAs IC Parallel Multiplier Circuit Design

The basic gate utilized in the design of the high-speed multipliers is the SDFL NOR gate shown in Fig. 4. In this gate, the logic OR function is performed by the very small area switching diodes (D_A - D_D). The active load pull-down (*PD*) provides the additional level-shifting diode (*DS*) provide the desired logic level shifting from the positive logic polarities at the FET drain to the negative FET gate voltages. The depletion mode MESFET Q_1 with its active pull-up (*PU*) provides inversion and gain. Since the input logic OR function is provided by the very low capacitance (2 fF) and small area (1 × 2 μm) Schottky diodes, input expansion can be easily achieved without much sacrifice in speed and device area.

Gate propagation delays between 62 and 130 ps, with power dissipation between 0.12 and 1.5 mW/gate, have been measured on SDFL NOR gate ring oscillators using gate widths ranging from 3 to 20 μm [12]. These propagation delays have been maintained on MSI integrated circuits as well. For example, three-stage *T*-connected *D* flip-flop (DFF) ripple divider circuits which operate at a 1.9 GHz clock input frequency have been demonstrated. Since the maximum operating frequency of the DFF is 1/5 τ_d, the 1.9 GHz clock input frequency corresponds to a propagation delay of 110 ps/gate, which is in good agreement with the ring oscillator results.

For the design of the 5 × 5 and 8 × 8 multipliers, a parallel

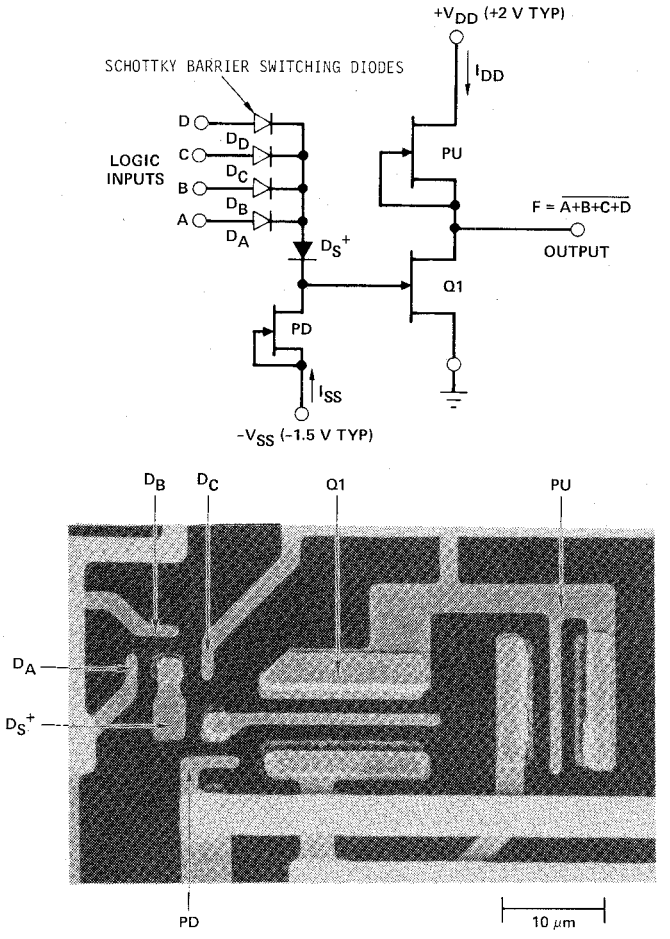


Fig. 4. Schematic and SEM micrograph of an SDFL NOR gate.

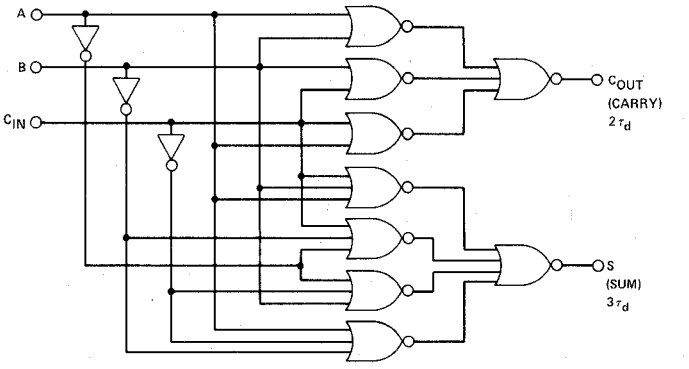


Fig. 5. Logic diagram of a full adder cell.

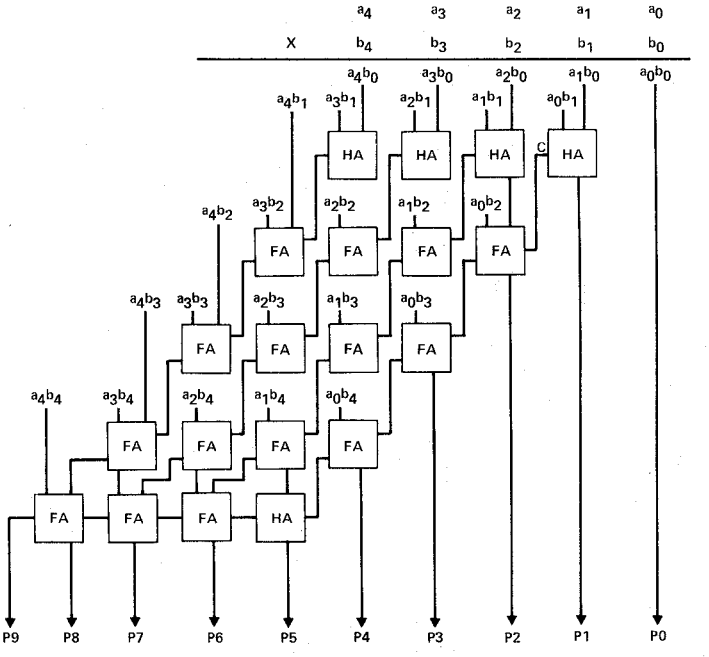


Fig. 6. Logic diagram of the 5 X 5 bit parallel multiplier.

array architecture was selected, primarily because of its modular and repetitive layout. Although there are architectures that are inherently faster, their interconnection pattern is quite complicated, requiring long layout design time. What was desired was a test vehicle circuit with LSI complexity that would demonstrate the material and lithographic processing capability, but for which the layout design time would be short. The array multiplier meets these criteria, and serves as a benchmark circuit for speed comparison as long as the actual number of gates in the delay path is accounted for. An $N \times N$ array multiplier comprises $N(N-2)$ full adders and N half adders in its implementation; the $2N$ bit product is available after a maximum of $(N-1)$ sum delays and $(N-1)$ carry delays. Since the delays can be related to individual gate delays, speed measurements can be made on an array multiplier implementation and can be used in predicting the performance of other multiplier architectures (employing, e.g., carry lookahead or Wallace tree approaches), while saving considerable layout design time.

Since the fundamental component of an array multiplier is the adder cell, the speed of the adder dictates the multiply time. The logic diagram for a full adder is shown in Fig. 5. The full adder adds three 1 bit numbers to produce a sum and a carry bit as outputs. Implemented with 12 NOR gates, this circuit provides the carry output in 2 τ_d and the sum output in 3 τ_d where τ_d is the propagation delay of a single NOR gate. A half adder that adds two 1 bit inputs requires half as many NOR gates as the full adder, but has the same carry and sum delays (2 τ_d and 3 τ_d). Adders with fewer propagation delays can be realized using two-level logic gates (OR/NAND, AND/NOR); as in the choice of architecture, the straightforward NOR implementation was used for this design to minimize design time, since readily interpreted results could be obtained.

A 5 X 5 parallel multiplier was designed using the full adder (*FA*) cell shown in Fig. 5. Half adders (*HA*) were also realized using NOR gates. A block diagram of the 5 X 5 adder array is shown in Fig. 6 with 15 full adders and 5 half adders being used to form the 10 bit product. Partial products $a_i b_j$, which are required as the input terms to the adders, were formed by inverting and "NORing" the input bits. The 5 X 5 multiplier chip included 260 gates and required only 1.1 X 1.3 mm of chip area, including all of the bonding pads.

An 8 X 8 bit parallel multiplier has also been designed using the same combinatorial array approach. In this case, 48 full adders and 8 half adders were required to form the 16 bit product. In addition to the array, input and output latches (*D* flip-flops) were also included so that the circuit could be

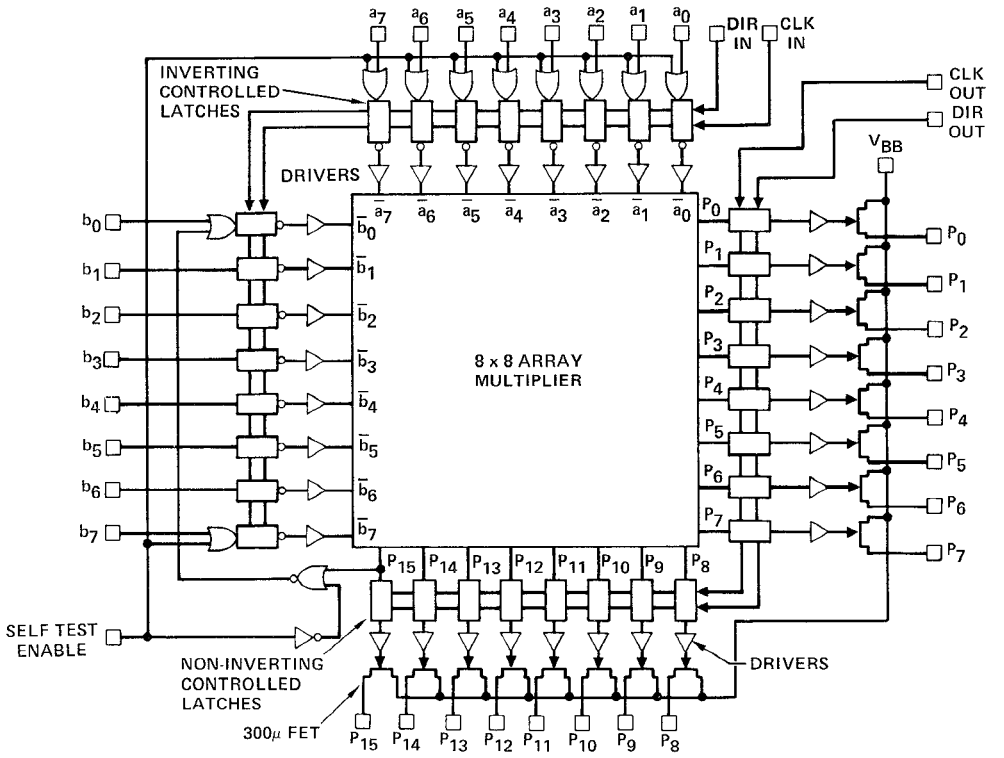


Fig. 7. Block diagram of the 8 X 8 parallel multiplier. The self-test feedback path is shown in this figure.

	a_6	a_5	a_4	a_3	a_2	a_1	a_0	
b_0	ICL	ICL	ICL	ICL	ICL	ICL	ICL	ICL	
b_1	ICL	HA	HA	HA	HA	HA	HA	HA	NICL
b_2	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_3	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_4	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_5	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_6	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
b_7	ICL	FA	FA	FA	FA	FA	FA	FA	NICL
a_7	ICL	FA	FA	FA	FA	FA	FA	HA	NICL
	NICL	NICL	NICL	NICL	NICL	NICL	NICL	NICL	NICL

Fig. 8. Computer-generated layout diagram of the 8 X 8 multiplier LSI chip. The very modular nature of the array architecture allowed the design to proceed with a high level of confidence in elimination of all errors.

more readily interfaced in synchronous systems. The latches are separately clocked for inputs and outputs, and can also be disabled, or made transparent, to facilitate asynchronous testing. A block diagram of the 8 X 8 bit multiplier is shown in Fig. 7. This circuit implementation required 1008 NOR gates (about 3000 FET's and active loads and 3000 diodes). This level of complexity clearly qualifies this multiplier as a GaAs LSI chip and also as the *most* complex GaAs IC demonstrated to date.

The layout is organized as a completely modular array (see Fig. 8). A central array of full and half-adder cells is surrounded by latch cells—input latch cells on the top and left sides, and output latch cells on bottom and right sides. Bus lines, internal bit line drivers, and output buffers are also modular cells. The cell dimensions were made such that the cells were simply stack-arrayed to form the chip, complete with interconnections. Digitizing and layout were done on a CALMA GDS II system. The number of different circuit cells was minimized

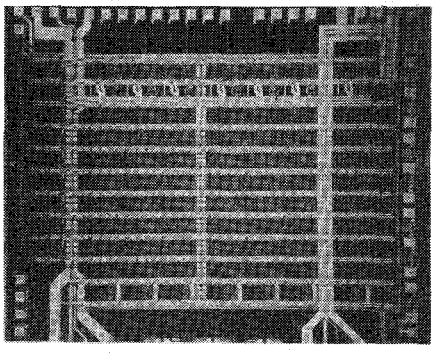


Fig. 9. Photomicrograph of the 8 X 8 multiplier chip. The chip, including bonding pads, covers a 2.7 X 2.25 mm area.

in order to reduce the probability of design error by allowing for exhaustive checking of a limited number of cells. This approach is essential to the efficient design of error-free LSI chips and, in fact, yielded a completely functioning LSI chip on the first mask set. The complete 8 X 8 parallel multiplier circuit measures 2.7 X 2.25 mm, including bonding pads. A photograph of a multiplier chip is shown in Fig. 9. Gate density, excluding pads, was about 33 000 gates/cm^2 for this circuit.

IV. GaAs IC Parallel Multiplier Evaluation

The 5 X 5 and 8 X 8 bit multiplier chips were fabricated using the planar, directly implanted process described in Section II. Chips were evaluated at wafer probe for functionality at low speeds using an automatic data acquisition system, and for high-speed performance using on-chip test circuitry.

Functionality testing was carried out at two levels—ripple testing and exhaustive testing. Exhaustive testing is done using all input data combinations, and is required to assure that all gates are working. Ripple testing is accomplished by applying a square-wave input to one of the input bit lines; if a judicious choice is made for the remaining inputs bit values, the square wave can be made to ripple through various paths of the adder array. Specifically, the worst case delay path by performing the products 31 X 16 and 31 X 17 for the 5 X 5 multiplier or 255 X 128 and 255 X 129 for the 8 X 8 multiplier where the least significant (b_0) input was driven by a square-wave pulse generator. For the 8 X 8 multiplier, the following multiplication is performed:

$$\begin{array}{l} A = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\ B = 1\ 0\ 0\ 0\ 0\ 0\ 0\ b_0 \\ \hline b_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 \\ 1\ 1\ 1\ 1\ 1\ 1\ 1\ 1 \\ \hline b_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0 \bar{b}_0\ \ \bar{b}_0 b_0 b_0 b_0 b_0 b_0 b_0 b_0 \end{array} . \quad (1)$$

The ripple test was used for prescreening chips, and to study bias sensitivities. Chips which passed the initial ripple test screening were subjected to a complete functionality test using a microcomputer to provide input data bits and to read the output product bits. The measured product was compared with the expected $A \times B$, and errors were flagged to allow any design or fabrication defects to be localized. This requires a

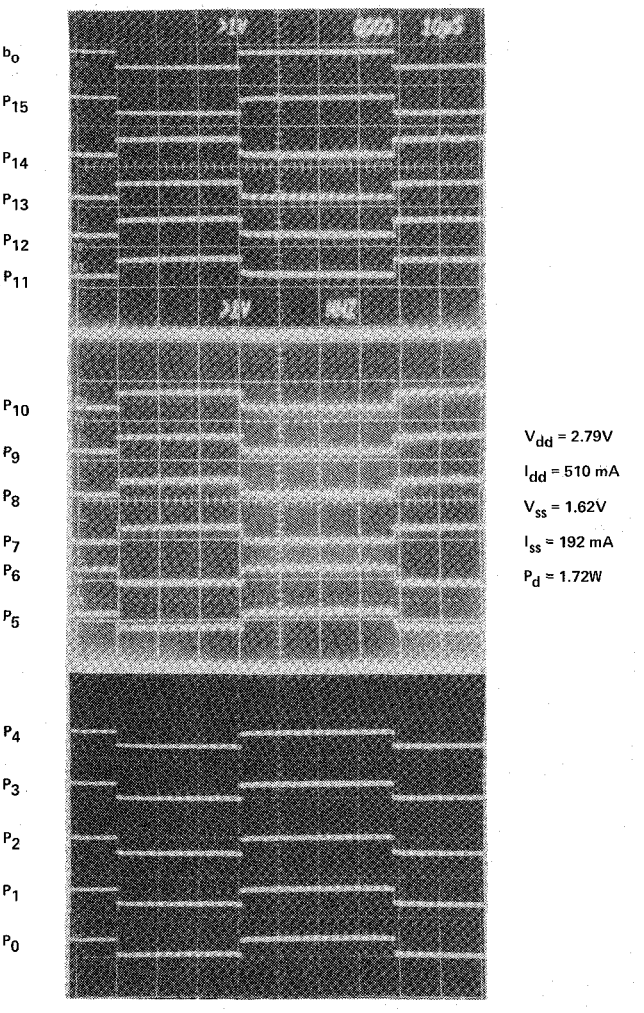


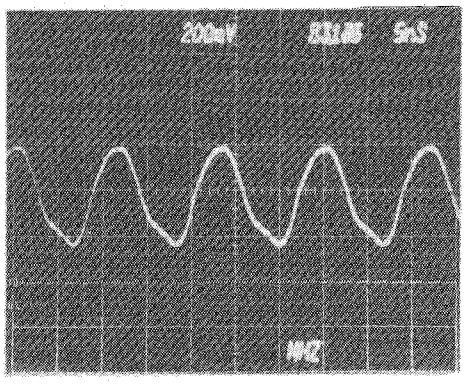
Fig. 10. Ripple (asynchronous) test of 8 X 8 multiplier with square-wave input at b_0.

total of 2^{10} (1024) input combinations for the 5 X 5 multiplier and 2^{16} (65 536) for the 8 X 8 multiplier to be automatically inspected. Test time for an 8 X 8 chip was approximately 20 min.

Evaluation of the high-speed performance was facilitated by the use of an on-chip feedback path which routes the complement of the most significant product bit (P_9 or P_{15}) to the least significant (b_0) input bit. This connection is unstable, as can be seen from the above multiplication (1), and results in an oscillatory condition which exercises 85 percent of the adders and their sum and carry propagation paths through the combinatorial array.

The oscillation period is determined by the time required by the signal to propagate through the loop. It turns out that changing bit b_0 (from 1 to 0 or 0 to 1) involves the second longest delay path through the multiplier array; the delay to the most significant product bit (P_{15}) is six sums and eight carries or a total of 34 τ_d.[1] Adding the delays caused by the control gates and the latch gates when operating with the

[1] The longest (data) delay path is 35 τ_d, from b_0 to the second most significant product bit, since it involves one less carry at 2 τ_d and one more sum at 3 τ_d.



V_{dd} = 2.72V f = 83.1 MHz τ_d = 150 ps

V_{ss} = -2.03V P_d = 2.08W $P_d\tau_d$ = 310 fJ

Fig. 11. Output waveform of the 8 X 8 multiplier when evaluated for high-speed operation in the self-oscillation mode. The on-chip feedback path was enabled and the latches disabled to perform measurement. Rise and fall times were limited by the test fixture interconnections which acted as a low-pass filter.

latches disabled or transparent, the half-period of oscillation in the test mode is 40 τ_d. In the 5 X 5 bit multiplier design, the corresponding path delay is 22 τ_d. By measuring the oscillation frequency, then, one is able to infer an average gate delay τ_d.

High-speed performance evaluation utilized the on-chip feedback test mode described above. In the case of the 8 X 8 multiplier, latches were disabled for the test so that the multiplier would function asynchronously. Latch performance was verified by independent synchronous tests. Fig. 8 illustrates the oscillation waveform observed in the self-test mode for the 8 X 8 bit multiplier. The oscillation frequency observed was 83.1 MHz, which corresponds to a propagation delay of 150 ps/gate. At this speed, a full 16 bit product would be available every 5.25 ns.

The observed performance of the two multiplier circuits is summarized in Table I. Power dissipation of the multiplier circuits varied with wafer pinchoff voltage and biasing voltages. Typical circuits operated normally at V_{DD} = 2.7 V and V_{SS} = -1.5--2.0 V. Chip yields as high as 25 percent were obtained for completely functional 5 X 5 bit multipliers, a 260 gate MSI/LSI circuit.

No significant differences in operating speed or chip yield have been observed among circuits fabricated using Bridgman-grown (Cr-doped) or LEC-grown (Cr-doped or undoped) substrates.

It is noteworthy that no impairment of circuit yield was observed due to dislocations in the substrate. On at least several wafers, dislocation densities were as high as 2×10^4 cm^{-2}. Assuming a random distribution of dislocations, it may be estimated that the probability that no critical circuit area is intersected by a dislocation is on the order of 10^{-1} for the 5 X 5 multiplier and of 10^{-3} for the 8 X 8 multiplier. Since these probabilities are significantly below observed yields, it may be concluded that the circuits are at least somewhat tolerant to the presence of dislocations in critical areas (where we have counted as critical areas the regions underneath the gates on the transistors and active load and the Schottky metal-covered regions of the switching diodes).

TABLE I
PERFORMANCE SUMMARY OF THE 5 X 5 BIT AND 8 X 8 BIT GaAs IC PARALLEL MULTIPLIER CIRCUITS

Multiplier	Power Dissipation		Propagation Delay/Gate		Multiply Time
	Minimum[a]	Maximum[a]	Minimum	Typical	
5 X 5 bit (260 gates)	43 mW	310 mW	190 ps	210 ps	3.8 ns
8 X 8 bit (1008 gates)	0.61 W	2.2 W	150 ps	175 ps	5.25 ns

[a]Range of power dissipation shown reflects variations from wafers with different pinchoff voltage.

V. DISCUSSION

An 1008 gate 8 X 8 parallel multiplier has been successfully designed and fabricated using a parallel (array) multiplier architecture chosen over faster architectures for ease of design and layout. A multiply time of 5.25 ns has been achieved. This result brings the GaAs technology into the realm of LSI, while advancing the state of the art for multiplier chips. The multiplication time obtained corresponds to a propagation delay of 150 ps/gate, which is in good agreement with the results of much simpler GaAs SDFL circuits such as ring oscillators and frequency dividers. This high speed of operation indicates that the extension of the planar SDFL circuit approach to the LSI level of complexity does not necessarily result in any significant speed degradation. The low power dissipation observed on the 5 X 5 and 8 X 8 multipliers also indicates that the SDFL approach is a suitable candidate for the VLSI range of complexity.

The performance indicated above was obtained for an array multiplier architecture for which the longest (data) delay path is 35 τ_d. As indicated earlier, it is possible to implement inherently faster architectures. A Wallace tree implementation reduces the number of delays in the adder array. For larger multipliers, Booth's algorithm recording (by 2 bits) reduces delays [13]. Then, use of a carry lookahead (CLA) adder to form the final sum eliminates many delays. If these features were incorporated into a GaAs multiplier using the adder from the circuit herein described, the longest delay path would be 15 τ_d. For such a multiplier, the 16 bit product would be available every 2.25 ns. This performance represents significant speed improvement over the fastest silicon 8 bit multiplier [14], [15]. Table II lists the best silicon multipliers available for comparison.

A question often raised is whether GaAs IC reliability will be a problem. The question is very legitimate because GaAs IC reliability has not been adequately explored yet. However, there is a wealth of reliability information available from discrete GaAs MESFET devices [16], [17] which have been on the market for several years. The studies show that the weakest fabrication step is, from a reliability standpoint, the alloyed

TABLE II

Manufacturer	Part No.	MPY Time (16 Bit Product)	PWR	Chip Org.	No. Chips 8 X 8 MPR
Motorola	MC109-1 (ECL)	19 ns	4.4 W	8 X 8	1
AMD	2505	76 ns	4.8 W	4 X 2	8
TRW	MPY-8HJ-1	45 ns	1.0 W	8 X 8	1
TRW	MPY-8AJ	130 ns	1.8 W	8 X 8	1
Motorola	10287 (ECL)	25 ns	11 W	2 X 1	28
Motorola	10183	50 ns	6 W	4 X 2	14
Rockwell	GaAs Array (Measured)	5.25 ns	≃1 W	8 X 8	1
Rockwell	GaAs Wallace Tree Booth's Algorithm, CLA Adder (Projected)	2.25 ns	≃1 W	8 X 8	1

ohmic contact metallization. However, these studies also show that the contacts can be made quite reliable with 10^8 h mean time to failure predicted at 80°C [16]. Since the same metallization is used for GaAs IC's, no insurmountable reliability problem is expected.

The future system applications of a gigabit digital circuits are possible at all levels of integrations. At SSI and MSI levels, the GaAs IC will find its application in frequency measurement (prescaler, variable modulus counter), high-speed data storage (latches shift, registers), serial parallel data conversion (multiplexer, demultiplexer), secure communication (*P/N* code generator), etc. A broad range of applications will be achievable as complexity increases through the LSI range and into the VLSI range. This will allow such systems as signal processors, microwave frequency synthesizers, high-speed A/D converters, and arithmetic systems to be built on a single chip in more efficient architectures than are currently achievable. The performance of the 8 X 8 multiplier clearly demonstrates the feasibility of the SDFL design for a high-speed LSI/VLSI technology.

Acknowledgment

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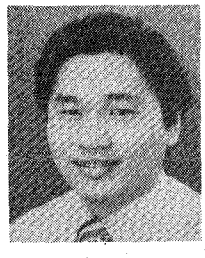

Frank S. Lee received the B.S. degree in electrical engineering from the National Cheng-Kung University, Taiwan, in 1971, and the M.S. and Ph.D. degress in electrical engineering from Southern Methodist University, Dallas, TX, in 1974 and 1978, respectively.

During 1974 he worked as a Research Assistant in the study of thermal electrical power and temperature coefficient of resistivity of Au–Ag alloy thin films. While pursuing the Ph.D. degree, he developed a group of low-pass filters by utilizing the properties of Cesäro summations to improve the convergence of infinite summations. He is presently a member of the

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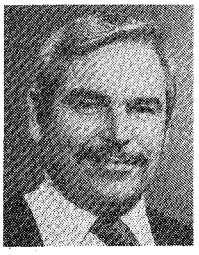

George R. Kaelin (S'57-M'62) was born in Los Angeles, CA, on May 27, 1936. He received the B.S., M.S., and Ph.D. degrees in electrical engineering, from the University of California, Los Angeles.

After receiving the M.S. degree, he was on a work-study program with Litton Industries in the Display Laboratory of the Data Systems Division. His Ph.D. dissertation was completed on a Graduate Study Fellowship from Litton, and comprised measurements of paramagnetic relaxation times in ionic crystals involved with the interaction of radiation and matter. After receiving the Ph.D., he began a program at Litton to investigate military display applications for light-emitting diodes. The result of that program, funded partially by the U.S. Army and the U.S. Air Force, was an integrated modular structure with LED's, driver circuitry, and memory, for which he received a patent. In 1973 he joined Motorola's Government Electronics Division. There he carried out development work on integrated driver circuits for plasma panel displays, ultimately resulting in an airborne plasma panel display terminal for the Navy's TACAMO program. He also designed deflection amplifiers and other circuits for Motorola's military CRT display terminal. More recently at Motorola, was investigating architectures, circuits, and integrated circuit processing technologies for video data processing systems and data links. He was primarily involved with investigating CCD implementations, and started a program to develop a combined CMOS and CCD IC technology. He was also involved in the design of an 8 bit video A/D converter, made in the MECL technology, and an arithmetic processor in CMOS. Since joining Rockwell International/Electronics Research Center, Thousand Oaks, CA, as a member of the Technical Staff in 1979, he has been involved in the design and development of low power high density GaAs digital integrated circuits.

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Bryant M. Welch (M'75) was born in New York, NY, on December 20, 1943. He received the A.A. degree in engineering from Miami Dade Junior College, Miami, FL, in 1963, and the B.S. degree in mathematics from the California State University, Northridge, in 1968.

From 1963 to 1965 he was associated with Westinghouse Electric Corporation, where he was involved in the early development of Si bipolar integrated circuits. Since 1965 he has been employed with Rockwell International, Thousand Oaks, CA, and is presently the Project Leader for integrated circuit processing. His areas of research and development have included all phases of ion implantation in both Si and GaAs. Since 1972 he has concentrated on the development of a planar GaAs ion implantation technology. Highlights of his work include the development and fabrication of GaAs FET's using implanted active layers, and fabrication of the first planar GaAs integrated circuits using multiple localized implantation techniques. He is currently involved with developing planar GaAs integrated circuit processes and is responsible for the fabrication of these circuits. He holds two patents and has numerous publications in the field of ion implantation and its application.

Mr. Welch is a member of the Electrochemical Society.

R. Zucca (SM'78) was born in Trieste, Italy, on February 7, 1936. He received the M.S. degree in engineering from the University of Rosario, Argentina, in 1960, and the Ph.D. degree in physics from the University of California, Berkeley, in 1971.

He initiated his research at Berkeley in the investigation of optical properties of solids by modulation techniques, making contributions to the understanding of the band structures of IV and III-V semiconductors and noble metals. Later he held a position of Professor in Physics at the University at Rosario, Argentina. Since joining Rockwell International, Thousand Oaks, CA, in 1972, he has been engaged in several aspects of semiconductor technology, focusing mainly on the electrical properties of semi-insulating GaAs, the substrate material for most GaAs high-frequency semiconductor devices. Most recently, he has been involved in the development of a high-speed, low-power planar GaAs digital IC technology with potential for LSI/VLSI applications. His work involves the development and application of testing techniques for process characterization and evaluation.

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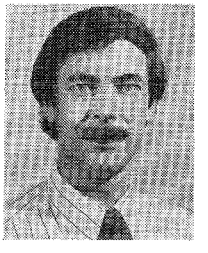
E. Shen received the B.S. degree in electrical engineering from National Taiwan University, Taiwan, China, and the M.S. degree, also in electrical engineering, from Stanford University, Stanford, CA.

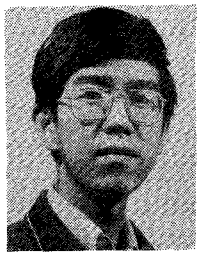
She worked at the Amdahl Corporation on designing software to perform timing analysis along critical paths of the CPU of the Amdahl 470 computer in order to determine the proper cycle time of the CPU. She then joined American Microsystems, Inc., where she designed and implemented an interactive logic simulator with a logic circuit description editor. Following this, she worked at the Intel Corporation on software development of circuit analysis programs for computer-aided IC design. She is presently a Senior Staff Associate in the IC Group of the GaAs Electronic Device Research Department, Microelectronics Research and Development Center, Rockwell International, Thousand Oaks, CA.



Peter Asbeck (M'75) received the B.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1969 and 1975, respectively.

As part of the M.I.T. Cooperative Program, he worked in far infrared spectroscopy and studied electrochromism at RCA Laboratories, Princeton, NJ. His thesis research dealt with the preparation and physics of PbSe homojunction lasers. Prior to joining Rockwell International, Thousand Oaks, CA, he worked at Philips Laboratories, Briarcliff Mannor, NY, where he was concerned with the characterization, physics, and applications of (Ga, Al)As double heterostructure lasers. Recently he has been active in the area of ion implantation in semiconductors, particularly in the relationship between implant behavior and substrate characteristics.

Dr. Asbeck is a member of the American Physical Society.



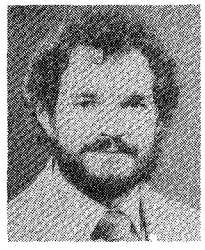
Chien-Ping Lee was born in Taiwan, China, in 1949. He received the B.S. degree in physics from the National Taiwan University in 1971, and the Ph.D. degree in applied physics from the California Institute of Technology, Pasadena, in 1978.

While at Caltech, he worked on GaAs based integrated optics. He was credited with the design and fabrication of several important optoelectronic components, including the first injection lasers on semi-insulating substrates and the integrated laser-Gunn device. After graduation, he joined Bell Laboratories, working on integrated optics and semiconductor lasers. He joined the GaAs Integrated Circuits Section of Rockwell International, Thousand Oaks, CA, in 1979 and since then has been involved in characterization and evaluation of GaAs integrated circuits.

C. G. Kirkpatrick (S'69-S'74-M'74-SM'79) received the B.S. degree in physics in 1969 and the A.M. degree, also in physics, in 1970, both from Washington University, St. Louis, MO, and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana, in 1974.

While at Washington University, she worked on programs which involved the development of techniques for studying radiation damage through track etching and microscopy in meteorites and lunar samples and studies of possible nonlinearities. Her thesis work at the University of Illinois was a study of radiation damage in silicon resulting from ion and electron irradiation by means of photoluminescence and electrical measurements. She held the Zonta International Amelia Earhart Fellowship during 1972-1973. In 1974 she joined the Corporate Research and Development Center, General Electric Company. Her research in that laboratory centered on beam (ion, electron, and laser) effects in semiconductors studied through a variety of analytical techniques especially electron microscopy (EBIC). The development of beam-addressed memory devices utilized the findings of these studies, and she holds five patents in this area. Her work at General Electric also entailed other applications of beams for imaging and display devices, electron lithography and microscopy, ion implantation, and laser and electron beam annealing. In 1979 she joined Rockwell International, Thousand Oaks, CA, where her work has involved ion implantation, beam annealing, and characterization of GaAs and InP. She subsequently became Project Leader, Ion Implantation and supervised implantation systems and activities for the Microelectronics Research and Development Center. She is presently Manager of the Materials Preparation Section, where her efforts are centered on GaAs bulk growth, ion implantation, encapsulation, and characterization. She has authored or coauthored more than 30 publications in the areas of ion and electron beam effects and semiconductor materials.

Dr. Kirkpatrick is a senior member of the Society of Women Engineers and a member of the American Physical Society and the Electrochemical Society.



Stephen I. Long (S'68-M'73-SM'80) received the B.S. degree in engineering physics from the University of California, Berkeley, in 1967, and the M.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1969 and 1974, respectively. His thesis research dealt with steady-state liquid phase epitaxial growth of GaAs.

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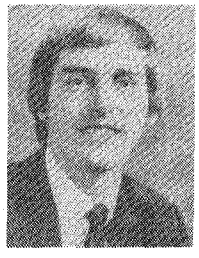

R. C. Eden was born in Anamosa, IA, on July 10, 1939. He received the B.S. degree from Iowa State University, Ames, the M.S. degree from the California Institute of Technology, Pasadena, and the Ph.D. degree from Stanford University, Stanford, CA, all in electrical engineering.

His most recent efforts have been focused toward the development of a very high-speed, ultra low-power planar GaAs digital integrated circuit technology with gate densities and power dissipation levels compatible with LSI or VLSI. Prior to this, he carried out development work on high-speed, high-efficiency heterojunction III-V alloy, 1.06 μm avalanche photodiodes and an ultra-high sensitivity, high-speed hybrid-integrated preamplifiers for these detectors. He was also involved in the design and analysis of a number of special device structures, including the recently successfully demonstrated GaAs CCD. After receiving the M.S. degree, he worked at the Advanced Systems Development Laboratory, IBM Corporation, San Jose, CA. His Ph.D. dissertation work involved detailed electronic energy band studies on GaAs, GaP, and Si using photoemission, work he extended after joining Rockwell International Science Center in 1968, to surface state observations in silicon by vacuum photoemission and internal photoemission in MOS structures. He is currently with Gigabit Logic, Torrance, CA.