TMC2220/TMC2221

CMOS Programmable Digital Output Correlators

4 x 32 Bit, 20 MHz; 1 x 128 Bit 20 MHz

Features

- 20 MHz continuous correlation rate
- Fully programmable masking
- Two's complement or unsigned magnitude correlation score
- User-programmable reference load multiplexing
- Channel weighting and output formatting (TMC2220)
- Multi-bit, dual-channel or non-coherent (quadrature) correlation (TMC2220)
- Single +5V power supply
- Low power CMOS construction
- Three-state TTL compatible outputs
- TMC2220 available in 68-pin grid array and 69-pin plastic PGA packages
- TMC2221 available in a 28-pin CERDIP

Applications

- Signal detection
- Radar signature recognition
- Secure communications
- Robotics/automated assembly
- Automatic test equipment
- Electro-optical navigation
- Pattern and character recognition
- Assembly line inspection

Description

The TMC2220, 20 MHz TTL compatible CMOS correlator is composed of four separate 1 x 32 correlator modules. The correlation scores of the four modules are weighted, combined and output on two separate parallel, three-state ports.

Each module contains a 32-bit serial data register, a 32-bit serial reference preload register, a 32-bit parallel reference latch and a 32-bit parallel mask latch. Correlation is performed by 32 exclusive-NOR (XNOR) gates. Each XNOR gate compares one (single bit) reference word. While correlation is being performed between the data and the present reference, the next reference pattern may be preloaded through one of two multiplexed input ports. Shorter sampling windows and bipolar correlation are also supported. Each module outputs a 6-bit binary correlation score. Either an unsigned (range 0 through 32) or bipolar (range -16 through +16) representation may be selected. The outputs of each pair of correlator modules is added, with user-selected weighting factors, producing intermediate correlation scores which can be combined or output directly to the main or auxilliary output ports.

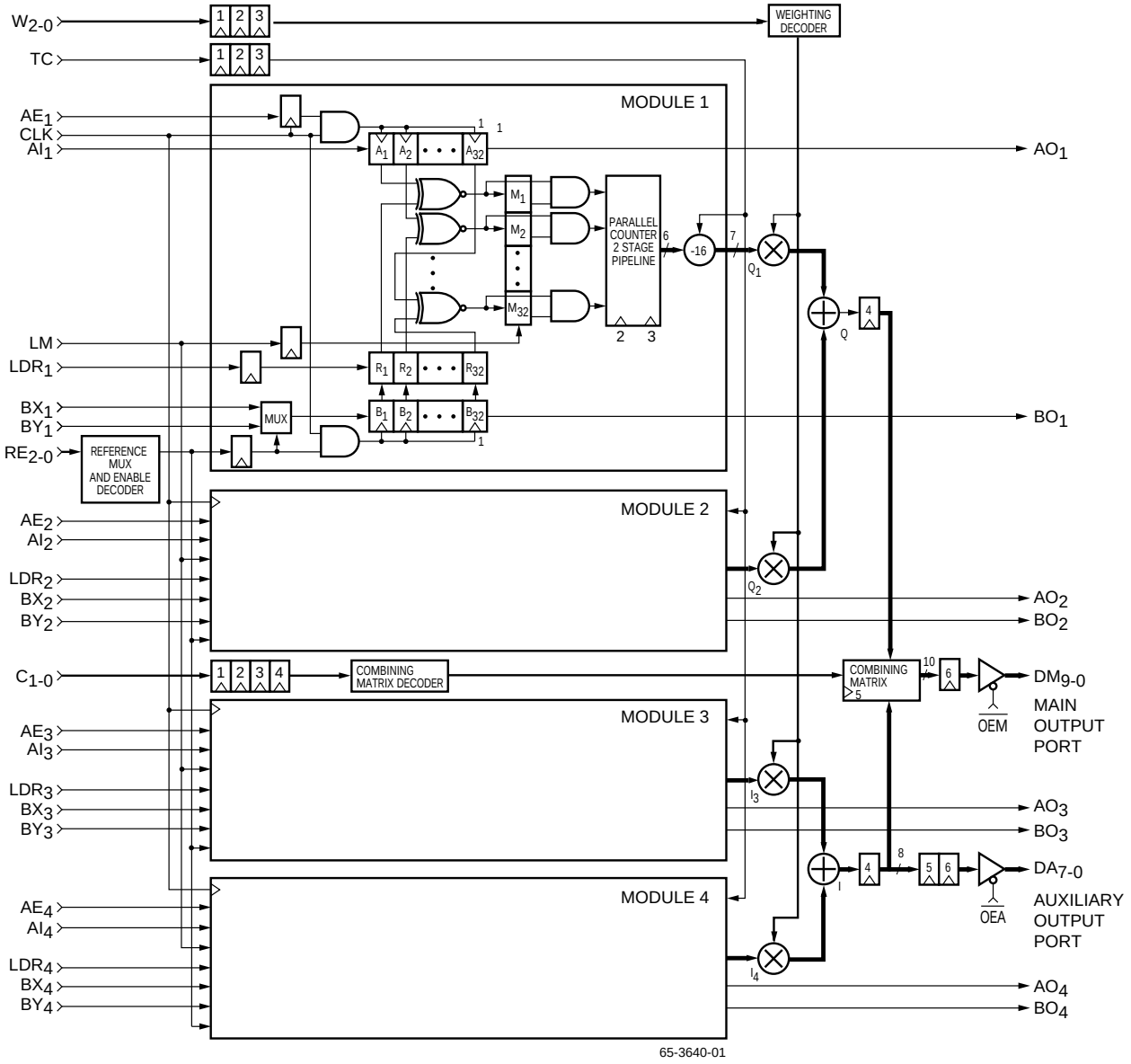
Since the four modules can be cascaded serially or in parallel, the TMC2220 supports numerous single and dual channel applications involving 1, 2, or 4-bit wide data and window lengths up to 32, 64, 96 or 128 bits. Multiple devices can be combined to support large correlation operations.

The TMC2221 combines the four 32-bit modules in series for a fixed channel configuration of 1-bit by 128. The reduced complexity and package size of the TMC2221 is ideal for applications requiring less versatility than the TMC2220. By making use of the mask function, any size single channel length of up to 128 bits is possible.

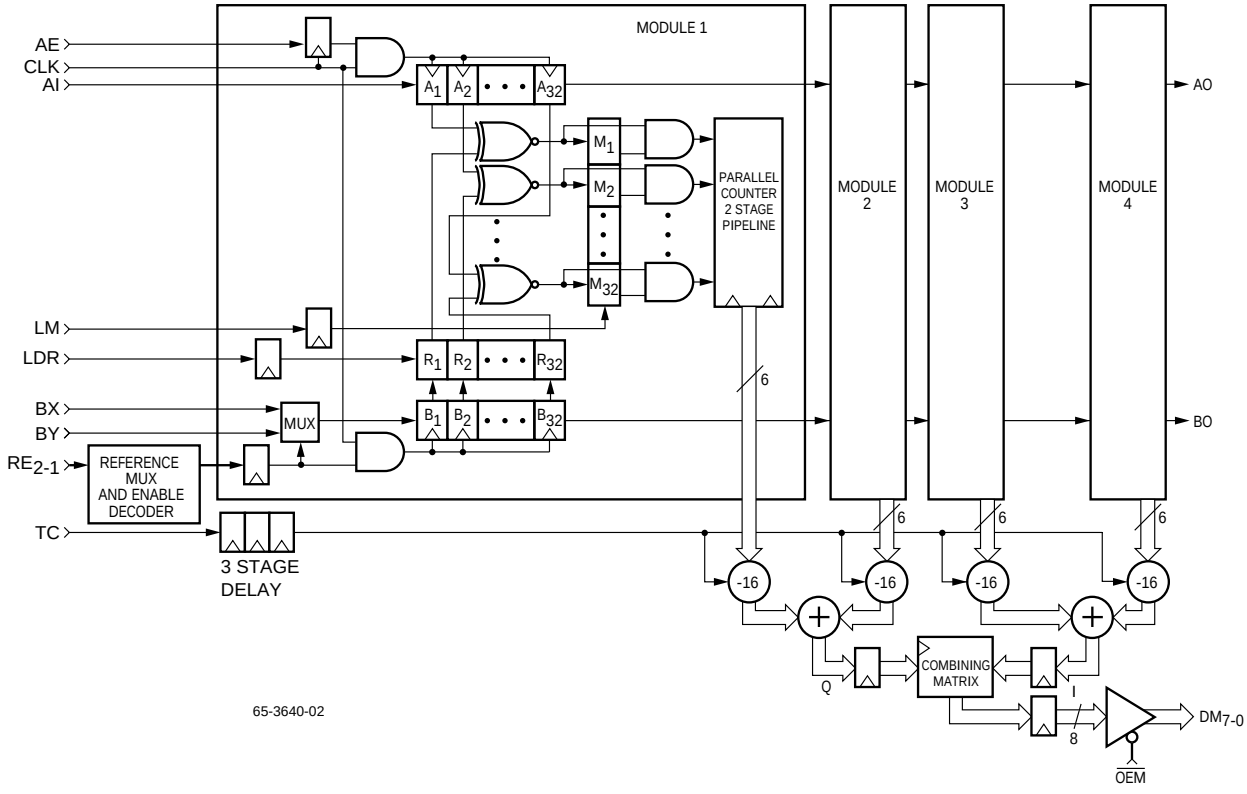
With the TMC2221, the reference word is serially loaded through the single two-input multiplexed reference port of the first correlator module. Although the configuration is fixed, the reference loading process and basic operation for each module is similar to that of the TMC2220. The outputs are summed with equal weighting, and the result is output through the single 8-bit output port. Unsigned magnitude or two's complement (bipolar) output score may be selected.

This document was created with FrameMaker 4.0.4

TMC2220 Block Diagram



TMC2221 Block Diagram



Functional Description

The TMC2220 consists of four independent 1 x 32 correlator channels with weighted correlation scores which are combined and output on the two output ports (main and auxiliary). By taking advantage of the instruction set and I/O structure, the TMC2220 can be adapted to a wide variety of applications.

The TMC2221 consists of the four 1 x 32 correlator modules cascaded internally for a single 1 x 128 correlator. The outputs of each module are given a unity weighting, summed and placed on the output port.

Correlator Channel Modules

Each of the four modules (i = 1 to 4) contains two 32-bit serial synchronous shift registers, A_i (data) and B_i (reference preload); two 32-bit parallel latches, R_i (reference) and M_i (mask); 32 exclusive-NOR gates; 32 AND gates; a 32-bit parallel binary counter with a 6-bit unsigned output and a defeatable half-scale (-16) subtracter with a 7-bit two's complement output.

Whenever a given A_i or B_i register is enabled, the next rising edge of the clock loads the value at the corresponding A_i or BX_i/BY_i input port into the first cell of the register, and shifts the contents of each cell to the next, overwriting the contents of the last cell. These serial-in, parallel-tapped registers form the first of six registers which account for the six internal delays. After an output buffer delay t_D, the new contents of the last cell of A_i and B_i become available at the outputs AO_i and BO_i respectively. These outputs are used for cascading multiple devices. In addition, the B_i input multiplexer selects which of two input ports, BX_i or BY_i, is to be used on that cycle.

The reference latch R_i tracks the contents of B_i when control LDR_i was HIGH on the previous cycle and holds when LDR_i was LOW. A HIGH on LDR_i transfers the contents of B_i in parallel into R_i on the next clock cycle where correlation takes place. When LDR_i is held HIGH, R_i is transparent, enabling direct correlation between A_i and B_i.

Each of the 32 outputs of R_i is correlated against the corresponding tap of A_i by an XNOR gate whose output is connected to both the masking AND gate and the masking latch M_i.

Each M_i tracks if LM was HIGH on the previous cycle and holds if LM was LOW. When LM is held HIGH, all M_i latches are transparent and the output of each XNOR gate is sent to both inputs of the corresponding AND gate to prevent

masking or disabling from occurring. A LOW on LM loads the next unmasked correlation pattern (from the XNOR gates) into each M_i. Wherever the latch holds a logic one, normal correlation is enabled; wherever it is a logic zero, correlation is masked by the AND gate.

A 32-bit parallel counter encodes the number of logic ones emerging from the AND gates as a 6-bit binary number between 0 and 32 (100000) The clock drives the two pipeline registers in the counter (the second and third registers in the six register pipeline).

The 6-bit unsigned binary output of each parallel counter then enters a half-scale subtracter where it passes unchanged if the pipelined control TC is LOW and is reduced by 16 if TC is HIGH. If TC is HIGH, the range of correlation scores becomes -16 through +16 where +16 denotes a perfect match between the contents of A_i and those of R_i with no masking. A score of -16 denotes that no unmasked data bit matches the corresponding reference bit (anti-correlation). The TC control is pipelined by 3 registers, such that it is aligned with new data entering the A_i or B_i register.

Weighing and Merging Circuitry

On the TMC2220, the 7-bit two's complement output of each correlator module (Q_1, Q_2, I_3, I_4) is multiplied by a factor of 0, 1, 2, 3, 4 or 5 according to controls W_{2-0}. The outputs of each pair of multipliers is then added and the results Q and I are loaded into the fourth pipeline register.

Following two additional pipeline delays from the fifth and sixth registers, correlation sum I is available on the TMC2220 at the 8-bit auxiliary output port, DA_{7-0}, if the buffer is enabled ($\overline{OEA}$ = LOW).

Under controls C_{1-0}, the TMC2220 combiner blends Q and I into a single final correlation score which is sent to the 10-bit main output port, DM_{9-0}, if $\overline{OEM}$ is LOW. The combiner pipeline register stage 5 and the main output register stage 6 are balanced by the auxiliary port double output register. In the simplest mode, the combiner outputs correlation sum Q permitting the TMC2220 to be used in two separate correlator channels. In this application, the combined results from modules 1 and 2 emerge through DM_{9-0} while the result-from modules 3 and 4 emerge through DA_{7-0}. In the three remaining modes, the output at the main port will reflect the correlations of all four modules.

In the second mode, the combiner outputs the unweighted sum, Q + I. In the third mode, it outputs the weighted sum, Q + 1/2, for single channel binary applications. In the fourth mode, the combiner extracts the absolute values of Q and I and adds the greater magnitude value to one half of the lesser value. This final mode is an approximation of the Pythagorean vector magnitude formula:

$$M = (X^2 + Y^2)^{1/2}$$

The TMC2220 contains a total of five pipeline registers plus the data and reference preload shift registers making the total delay six clock cycles. Instructions and data paths are pipelined so the instructions presented on a given clock cycle apply to the value entering registers A_i and B_i. Instructions RE, LM, LDR and AE, all of which enable registers or latches, must be set one cycle early (see timing diagram).

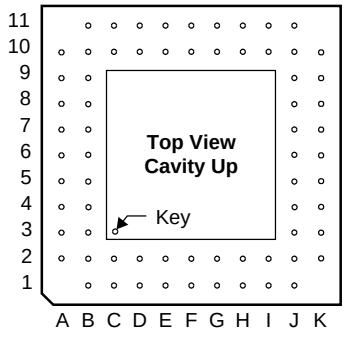
For the TMC2221, the correlation score of each module is passed unchanged (TC = LOW) or reduced by sixteen (TC = HIGH). Each module score is given a unity weighting then sent to the combining matrix where the four scores are added and output on the 8-bit data bus if $\overline{OEM}$ is LOW.

In magnitude mode (TC = LOW) and masking disabled, a perfect match between the data and reference will produce a correlation score of 128 (10000000_B) and correlation score of 0 shall indicate no matches (anti-correlation). In two's complement mode (TC = HlGH), perfect correlation will produce a score of 64 (01000000_B) and anti-correlation shall have an output of -64 (11000000_B). A total of five register delays plus the input register cause the result to be available on the sixth clock cycle after the loading of the input data.

TMC2220 Pin Assignments

68 Pin Grid Array – G8 Package

69 Pin Plastic Pin Grid Array – H8 Package[1]



Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
A2	GND	B9	LDR_3	F10	CLK	K4	W_2
A3	DA_2	B10	LDR_4	F11	GND	K5	W_0
A4	DA_4	B11	V_{DD}	G1	DM_8	K6	C_0
A5	DA_6	C1	DM_1	G2	DM_7	K7	LM
A6	BO_3	C2	DM_0	G10	BX_1	K8	AE_1
A7	BO_4	C10	BX_4	G11	GND	K9	AE_2
A8	V_{DD}	C11	AI_4	H1	BO_1	K10	RE_2
A9	AE_3	D1	DM_3	H2	DM_9	K11	AI_2
A10	AE_4	D2	DM_2	H10	AI_1	L2	V_{DD}
B1	DA_0	D10	AI_3	H11	BY_1	L3	$\overline{OEM}$
B2	DA_1	D11	BY_4	J1	BO_2	L4	W_1
B3	DA_3	E1	DM_5	J2	AO_1	L5	C_1
B4	DA_5	E2	DM_4	J10	BY_2	L6	TC
B5	DA_7	E10	BY_3	J11	BX_2	L7	LDR_1
B6	AO_3	E11	BX_3	K1	AO_1	L8	LDR_2
B7	AO_4	F1	DM_6	K2	GND	L9	RE_0
B8	$\overline{OEA}$	F2	V_{DD}	K3	GND	L10	RE_1

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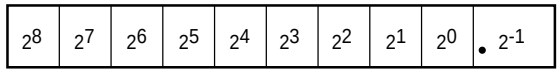
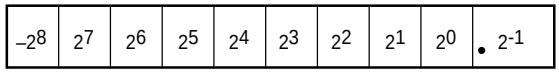
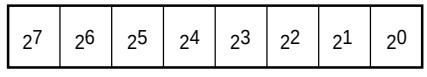
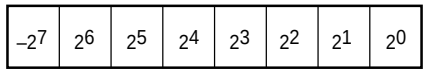
Note:
1. Pin C3 is a mechanical orientation pin on the H8 package at manufacturer's option.

TMC2220 Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Power		
V_{DD}	F2, L2, B11, A8	**Supply Voltage.** The TMC2220 operate from a single +5V power supply. All power and ground pins must be connected.
GND	K2, K3, G11, F11, A2	**Ground.** The TMC2220 operate from a single +5V power supply. All power and ground pins must be connected.
Inputs		
AI_{1-4}	H10, K11, D10, C11	**Data Input.** Each data input is a single-bit serial input to the A_i register of each correlator module.
BX_{1-4}	G10, J11, E11, C10	**Main Reference Preload.** The main, BX_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
BY_{1-4}	H11, J10, E10, D11	**Alternate Reference Preload.** The alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
Outputs		
AO_{1-4}	J2, K1, B6, B7	**Data Output.** Each cascade data output is a single-bit serial output from the A_i register of each correlator module.
BO_{1-4}	H1, J1, A6, A7	**Reference Preload Output.** Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.

TMC2220 Pin Descriptions (continued)

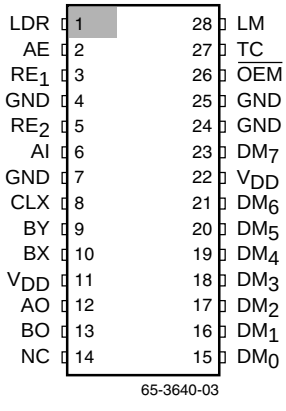
Pin Name	Pin Number	Pin Function Description
DM_{9-0}	H2, G1, G2, F1, E1, E2, D1, D2, C1, C2	**Main Port.** The 10-bit main correlation output is a combination of the four module output scores, Q_1, Q_2, I_3, I_4, which are dependent on the W_{2-0} weighted adder and C_{1-0} combining matrix controls. The main output port is enabled by $\overline{OEM}$. The TMC2220 10-bit output format is:  if TC is LOW  if TC is HIGH
DA_{7-0}	B5, A5, B4, A4, B3, A3, B2, B1	**Auxiliary Port.** The 8-bit auxiliary correlation output is the sum of two module output scores, I_3 and I_4, which are dependent on the W_{2-0} weighted adder controls. The auxiliary output port is enabled by $\overline{OEA}$. The 8-bit binary output format is:  if TC is LOW  if TC is HIGH
Clock		
CLK	F10	**Master Clock.** The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-0} for the B_i registers. The pipeline delay registers for the controls, W_{2-0}, C_{1-0}, and TC are also strobed on the rising edge of CLK.
Controls		
AE_{1-4}	K8, K9, A9, A10	**Register Clock Enable.** The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.
C_{1-0}	L5, K6	**Combining Matrix.** These pipelined instructions select the function to be executed by the combining matrix and output through the main output port, DM_{9-0}.
LDR_{1-4}	L7, L8, B9, B10	**Reference Load.** The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.
LM	K7	**Mask Load.** The Load Mask control allows the user to mask or select “no compare” bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i If no masking is required, LM is kept HIGH, making M_i transparent.
$\overline{OEA}$	B8	**Auxilary Port Output Enable.** The asynchronous output enable for the auxiliary output port, DA_{7-0}, is an active LOW control. When $\overline{OEA}$ is HIGH, the output is in a high-impedance state.
$\overline{OEM}$	L3	**Main Port Output Enable.** The asynchronous output enable for the main output port, DM_{9-0}, is an active LOW control. When $\overline{OEM}$ is HIGH, the output is in a high-impedance state.

TMC2220 Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
RE_{2-0}	K10, L10, L9	**Reference Load Select.** The encoded clock enable and load selector controls determine the various combinations of BX_i and BY_i reference inputs that may be selected for the four reference preload registers B_i. The B_i register clocks may also be selectively enabled. Like LDR, LM and AE_i, this control is delayed by one clock cycle. See Table 1.
TC	L6	**Two's Complement.** The Two's Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (-16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.
W_{2-0}	K4, L4, K5	**Module Weighing Factor.** The weighted adder controls determine the relative weightings of the four correlation module scores.

TMC2221 Pin Assignments

28 Pin CERDIP – B6 Package



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TMC2221 Pin Descriptions

Pin Name	Pin Number	Pin Function Description
Power		
V_{DD}	11, 22	**Supply Voltage.** The TMC2221 operates from a single +5V power supply. All power and ground pins must be connected.
GND	4, 7, 24, 25	**Ground.** The TMC2221 operates from a single +5V power supply. All power and ground pins must be connected.
Inputs		
AI	6	**Data Input.** Each data input is a single-bit serial input to the A_i register of each correlator module.
BX	10	**Main Reference Preload.** The main, BX_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.
BY	9	**Alternate Reference Preload.** The alternate, BY_i, reference preload inputs to the B_i register of each correlator module are selected by controls RE_{2-0}.

TMC2221 Pin Descriptions (continued)

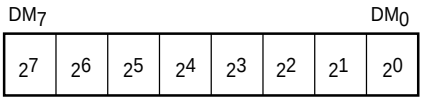
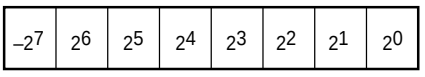
Pin Name	Pin Number	Pin Function Description
Outputs		
AO	12	**Data Output.** Each cascade data output is a single-bit serial output from the A_i register of each correlator module.
BO	13	**Reference Preload Output.** Each cascade reference preload output is a single-bit serial output from the B_i register of each correlator module.
DM_{7-0}	23, 21, 20, 19, 18, 17, 16, 15	**Main Port.** The TMC2221 has an 8-bit correlation output DM_{7-0} which always outputs the sum: $Q_1 + Q_2 + I_3 + I_4$ Where each term is either unsigned magnitude or magnitude minus 16 depending on the TC control. The TMC2221 8-bit output format is:  if TC is LOW  if TC is HIGH
Clock		
CLK	8	**Master Clock.** The clock for A_i data and B_i reference preload registers can be toggled at up to 20MHz. All registers are strobed on the rising edge of CLK and dependent on the registered enable controls, AE_i for the A_i registers, and RE_{2-1} for the B_i registers. The pipeline delay registers for the controls, W_{2-0} and TC are also strobed on the rising edge of CLK.
Controls		
AE	2	**Register Clock Enable.** The clock enable for the four A_i data registers is a registered, active HIGH control. When AE_i is LOW on the previous cycle, no shifting of data occurs on A_i. AE_i is read on the rising edge of CLK, thus the shifting of data in A_i will occur on the next rising edge of CLK.
LDR	1	**Reference Load.** The Load Reference control copies the contents of register B_i into latch R_i for correlation. If LDR_i was LOW on the previous clock cycle, the present contents of the latch remain in R_i. If LDR_i was HIGH, R_i is transparent and the B_i are values used in the current correlation.
LM	28	**Mask Load.** The Load Mask control allows the user to mask or select “no compare” bit positions in each channel. Inputs shifted into A_i and B_i produce a correlation pattern as the desired mask. Control LM must be HIGH on the previous cycle to track and LOW to store the pattern in the mask latches M_i If no masking is required, LM is kept HIGH, making M_i transparent.
$\overline{OEM}$	26	**Main Port Output Enable.** The asynchronous output enable for the main output port, DM_{7-0}, is an active LOW control. When OEM is HIGH, the output is in a high-impedance state.
RE_{2-1}	5, 3	**Reference Load Select.** The encoded clock enable and load selector controls select BX and BY reference input. Like LDR, LM and AE_i, this control is delayed by one clock cycle. See Table 1.
TC	27	**Two’s Complement.** The Two’s Complement control forces the outputs of the four correlator modules to be unipolar (0 to 32) or bipolar (-16 to +16). When TC is LOW, the outputs of the correlator modules are passed unchanged to the weighting circuitry. When TC is HIGH, 16 is subtracted from each correlator output which is then interpreted as a two's complement value.
No Connection		
NC	14	

Table 1. Reference Preload Register Input and Enable Operation

RE_i Controls	Selected Reference Port (TMC2220)				Selected Reference Port (TMC2221)
RE_{2-0}	1	2	3	4	
000	Dis	Dis	Dis	Dis	Dis
001	Dis	Dis	Dis	BX_4	Dis
010	Dis	Dis	BY_3	BX_4	BY
011	Dis	Dis	BY_3	BY_4	BY
100	BX_1	BX_2	BX_3	BX_4	BX
101	BY_1	BX_2	BX_3	BX_4	BX
110	BY_1	BX_2	BY_3	BX_4	BY
111	BY_1	BY_2	BY_3	BY_4	BY

Notes:
1. Dis = B_i register disabled (hold model).
2. LSB (RE_0) not used on the TMC2221.

Table 2. Module Weighting Factor Operation (TMC2220 Only)

W_i Controls	Internal Channel Configuration	
W_{2-0}	Q	I
000	$Q_1 + Q_2$	$I_3 + I_4$
001	$3Q_1 + Q_2$	$3I_3 + I_4$
010	$4Q_1 + Q_2$	$4I_3 + I_4$
011	Q_2	I_4
100	Q_1	I_3
101	$3Q_1 + 2Q_2$	$3I_3 + 2I_4$
110	$4Q_1 + 2Q_2$	$4I_3 + 2I_4$
111	$5Q_1 + 2Q_2$	$5I_3 + 2I_4$

Table 3. Combining Matrix Operation (TMC2220 Only)

C_i Controls C_{1-0}	Main Output Port Function DM_{9-0}
00	Q
01	Q + I/2
10	Q + I
11	Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)[1]

Notes:
1. The larger magnitude value of Q or I plus one-half of the smaller magnitude value.
2. The TMC2221 always outputs the sum $Q_1 + Q_2 + I_3 + I_4$.

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply	-0.5	7.0	V
Output Applied Voltage[2]	-0.5	V_{DD} + 0.5	V
Output Forced Current[3,4]	-0.5	V_{DD} + 0.5	V
Short Circuit Duration (single output in HIGH state to ground)		1	sec
Storage Temperature	-65	150	°C
Operating, case temperature	-60	130	°C
Junction Temperature		175	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			-2.0			-2.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC Characteristics within Specified Operating Conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V, $\overline{OEM}$, $\overline{OEA}$ = 5V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OEM}$, $\overline{OEA}$ = 5V		70		80	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	-40			-40	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	-40		-40		µA

DC Characteristics within Specified Operating Conditions[1] (continued)

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		+40		+40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified

AC Characteristics within Specified Operating Conditions

Parameter		Test Conditions	Temperature Range								Units
			Standard				Extended				
			-1				-1				
			Min	Max	Min	Max	Min	Max	Min	Max	
F_C	Clock (Correlation) Rate	V_{DD} = Min		20		17		20		17	MHz
t_{pWL}	Clock Pulse Width, LOW	V_{DD} = Min	25		30		25		30		ns
t_{pWH}	Clock Pulse Width, HIGH	V_{DD} = Min	15		15		15		15		ns
t_S	Input Setup Time		15		15		17		17		ns
t_H	Input Hold Time		0		0		0		0		ns
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		25		25		25		25	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	3		3		3		3		ns
t_{ENA}	Three-State Output Enable Delay[1]	V_{DD} = Min. C_{LOAD} = 40pF		17		17		17		17	ns
t_{DIS}	Three-State Output Disable Delay[1]	V_{DD} = Min. C_{LOAD} = 40pF		22		22		22		22	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Sliding Correlation Timing

The TMC2220 and TMC2221 have a six register pipeline. There are registers for the input data and reference, parallel counter, weighting circuitry, combining matrix, and output. CLK is used to load all A_i, B_i and instruction pipeline registers. With the register controls enabled, a data or reference word is loaded into its respective A_i or B_i register on every rising edge of CLK. Data A_N enters register A_i on the rising edge of clock C_N. The reference latch is static if the previous LDR_i was LOW or tracks B_i if LDR_i was HIGH. If reference preload is not desired, holding control LDR_i HIGH makes latch R_i transparent and direct correlation between A_i and B_i occurs. Data is valid if present at the input for a setup time t_S before and a hold time t_H after the rising clock edge. Setup and hold time requirements also apply to instructions and controls, however, AE, LDR, LM and RE must be valid one cycle before taking effect.

Because of the six internal pipeline delays, the correlation score for a given set of A_i and B_i register contents appears at the output ports six clock cycles plus an output delay t_D later. When the main and auxiliary (TMC2220 only) output ports are enabled ($\overline{OEM}$ = $\overline{LOW}$ and $\overline{OEA}$ = LOW), the correlation score O_N of data window A_{N-31} through A_N is output after rising clock edge C_{N+5} (A_{N-127} through A_N on the TMC2221). Instructions TC, W, and C are registered and pipelined so that the instructions will be aligned with the data. The instructions I_N (see timing diagram) which are loaded on rising clock edge C_N apply to a correlation between data and reference words N-31 (N-127) through N. Masking is assumed to be preset (previous LM = LOW) or unused (previous LM = HIGH). The same timing applies if the reference is shifting and data is fixed.

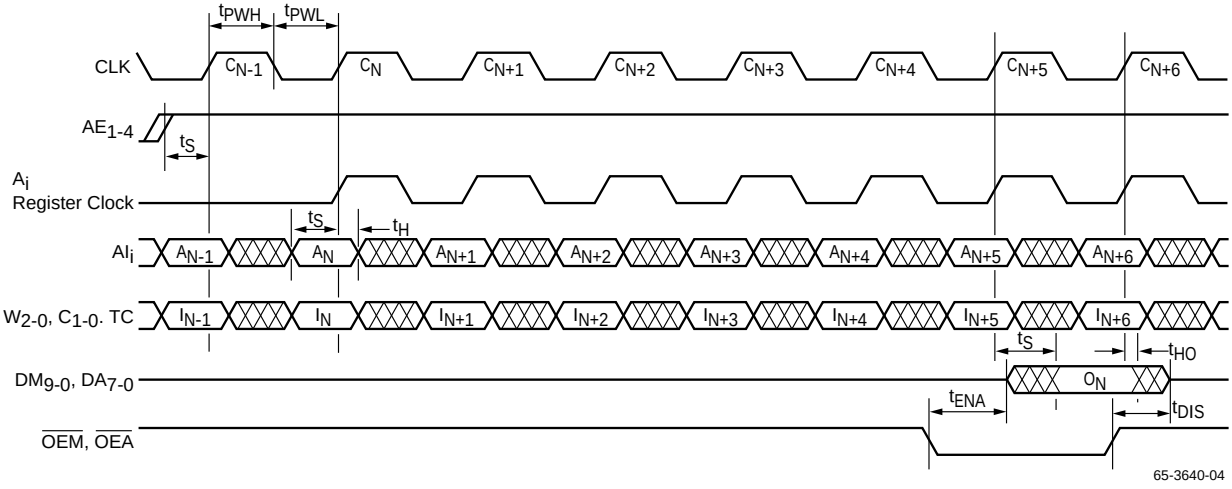


Figure 1. Sliding Correlation Timing

Reference Register Load Timing

The HIGH on LDR_i transfers the contents of B_i in parallel into R_i in the next clock period. R_i tracks B_i when control LDR_i is HIGH and holds when LDR_i is LOW. N rising edges of CLK are required to load N reference words into the reference preload register B_i. The rising edge of clock C_N loads reference word B_N so that B_i contains words B_{N-31} through B_N.

Figure 2 illustrates the LDR_i instruction timing to transfer reference window B_{N-31} through B_N into the reference latch. With this timing, correlation against the old reference pattern is preserved during the "LDR" clock cycle and that correlation against the new reference pattern B_{N-31} to B_N should commence immediately after the "LDR" clock cycle. The user must meet the normal input setup and hold time requirements and setup the instruction one clock cycle before the desired transfer.

A completely new reference can be loaded into latch R on every 32nd clock cycle. With the output ports enabled, the correlation score O_N (correlation between data A_{N-31} through A_N and reference B_{N-31} through B_N) is available an output delay t_D after the rising edge of clock C_{N+5} because of the six register pipeline.

Operation of the TMC2221 is similar to the operation described for the TMC2220 except the length of the reference word is 128 bits rather than 32. The reference register will therefore contain the pattern B_{N-127} through B_N, and correlation occurs between this reference and data A_{N-127} through A_N. A new reference word therefore requires 128 clock cycles to completely load the new value. With the output ports enabled, the correlation score O_N (correlation between data A_{N-127} through A_N and reference B_{N-127} through B_N) is available on output delay t_D after the rising edge of clock C_{N+5}.

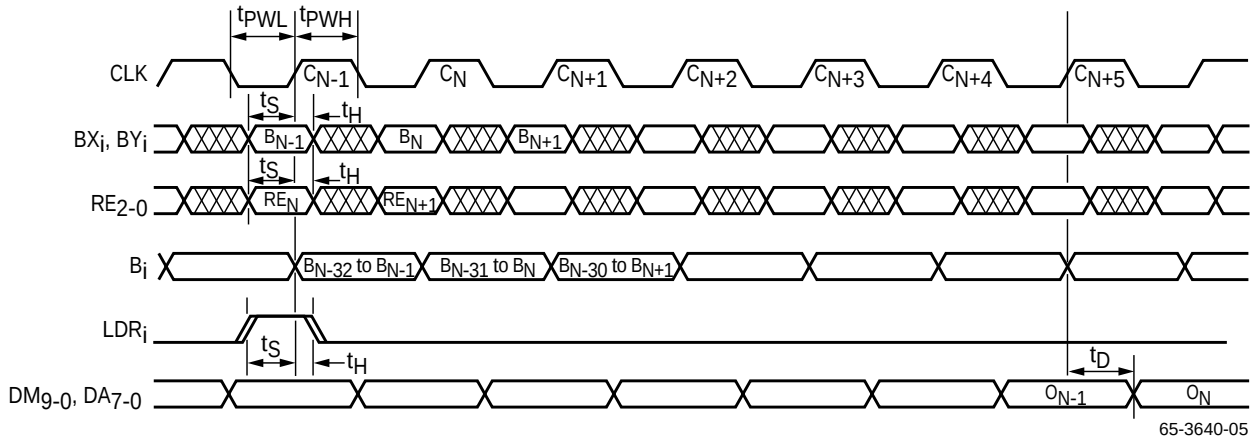


Figure 2. Reference Latch Load Timing

Mask Register Loading

Control LM latches a mask pattern into M_i which selectively disables word positions in each correlator module. Masking latch M_i tracks the XNOR output if, on the the previous clock cycle, LM was HIGH and holds if LM was LOW. Figure 3 illustrates the TMC2220 LM timing to latch a mask generated by the exclusive NOR of A_{N-31} through A_N with R_{N-31} through R_N. LM must be set HIGH t_S before the rising edge of clock C_{N-1} to load the mask for A_{N-31} thru A_N. LM must be set LOW before the next rising edge of C_N to ensure words N-31 to N remain latched as the mask pattern. A completely new mask may be loaded on every 32nd clock cycle. However, to permit time for data and reference loading, mask loading is generally limited to every 64th clock cycle. The first correlation score which reflects mask N is output t_D after the rising edge of clock cycle C_{N+6}.

Operation of the TMC2221 is similar that of the TMC2220 but requires 128 clock cycles to completely load a new mask pattern. To permit time to load new data and a new reference pattern once the mask is loaded, an additional 128 clock cycles is required. Therefore, mask loading is generally limited to every 256 clock cycles in the TMC2221. The mask pattern loaded will be the exclusive-NOR of A_{N-127} through A_N with R_{N-127} through R_N.

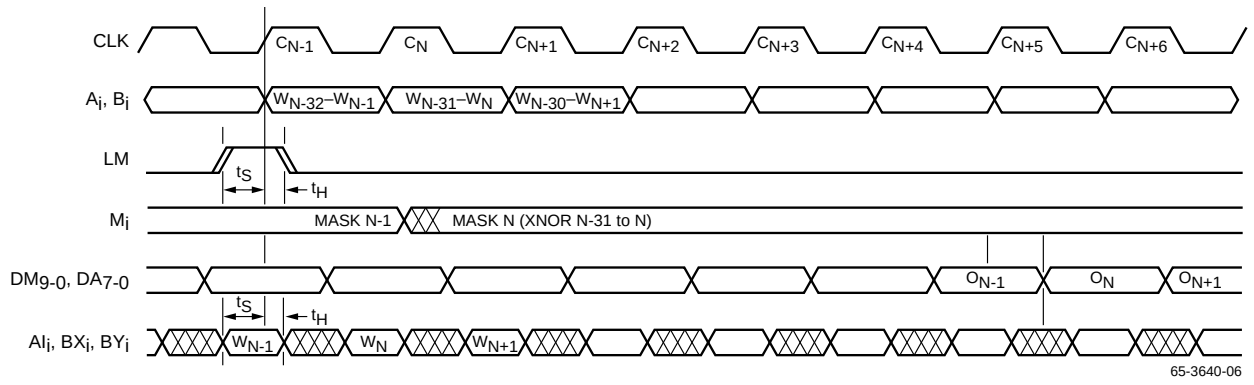


Figure 3. Masking Latch Load Timing

Applications Discussion

The TMC2220 architecture provides the flexibility for a number of configurations. The cascade outputs and the internal weighting and adder logic allow a single TMC2220 to be configured as four independent 32-bit correlators, independent 96-bit and 32-bit correlators, two independent 64-bit correlators, or as a single 128 x 1 correlator. The TMC2220 may also be cascaded serially or in parallel to increase the length or width of correlation.

To increase the correlation length in a single TMC2220 system, the cascade outputs of a module (AO_i, BO_i) can be connected to the inputs of the next module (AI_{i+1}, BI_{i+1}) When using this configuration, the input enables and load controls should be connected together. Figure 4 shows the configuration for a dual 64 x 1 correlation. In this application, the outputs of module 1 are connected to the inputs of module 2 and the outputs of module 3 are connected to the inputs of module 4. The weighting logic is set for 1:1 weighting and the combining logic is set to output $Q_1 + Q_2$ on the main output DM_{9-0}, and $I_3 + I_4$ on the auxiliary output DA_{7-0}

Figure 5 shows an example of multi-bit correlation with extended length. This example shows 4-bit correlation with a length of 64-bits. The outputs of the two TMC2220s must be externally added to obtain the 64-bit correlation score. The weighting and combining of the module correlation scores should be set as required by the application.

Figure 6 shows an example of 8-bit, two's complement correlation. Two TMC2220's are used in parallel and externally summed to obtain the properly weighted correlation score. To obtain a properly weighted correlation score, each bit of the output must be multiplied by an appropriate binary scaling factor. The 8-bit data input and reference are connected as shown. The weighting control of each TMC2220 is set for 4:1 weighting ($W_{2-0} = 010$). This multiplies the upper two bits of each TMC2220 by a factor of 4(Q_1, I_3). The next step is to multiply the 2nd and 4th bits (Q_2, I_4) by a factor of 2. This operation is accomplished by setting the combining logic to output the sum $Q + 1/2(C_{1-0} = 01)$. The final output of each TMC2220 will be equivalent to:

$$DM_{9-0} = (4 \times Q_1) + (2 \times I_3) + (1 \times Q_2) + (1/2 \times I_4)$$

Setting the weighting and combining controls as described will produce a correlation score with each bit properly weighted based on its 4-bit binary position. The final step is to multiply the correlation output of the most-significant TMC2220 (bits 7-4) by a factor of 16 then combine the outputs of the two TMC2220s. This is done using external adder circuitry. Multiplication is performed by simply shifting the output lines of the upper TMC2220 by four places at the input to the adder logic. The output of the summer, therefore, shall give the binary weighted correlation score of a quantized 8-bit input. The same circuit can be used with unsigned data if the inverter on the most-significant-bit of the reference input is omitted.

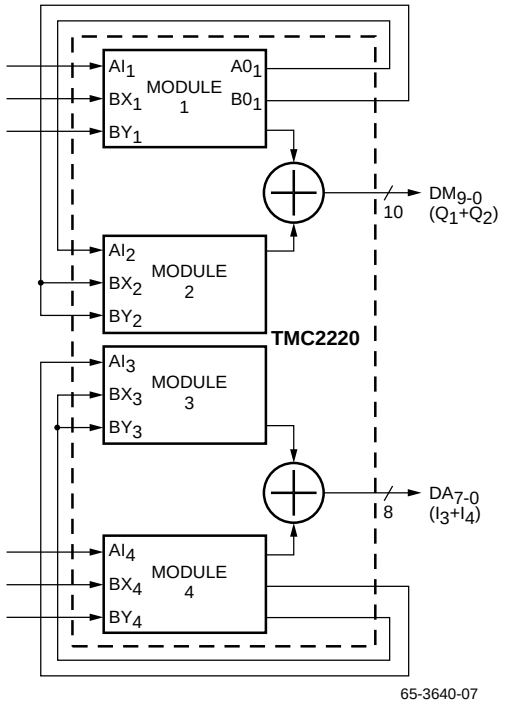


Figure 4. Dual 64 x 1 Configuration

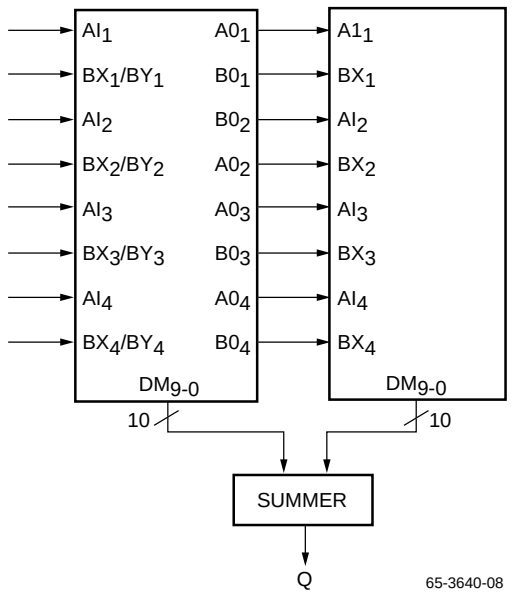


Figure 5. Cascading the TMC2220 for Extended-Length Correlation

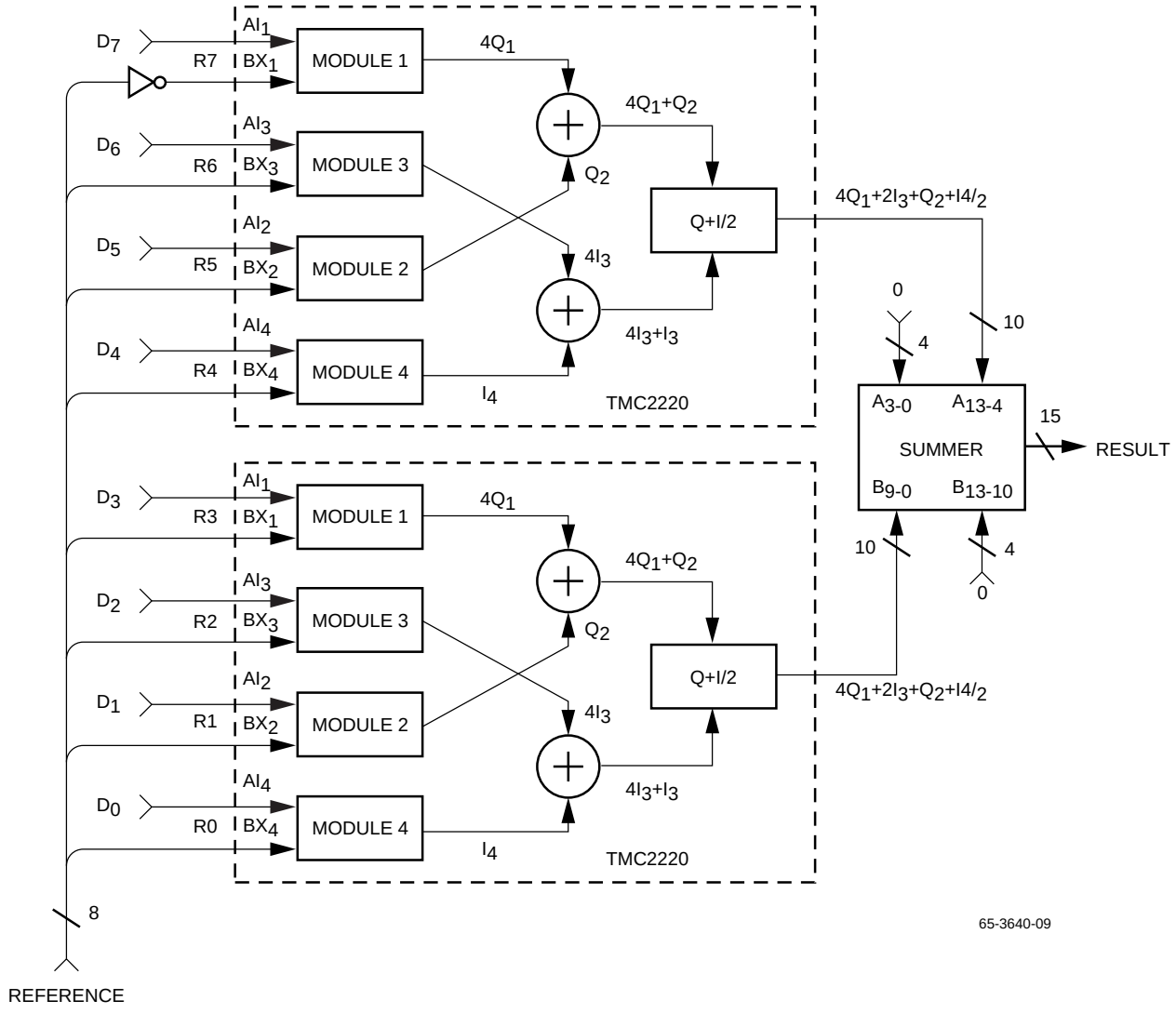


Figure 6. 8-Bit Correlation with the TMC2220

Figure 7 is an example of full complex correlation. In this example, separate real and imaginary terms are multiplied and summed internally to provide a real and imaginary result. This method preserves the phase information of the input. Inputs are connected as shown in the figure. The imaginary term in Im(D) x Im(R) is negated (inverted) for proper sign in the summation. The TMC2220 is set for 1:1 (Q_1 + Q_2, I_3 + I_4) weighting, two's complement mode, and the combining control is set to output Q on the main output and I on the auxiliary output. All 32 internal taps are used.

A simple example would be to find a sine wave in a demodulated data stream. The references would be set to:

Re(R) = Cos (ω t) and Im(R) = Sin I (ω t)

where, ω is the modulation frequency. Each term is set to 1 for positive and 0 for negative.

The data inputs are set to:

Re(D) = $data_{in}$ x Cos(ft) and Im(D) = $data_{in}$ x Sin (ft)

where, f is the mixer or carrier frequency.

Figure 8 is similar to full complex correlation, however, in this example the output is magnitude only. This application is used when the phase relationship is not required. The inputs are connected as in the previous example, however, rather than a full complex output, the outputs are combined internally to:

Max (|Q|, |I|) + 1/2 Min (|Q|, |I|)

(C_{1-0} = 11) to obtain the approximate magnitude output. Multiplying the output by 15/16 will reduce the error in the magnitude approximation.

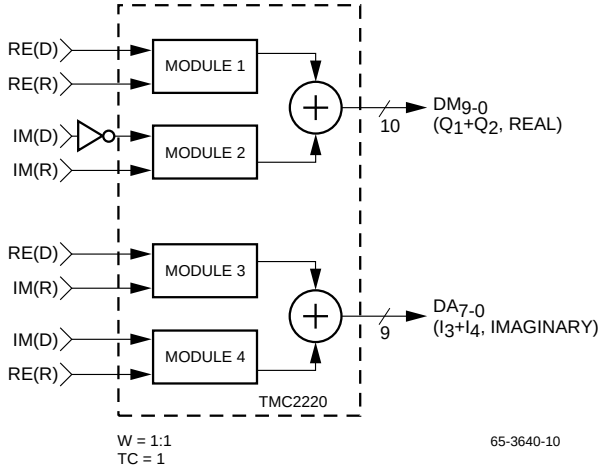


Figure 7. Full Complex Correlation with the TMC2220

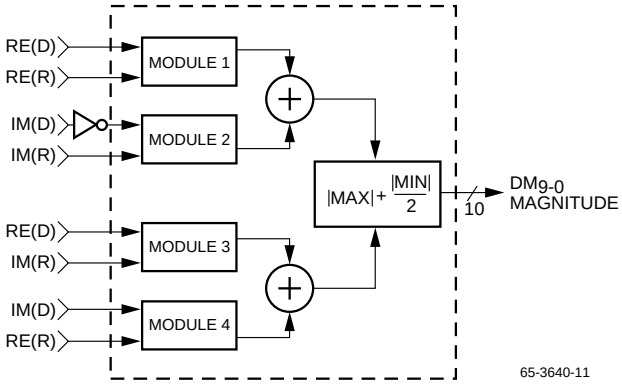


Figure 8. Complex Correlation with Magnitude Result

The TMC2221 can be cascaded to implement correlations of more than 128-bits. Typically all clocks, reference inputs and enables are connected together and the A and B outputs of preceding stages are connected to the respective inputs of subsequent stages. An external summer is required to generate the composite correlation score.

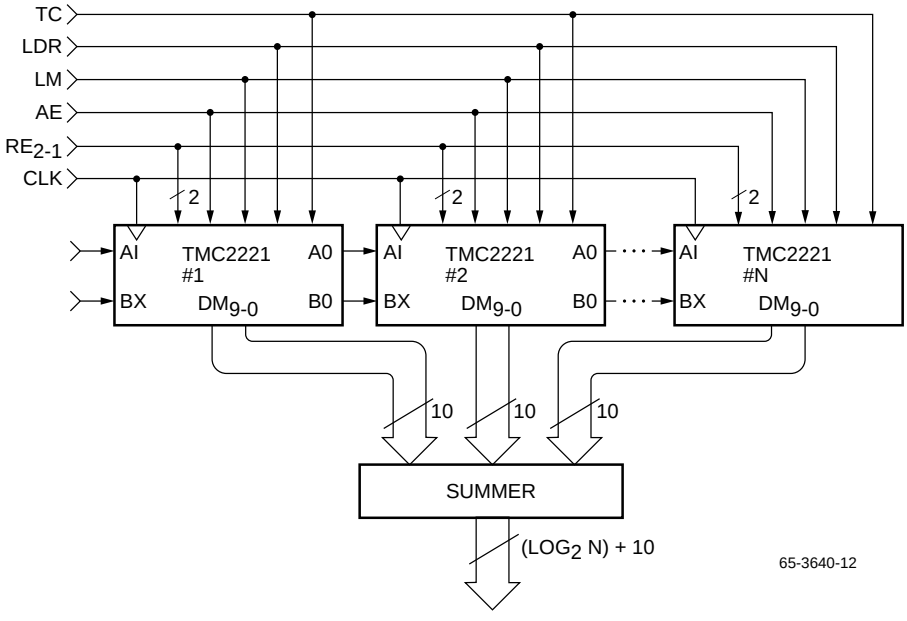


Figure 9. Cascading the TMC2221 for Extended - Length Correlation

The TMC2221 may also be used to compare multi-bit words with a single-bit reference. When this is done, the output of each TMC2221 must be appropriately weighted to the adder circuitry. The weighting reflects the relative importance of the different bit positions. Weighting can normally be accomplished by simple bit shifts at the input to the summer.

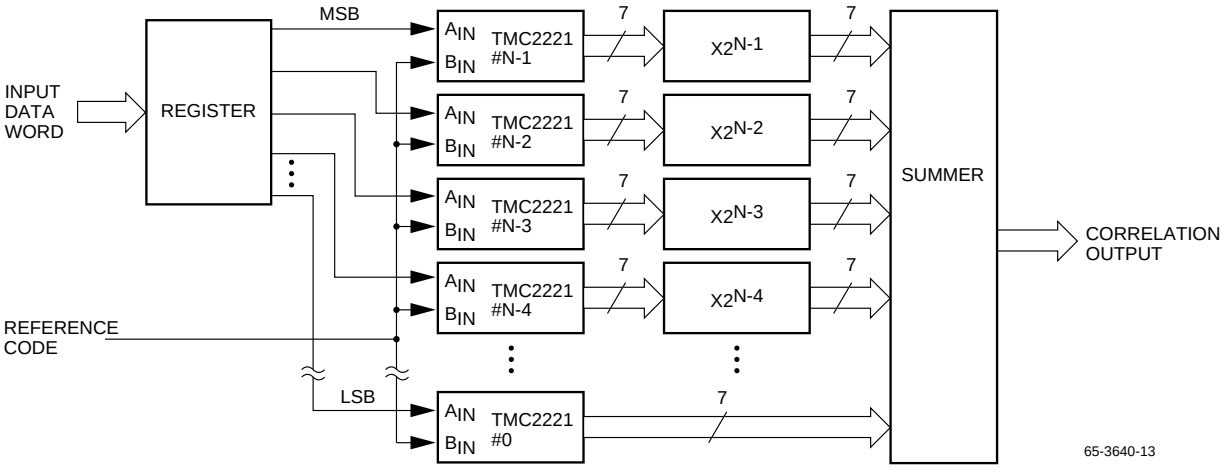


Figure 10. Multi-Bit x 1 Bit Correlation

Equivalent Circuits

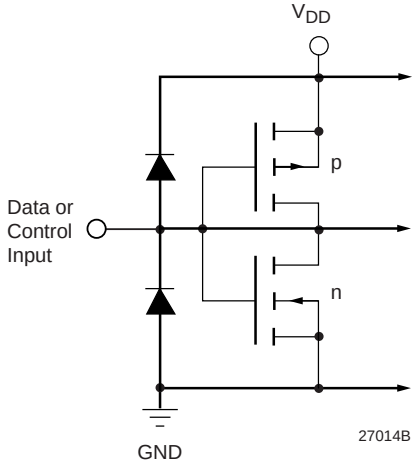


Figure 11. Equivalent Input Circuit

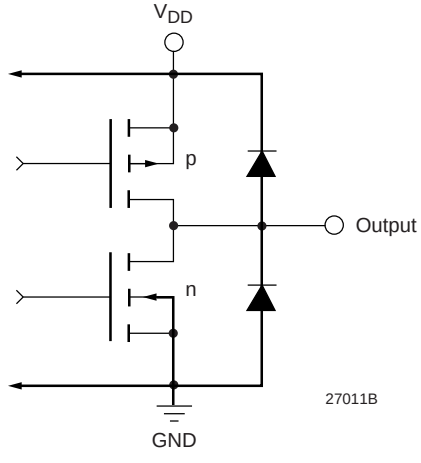


Figure 12. Equivalent Output Circuit

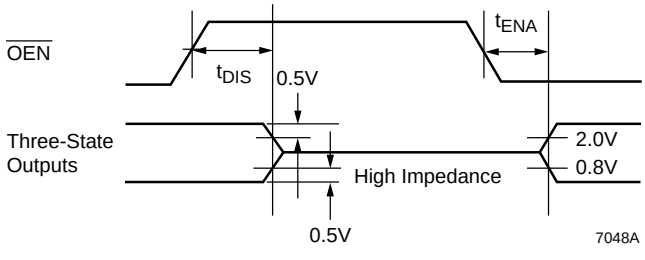


Figure 13. Threshold Levels for Three-State Measurements

Notes:

Notes:

Notes:

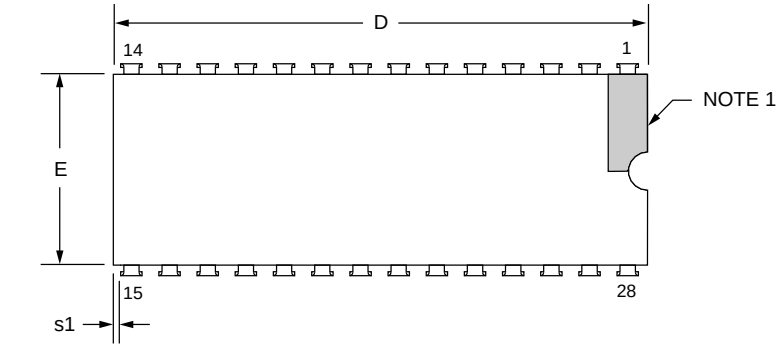
Mechanical Dimensions

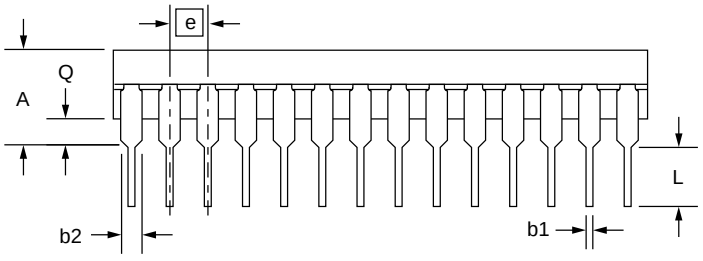
28 Lead Ceramic DIP Package

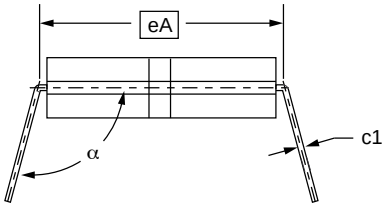
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.232	—	5.92	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.490	—	37.85	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5
eA	.600 BSC		15.24 BSC		7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 14, 15 and 28 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 28.
6. Applies to all four corners (leads number 1, 14, 15, and 28).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-six spaces.







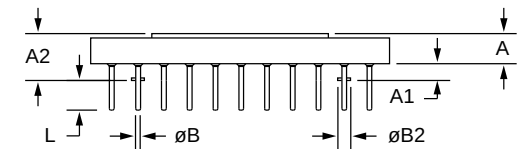
Mechanical Dimensions (continued)

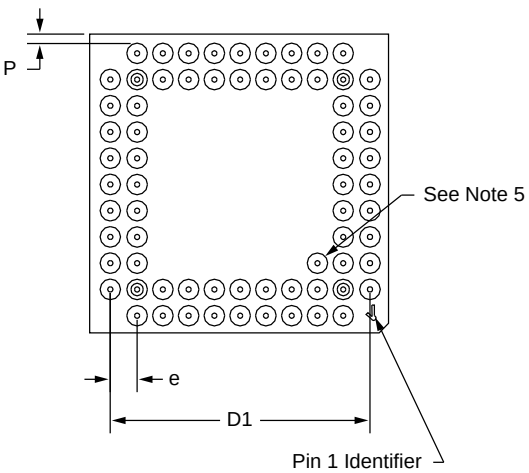
68 Lead Pin Grid Array Package

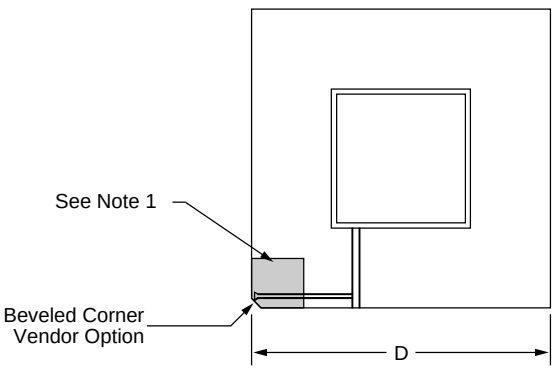
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.040	.060	1.02	1.52	
A2	.115	.190	2.92	4.83	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.
5. Optional index pin.







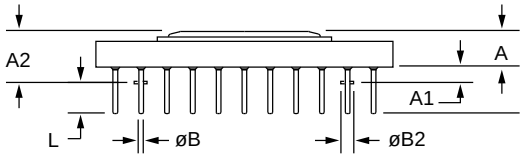
Mechanical Dimensions (continued)

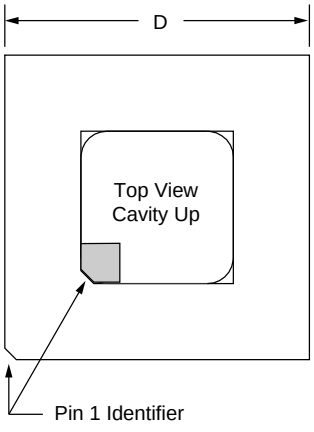
69 Lead Pin Grid Array Package

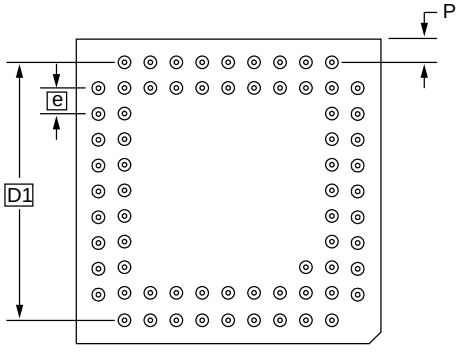
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.140	1.180	28.96	29.97	SQ
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
M	11		11		3
N	68		68		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2220G8C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	68 Pin Grid Array	2220G8C
TMC2220G8V	EXT-T_C = 55°C to 125°C	MIL-STD-883, 17MHz	68 Pin Grid Array	2220G8V
TMC2220G8C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	68 Pin Grid Array	2220G8C1
TMC2220G8V1	EXT-T_C = -55°C to 125°C	MIL-STD-883, 20MHz	68 Pin Grid Array	2220G8V1
TMC2220H8C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	69 Pin Plastic Pin Grid Array	2220H8C
TMC2220H8C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	69 Pin Plastic Pin Grid Array	2220H8C1
TMC2221B6C	STD-T_A = 0°C to 70°C	Commercial, 17MHz	28 Pin CERDIP	2221B6C
TMC2221B6V	EXT-T_C = -55°C to 125°C	MIL-STD-883, 17MHz	28 Pin CERDIP	2221B6V
TMC2221B6C1	STD-T_A = 0°C to 70°C	Commercial, 20MHz	28 Pin CERDIP	2221B6C1
TMC2221B6V1	EXT-T_C = 55°C to 125°	MIL-STD-883, 20MHz	28 Pin CERDIP	2221B6V1

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