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# FILU-200™ ⇨ 200 MIPS 30000 gate DSP Coprocessor Core

## *Performance*

- 200 MIPS in 0.25 μm
- Dual Mac architecture
- 16-bit architecture, 20-bit internal data path, 44-bit accumulation

## *Features*

- Fully synthesizable Verilog – single clock design
- Technology independent
- Scan testable – high test coverage
- Enables efficient DSP on RISC or CISC processors
- Enables DSP development in C

## *Microcoded Functions*

- Real & Complex FFT/IFFT
- FIR filters
- Adaptive filters
- 1st, 2nd & Nth order IIR filters
- Real & Complex Matrix/Vector operations

## *Applications*

The FILU enables the efficient realization of very high performance DSP in a large variety of applications where a RISC or CISC is already present.

- Telecomms (Soft Modems/xDSL)
- Consumer (Speech, Audio)
- General purpose DSP

## *Introduction*

The FILU-200™ is a small 16-bit 200 MIPS DSP coprocessor core. It is a dual MAC architecture with dual adders and dual barrel shifters and is tailored to enable highest performance DSP on RISC/CISC processors. Applications include soft modems, speech & audio processing and a wide range of other DSP based products.

The FILU is capable of implementing various DSP functions which are pre-programmed and are accessed by a host processor (RISC/CISC) via a shared RAM. This RAM is viewed by the Host as a memory mapped peripheral. The Host has Master control of the RAM via control bits. All the DSP functions are fully parameterizable and configurable by the Host. A simple API is provided to allow the Host to access the FILU through simple C macro function calls.

The microcoded kernel includes FFT/IFFT, FIR and IIR filters, adaptive filters, correlation, Taylor series, real and complex matrix/vector operations. Extra DSP functions can be microcoded to suit particular applications.

The FILU-200™ is particularly well suited to fast complex number arithmetic. A Radix-4 butterfly can be implemented in 8 cycles yielding a fully complex 1024 point FFT in 128 μs. Near floating point performance is achieved via a 20-bit internal data path and block-floating point arithmetic.

It is expected that the user will develop their application entirely in C using an API to invoke FILU functions. To aid in the development process C and Verilog models are provided to allow system simulation.

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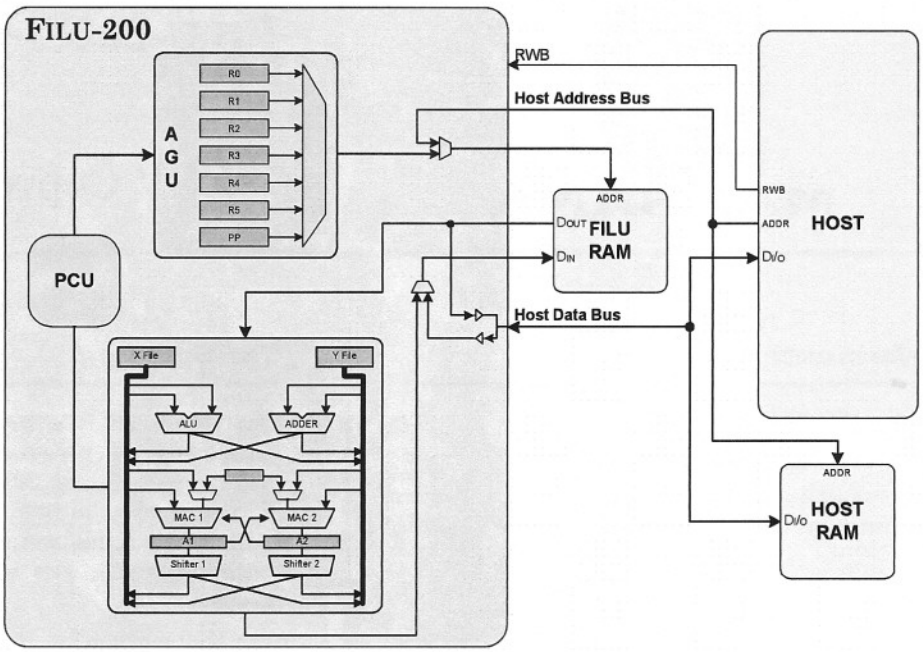


**Figure 1** FILU-200™ *block diagram and Host Interface.*

## *Benchmarks*

The following benchmarks assume a 100 MHz clock.

| Function | Data Points | Num of Coeff | Num of Cycles | Exec Time µs |
|---|---|---|---|---|
| **Real FIR** | N =100 | p = 20 | N(p/2+1)+p+18 | **11 µs** |
| **Real FFT** | N = 1024 | - | $N(\log_4 N+1)+49$ | **62 µs** |
| **Complex FFT** | N = 1024 | - | $2N(\log_4 N+½)+30$ | **103 µs** |
| **Complex Mult**[1] | N = 256 | N = 256 | 3N+9 | **8 µs** |
| **2nd Order IIR** | N = 256 | M = 8 | 2N+17 | **5 µs** |

[1]Complex vector multiply of 256 complex data points.

## *Technical Specification*

- ❑ Fully synthesizable – library independent
- ❑ 20-bit internal data path, 44-bit accumulation
- ❑ 16/32-bit host interface
- ❑ 30000 gates
- ❑ 0.75 $mm^2$ in 0.25 µm TLM

## *Hardware & Software Interface*

The FILU uses a very simple hardware and software interface. The FILU RAM is memory mapped into Host address space. An API allows the Host to use C function calls. These automatically generate the appropriate initialization vector for the RAM.

- ❑ Coefficients & data written as vectors in RAM, accessed with pointers
- ❑ A busy bit indicates start/end of processing
- ❑ Host has Master control of RAM via control/status bits in RAM

## *For More Information*

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