Power, Area and Delay Performance Comparison of Multipliers for Embedded Systems

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Abstract:
Fast and low cost multiplier units are imperative in designing highly reliable and efficient embedded systems. Most options available for embedded systems provide a tradeoff between power and speed of multiplier circuits. In this study, we have analyzed the performance (power, delay and area) of 3 different multipliers suitable for embedded applications. Both array and tree multipliers with varying word lengths and with different full adder topologies were implemented using Magic 7.3, and simulated using IRSIM 9.5 and Orcad/PSpice 9.2.3. Behavioral synthesis of the multipliers was implemented using Verilog. Simulation results demonstrated that Wallace tree multiplier is efficient for use in high-speed embedded systems, whereas array multipliers are suitable for low-power and area-constrained embedded applications. Voltage scaling has reduced the power consumption by almost 4-fold, due to its quadratic effect.

1. Introduction

Power estimation, evaluation and optimization have become pivotal factors in embedded system design, especially in the rapidly growing market of mobile handheld computing, communication and Internet devices. Decreasing channel sizes in embedded systems can result in overheating of the integrated circuits and reduction in the operation time between recharging phases of mobile computing devices [1][2][3]. Consequently various embedded systems are now designed with low-power dissipation as a primary design constraint [4][5][6]. Multiplier is a fundamental arithmetic unit in these systems [7]. Although multipliers operate at slower speeds, they occupy relatively large portion of the chip area, and are power consuming[8][9]. Many researchers have been focusing on various techniques to develop low power multipliers operating at high speeds [8][10][11][12][13]. The main focus of this research is on implementing multipliers at transistor level and applying low-level power optimization techniques. We have also implemented the layouts of all the multipliers analyzed in this research using 0.13μm technology. The rest of the paper is organized as follows: Section 2 describes about the multipliers used for our analysis, Section 3 explains the various power reduction techniques implemented, Section 4 presents the experimental setup and simulation results, and Section 5 provides concluding remarks.

2. Multipliers

High–speed and low-power multiplier units are inevitable in embedded system applications, digital signal processors [14] and high-performance computer graphics processors. The fast multipliers used for our analysis are Braun's carry-save multiplier [15], Wallace tree multiplier [16] and Baugh-Wooley multiplier [17]. Braun's carry-save multiplier [15] is based on add and shift algorithm. In these multipliers, the number of partial products are shifted according to their orders and then added. In an nxm carry-save multiplier, there are $n(n-2)$ full adders, n half adders and n^2 AND gates. Baugh-Wooley Multiplier [17] performs 2's complement multiplication. This is developed to design regular multipliers for 2's complement multiplication and to maximize regularity of multiplication array. Partial products in the final stage are adjusted with negative signs. Wallace tree multipliers [16] are the best tree array multipliers. For faster multiplication, these are used, as all bit products are generated simultaneously. Partial sum adders can be

Full Adder Topology	Wallace Tree			Baugh Wooley			Braun's carry save		
	4 x4	8 x 8	16 x 16	4x4	8 x8	16 x16	4x4	8x8	16x16
10 Transistor	21600	94400	388600	21000	91600	120400	21600	62400	72000
14 Transistor	26400	104000	426000	24600	98700	140600	24800	68300	76000
16 Transistor	28800	128000	520600	33300	388600	523600	26400	201600	220800
28 Transistor	43200	194000	685200	43800	477800	597000	36000	284000	310500

Table1: Area measurement of multipliers with different adder topologies (in μm^2)

rearranged in a tree like fashion, reducing the critical path and the number of cells needed. In Wallace tree architectures, all bits of all the partial products in each column are added together by a set of counters in parallel without propagating any carries.

Each of the above multiplier is implemented with 4 different full adder [FA] topologies: 10 transistor FA [18], 14 transistor FA [19][20], 16 transistor FA [19] and 28 transistor FA [15]. The 10 transistor full adder is implemented using pass transistor logic. Transmission gates and pass transistors are used in 16 and 14 transistor full adders. 28-transistor fill adder is regular CMOS full adder.

3. Reduction Techniques

In our analysis we have implemented low-level optimization techniques, such as transistor sizing, voltage scaling and signal gating on each of the multipliers and evaluated the effects on performance of the circuits. As well known**,** transistor-sizing [12][13] approach reduces dynamic power consumption and leakage power consumption. Using minimal size transistors for gates with maximum switching activity reduces the dynamic power. The approximate dynamic power dissipation of CMOS circuits [12][15][19] is given by

$$P \approx CV^2f, \quad (1)$$

where C is the capacitance, V is the supply voltage and f is the frequency at which it operates. Voltage reduction [5][12][15] is one of the well-known techniques implemented due to its quadratic effect. In low voltage devices the threshold voltage is also reduced, but not at the same rate as the operating voltage. Reducing the threshold voltage increases the sub threshold leakage current exponentially. Signal gating [12][21] is another well-known power reduction technique, where unwanted switching activities are masked. Using AND gate, tri-state buffer, latch or transmission gate is the simplest way to mask the unwanted signals. The logic designer should consider the fact that the power consumption for this control circuitry should be less than the propagation of unwanted signals. We have implemented all the above techniques in our analysis and the results are discussed in the next section.

4. Experimental Setup

A. Simulators

For our simulations, we used: Magic 7.3 for layout, IRSIM 9.5 for circuit-level simulation and Pspice 9.3 for transistor level simulation. Verilog was used for behavioral modeling. The host machine for Magic was Red Hat Linux 9.0 and for Verilog and Orcad/PSpice it is Windows 2000 (on a Pentium-IV processor). All the simulations were single tasks with no other application running in the background. Each of the results is an average of 8 iterations of simulations. We have used both array and tree multipliers in our analysis. Braun's carry-save and Baugh Wooley are array multipliers, while Wallace tree is a tree multiplier.

B. Results

Estimates of the total area of the three multipliers are presented in Table1. Each multiplier is implemented with 4 different types of full adders with 10-transistor full adder being the smallest and 28-transistor adder being the largest. The area and power of the 10 transistor adder multipliers are relatively smaller compared to the other multipliers. All the area is measured in μm^2. Array multipliers consumed lesser area than Wallace tree multiplier even with increasing number of bits and high-count transistor adders. This is due to the highly irregular structure of the Wallace tree multiplier. Signal gating is implemented on array multipliers as proposed in [21]. This algorithm implements partial gating of

the array multipliers. The area of array multipliers with signal gating is 1.24 times that of non-gated version. For Wallace tree multiplier, the area is 1.24 times that of non-gated version. Hence area optimization is of prime concern when using gating technique.

Power consumed by all the multipliers is plotted in Fig 1. CMOS implementations of these circuits were done using 0.13µ technology. The power consumed by the array multiplier is less than the power consumed by the Wallace tree multiplier. This is due to the increased area of the Wallace tree multiplier. There have been propositions made to overcome this problem by using rectangular tree structures [16]. For 2.5v the power consumed is 30% less than that consumed for 5v.

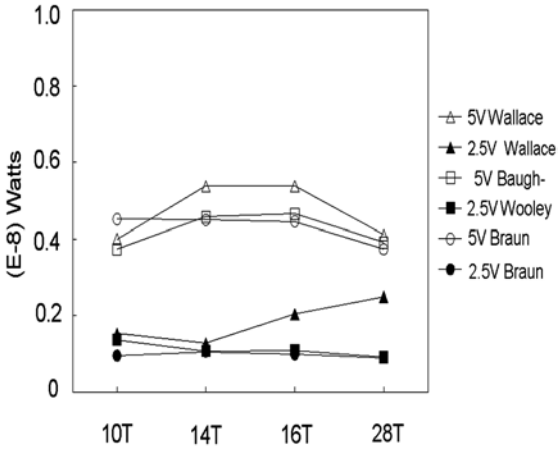

Fig1: Power consumption of 4x4 multipliers with different full-adders and varying voltage

Hence voltage reduction technique is very important method to reduce power dissipation. The graph also shows that having more number of transistors does not mean more power in all the cases. The power consumed by 16-transistor adder circuit is more than 28 transistor adder circuit due to the transmission gates used in 16-transistor adder circuit. Fig 2 shows the power consumption of 8x8 and 16x16 multipliers with 10 and 16 transistor full adders. There is no significant difference in the power for 8x8 multipliers. For 16x16 multipliers, using Braun's multipliers is optimal with 10-transistor topology. The difference between power consumption (for 16x16 multipliers) with 10 transistor and 16 transistor topology adders is negligible in Wallace, whereas it's too high in Braun multiplier. Fig 3 shows the graph with varying threshold voltages and the operating voltage fixed at 5V; there is a significant decrease in power for 10 and 28 transistor full adders. Decreasing threshold voltage has increased the power dissipation significantly. Hence there should be a balanced variation between threshold voltage and operating voltage.

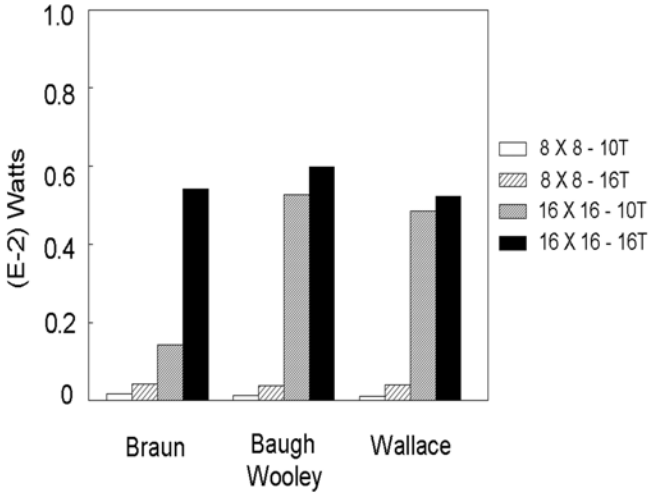

Fig 2: Power consumption of 8x8 and 16x16 multipliers

Effects due to varying threshold voltage are very structure dependent. Applying transistor sizing to the multiplier circuits has resulted in an interesting observation. Using equal length N and P transistors has more power consumption as compared to using N and P transistors with 1:3 ratio. Critical paths in each multiplier are identified using [13] and the sizing is applied to transistors in that path. There is a one-fold decrease in the power consumption of the multipliers using sizing.

Delay is the most significant factor in the design of any high-speed embedded processors. Table 2 presents the critical path delay of 4x4 multipliers. Wallace tree multiplier is the fastest of all the three multipliers. For a 16 transistor full adder the delay is higher than the 28-transistor adder. The delay of 10 transistor and 14 transistor adder topologies for Wallace tree is same. Wallace tree multiplier with 10-transistor topology seems to be a good choice for high-speed embedded systems. When signal gating [21] was applied, the delay of the multipliers is increased by a factor of 0.13 % for Wallace tree, 0.17% for Braun's carry-save and 0.194% for Baugh wooley multiplier.

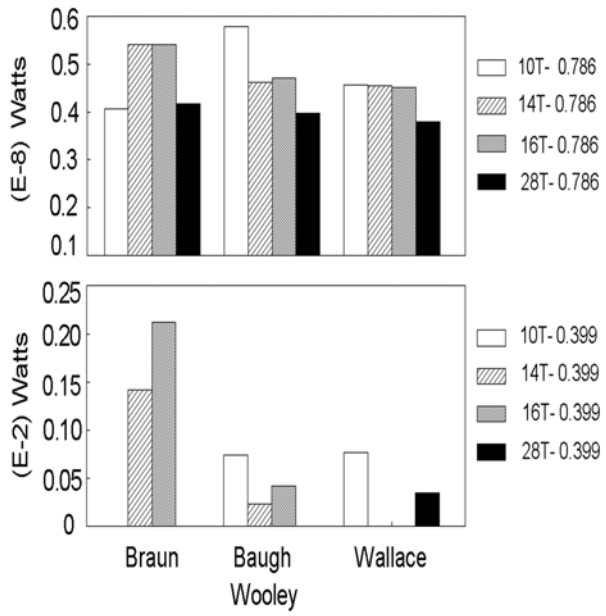

Fig 3: Power consumption of Multipliers with varying threshold voltage

4x4 multiplier	Wallace Tree	Baugh Wooley	Braun-Carry save
10 Transistor	4.118 ns	6.742 ns	6.092 ns
14 Transistor	4.118 ns	6.322 ns	6.175 ns
16 Transistor	6.092 ns	6.207 ns	6.246 ns
28 Transistor	4.183 ns	6.109 ns	6.207 ns

Table. 2. Critical Path Delay of 4x4 multipliers

5. Conclusions

In this paper we have studied and analyzed power dissipation, delay and area of 3 different multipliers with 3 different word sizes. Each multiplier was implemented using 4 different types of full adders. The study shows that tree multipliers are the fastest multipliers for high-speed embedded systems. Area consumed by Wallace tree multipliers is 18 % more than that of Braun multiplier for 16-bit multiplier implementations. There is a significant change in the power dissipation for higher bit multipliers compared to smaller multipliers. The power consumed by 16-bit multiplier with 16-transistor adder topology is approximately same for both Wallace and Braun multipliers. For low-power embedded systems it is suggestible to use Braun's multiplier compared to tree multipliers. However using power reduction techniques resulted in 30% savings in these multiplier units. Wallace tree multiplier (10-transistor full adder) with transistor sizing and voltage reduction techniques would be the most efficient one to use for embedded systems.

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