TP 14.6: A 70Mb/s Variable-Rate DMT-Based Modem for VDSL

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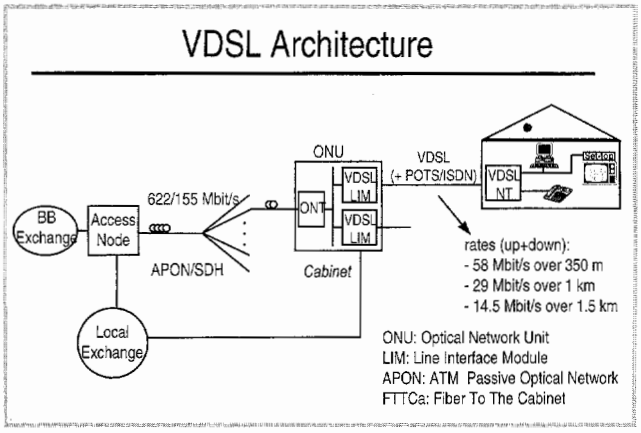
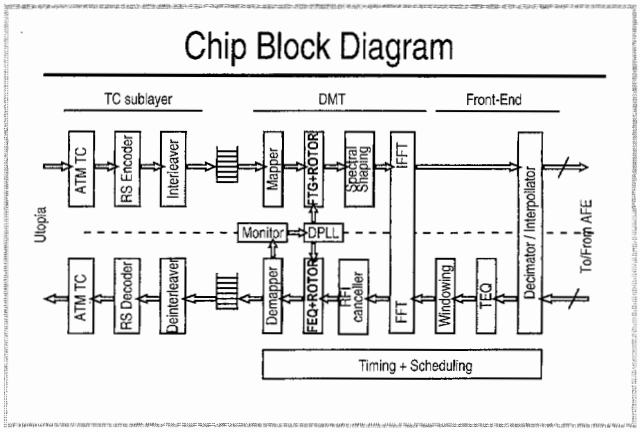
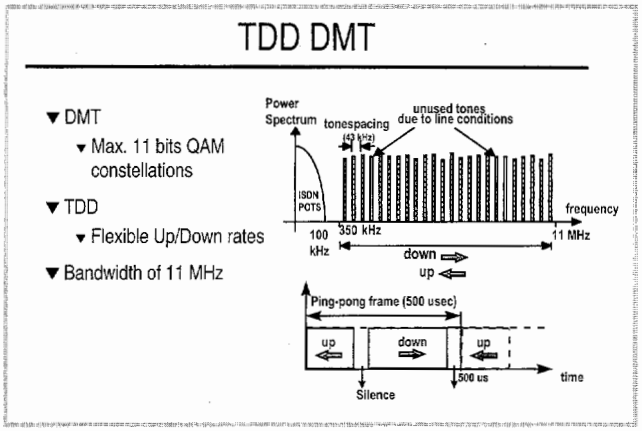
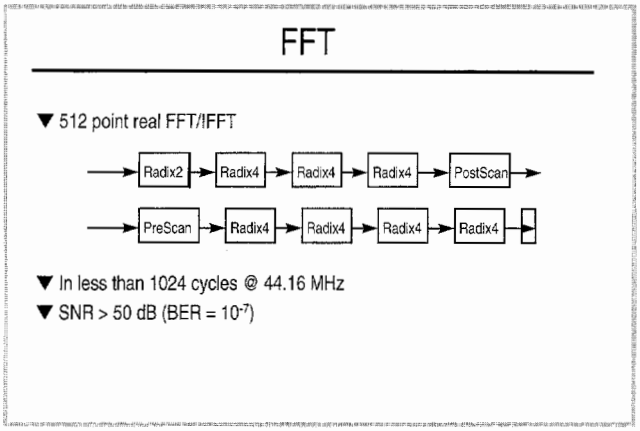
A chip integrates digital signal processing required by a TDD-DMT VDSL system and transport convergence sublayer functions. The chip processes a 512-point real FFT/IFFT in <20μs. A fully-programmable RS encoder/decoder and (de)interleaver provides error-correction. The 150mm² chip in 0.35μm CMOS dissipates 2.7W at 3.3V.

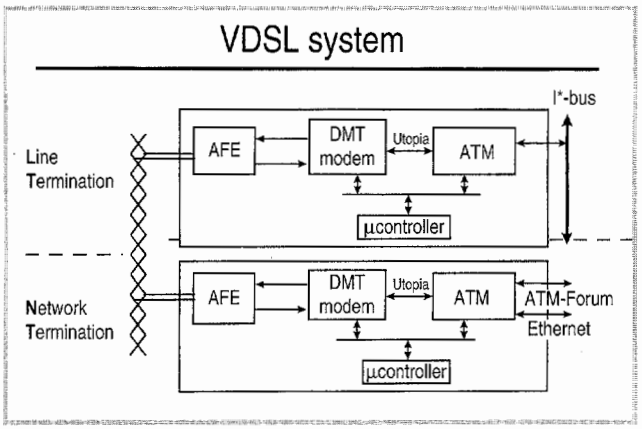
See Digest page 248

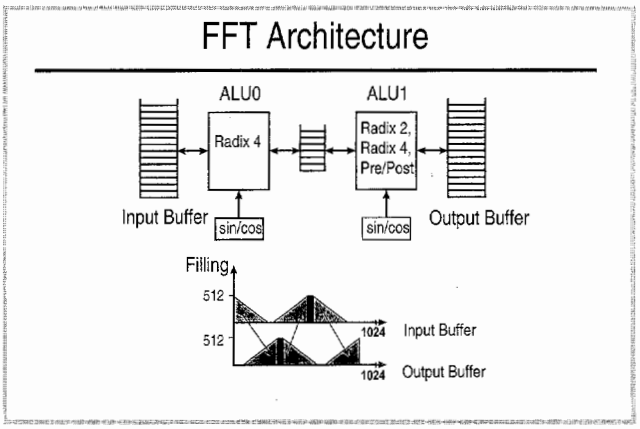






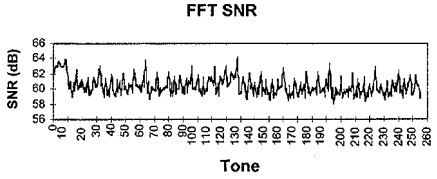






FFT Architecture

- ▼ Floating point : 13 bits mantissa, 4 bits exponent
- ▼ Smaller multiplier
- ▼ Increased signal dynamics
  - ▼ Enable digital RFI cancellation
- ▼ SNR

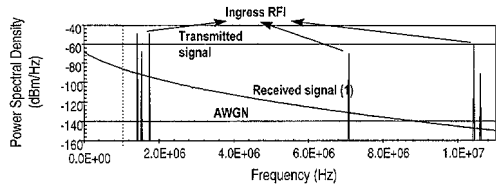


RFI cancellation

- ▼ Floating point
  - ▼ 13 bits mantissa, 4 bits exponent
- ▼ Ressource sharing between different steps
  - ▼ Floating point complex division
  - ▼ Floating point complex multiplication
- ▼ Performance
  - ▼ up to 2 RFI per DMT
  - ▼ 45 dB interference reduction

RFI cancellation

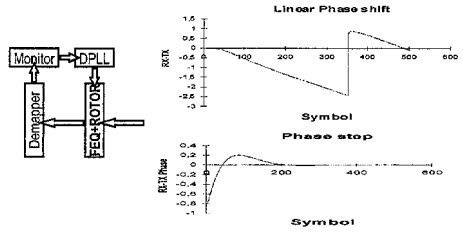
- ▼ Characteristics



(1) Cable type 26 AWG, 1 km
AWGN = Average White Gaussian Noise

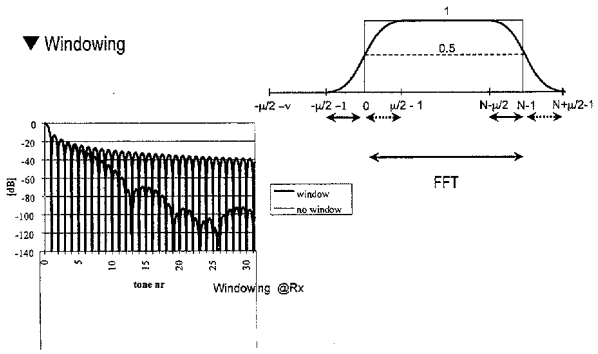
DPLL

- ▼ Programmable order
- ▼ Bandwidth from 0.1 Hz to 100 Hz



RFI cancellation

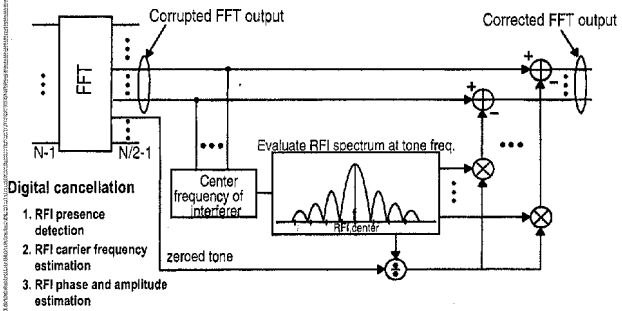
- ▼ Windowing



FEC

- ▼ RS encoder/decoder
  - ▼ Overhead programmable from 0 to 16
  - ▼ Data programmable from 2 to 255
  - ▼ RS Decoding in 1200 cycles
    - ▼ Maximum 70 Mb/s throughput
  - ▼ Dynamic parameter adaptation without loss of data

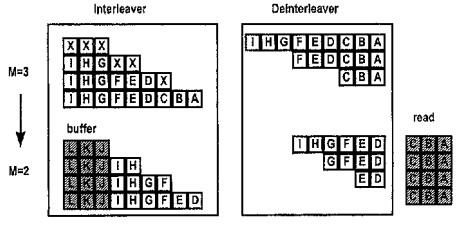
RFI cancellation



11

FEC

- ▼ Interleaving
  - ▼ Correct error burst up to 300 us
  - ▼ Dynamic rate adaptation without loss of data : use of dummies



Continued on Page 451

Continued from page 217

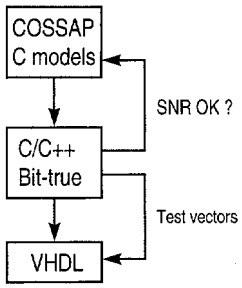
ATM TC

- TC layer
  - Scrambling/descrambling
  - HEC generation, HEC check
  - Cell delineation
  - Idle cell generation, Idle cell removal
- Utopia Slave interface
  - Level 2, byte based
  - 19.44 MHz

Conclusions

- Flexible DMT TDD modem in 0.35 um technology
- New FFT architecture
- Digital RFI cancelling
- Maximum performance of 70 Mb/s

Design Methodology



Chip Characteristics

Technology :	0.35 μm 5-metal CMOS
Gate :	680 k
RAM :	900 kbit
Frequency :	44.16 MHz
Area :	150 mm^2
Package :	PQFP-208
Transistors :	9.0 M
Power dissipation :	2.7 W @ 3.3 V

Chip photograph