Multichannel adaptive filtering with the DSP56200

A multichannel adaptive filter has more than one reference signal, each of which passes through a finite impulse response (FIR) filtering structure. The DSP56200 can perform this type of filtering by using its data RAM access register to provide a third input as shown in the diagram. The number of taps in each FIR structure is programmable using the values in the FIR tap length register and RAM address register.

To configure the DSP56200 as a multichannel adaptive filter follow these steps:

1. The DSP56200's FIR tap length register must be loaded with the sum of the number of taps in each of the two FIR structures. This is different than the normal operating modes of the DSP56200, where the register is loaded with the number of taps minus one. The sum of the number of taps must not be greater than 255 or less than four taps. The number of taps in the first FIR structure does not have to equal the number of taps in the second FIR structure.

2. The DSP56200's configuration register must be programmed as a single adaptive FIR filter (bits 6 and 7). The rounding enable, coefficient update disable, and leakage enable bits in the configuration register work identically to normal adaptive filter operation. The DC tap option, however, is only available to the second FIR structure, and is controlled with the DC tap enable bit.

3. In addition to writing the X1 and D registers, the host processor must also write the RAM address, data and coefficient RAM access registers every sample period. All three bytes of the coefficient RAM access register must be written with zeros. The data RAM access the first FIR structure. Once the DSP56200 is initialized, these registers must be written every sample period. Note that internal to the DSP56200 there is an inherent delay of one sample period on the second FIR structure's input stream as shown in the diagram.

4. Unused data and coefficient RAM locations are not available to the user during real-time operation since the data and coefficient RAM access registers must be written every sample period.

5. As in the standard adaptive filtering mode, the DSP56200 provides the two's complement of the error term in the output register when operating as a multichannel adaptive filter.

6. Performance is determined using the DSP56200 performance calculations for the single adaptive filter mode:

Maximum $f_s \le f_{ck}/\#cycles$,

where
f_{ck} = DSP56200 input clock frequency
#cycles = 17+2N+r
(single adaptive filter mode)
r = 30+n-N : (30+n-N)>0
= 0 : otherwise
n = #chips cascaded together
N = Value of FIR tap length register + 1

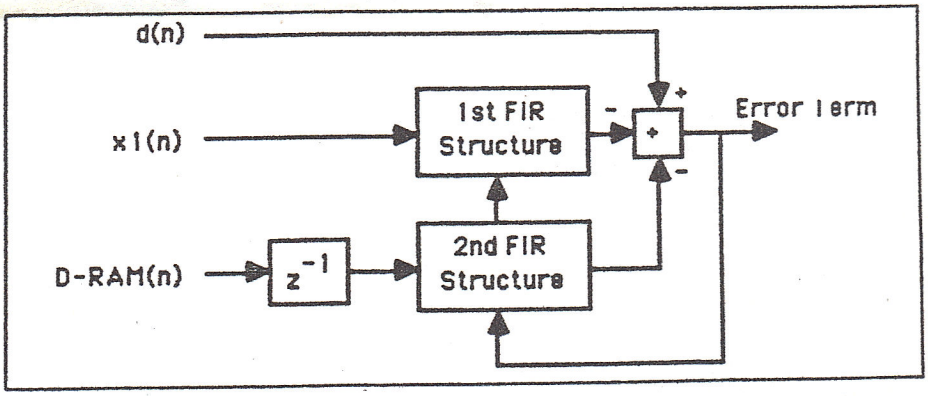
The following example will determine the DSP56200 register values both the initialization and real-time filtering phases. During real-time filtering these five registers must be written every sampling period. The values of all other registers and of the don't care bits are determined by the application.

Register Values for Initialization
FIR tap length = Sum of #taps
(3 taps + 8 taps = 11 taps)
Configuration = 100xxxxx
(binary, "x"is "don't care")

Register Values for Real-time Filtering
D = Primary input
X1 = Reference input
(3-tap channel)
Data RAM access = Reference input
(8-tap channel)
Coefficient RAM access = 0
RAM address = #taps in the first FIR
= 3

Performance Calculation
Using the performance equations:

n = #chips cascaded together
= 1
N = FIR tap length+1
= 11 + 1
= 12
#cycles = 17+2*N+r
= 17+2*N + (30+n-N)
= 17+2*12 + (30+1-12)
= 60
Maximum $f_s = f_{ck}/\#cycles$
= 10.25 Mhz/60
= 170 Khz.



The DSP56200 data RAM access register provides a third input for a multichannel adaptive filter