SESSION VI: LSI Logic

Chairman: W. David Pricer
IBM Components Div., Essex Junction, Vt.

WPM 6.1: A Monolithic 16 x 16 Digital Multiplier

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THE DESIGN, FABRICATION and testing of a 16 x 16 multiplier fabricated on a single monolithic chip will be described.

The chip was designed for use in a small, fast, multipurpose processor being built for avionics applications. The multiplier is set up for a two's complement number system to be compatible with that processor. The chip also features tri-state buffers for the output signals and holding registers for the input signals. This feature not only allows the external leads in the system to be time shared, but also allows the chip signal leads to be time shared, reducing the total number of leads to 32 data lines, 4 control signals, plus several leads for power supply and ground.

Figure 1 shows a schematic for the most commonly repeated cell. One important difference in the design of this circuit from most previous circuits can be determined by studying this schematic; the logic levels are not restored at the output of each block. The reasons for this is that risetimes do not add linearly but approximately as root sum of squares. Thus, if one stage has τ risetime to some circuit threshold, N stages between thresholds have $N^{1/2}\tau$ delay rather than $N\tau$ as one would get with thresholding at each stage. This makes an important difference in the delay times for large asynchronous circuits. The reason one can afford to do this for an LSI chip is that the on-chip environment is much less subject to switching transients, ground noise, etc.

This technique of using many stages of logic before restoration of logic levels is particularly appropriate for a *double-railed* logic system, where a signal and its complement are separately synthesized and both are sent to the next logic elements; eliminating intermediate inverters which would have threshold effects leading to linearly accumulating delay times.

Figure 2 is a photograph of a completed chip, showing that portion of the circuit which corresponds to Figure 1. Corresponding circuit elements occupy about the same realtive positions in both Figure 1 and Figure 2. Figure 3 is a block layout showing how the individual cells are assembled to form the complete circuit. The circuit is exceedingly repetitive; this was used to good advantage, as mask generation was accomplished via layout on automated layout equipment*. The layout of *cell* A was optimized for minimum dimensions, and the other cells were made to fit.

This circuit was fabricated by the triple diffusion process[1] starting with homogenous P-type wafers of 3 Ω-cm resistivity. In this process, the collector, base and emitter are formed by successive diffusion steps. This process is actually very old in the history of integrated circuits, but was abandoned in favor of buried layer epitaxial construction for most applications. There were two major reasons: (1)—the lightly doped collector diffusion was very difficult to control; (2)—the lower r_c' of the buried layer. This second objection is still present, but is not an important item in the design of emitter follower logic circuits.

With the present technology it is easy to control the collector doping sufficiently well to make LSI circuits. Using ion implantation for the collector deposition, the collector sheet can be held to ±5 per cent with relative ease. Most resistors are made using the collector under a base diffusion, however, and the accuracy of these resistors is only ±20 per cent because of diffusion variability, Figure 4 is a cross section of triple diffused devices, showing a coalesced NPN, PNP and load resistor.

Counting each emitter or resistor as a device, the device count for this chip is about 16,700. The chip size is 301 x 279 mils, giving a figure about 5 mil^2/device. This device density is somewhat higher than for standard epitaxial construction due to the fact that all devices are self-isolated and may be closely packed.

Yield of functional devices at wafer probe test has been excellent, averaging about 3 good die per wafer – out of only 19 possible. This good yield is due to the combination of the triple diffusion process – which gives very few defects, albeit poorer transistors than epitaxial construction – with emitter follower logic, which does not require exceptional device performance.

The wafer probe test is performed in the following way. A read-only memory is programmed to have a sequence of input data in one block and the corresponding correct answers in another block; the input words are fed to the chip and the output of the chip compared bit-by-bit to the correct answer. The results of the comparison are displayed on an oscilloscope to give the operator instant visibility as to which bits are in error and in which word position. The display is a plot with X-position corresponding to input word number and Y-position corresponding to output bit number. The Z-axis is modulated in such a way that one gets a spot at each position where a bit did not compare. In this way systematic errors can be detected and the mask set corrected.

Tests have been performed on packaged units. The results of these tests indicate a fixed delay of about 200 ns for all data outputs, plus a delay proportional to $N^{1/2}$ where N is the number of logic delay stages in the matrix associated with the output. This last term is about 130 ns for 31 stages (the maximum) giving a total multiply time of 330 ns.

*Applicon 762

[1] Buie, J. L., and Breuer, D. R., "A Large-Scale Integrated Correlator," *The Journal of Solid-State Circuits*", p. 357-363; Oct., 1972.

Operation of the Circuit

To load data into the holding registers, the tri-state buffers for that register are disabled by applying 2.5 V to the READ terminal, the data lines are energized, and the appropriate LOAD terminal is toggled high. After about 330 ns, the data may be taken from the multiplier by enabling the READ commands. Data may be loaded into both registers simultaneously if desired, and output of the most significant half product may be taken at the same time as the least significant half product. Alternatively, the load may be accomplished one word at a time and either the most significant half or least significant half product may be read out first.

Figure 5 shows a set of typical waveforms for this circuit.

Acknowledgments

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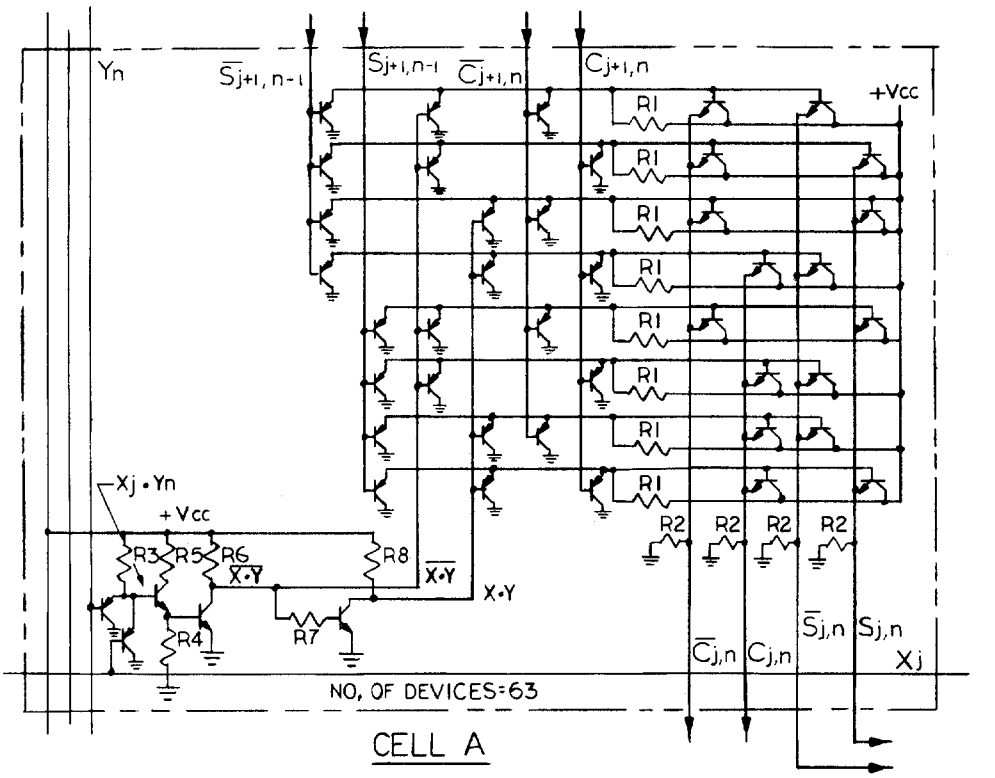


FIGURE 1—Schematic diagram for most commonly repeated cell.

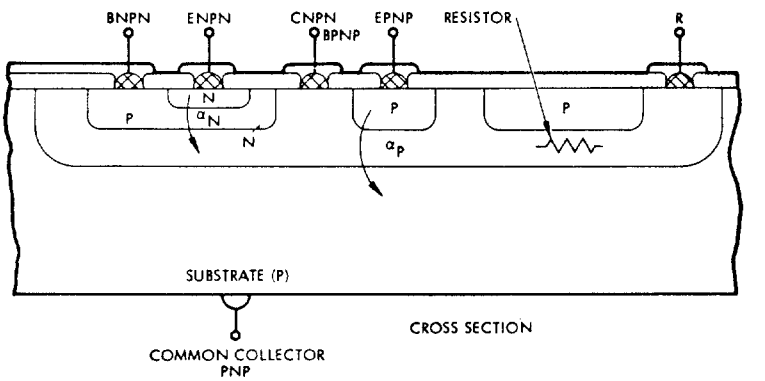


FIGURE 4—Cross-section of NPN and resistor. This figure illustrates how these devices may be coalesced to save space.

[See page 228 for Figures 2, 3 and 5.]

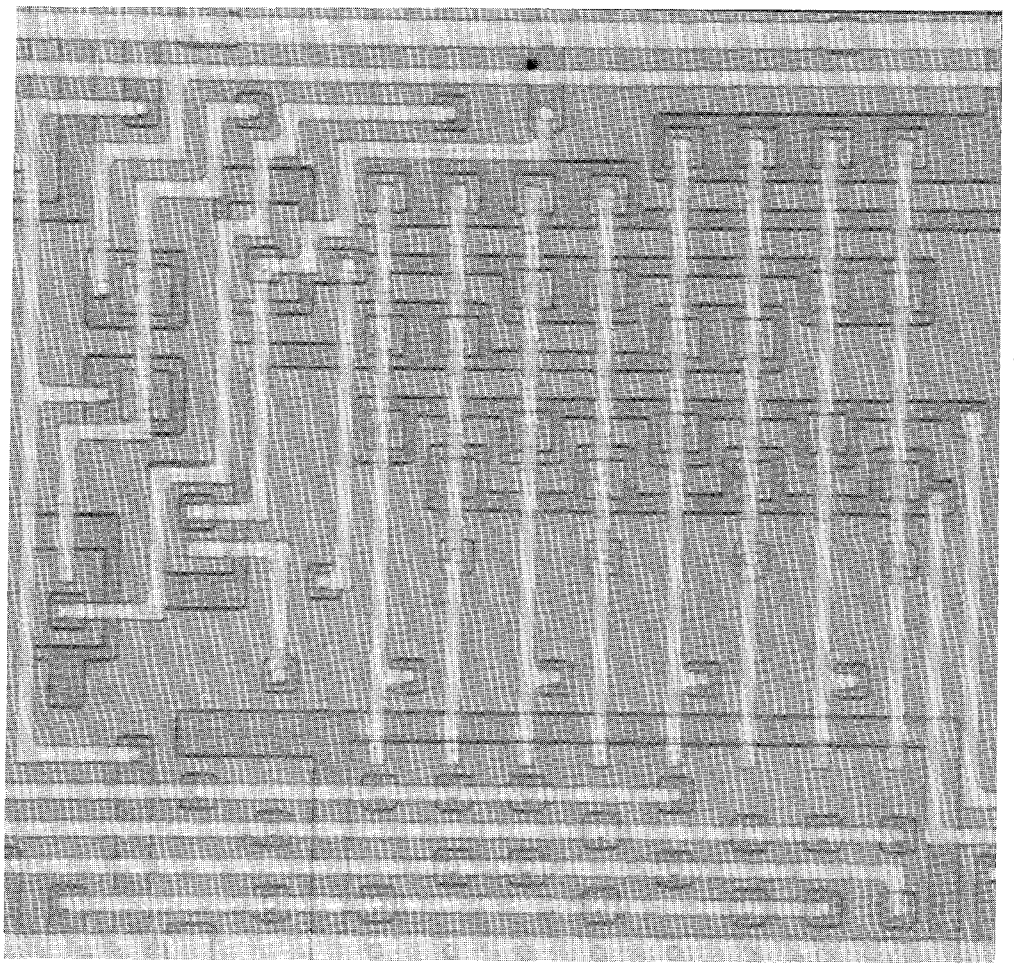
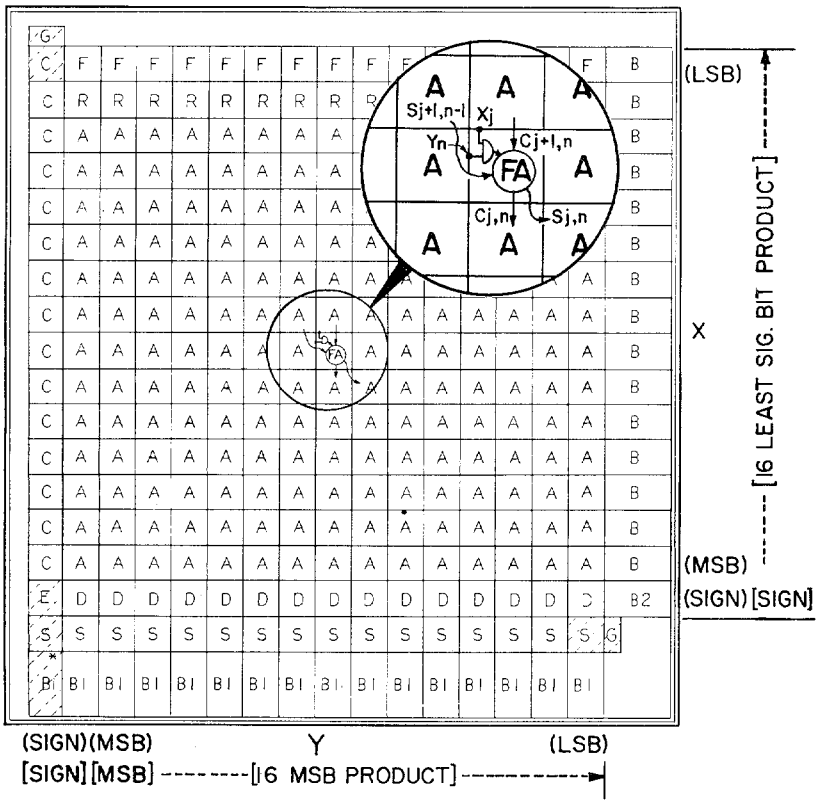


FIGURE 2—Photograph of most commonly repeated cell on a completed chip.



[Left]

FIGURE 3—Block layout showing how individual cells are assembled to make a multiplier.

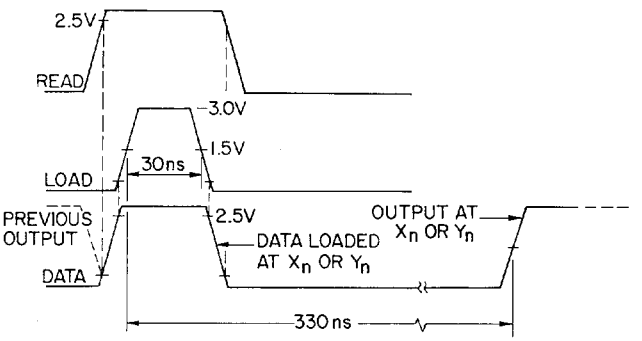


FIGURE 5—Timing illustration showing the relationship between READ, LOAD and DATA signals.