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TECHNOLOGIES

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Digital Signal Processing on the Industry-Standard MIPS® Architecture

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Fall Processor Forum, 2004

Introducing the MIPS® DSP ASE

➔ **DSP extension** to the MIPS32® and MIPS64® architectures in the integer pipeline
  ➔ Integrates functionality

➔ New Instructions and architectural state
  ➔ Performance improvement for many applications
  ➔ < 6% additional die area

➔ Full development support

Enhancing the MIPS® Architecture with a DSP Extension for Lower System Costs

Agenda

→ MIPS® Markets
  → DSP Application Example

→ Market Drivers for Signal Processing

→ DSP ASE Details
  → Performance Benefits
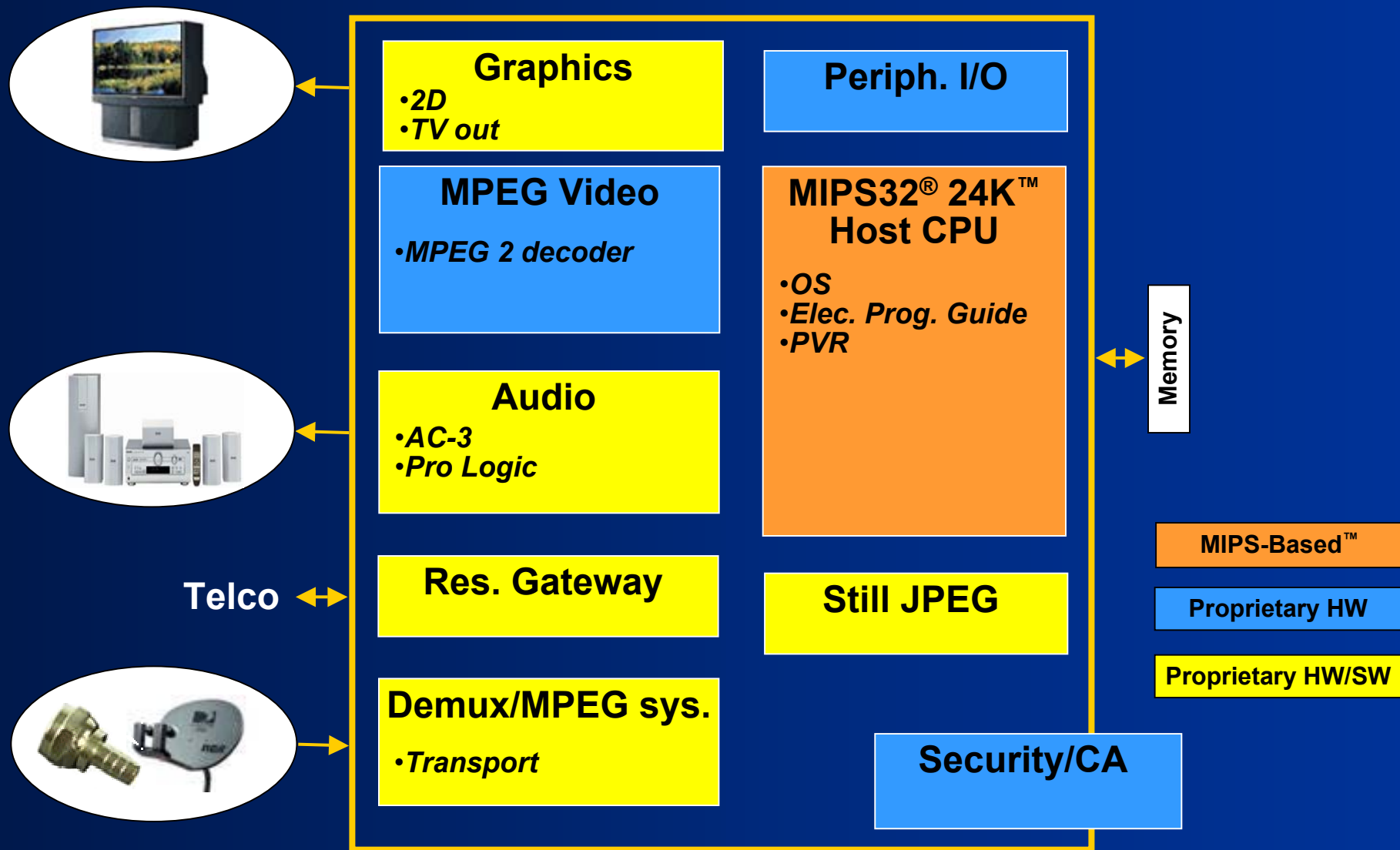 → Tools and Infrastructure Support

→ Summary

MIPS® Market Leadership

- ➜ Internet Backbone 40%

- ➜ DVD Recorders 75%

- ➜ IDTVs 40%

- ➜ DSL Modems 40%

- ➜ Digital STBs   40%
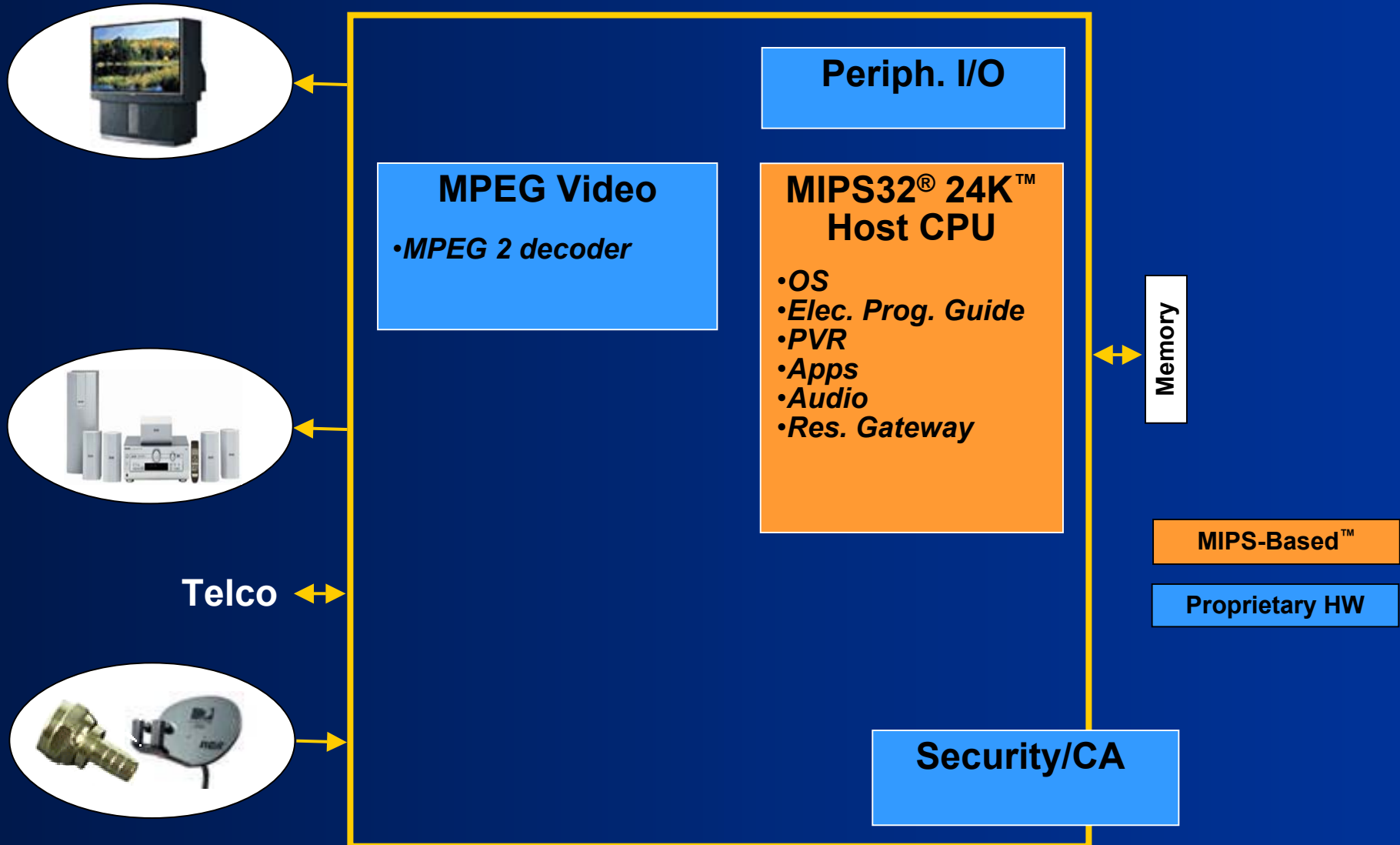 - ➜ Cable STBs   76%

- ➜ Office Automation 48%

Sources: IDC, Semico, In-Stat, Iconocast and MIPS Technologies.
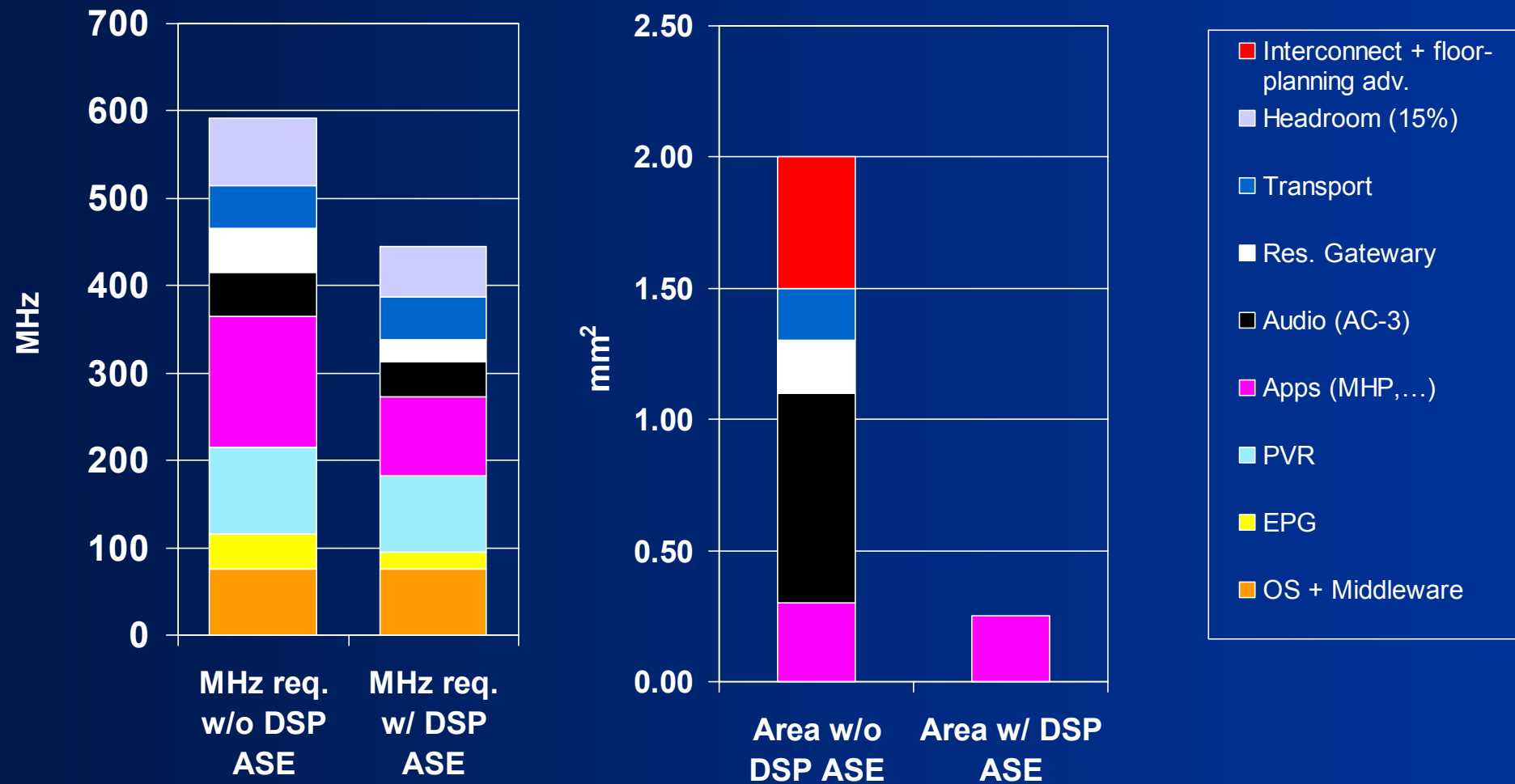*Values are percentage of W.W. box shipments.*

Advanced Set-Top Box SOC

Graphics
- *2D*
- *TV out*

Periph. I/O

MPEG Video
- *MPEG 2 decoder*

MIPS32® 24K™ Host CPU
- *OS*
- *Elec. Prog. Guide*
- *PVR*

Audio
- *AC-3*
- *Pro Logic*

Memory

Telco

Res. Gateway

Still JPEG

Demux/MPEG sys.
- *Transport*

Security/CA

MIPS-Based™

Proprietary HW

Proprietary HW/SW

Advanced Set-Top Box SOC

Periph. I/O

MPEG Video

•*MPEG 2 decoder*

MIPS32® 24K™ Host CPU

•*OS*
•*Elec. Prog. Guide*
•*PVR*
•*Apps*
•*Audio*
•*Res. Gateway*

Memory

MIPS-Based™

Proprietary HW

Telco

Security/CA

STB SOC Benefits with MIPS® DSP ASE

DSP Algorithms Need Less MHz and Area

Market Drivers For Signal Processing

Consumer Market Drivers

➜ Lower system costs

➜ Integrated DSP functions in the host yield smaller SOCs and **cost-effective systems**

➜ Single tool chain for signal processing and host

➜ MIPS ecosystem

➜ Feature creep and evolving standards

➜ **Programmability** allows easy adaptation to changing standards

➜ Synthesizable **performance** leader

➜ Increase product lifespan

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Applicability of the MIPS® DSP ASE

	Still JPEG Printer Imaging	**8-Bit Data**
	Voice Codecs, etc MP3, MPEG-2 Audio ... V.90 .... Other General DSP	**16-Bit Data**
	AC-3, MPEG-2 AAC ... Communication	**32-Bit Data**

MIPS® DSP ASE Details

What is the MIPS® DSP ASE?

Typical DSP-Like Instructions

- SIMD (8/16/32)
- Saturating fractional math
- MAC/dot-product
- Expand/reduce
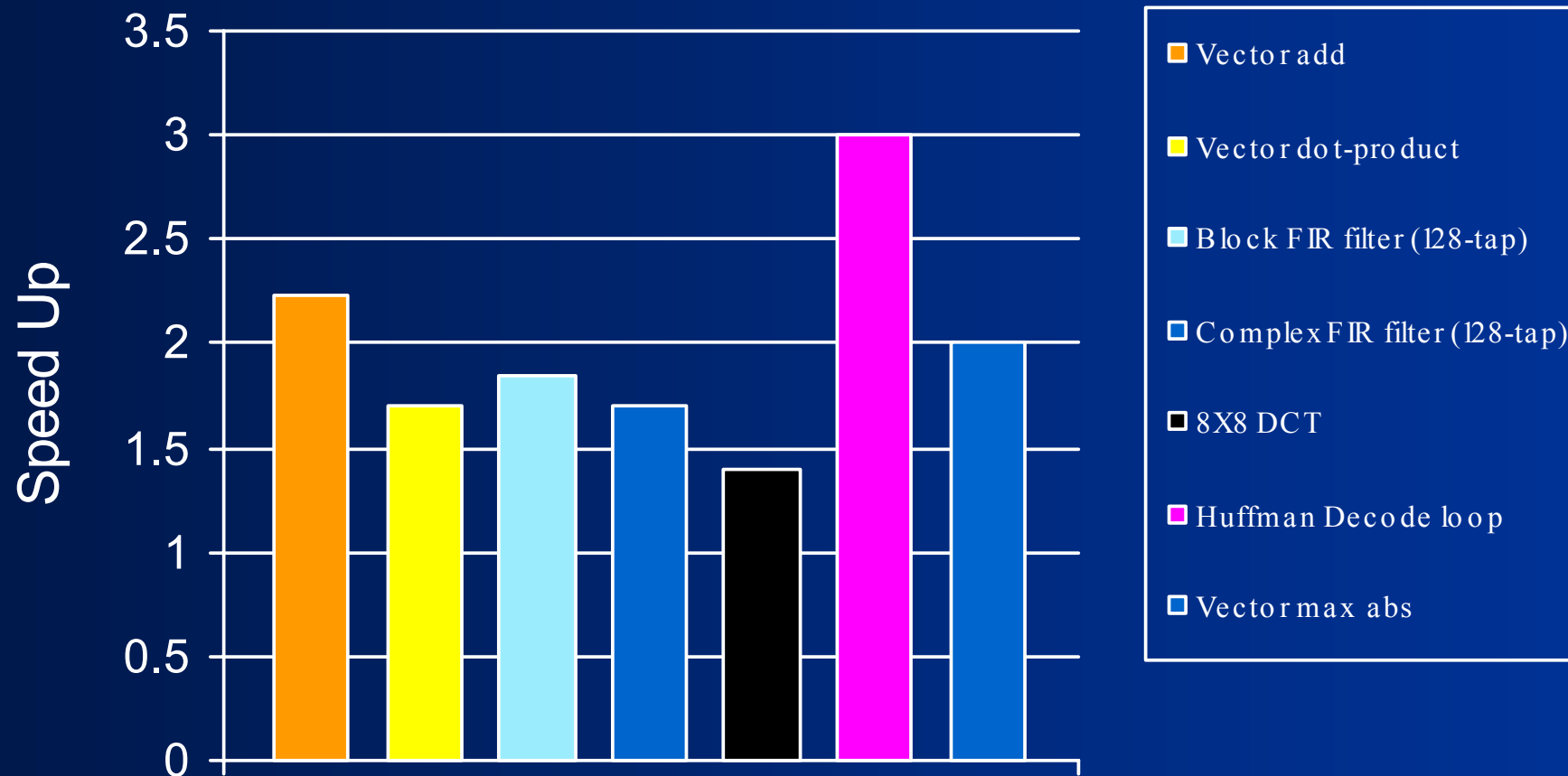- Absolute
- Bit-reverse
- Etc

Key Features

- Complex multiply support
- Variable bit insert
- Variable bit extract
- Virtual circular buffers
- Etc

New State

- Accumulators
- DSP Control

DSP Algorithm Speedup

Speed Up

3.5
3
2.5
2
1.5
1
0.5
0

Legend:
- ■ Vector add
- ■ Vector dot-product
- ■ Block FIR filter (128-tap)
- ■ Complex FIR filter (128-tap)
- ■ 8X8 DCT
- ■ Huffman Decode loop
- ■ Vector max abs

**Speedup Compared to Hand-Optimized MIPS32®
Assembly Implementation on a 24K™ Core**

MIPS® DSP ASE Key Feature Example

Example – Efficient Bit Extraction

➔ Many embedded applications use streaming input data
  ➔ Video, audio, communication packets, etc.

➔ The issue with formatted streaming data
  ➔ **Variability** in the field widths of packet headers
  ➔ Extract operation needs a different **shift and mask value** per width – inherently inefficient

MIPS® DSP ASE Makes the Variable Bit Extraction Process Very Efficient

Efficiency of Variable Bit Extraction

Variable Bit Extract Using the DSP ASE

Size
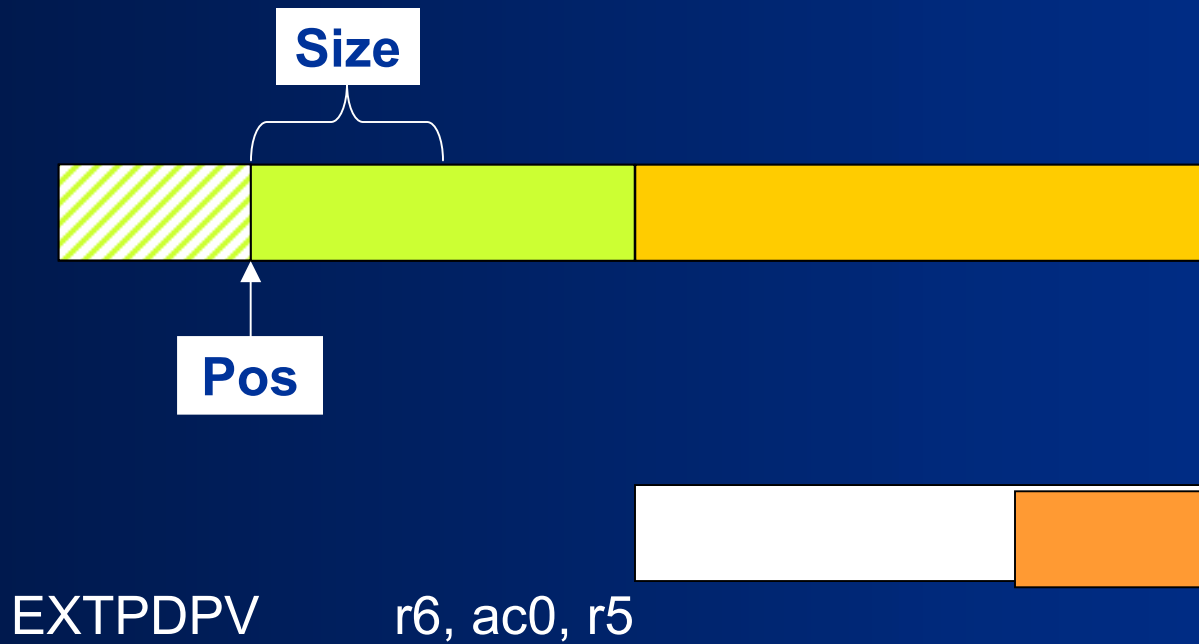

Pos
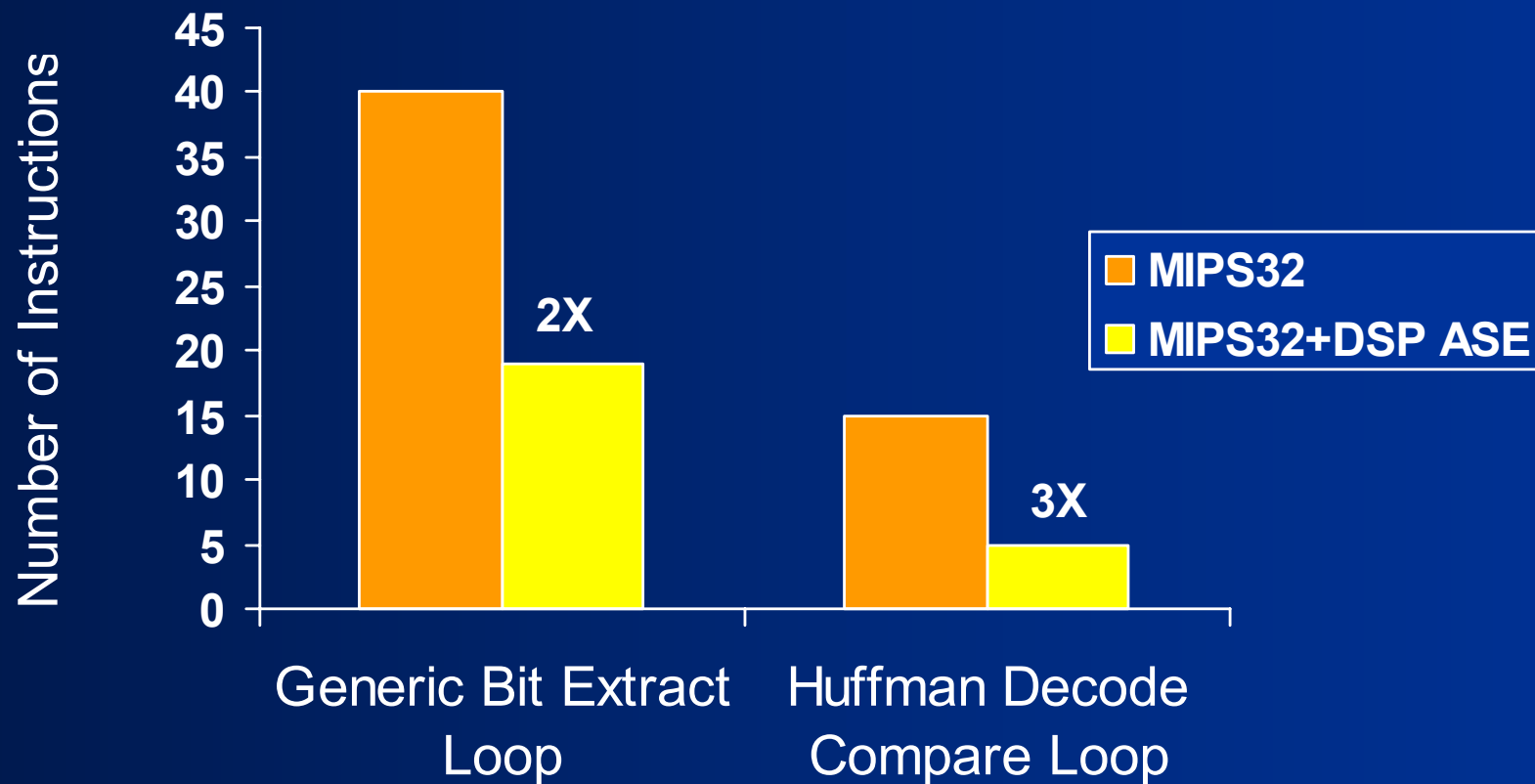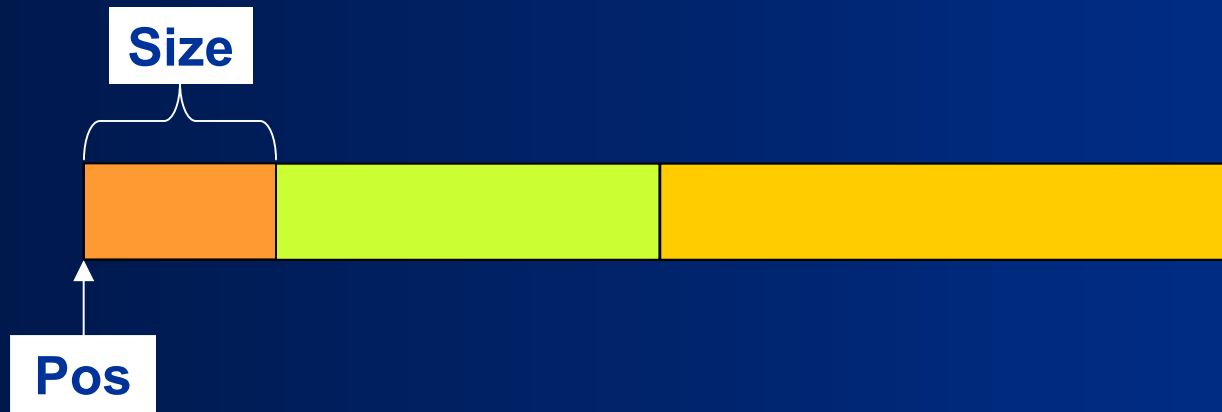
```
LW      r10, 0(r9)

LW      r11, 4(r9)

MTHI    r10,ac0

MTLO    r11,ac0

LI      r5, size
```

Variable Bit Extract Using the DSP ASE

Size

Pos

EXTPDPV   r6, ac0, r5

Variable Bit Extract Using the DSP ASE

Size

Pos
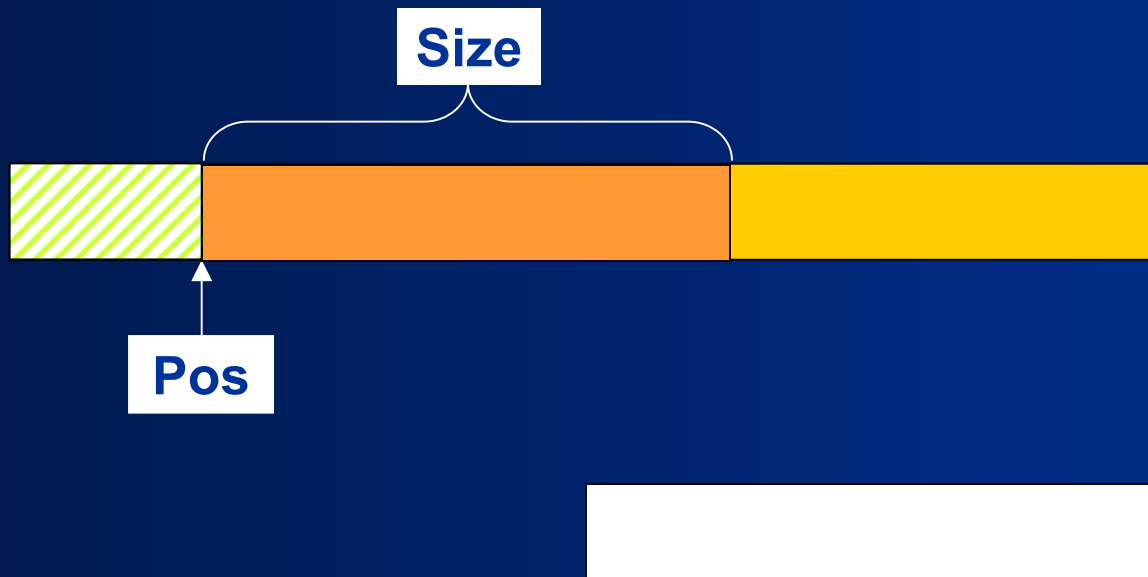
Recalculate size

LI   r5, size

Variable Bit Extract Using the DSP ASE

Size

Pos

EXTPDPV   r6, ac0, r5

Variable Bit Extract Using the DSP ASE

Size

Pos
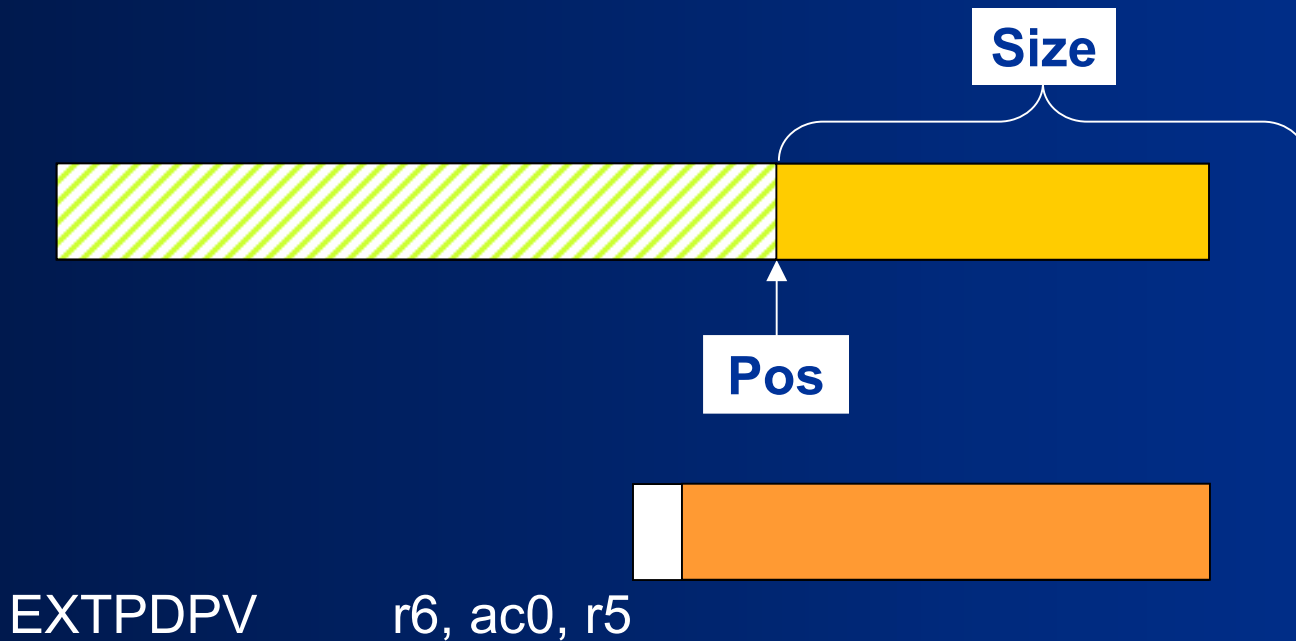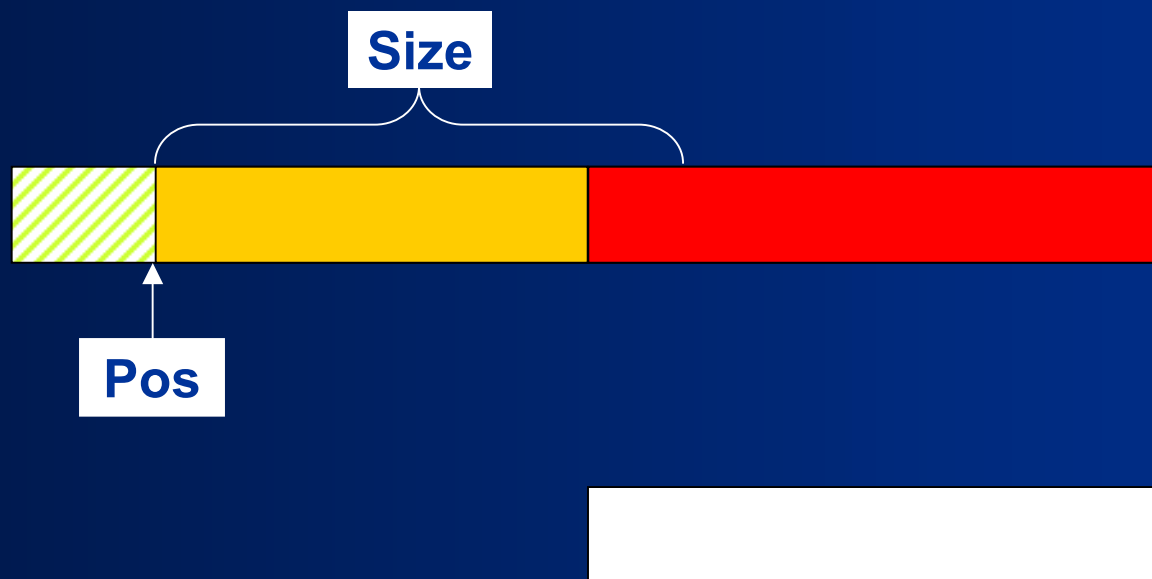
Respond to underflow

CLTHIP   ac0

LW   r10, 8(9)

MTLO   r10,ac0

MIPS® DSP ASE Software Support

MIPS Linux
•Support new context

Application Layer
•Audio, VoIP

MIPS DSP Library
•Common DSP routines tuned for DSP ASE

MIPS Toolkit
•Compiler, Assembler, Debuggers, etc
•Simulator
•Performance analysis

MIPS DSP ASE

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