A Self-Testing 2-μm CMOS Chip Set for FFT Applications

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Abstract — **A chip set for high-speed radix-2 FFT applications up to 512 points is described. The chip set comprises a $(16+16)\times(12+12)$-bit complex number multiplier, and a 16-bit butterfly chip for data reordering, twiddle factor generation, and butterfly arithmetic. The chips have been implemented using a standard cell design methodology on a 2-μm bulk CMOS process. Three chips implement a complex FFT butterfly with a throughput of 10 MHz, and are cascadable up to 512 points. The chips feature an off-line self-testing capability.**

I. Introduction

THE performance and level of integration offered by modern VLSI CMOS processes has enabled digital processing techniques to make a significant impact on system design and performance. This is particularly so in sonar, avionics, radar, and telecommunications systems. In military applications there has been a gradual replacement of analog components by digital alternatives offering improved performance, resolution, and stability. To this end there is now a range of general-purpose digital signal processing devices becoming available.

However, the available complexity of VLSI has made such devices increasingly difficult to test, particularly system *in-situ* testing. There are numerous techniques for enhancing the testability of VLSI devices. For both production and *in-situ* testing, however, the use of signature analysis techniques is becoming increasingly attractive. The chip set described in this paper provides an efficient solution to FFT hardware implementations and attempts to solve the associated testing problems.

II. Chip Set Architecture

A. Background

A number of approaches for the hardware implementation of FFT's are available [1]. To achieve a given throughput differing degrees of parallelism, pipelining, and radices may be employed. It is well known that higher radix FFT structures, such as radix-4 and radix-8, result in a lower number of multipliers, etc., but at the expense of greater control hardware complexity. Control hardware for radix-4 implementations has previously been described [2]. The chip set described in this paper allows radix-2 transform sizes up to 512 points to be efficiently implemented by a simple cascade of devices. To achieve continuous data throughputs of up to 10 MHz we have chosen a pipelined FFT structure, shown in Fig. 1. In the future, 1.5- or 1-μm feature size VLSI technologies are likely to offer single-chip complexities at which high radix transforms will be optimal.

The chip set is aimed at high-performance Fourier transform applications, implementing a decimation in frequency in-place algorithm. The chip set has been partitioned for devices that exhibit maximum flexibility. The chip set includes all the control and twiddle factor memory normally associated with the FFT structure. The chips are designed using a standard cell library containing both simple gates and larger parameterized cells such as RAM, ROM, and PLA (see Section VI).

B. Complex Number Multiplier

The complex number multiplier *CMULT* will multiply a complex $(16+16)$-bit data word by a complex $(12+12)$ complex coefficient and return a complex $(17+17)$-bit rounded product. By consideration of common transform and word-size lengths, it was found that the coefficients could be reduced to 12-bit complex, thereby minimizing chip area without degrading the system performance. Transforms were performed on various input waveforms (e.g., chirp waveforms) using ELLA [3] to investigate the properties of the architecture.

The input data format is fractional two's complement. The input number range is $-1.0 \leqslant x < 1.0$, while the product number range is $-2.0 \leqslant p < 2.0$. The *CMULT* consists of four identical 16×12 real multipliers, based on the Booths 2 bits at a time algorithm, and is pipelined to achieve a 10-MHz throughput. The multiplier pipeline unit comprises a three-row by six-column array of full adders, yielding a total latency of eight clock cycles. The multiplier cell is constructed from basic standard cell library components, as shown in Fig. 2. The four real/imaginary parts of the products are summed in two pipelined 16-bit adders.

The complete chip layout is shown in Fig. 3. The chip complexity is approximately 10 800 gates. The chip size is 268×289 mil and the device is packaged in a 120-lead pin grid array.

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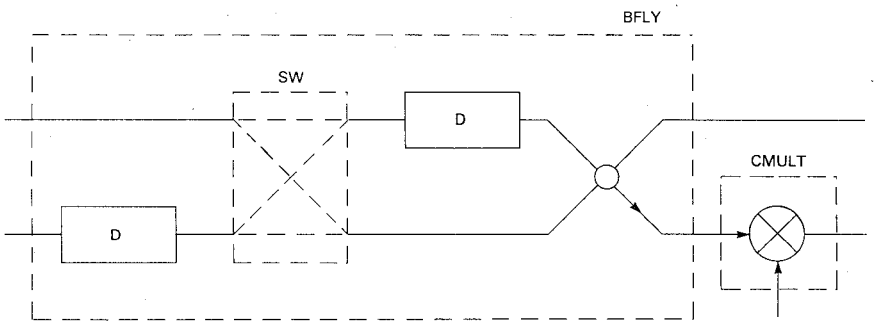

Fig. 1. General structure of a pipeline FFT indicating basic chip set partition.

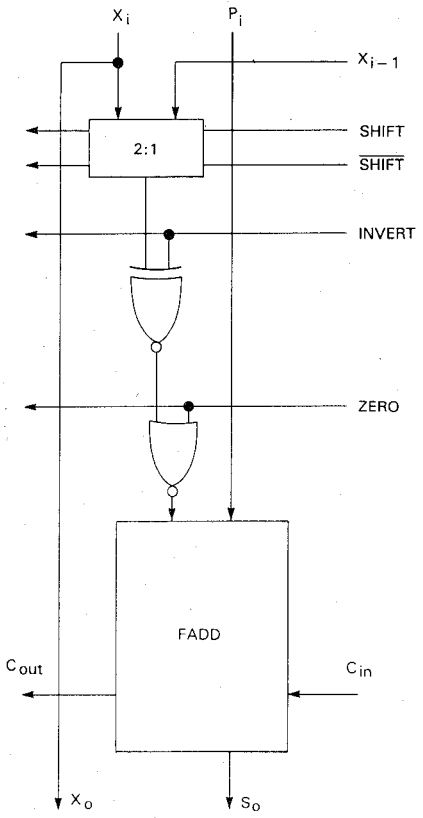

Fig. 2. Basic multiplier cell.

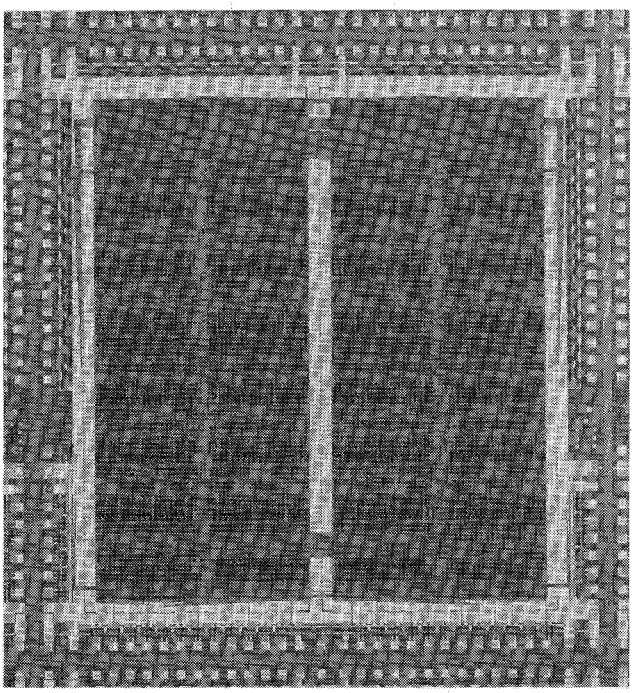

Fig. 3. *CMULT* chip microphotograph.

C. FFT Butterfly

The butterfly chip *BFLY*, shown in Fig. 4, provides the data reordering and add/subtract function for one channel of one rank of the pipelined FFT. In addition, the chip contains a 512×12-bit ROM to store the complex coefficients for transforms up to 512 points. The real and imaginary parts of the coefficient are stored as alternate words. Chip controls select whether the device lies in the real or the imaginary channel. A single RAM structure was chosen to implement the two pipeline delays required by the pipelined FFT. A RAM cell was chosen over a shift register structure because it provides a more efficient solution, being approximately 60 percent smaller and consuming 75 percent less power than a static shift register approach. A dynamic shift register would reduce the area but the 16-bit-wide programmable taps remain expensive in terms of routing area. Internally the RAM is constructed as 64 words of 64 bits to maximize throughput. The RAM and ROM are addressed by counters, whose count length and increment are set by the FFT rank position control pins.

The input data format is 16 bits real only. As the add/subtract function of the butterfly can return a 17-bit result, a "scale" control function has been added to select either the lower or upper 16 bits of the result. This control allows for signal growth within the FFT. For controlled operation of the FFT, the *BFLY* chip adder/subtractors hard limit under overflow conditions, thereby maintaining degraded but correct FFT transform operation.

The *BFLY* chip layout is shown in Fig. 5. The chip contains a total of 5500 gates, 4 kbits of RAM, 6 kbits of ROM, plus a 64-word by 9-bit test control NAND PLA. The majority of the data path is implemented as three auto-routed parameterized gate arrays, while the control is implemented mainly as standard cells. The chip size is 263×317 mil, and the device is packaged in a 120-lead pin grid array.

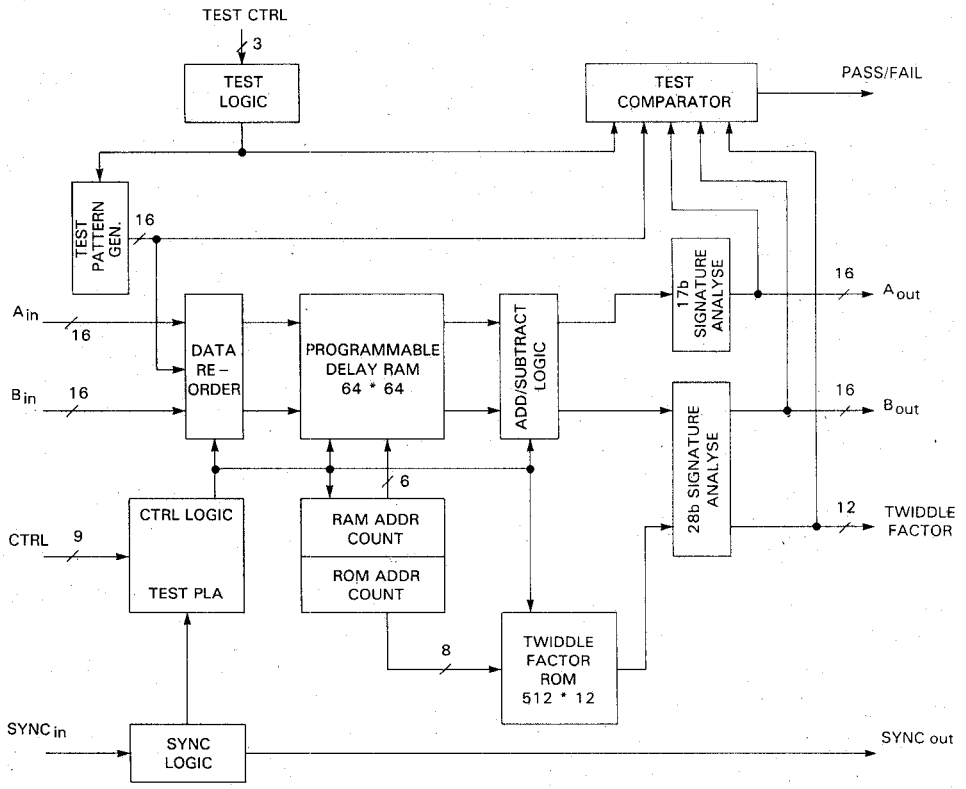

Fig. 4. *BFLY* chip architecture.

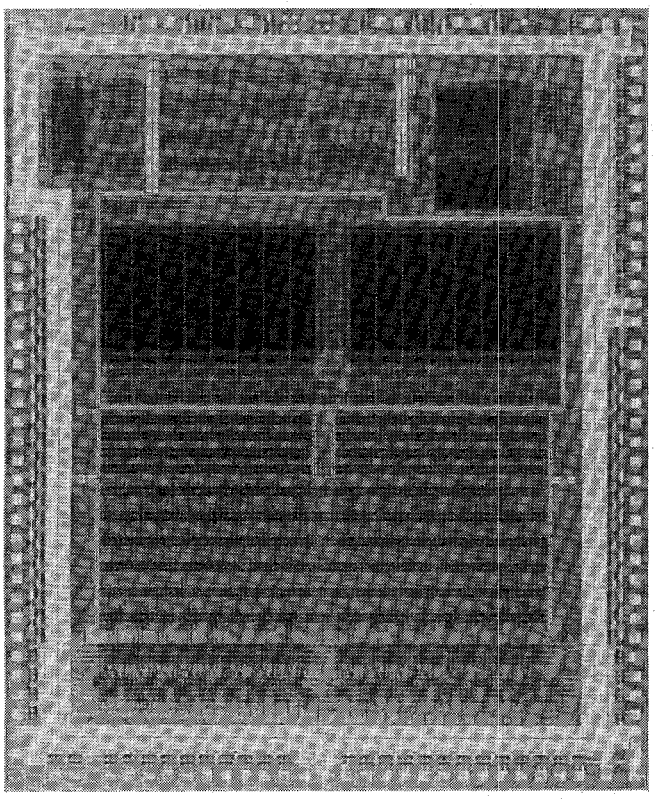

Fig. 5. *BFLY* chip microphotograph.

III. FFT Implementation

To implement an FFT butterfly, three chips are required, one *CMULT* and two *BFLY*'s, as shown in Fig. 6. To assemble an FFT structure, butterfly stages are cascaded. Each stage doubles the transform length and so the limit of nine stages (27 chips) corresponds to 512-point transforms. Four control pins on the *BFLY* chip select the rank position and hence the appropriate pipeline delay and twiddle factor sequence. A fifth pin sets either forward or inverse transforms, while another determines the real or imaginary channel. To compensate for the pipeline delay of the *CMULT*, the *BFLY* includes an eight-stage delay in the upper channel.

The chip set requires only one data control signal SYNC. A negative edge of the SYNC control activates the transform. At the beginning of a transform there will be unknown data contained in the pipeline delay RAM's. So for a 512-point transform, the first 256 values output from the RAM in the first rank are set to zero. The chip set continues processing until the SYNC control returns high. When SYNC goes high zero data is forced on the zero delay channel of the *BFLY* chips in the first FFT rank. The transformer therefore completes a valid transform. This sequence, however, results in a minimum delay of 256 clock cycles (SYNC high) between transforms. Fig. 7 illustrates how valid input data are defined by SYNC_{in} low and valid output by SYNC_{out} low. Data blocks $A, B, C, \cdots$ are up to 256 words in length, depending on transform length, and are used in pairs to perform 50-percent overlapping transforms. The transform result blocks are labeled $1, 2, 3, \cdots$.

IV. Performance

The latency of a 512-point (nine-rank) pipeline FFT, implemented using these chips, is 390 clock cycles. When performing a single 512-point transform, the delay be-

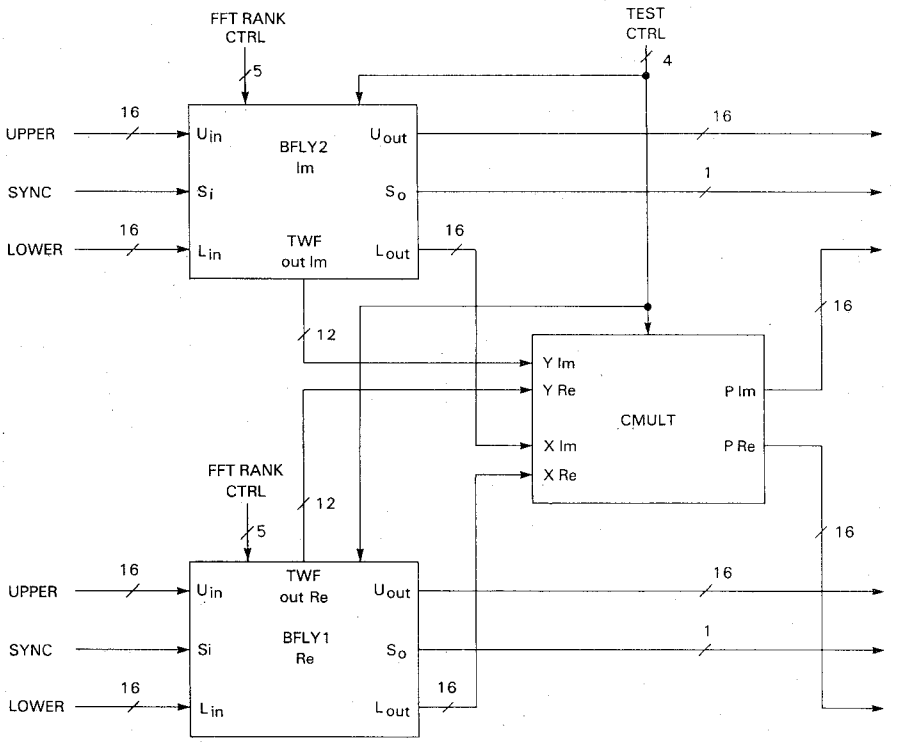

Fig. 6. Chip set implementing a complex FFT butterfly.

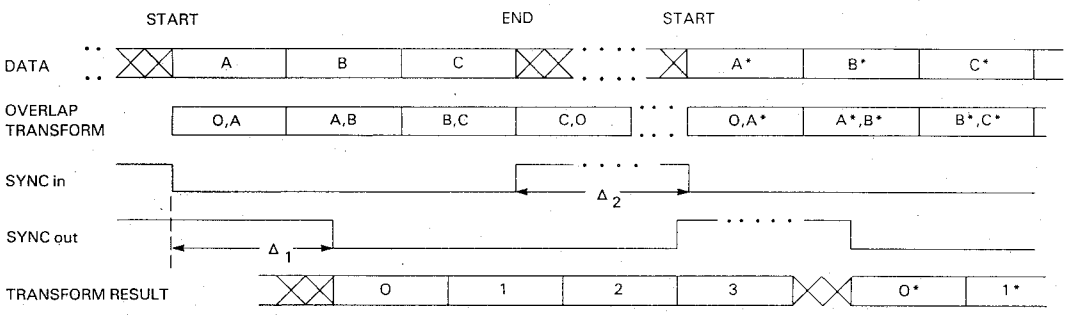

Fig. 7. FFT chip set timing; 50-percent overlap transform.

tween the first data word in and last data word out is 902 clock cycles. At a clock rate of 10 MHz these values correspond to 39.0 and 90.2 μs. When running continuously, the transform rate is equivalent to 512 clock cycles, i.e., a 512-point transform in 51.2 μs. In comparison, this is several hundred times faster than DSP processors such as the TMS320 (Texas Instruments) or uPD7720 (NEC), and several thousand times faster than general-purpose microprocessors such as the 68000 or 8086 (Motorola). Although silicon area has been used to increase throughput and word size compared with other possible implementations [4], the set is based on only two chips; interchip connection is regular and operation of the set very simple.

V. Self-Test Philosophy and Signature Prediction

Both the *CMULT* and the *BFLY* chips feature a self-test capability. A single output pin on each device indicates pass or fail at the end of test. The self-test is based on local pseudorandom pattern generation and signature analysis. Due to the modular construction of an FFT butterfly with this chip set a number of test modes are possible. Three control pins on each device set the test mode.

On each device both the data inputs and outputs are latched. During test mode these data latches may be configured to act as either pattern generators or signature analyzers. Hence, in the case of a *BFLY*, for example, test patterns may be sourced from either its own input registers or from the output registers of a *CMULT* and *BFLY*. This enables full chip-to-chip interconnect test. Similarly, the *CMULT* signature may be accumulated from a pair of *BFLY* chips.

In the *CMULT* the x and y input latches are configured into a 28-bit pattern generator. The output latches accumulate a 17-bit signature. At 10 MHz the time for an exhaustive test sequence is 26 s. In the case of the *BFLY*, 17-bit pseudorandom patterns are required. An on-chip test control PLA cycles the *BFLY* through each of the possible operating modes, i.e., each rank position, inverse and forward transform, and real and imaginary channels.

One-hundred-percent stuck-at fault detection in the RAM is achieved using 16 RAM address cycles with pseudorandom data. At 10 MHz a test time of 13.1 ms is achieved.

An on-chip comparator compares the accumulated signature with a predicted signature which is coded on-chip in second-layer metal. The test signatures have been computed using Fortran modeling of the chips. This approach was necessary due to the excessively long simulation times that would have resulted using a logic simulator, 15 CPU years (!) and 140 CPU hours on a VAX 11/780 for the *CMULT* and *BFLY*, respectively. The Fortran-models required simulation times of 6.5 CPU hours and 11 CPU minutes, respectively.

VI. Design Methodology

The chip set has been designed using a standard cell design methodology [5]. High-level system and chip design was performed using a hardware description language [3]. The use of abstract data and multivalued types within the hardware description allowed the chip set functions, global timing, and word-size performance to be determined at the earliest possible time.

The standard cell system features a library of predesigned and precharacterized elements [5]. The library contains a number of the basic logical functions, NAND, NOR, full adder, etc. However, to support complex VLSI system design the library contains a number of parameterized cells such as RAM, ROM, PLA, etc. This approach enables the chip designer to specify the exact size required for the design, i.e., number of addresses and word size. The cell is then assembled automatically by assembly software to produce the desired instance of the cell. The assembly software also provides layout information such as size and interconnect points. The *BFLY* chip makes use of the parameterized cells comprising a RAM (64×64 bits), a ROM (512×12 bits), and a PLA (six inputs, nine outputs, and 64 product terms).

The chip layout is carried out by placing and interconnecting cells. As the cells are precharacterized only their interconnection constitutes a design risk. This is minimized by software checking the final layout to produce net-list information, plus track parasitic capacitance information for resimulation purposes.

VII. 2-μM CMOS Technology

The standard cell library is implemented on a 2-μm bulk CMOS process. The process is epitaxy based giving a high immunity to latch-up without constraining the chip layout. Two levels of metallization are available for interconnect. The process is capable of producing simple gate delays in the 1–2 nS region (typical, 25°C). Circuits comprising simple gates only may be operated at clock rates up to 40 MHz, while designs containing parameterized cells are restricted by their access times to approximately 10 MHz.

VIII. Summary

A self-testing chip set for the implementation of complex radix-2 decimation in frequency FFT's up to 512 points at data rates up to 10 MHz has been described. Three chips, one complex multiplier and two butterflies, implement a 16-bit data complex FFT butterfly. The chips have been designed using a standard cell design methodology featuring parameterized cells, on a 2-μm bulk CMOS technology.

Acknowledgment

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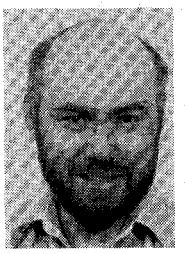

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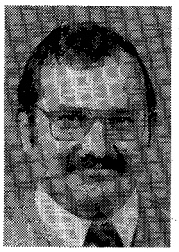

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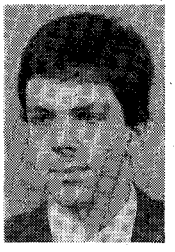

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