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Differences Between the DSP56300 and MSC8101 Enhanced Filter Coprocessors (EFCOPs)

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The Enhanced Filter Coprocessor (EFCOP) is a general-purpose, fully programmable filter that operates concurrently with the DSP core, with minimal CPU intervention. Motorola introduced the EFCOP into the DSP56300 family of DSPs, specifically into the DSP56307 and the DSP56311. Now, Motorola has ported an updated and enhanced EFCOP to the next generation of DSPs based on the StarCore SC140 core, beginning with the MSC8101. This document describes the programming differences between the DSP56300 EFCOP and the MSC8101 EFCOP. These differences include the data resolution, the initialization, input/output, request sources, memory structure, and control registers.

For details on EFCOP architecture and functionality, consult the following manuals and application notes:

- Chapter 10, Enhanced Filter Coprocessor, *DSP56307 User's Manual* (DSP56307UM/D)
- Chapter 10, Enhanced Filter Coprocessor, *DSP56311 User's Manual* (DSP56311UM/D)
- Chapter 10, Enhanced Filter Coprocessor, DSP56L307 User's Manual (DSP56L307UM/D)
- *Programming the DSP56307 Enhanced Filter Coprocessor (EFCOP)* (APR39/D)
- Chapter 18, Enhanced Filter Coprocessor, *MSC8101 Reference Manual* (MSC8101RM/D)
- Chapter 9, Programming the EFCOP, *MSC8101 User's Guide* (MSC8101UG/D)

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1 Resolution

The most basic difference between the DSP56300 EFCOP and the MSC8101 EFCOP is the data resolution, as summarized in **Table 1**.

Table 1. Data Resolution Differences Between the DSP56300 and MSC8101 EFCOPs

	Input/Output Register Width	FMAC Multiplication for Intermediate Results During Filter Calculations	Accumulator
DSP56300 EFCOP	24 bits	56 bits	56 bits
MSC8101 EFCOP	32 bits	32 bit × 32 bit	72 bits

2 Initialization

Another significant difference between the two EFCOPs is the MSC8101 coefficient initialization mode to initialize the coefficient buffer before processing begins. This mode is selected via the FCTL[FCIM] bit:

- If FCIM is clear, coefficient initialization mode is disabled and processing completes exactly as in the DSP56300 EFCOP.
- If FCIM is set, the coefficients are initialized by a coefficient update session with the original coefficients equal to zero. The data buffer is initialized first, either by the SC140 core or the EFCOP with data initialization. Then the update parameter is written to FKIR, and the EFCOP initializes the coefficient buffer by multiplying each sample in the data buffer by the update parameter and placing the result in the coefficient buffer.

If data and coefficient initialization are both enabled on the MSC8101, data initialization completes first, but the EFCOP does not begin processing the first result. After FKIR is written, the EFCOP initializes the coefficients and another input sample is written to FDIR to begin processing. Coefficient initialization is usually used in adaptive mode or is used to clear the coefficients by writing zero to FKIR.

Example 1 shows how the EFCOP can be programmed with data and coefficient initialization enabled. This example uses equate labels for the location of the EFCOP registers and assumes that these equates are declared before the example code. These labels include the register name preceded with "M_". An address register pointer is initialized for the filter input data (INPUT), and the EFCOP control parameters are written to the appropriate memory-mapped control registers. A value of 0x0101 is written to the control register to enable the EFCOP with data and coefficient initialization enabled. The FDM buffer is initialized by writing FCNT number of samples to the FDM through the FDIR. The code uses a short loop to write the first FCNT input samples to the FDIR using a **move.l** instruction. After the FKIR value is written to the K-constant input register, the EFCOP automatically initializes the FCM buffer. Processing begins with the write of the first input data sample to the FDIR.

Example 1. Coefficient Initialization Example

```
move.w #INPUT,r0                        ;Init data pointer
move.w #0,d0                            ;Init FDBA
move.w d0,M_FDBA
move.w #0,d0                            ;Init FCBA
move.w d0,M_FCBA
move.w #FCNT-1,d0                       ;Init FCNT
move.w d0,M_FCNT
```

```
move.w #$0101,d0                                ;Init FCTL
move.w d0,M_FCTL
doensh0 #FCNT
loopstart0                                      ;Init data taps
move.l (r0)+,d0
move.l d0,M_FDIR
loopend0

move.l #FKIR,d0                                 ;Init coeffs
move.l d0,M_FKIR

move.l (r0)+,d0                                 ;Write first input
move.l d0,M_FDIR
```

3 Input/Output

The EFCOP input and output registers for the DSP56300 and the MSC8101 have different sizes and different flags that determine when the registers are available for reading or writing (see **Table 2**).

Table 2. FDIR/FDOR DIfferences

Register	DSP56300		MSC8101	
	Size (24-bit words)	Flags	Size (32-bit words)	Flags
FDIR	4 words deep	FCSR[FDIBE], Input Buffer Empty	8 words deep	FSTR[FDIBE], Input Buffer Empty
				FSTR[FIBNF], Input Buffer Not Full
FDOR	1 word deep	FCSR[FDOBF], Output Buffer Full	8 words deep	FSTR[FDOBF], Output Buffer Full
				FSTR[FOBNE], Output Buffer Not Empty

3.1 FDIR

The DSP56300 FDIR is a 4-word deep FIFO that is 24 bits wide. Up to four data samples are written to the DSP56300 FDIR at the same address. The EFCOP sets one flag, FCSR[FDIBE], when all four slots of the FDIR are empty. The DSP56300 FDIR is written only when this bit is set. The MSC8101 FDIR is an 8-word deep FIFO that is 32 bits wide. Up to eight data samples can be written to the MSC8101 FDIR at the same address. The EFCOP sets two flags, FSTR[FDIBE and FIBNF], when the FDIR is empty or not full, respectively. The MSC8101 FDIR is written only when either of these bits is set.

3.2 FDOR

The DSP56300 FDOR is a read-only register that is 24 bits wide. Only one data sample is read from the DSP56300 FDOR at the same address. The EFCOP sets one flag, FCSR[FDOBF], when FDOR is full. The DSP56300 FDOR is read-only when this bit is set. The MSC8101 FDOR is an 8-word deep FIFO that is 32 bits wide. Up to eight data samples are read from the MSC8101 FDOR at the same address. The EFCOP sets two flags, FSTR[FDOBF and FOBNE], when the FDOR is full or not empty, respectively. The MSC8101 FDOR is read-only when either of these bits is set.

4 Requests

This section discusses the differences between the DSP56300 and MSC8101 EFCOP request sources. The EFCOP can request service to write the FDIR or read the FDOR using an interrupt or the DMA controller. An interrupt or DMA transfer is triggered by any of the input/output flags shown in **Table 2**. The differences in these flags result in the differences in the request sources between the DSP56300 and the MSC8101. The MSC8101 has an extra flag, FSTR[FUDN], that indicates when a coefficient update session has completed. This flag can trigger an interrupt in the MSC8101. **Table 3** summarizes the DMA and interrupt request differences.

Table 3. Request Differences

Request	DSP56300		MSC8101		
	Flag	Interrupt	Flag	Interrupt	DMA
Input Buffer Empty	FCSR[FDIBE]	FCSR[FDIIE]	FSTR[FDIBE]	FCTL[FIEIE]	FCTL[FDIM] = 1
Input Buffer Not Full	—	—	FSTR[FIBNF]	FCTL[FINFIE]	FCTL[FDIM] = 0
Output Buffer Full	FCSR[FDOBF]	FCSR[FDOIE]	FSTR[FDOBF]	FCTL[FOFIE]	FCTL[FDOM] = 1
Output Buffer Not Empty	—	—	FSTR[FOBNE]	FCTL[FONEIE]	FCTL[FDOM] = 0
Coefficient Update Done	—	—	FSTR[FUDN]	FCTL[FUDIE]	—

4.1 Interrupts

The DSP56300 EFCOP has only two input/output flags, so it has only two interrupt request sources:

- *Input buffer empty interrupt*. Enabled by setting FCSR[FDIIE] and triggered when FCSR[FDIBE] and FCSR[FDIIE] are both set. The service routine is located at VBA + 0x68. This interrupt can be used to write up to four input samples to FDIR.
- *Output buffer full interrupt*. Enabled by setting FCSR[FDOIE] and triggered when FCSR[FDOBF] and FCSR[FDOIE] are both set. The service routine is located at VBA + 0x6A. This interrupt can be used to read one output sample from the FDOR.

The MSC8101 EFCOP has five interrupt sources, four input/output flags, and one coefficient update done flag:

- *Input buffer empty interrupt*. Enabled by setting FCTL[FIEIE] and triggered when FSTR[FDIBE] and FCTL[FIEIE] are both set. The service routine is located at VBA + 0x800. This interrupt can be used to write up to eight input samples to FDIR.
- *Input buffer not full interrupt*. Enabled by setting FCTL[FINFIE] and triggered when FSTR[FIBNF] and FCTL[FINFIE] are both set. The service routine is located at VBA + 0x840. This interrupt can be used to write only one input sample to FDIR.
- *Output buffer full interrupt*. Enabled by setting FCTL[FOFIE] and triggered when FSTR[FDOBF] and FCTL[FOFIE] are both set. The service routine is located at VBA + 0x880. This interrupt can be used to read up to eight output samples from the FDOR.

- *Output buffer not empty interrupt*. Enabled by setting FCTL[FONEIE] and triggered when FSTR[FOBNE] and FCTL[FONEIE] are both set. The service routine is located at VBA + 0x8C0. This interrupt can be used to read one output sample from the FDOR.
- *Coefficient interrupt done interrupt*. Enabled by setting FCTL[FUDIE] and triggered when FSTR[FUDN] and FCTL[FUDIE] are both set. The service routine is located at VBA + 0x900.

4.2 DMA

The DSP56300 EFCOP has two DMA request sources that correspond to the two input/output flags:

- *Input buffer empty transfer*. Triggered when FCSR[FDIBE] is set and a DMA channel is enabled with the DMA request source bits DCRx[DRS] = 0b10101.
- *Output buffer full transfer*. Triggered when FCSR[FDOBF] is set and a DMA channel is enabled with the DMA request source bits DCRx[DRS] = 0b10110.

The MSC8101 EFCOP has four DMA request sources that also correspond to the four input/output flags (the coefficient update done flag cannot trigger a DMA transfer). The MSC8101 DMA request source is controlled by the requestor number bits DCHCRx[RQNUM]. If these bits are equal to 00010, the DMA controller is triggered by an EFCOP read request and if these bits are equal to 00011, the DMA controller is triggered by an EFCOP write request. The MSC8101 DMA cannot distinguish between input buffer empty and input buffer not full or between output buffer full and output buffer not empty requests. Therefore, the MSC8101 EFCOP has four extra bits in the FCTL register that tell the DMA controller which input or output request to service:

- *Input buffer empty transfer*. Triggered when FSTR[FDIBE] and FCTL[FDIM] are set and a DMA channel is enabled with the DMA requestor bits DCHCRx[RQNUM] = 00011. Use this mode when the DMA is programmed to transfer more than one 32-bit long sample to the FDIR.
- *Input buffer not full transfer*. Triggered when FSTR[FIBNF] is set, FCTL[FDIM] is clear and a DMA channel is enabled with the DMA requestor bits DCHCRx[RQNUM] = 00011. Use this mode when the DMA is programmed to transfer single 32-bit long samples to the FDIR.
- *Output buffer full transfer*. Triggered when FSTR[FDOBF] and FCTL[FDOM] are set and a DMA channel is enabled with the DMA requestor bits DCHCRx[RQNUM] = 00010. Use this mode when the DMA is programmed to transfer more than one 32-bit long sample from the FDOR.
- *Output buffer not empty transfer*. Triggered when FSTR[FOBNE] is set, FCTL[FDOM] is clear, and a DMA channel is enabled with the DMA requestor bits DCHCRx[RQNUM] = 00010. Use this mode when the DMA is programmed to transfer single 32-bit long samples from the FDOR.

5 Memory

Both the DSP56300 and MSC8101 EFCOPs contain two memory banks: the FDM and FCM. These memory banks are influenced by the FDBA and the FCBA Registers.

5.1 Organization

The DSP56300 FDM is shared with the lowest locations of on-chip internal X memory and the FCM is shared with the lowest locations of on-chip internal Y memory. The size of the DSP56300 FDM and FCM

depends on the particular device. The DSP56307 and DSP56L307 memory banks share the lowest 4K (0x000–0xFFF) memory locations and the DSP56311 memory banks share the lowest 10K (0x0000–0x2800) memory location. The MSC8101 does not have separate X and Y memory. Therefore, the MSC8101 memory banks are located sequentially in the on-chip internal memory. The MSC8101 memory banks each have a capacity of 32 KB. FDM is shared with the internal memory locations between 0x70000–0x77FFF and the FCM is shared with the internal memory locations between 0x78000–0x7FFFF.

Simultaneous access by both the DSP56300 core and the EFCOP to the same memory block of sixteen 256 word blocks in the DSP56307, four 1024 word blocks in the DSP56L307, or ten 1024 word blocks in the DSP56307 of the shared memory is not permitted and results in erroneous data. In the MSC8101, the SC140 core and the EFCOP can access the shared memory simultaneously. When it is impossible to perform the access at the same time, the MSC8101 core access is delayed by one clock. The DSP56300 EFCOP connects to the shared memory in place of the DMA bus. Therefore, the DSP56300 DMA cannot access the shared memory. However, the MSC8101 memory organization allows the DMA controller to access the shared memory when the EFCOP is disabled.

5.2 Memory Registers

The DSP56300 base address registers are both 16-bit registers that point to the corresponding memory bank. The FDBA register contains the 24-bit address of the location to write the next data sample, and the FCBA register contains the 24-bit address of the beginning of the coefficients. For example, if the FDBA and FCBA registers are written with 0x100 when the EFCOP is initialized, the data and coefficient buffers start at X:$100 and Y:$100, respectively. The MSC8101 base address registers are also 16-bit registers. However, the values in these registers are an offset from the beginning of the corresponding memory bank in 32-bit (four byte) resolution. Only the lowest 13 bits of each register are used, since the data is organized as 8K 32-bit samples (32 KB total) and only 13 bits are needed to address 8K samples. For example, if the FDBA and FCBA registers are written with 0x100, the data and coefficient buffers are located at 0x100 multiplied by four plus the base address, which is memory location 0x70400 for the data buffer and memory location 0x78400 for the coefficient buffer.

6 Registers

In both DSP56300 devices and the MSC8101, the Filter Count (FCNT) register defines the filter size and the control registers define the operation mode and status of the EFCOP.

6.1 Filter Count

In the FCNT Register, the difference is in the number of bits that define the filter length. The DSP56300 FCNT uses 12 bits; the MSC8101 FCNT register uses 16 bits. Therefore, the largest filter the DSP56300 can process has a length of 4K coefficients, and the largest filter the MSC8101 can process has a length of 64K coefficients.

6.2 Filter Control

Table 4 summarizes the difference between the DSP56300 and MSC8101 filter control register bits. The bits are listed in the order in which they are located in their corresponding registers, but extra spaces are added so that similar bits are on the same line. This table ignores the fact that the bit ordering is reversed

between the DSP56300 family and the MSC8101 and shows one of the register bits reversed so that the bits are easily compared. First, note that the main control register has a different name between the two devices. It is called the Filter Control Status Register (FCSR) in the DSP56300 and the Filter Control (FCTL) register in the MSC8101. Second, note that the MSC8101 has a separate status register, the Filter Status Register (FSTR).

The DSP56300 status bits, including the two input/output flags discussed in **Section 3** (FDOBF and FDIBE), are located in the DSP56300 FCSR. The MSC8101 status bits, including the four input/output flags discussed in **Section 3** (FOBNE, FDOBF, FIBNF, and FDIBE) and a coefficient update done flag (FUDN), are included in the MSC8101 FSTR. The DSP56300 FCSR and the MSC8101 FCTL are the main control registers and contain many of the same bits. The differences between these registers are as follows:

- The DSP56300 FCSR contains the bit to control the shared coefficient mode for multichannel mode, FCSO. In the MSC8101, this bit is located in the FACR.
- The two registers contain different bits to control the different request sources, as discussed in **Section 4**. The DSP56300 FCSR contains two I/O interrupt enable bits (FDOIE and FDIIE). The MSC8101 FCTL contains four I/O interrupt enable bits (FONEIE, FOFIE, FINFIE, and FIEIE) and one coefficient update done interrupt enable bit (FUDIE). The MSC8101 FCTL also includes the two DMA I/O mode bits (FDOM and FDIM).
- The MSC8101 contains a bit to enable the coefficient initialization (FCIM), which is discussed in **Section 2**.

The Filter ALU Control Registers (FACR) are the same in both the DSP56300 devices and the MSC8101, except that the MSC8101 does not have 16-bit arithmetic mode (FSA) or saturation mode (FSM) bits because these modes are not available for the MSC8101.

Table 4. Control Register Differences

DSP56300 FCSR	DSP56300 FACR	MSC8101 FCTL	MSC8101 FACR	MSC8101 FSTR
				FOBNE (bit 9)
FDOBF (bit 15)				FDOBF (bit 10)
				FIBNF (bit 11)
FDIBE (bit 14)				FDIBE (bit 12)
				FUDN (bit 13)
FCONT (bit 13)				
				FOVF (bit 14)
FSAT (bit 12)				FSAT (bit 15)
		FDOM (bit 0)		
		FDIM (bit 1)		
FDOIE (bit 11)		FONEIE (bit 2)		
		FOFIE (bit 3)		
FDIIE (bit 10)		FINFIE (bit 4)		
		FIEIE (bit 5)		
		FUDIE (bit 6)		

Table 4. Control Register Differences (Continued)

DSP56300 FCSR	DSP56300 FACR	MSC8101 FCTL	MSC8101 FACR	MSC8101 FSTR
		FCIM (bit 7)		
FSCO (bit 8)			FSCO (bit 8)	
FPRC (bit 7)		FPRC (bit 8)		
FMLC (bit 6)		FMLC (bit 9)		
FOM (bit 4:5)		FOM (bit 11:10)		
FUPD (bit 3)		FUPD (bit 12)		
FADP (bit 2)		FADP (bit 13)		
FLT (bit 1)		FLT (bit 14)		
FEN (bit 0)		FEN (bit 15)		
	FISL (bit 6)		FISL (bit 9)	
	FSA (bit 5)			
	FSM (bit 4)			
	FRM (bit 2:3)		FRM (bit 13:12)	
	FSCL (bit 0:1)		FSCL (bit 15:14)	

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