SP 22.6: A 4.3ns 0.3μm CMOS 54x54b Multiplier Using Precharged Pass-Transistor Logic

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A 54x54b multiplier with 4.3ns latency at 2.5V supply and a 16.96mm² active area is implemented in 0.3μm CMOS with 6.5nm gate oxide and four-layer metal.

This 4.3ns-latency multiplier is for a floating-point unit (FPU) on a CMOS RISC processor capable of performing IEEE double precision multiply operations in three pipelined stages at 400MHz (7.5ns latency and 2.5ns throughput). This multiplier consists of a 54x54b carry-save adder tree and a 108b carry propagation adder. A block diagram of it is shown in Figure 1.

This multiplier achieves 4.3ns performance using a modified Wallace tree implemented from 4:2 compressors with precharged pass-transistor circuits, radix-2 Booth encoding with an unbalanced buffer for generating select signals, and a short-path carry-lookahead adder (CLA).

The 4:2 compressor circuit shown in Figure 2 is one of the key logic circuits of this multiplier. The 4:2 compressor adds four partial products (I1-I4) and generates a sum signal (S) and two carry signals (C and Co). The logic diagram of the 4:2 compressor is shown in Figure 2a. A four-input exclusive OR circuit, a 2-2 AND-OR circuit, and a 2-2 OR-AND circuit and two multiplexer circuits allow a short delay of only two gates for generating S and C outputs. In contrast, the number of critical-path gate stages in conventional 4:2 compressors is three or four. The four-input exclusive OR circuits are easily implemented using domino logic with some precharge devices to reduce charge-sharing noise, as shown in Figure 2b. The multiplexer circuits are constructed from two nMOS pass-transistors and an inverting buffer with a feedback pMOS. Each of the source nodes of the nMOS multiplexer is directly connected to a precharged node (C1, C1B) or the output node of the inverter with a small pMOS (Ci, CiB). The output nodes of the inverters are precharged because Ci and CiB signals are generated by domino logic circuits. Use of the precharged pass transistor circuits reduces the delay time of the four-stage 4:2 compressor tree to 1.67ns. This result translates into 417ps propagation delay for each 4:2 compressor.

To speed up the Booth encoder to drive 54 selector circuits, the unbalanced buffer circuit shown in Figure 3 is used. This buffer consists of three stages of tapered CMOS inverters. The first-stage buffer is an inverter for domino logic. The channel widths of the nMOS in the first- and third-stage inverters are smaller than those of normal balanced inverters, and on the other hand the second-stage inverter pMOS channel width is smaller than normal. The input logical threshold voltages of these inverters are shifted and the internal parasitic capacitances are reduced. The logic evaluation delay time of the unbalanced buffer is 20% faster than that of the conventional buffer, while the precharge timing (1.25ns) is satisfied in both cases. The Booth encoder with the unbalanced buffer and the 4:2 compressor with precharged pass-transistor circuits make it possible to perform 54x54b carry-save addition in 2.4ns.

The inputs of the final carry-propagation adder consist of two parts, a higher 76b portion and a lower 32b portion of the carry-save adder tree outputs. The final carry-propagation adder is separated into four carry-lookahead adders of the highest 64b, 12b, 16b, and lowest 16b. The carry generation from the lower 32b portion does not become a critical delay path, because the higher 76b are generated by a four-stage 4:2 compressor tree, and on the other hand, the least significant 16 bits and the remaining 16b of the lower portion are respectively created by two and three stages of the 4:2 compressor tree. So the carry generation from the 12b CLA (c44) is critical. The delay critical path from c44 to the slowest output (c107) at the 64b CLA is illustrated in Figure 4. This path runs on the nearest nMOS of the precharged nodes of three-stage domino circuits. Other input signals (carry-propagation signals: Pxx, and carry-generation signals: Gxx) are already fixed until the c44 signal level becomes high. It is possible to perform final carry (c107) creation at the most significant 64b CLA in 0.7ns.

The simulated total multiplication time of the 54x54b multiplier in the critical delay path is illustrated in Figure 5. It is 4.3ns with a 2.5V power supply. The delay time for conventional CMOS implementation, also shown in Figure 5, is 7.5ns at the same process technology and same power supply voltage.

A micrograph of the multiplier is shown in Figure 6. The chip is in four-metal 0.3μm CMOS. The major process parameters are summarized in Table 2. The chip integrates 126,024 transistors in an active area of 16.92mm². The measured waveforms are shown in Figure 7. The first signal (Y input) in Figure 7 is the input to the Booth encoder, and the second signal (product output) is the final output through the critical path. The 4.3ns measured latency is in agreement with the simulated latency illustrated in Figure 5.

Acknowledgments:

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References:

[1] Ohkubo, N., et al., "A 4.4ns CMOS 54x54-b Multiplier Using Pass-Transistor Multiplexer," IEEE J. Solid-State Circuits, pp. 251-257, March, 1995.

[2] Hilker, S., et al., "A 3.4ns 0.8μm BiCMOS 53x53b Multiplier Tree," ISSCC Digest of Technical Papers, pp.292-293, Feb., 1994.

[3] Heikes, C., "A 4.5mm² Multiplier Array for a 200MFLOPS Pipelined Coprocessor," ISSCC Digest of Technical Papers, pp.290-291, Feb., 1994.

	Delay time in logic evaluation	Precharge time
Unbalanced buffer	294 ps (0.80)	877 ps <1.25 ns (1.35)
Conventional buffer	368 ps (1.00)	650 ps (1.00)

Table 1: Unbalanced buffer effects (FO=54Booth-selectors).

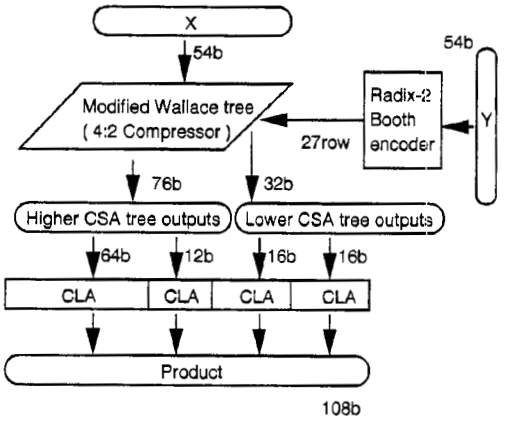

Figure 1: 54x54b multiplier block diagram.

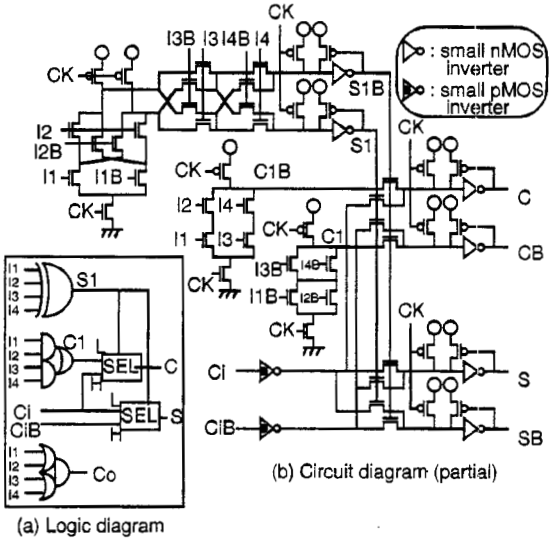

Figure 2: 4:2 compressor.

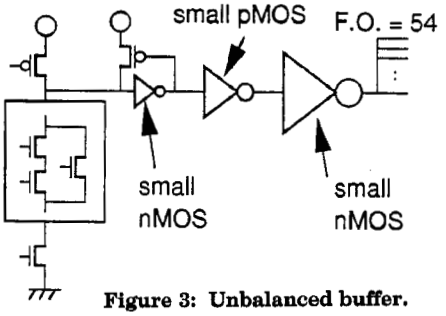

Figure 3: Unbalanced buffer.

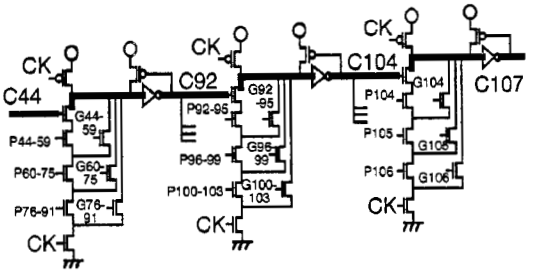

Figure 4: Critical path of final carry lookahead circuits.

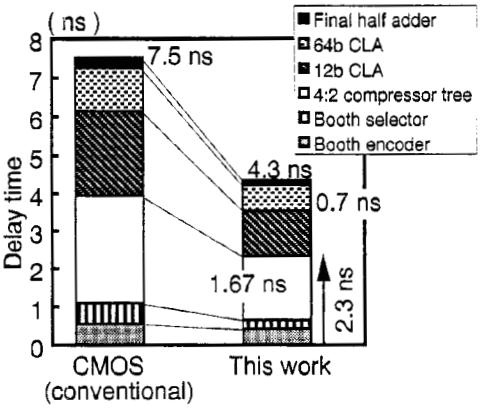

Figure 5: Multiplier critical path delay.

Figure 6: See page 474.

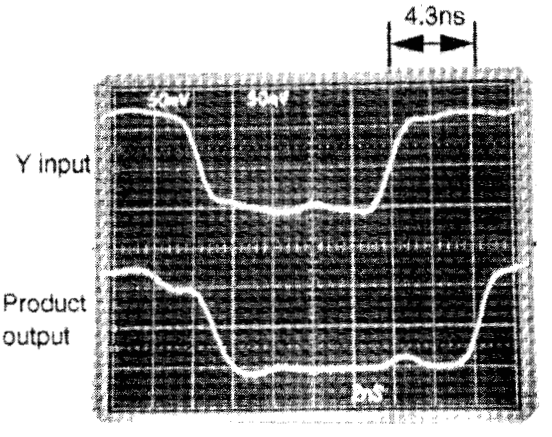

Figure 7: 54x54b multiplier measured waveforms.

Technology	0.3μm CMOS, 4-metal layer
Gate length / oxide	0.3μm / 6.5nm
1st, 2nd metal (width/space)	0.5μm / 0.5μm
3rd, 4th metal (width/space)	1.0μm / 1.0μm

Table 2: Process technology.

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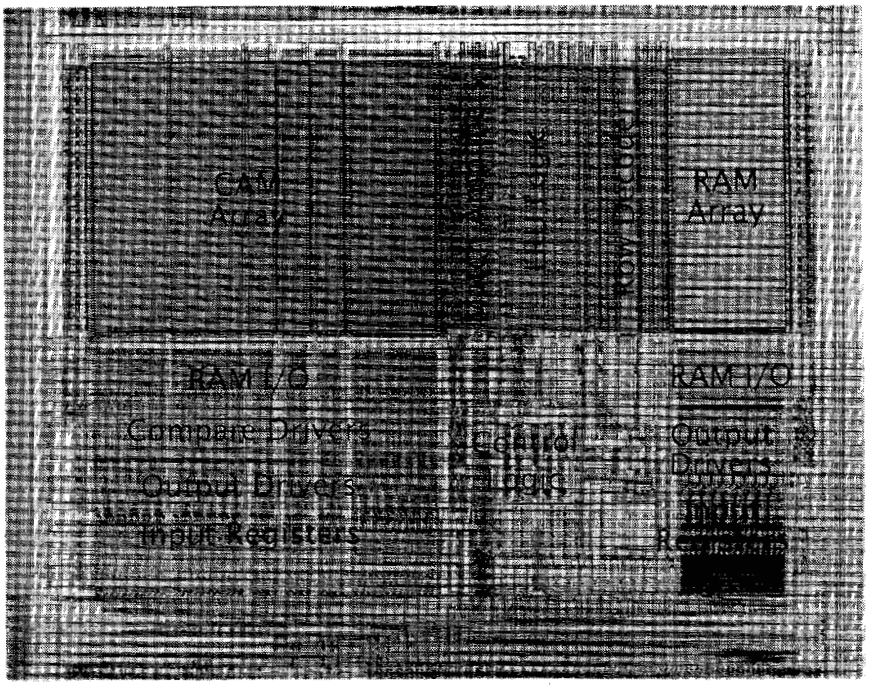

Figure 6: Chip micrograph.

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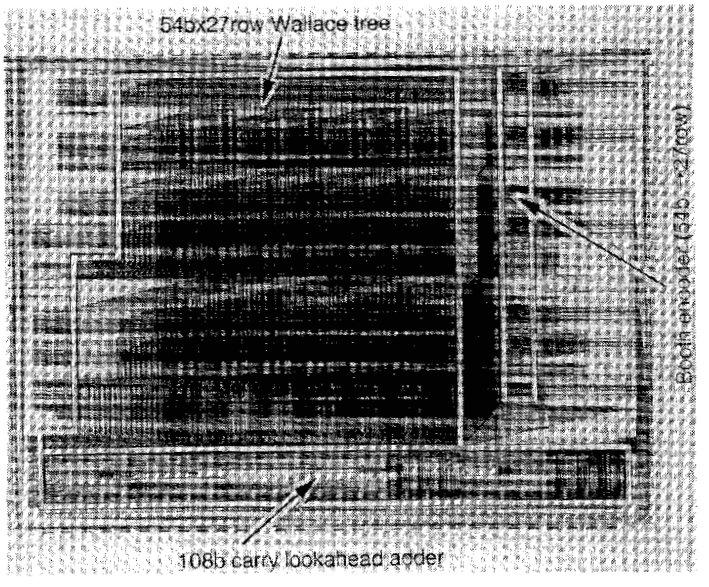

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