MASSANA

FILU Development System

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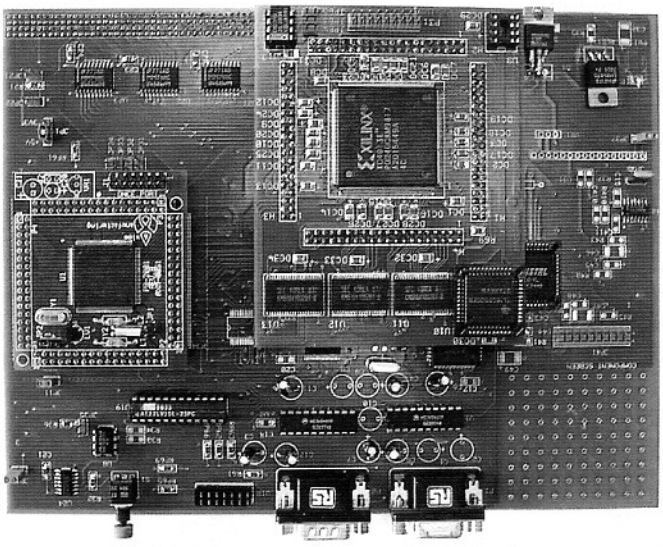

Figure 1 FILU *Development System.*

Features

- FPGA implementation of FILU-200 or FILU-50HC11 or FILU-50.
- 20 MHz operation.
- Motorola® MCORE/FILU-200 combination.
- FILU-50HC11, 68HC11 MCU (instruction set compatible with the Motorola® MC68HC11) integrated with FILU-50 in a single core.
- Interface to Xemics CoolRISC™ Emulation System.
- MCORE and HC11 Monitor programs included.
- 16-bit stereo audio codec.
- Prototyping area.
- LCD display interface.
- RS232 interface.

Introduction

The FILU Development System allows designers to evaluate any member of the FILU family of DSP coprocessor cores in conjunction with a number of industry standard microcontrollers. The FILU devices are implemented in an FPGA and are clocked at 20 MHz.

A number of microcontroller/FILU combinations are supported:

- Motorola MCORE®/FILU-200
- FILU-50HC11 (FILU-50 + 68HC11)
- Xemics CoolRISC™/FILU-50

The Development System is designed in a modular fashion with the MCORE microcontroller designed as a replaceable module. Other microcontroller modules are planned.

Designers can use the Development System to verify their S/W and algorithms. FILU DSP functions are called using the FILU API. Algorithms can be developed using the Instruction Set Simulator and executed in the target system in real time

Motorola MCORE and FILU-200

A complete MCORE micro-computer system is implemented on the Development System and interfaced to the FILU-200. The Motorola MBUG Monitor is resident on the MCORE and allows the user to download application programs from a PC and execute them in the Development System. The FILU API provides the software interface between the MCORE and the FILU-200. The FILU API is compiled using the MCORE GNU compiler and is supplied as a run time library.

FILU-50HC11

An integrated 68HC11 core and a FILU-50 are implemented in the FPGA. The 68HC11 is instruction set compatible with the Motorola® MC68HC11. The HC11 resources– Flash memory, Static Ram, UART and address decoding– are provided externally on the Development System thus implementing a complete HC11 micro-computer system. A HC11 monitor is provided in Flash memory. The FILU API provides the software interface between the HC11 and the FILU-50.

Xemics CoolRISC™ and FILU-50

The Xemics www.xemics.com CoolRISC™ is an ultra low power 8-bit microcontroller. The FILU-50 provides DSP capability and performance for the CoolRISC.

Xemics provide an Emulation System for the CoolRISC™ processor. The FILU Development System is compatible with the Xemics Emulation System allowing the CoolRISC™/FILU-50 combination to be evaluated using the emulator.

Codec Interface

A 16-bit stereo audio codec is provided on the Development System for real-time application evaluation. The FILU interfaces with the codec using a synchronous serial (SSI) interface. The codec is the Crystal Semiconductor CS4216/CS4218. A prototyping area is provided for user defined signal conditioning.

For More Information

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