A 288-kb Fully Parallel Content Addressable Memory Using a Stacked-Capacitor Cell Structure

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Abstract—**This paper describes a 288-kb (8K words × 36 b) fully parallel content addressable memory (CAM) LSI using a compact dynamic CAM cell with a stacked-capacitor structure and a novel hierarchical priority encoder. The stacked-capacitor structure results in a very compact dynamic CAM cell (66 μm^2) which is operationally stable. The novel hierarchical priority encoder reduces the circuit area and power dissipation. In addition, a new priority decision circuit is introduced. The chip size is 10.3 × 12.0 mm^2 using a 0.8-μm CMOS process technology. A typical search cycle time of 150 ns and a maximum power dissipation of 1.1 W have been obtained using circuit simulation. In fabricated CAM chips, we have verified the performance of a search operation at a 170-ns cycle and have achieved a typical read/write cycle time of 120 ns. This CAM LSI performs large-scale search operations very efficiently, and therefore, has the possibility of broad applications to high-performance artificial intelligence machines and data-base systems.**

I. Introduction

DATA processing that involves many search operations performed by software consumes enormous time. This is a hindrance to high-speed data processing. A fully parallel content addressable memory (CAM) compares search data with storage data in a parallel fashion, and is extremely suitable for high-speed data searching. A search operation carried out by a fully parallel CAM is several hundred times faster than that performed by software [1]. Therefore, there have been many studies that have addressed the applicability of CAM's to artificial intelligence (AI) machines, data-base systems, and so on in which search operations are conducted frequently. For example, the studies on a Lisp machine [2], a Prolog machine [3], [4], a data-base accelerator [1], [5], [6], [7], pattern inspection [8], address filtering for local area networks [9], TLB for a RISC processor [10], and others have been reported.

Similarly, there have been many studies concerning high-density CAM's that use LSI technology, ever since a CAM cell using MOS transistors was introduced in 1966 [11]. It has been difficult to develop a large-bit-capacity CAM, because fully parallel CAM's require an EXCLUSIVE-NOR circuit in each CAM cell for a match operation. Representative attempts to rectify this problem are a 1-kb CAM in 1983 [12], 4- and 8-kb CAM's in 1985 [13], [14], and a 20-kb CAM in 1989 [15]. However, CAM's with larger bit capacities are required for large-scale data searching and for broadening CAM applications.

In this paper, a compact dynamic CAM cell with a stacked capacitor structure and a novel hierarchical priority encoder are proposed for expanded large-scale integration. Utilizing these new techniques, a 288-kb (8K words × 36 b) fully parallel CAM has been successfully developed. In order to achieve high-performance data searching, this CAM LSI was also designed to perform various functions. In the following sections, the CAM cell, the novel priority encoder, the chip architecture, and the functions and features of this CAM LSI are described [16].

II. Dynamic CAM Cell with Stacked-Capacitor Structure

Conventional CAM's use a static CAM cell, which keeps storage data in a latch, to accomplish a stable operation [12]–[15]. Static CAM cells, however, take up large areas of the chip due to the large numbers of transistors in the cell. Therefore, the static-type cell is not suitable for high-density CAM's. To address this problem, a dynamic CAM cell that stores data on the gate capacitance of transistors has been proposed [17], [18]. The dynamic-type cell provides a compact cell area due to the smaller number of transistors required. However, there is still a serious problem with the conventional dynamic CAM cells. In the dynamic cells, since a charge is stored on the gate capacitance of a transistor, the storage capacitance decreases as the transistor size decreases. Therefore, in a compact CAM cell using a submicrometer process, it is difficult to attain a storage capacitance of more than 30 fF, which is necessary to be immune from the alpha-particle-induced soft error as described in dynamic RAM's. This section presents an operationally stable, compact, dynamic CAM cell for large-scale integration.

The proposed CAM cell is shown in Fig. 1. It consists of five NMOS transistors and two stacked capacitors [19]. Four of the transistors (M_{s0}, M_{s1}, M_{w0}, M_{w1}) are used to

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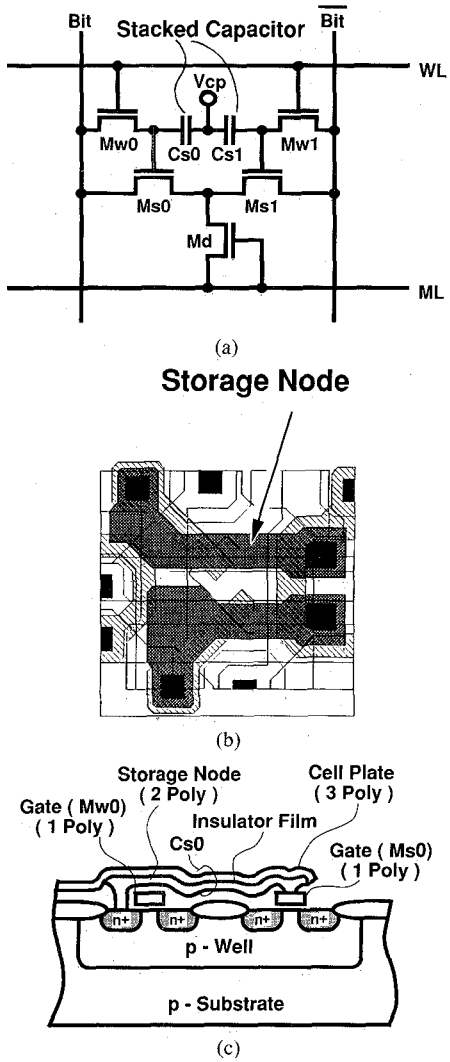

Fig. 1. Dynamic CAM cell with stacked-capacitor structure. (a) Cell circuit diagram ($V_{cp} = V_{cc}$: supply voltage). (b) Layout of CAM cell. Cell size is 8.8 × 7.5 μm^2. (c) Cross-sectional view of CAM cell.

store and access data, and one (M_d) is used as a diode to isolate current paths during match operations. Charges are stored on stacked capacitors (C_{s0}, C_{s1}) and the M_{s0} and M_{s1} gates. The opposite electrodes of the C_{s0} and C_{s1} are connected to a cell plate voltage V_{cp}, which is equal to half V_{cc} (V_{cc}: supply voltage). Two bit lines (Bit, $\overline{\text{Bit}}$) are supplied with data in write and search operations. The word line (WL) allows write access to each cell in a word (36 b). The match line (ML) passes through a word to perform a logical AND of the results of each cell's comparison. The ML is also used to read cell data. The storage capacitor (C_{s0}) is stacked on the gate of the M_{s0} and M_{w0}, as shown in Fig. 1(c). The gate electrodes of the M_{s0} and M_{w0} are fabricated with the first poly-Si layer. The stacked capacitor is composed of the second poly-Si layer, the insulator film, and the third poly-Si layer. The second poly-Si layer (storage node) is also used to connect the drain (or source) of the M_{w0} to the gate of the M_{s0}. Similarly, the storage capacitor (C_{s1}) is formed on the gate of the M_{s1} and M_{w1}. A SEM micrograph of the CAM cell after storage node layer formation is shown in Fig. 2.

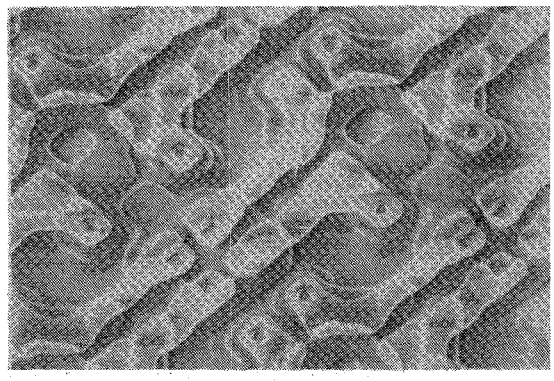

Fig. 2. SEM micrograph of CAM cell after storage node formation.

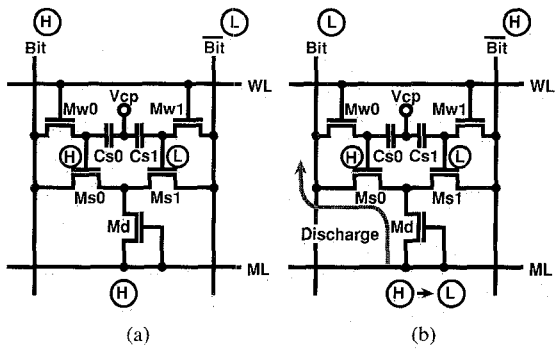

Fig. 3. Match operation of novel CAM cell: the case of (a) match and (b) mismatch. Match result is transferred to match line ML.

A write operation is performed by activating a select WL and then driving the bit lines according to the write data. Utilizing this process, the data are written on the stacked capacitors and the gates of M_{s0} and M_{s1} via the M_{w0} and M_{w1}.

A match operation is achieved by precharging both the bit lines and the match lines to a high level, and then loading the bit lines with search data. As shown in Fig. 3, it is assumed that high data are stored in a CAM cell. The Bit, $\overline{\text{Bit}}$, and ML are precharged to a high level beforehand. If a high potential and a low potential are supplied to the Bit and $\overline{\text{Bit}}$, respectively, the ML retains the high level, and "match" is detected (Fig. 3(a)). On the other hand, if a low potential and a high potential are supplied to the Bit and $\overline{\text{Bit}}$, respectively, the ML is discharged via the transistors M_{s0} and M_d, and the ML drops to a low level. Therefore, "mismatch" is indicated (Fig. 3(b)). In this way, match information is transferred to match lines.

A read operation is accomplished by discharging the bit lines, and then driving a selected ML to a high level. If high data are stored in the cell, the Bit is charged via the M_d and M_{s0} from the ML, and the $\overline{\text{Bit}}$ remains at a low level. Similarly, if low data are stored in the cell, the Bit remains at a low level and the $\overline{\text{Bit}}$ is charged. In this way, the storage data in the cell are read out on the bit lines.

In the novel CAM cells, since a stacked capacitor is adopted as the storage capacitor, a storage capacitance of 90 fF is attained in a 66-μm^2 CAM cell using a 0.8-μm CMOS process. This is sufficient for the high soft-error immunity and provides stable performance of the opera-

tions mentioned above. Futhermore, it suggests the possibility of achieving a more compact CAM cell by device scaling.

III. Novel Hierarchical Priority Encoder

When a match occurs at several words in a search operation (multiple response), the CAM outputs the address of the matched word with the highest priority. A priority encoder (PE) circuit is utilized for multiple-response resolution and match address generation. As a bit capacity of CAM's becomes larger, the number of words increases rather than the bit length of words. Therefore, in a high-density CAM chip, the configuration must be such that the cell array is divided into several blocks. This creates a serious problem concerning the layout of the PE. When the PE is incorporated in each block, the silicon area occupied by the PE and the power dissipation of the PE are increased in proportion to the number of divided blocks. We therefore propose a novel hierarchical PE architecture suitable for high-density CAM's, as shown in Fig. 4. In the architecture, an OR circuit and a switching circuit are provided in each block, and a main priority encoder (MPE) and a block priority encoder (BPE) are located in the peripheral area of the CAM array. In a search operation, each OR circuit generates a block-hit signal, which shows whether matched words exist in the block or not. Then, the block-hit signal is connected to the BPE and scrutinized by the BPE. The BPE then generates an encoded block address and block-select signals which indicate the block with the highest priority. Next, the switching circuit of the selected block is activated, and the match information of the selected block is transferred to the MPE. Finally, the MPE generates an encoded main address, which combines with the encoded block address to form a match address.

In this architecture, the OR circuit and the switching circuit, which occupy a very small silicon area and dissipate little power, are located in each block. Furthermore, only one BPE and MPE, which have large areas and dissipate much power, are placed in the peripheral area. Therefore, an increase in the silicon area and power dissipation in the PE due to an increase in the number of divided blocks can be suppressed using this architecture.

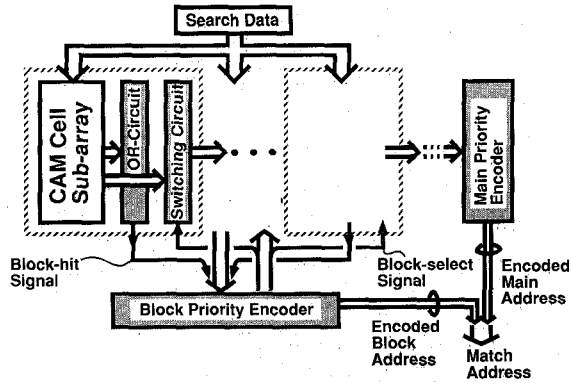

Fig. 4. Novel hierarchical priority encoder. BPE indicates block with the highest priority and MPE indicates word with the highest priority in the selected block.

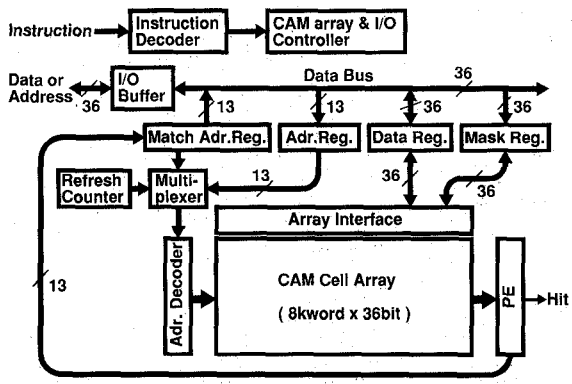

Fig. 5. Block diagram of 288-kb CAM.

IV. CAM Architecture

A. Basic Architecture and Operations

A block diagram of a 288-kb CAM is shown in Fig. 5. The CAM LSI consists of an 8K word × 36-b memory cell array, an address decoder for address access operations, a PE for search operations, registers, I/O buffers, and control circuits managed by instructions from external ports. Since the CAM utilizes dynamic-type CAM cells, a refresh operation is needed. Therefore, a refresh address counter is also prepared for the refresh operation. The PE has the hierarchical architecture previously described, the details of which will be discussed in the next section. A match address register contains the match address received from the PE after a search operation. An address register is provided to store an address for write and read operations. A data register keeps search and write data from external ports and read data from the memory cell array. The search and write data can be masked by mask control bits contained in a mask register, for masked search operations and partial writing, respectively.

The search, write, and read operations are performed in one cycle, between the CAM cell array and registers. One cycle is also required for data transmission between the registers and the external ports. The search operation is carried out as follows: in the first cycle, 36-b research data are transferred from the external ports to the data register via data buses; in the second cycle, the search data are simultaneously compared with 8K words stored in the CAM cell array, and the match address is then transferred to the match address register; and in the third cycle, the match address is output to the external ports via the data buses. Therefore, content addressing is achieved in three cycles. Similarly, the write and read operation by an address access can be performed in three cycles. In the refresh cycle, an internal address generated by the refresh address counter is supplied to the address decoder via a multiplexer. All CAM cell data are refreshed by 512 refresh cycles.

In addition, the CAM can perform logical AND/OR operations between previous and curent search results, and

TABLE I
INSTRUCTIONS OF 288-kb CAM

Search	• search word • OR search • AND search • LINK search • NEXT search • search empty word
Write	• write data to addressed word • write data to matched word
Read	• read data from addressed word • read data from matched word
Empty	• empty addressed word • empty matched words in parallel
others	• reset • refresh

can store the results in match flags which are provided each word and show whether the word is matched or not (AND/OR search). This function facilitates relational search operations such as less-than search [15]. The CAM can also carry out a logical AND operation among search results of two or more successive words for wide-band searching (LINK search) [15]. When a multiple-response occurs in a search operation, the CAM can output the address of the next most closely matched word after generating the match address with the highest priority (NEXT search). By repeating this operation, the CAM can output match addresses in order of priority. Furthermore, empty flags are provided every word location to indicate whether the word is empty. The CAM LSI can empty desired words by address access, and also empty matched words at once. Moreover, the CAM can search for empty words and output the addresses of empty words. The main instructions of the CAM LSI are summarized in Table I. The functions previously mentioned, in combination with a 288-kb memory cell array, contribute to the actualization of high-performance data processing.

B. CAM Cell Array Architecture

The memory cell array architecture is shown in Fig. 6. The CAM array is divided into 32 blocks. Each block has a CAM cell subarray of 256 words × 36 b, a word operation circuit, a bit operation circuit, and a block controller. The word operation circuit drives the WL's and ML's in write and read operations and latches search result signals in every word's match flags. The word operation circuit also contains the OR circuit and the switching circuit of the new priority encoder described in Section III. The bit operation circuit supplies the CAM cell subarray with data from the array data buses during search and write operations, and provides CAM cell data to the array data buses during read operations. The block controller manages the word operation circuit and the bit operation circuit. One BPE and four MPE's are placed for

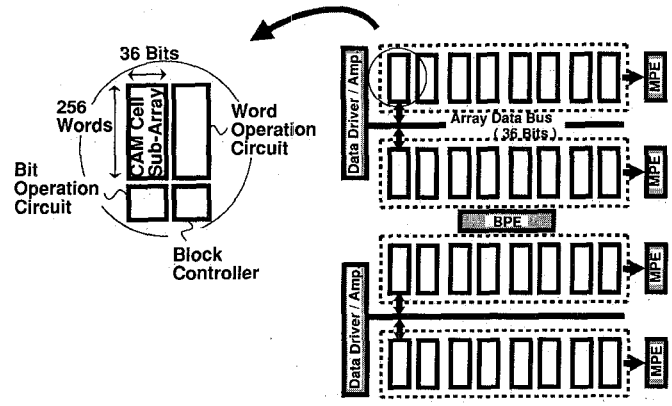

Fig. 6. CAM cell array architecture. CAM array is divided into 32 blocks. One BPE and four MPE's are placed for novel PE architecture.

the novel hierarchical PE architecture, and each MPE is connected to eight CAM cell blocks, as shown in Fig. 6. Moreover, data drivers and amplifiers that are connected to the array data buses are povided as interfaces between the peripheral circuit and the CAM array.

The block-hit signals generated in every block are sent to the BPE in parallel, and the search result of the selected block, from among 32, is transferred to one of the four MPE's by block-select signals from the BPE. The other three MPE's are not activated. By utilizing this unique hierarchical PE, the area the PE occupies is only 12% of the CAM array's total area. (A conventional PE occupies 35%.)

V. MULTIPLE-RESPONSE RESOLVER

A multiple-response resolver (MRR) in the BPE is designed using a binary tree structure [20], as illustrated in Fig. 7. In a basic selection circuit, *HB*0 and *HB*1 are hit-signals from lower level circuits, and *SB*0 and *SB*1 are select-signals sent to the lower-level circuits. *HBA* is a logical OR result of *HB*0 and *HB*1, and is sent to an upper level circuit. *SBA* is a select signal from the upper level circuit and controls the activation of the basic selection circuit. Here, it is assumed that *SBA* is activated (*SBA* = "1"). If *HB*0 = "1," *SB*0 is activated and *SB*1 is not activated, in spite of the value of *HB*1. *SB*1 is activated only when *HB*0 = "0" and *HB*1 = "1". When *SBA* is not activated (*SBA* = "0"), both *SB*0 and *SB*1 are not activated. The hit signals (*HB*0, *HB*1) and select signals (*SB*0, *SB*1) in the lowest level circuits correspond to the block-hit signals from the CAM cell blocks and the block-select signals to the blocks, respectively. The *HBA* of the circuit with the highest level indicates whether there are matched words in the CAM LSI (shown as "Hit" in Fig. 7). As a result, the block with the highest priority matched word is selected by the block-select signals.

Fig. 8 illustrates the configuration of a MRR in the MPE. This MRR has a tree structure based on lookahead circuits for high-speed operation. *M*0–*M*255 are match signals from 256 words in the CAM cell block selected by the BPE. Conventional four-input lookahead priority

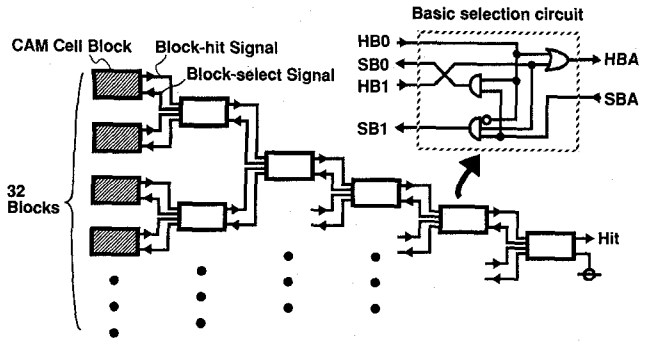

Fig. 7. Multiple-response resolver in BPE. The circuit is designed using a binary tree structure.

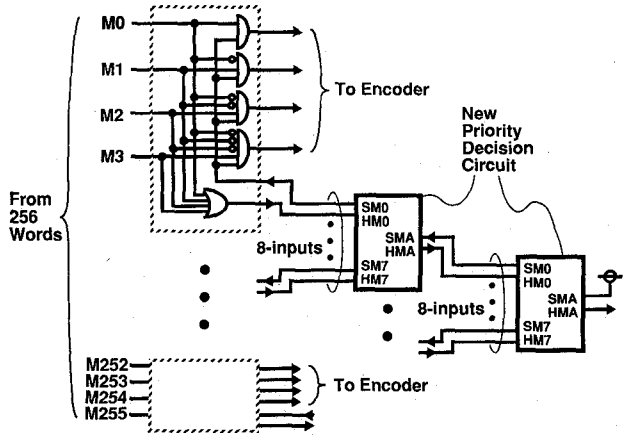

Fig. 8. Multiple-response resolver in MPE. The MRR has a tree structure based on lookahead circuits for high-speed operation.

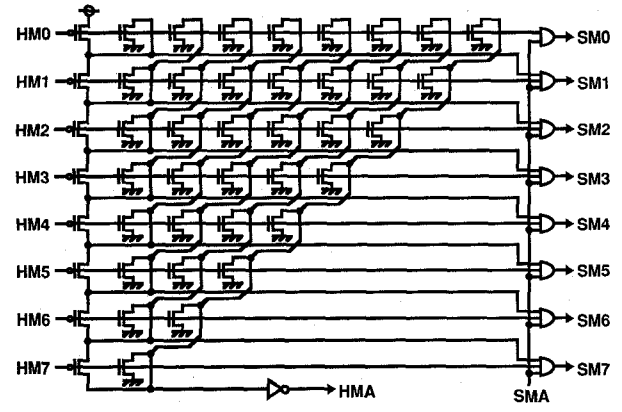

Fig. 9. New priority decision circuit. The circuit scheme brings small circuit area because an OR circuit to generate HMA is merged in the lookahead circuit.

decision circuits are used for first level of the tree structure, and new eight-input lookahead circuits are adopted for the second and third levels. Fig. 9 shows the new priority decision circuit. *HM*0–*HM*7 are hit signals from lower level circuits, and *SM*0–*SM*7 are select signals sent to the lower level circuits. *SMA* is a select signal from an upper level circuit and controls the activation of *SM*0–*SM*7. Here, it is assumed that *SMA* is activated (*SMA* = "1"). If *HM*0 is "1," *SM*1–*SM*7 with lower priority are inhibited from outputting and only *SM*0 is activated.

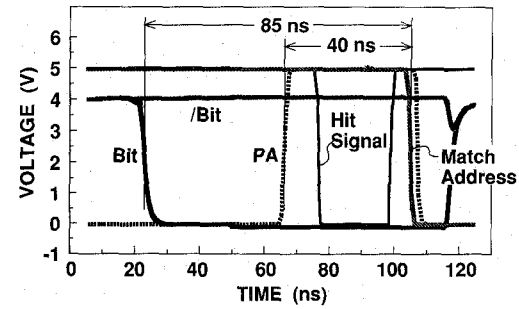

Fig. 10. Simulation result of search operation. *PA* is activating signal of PE.

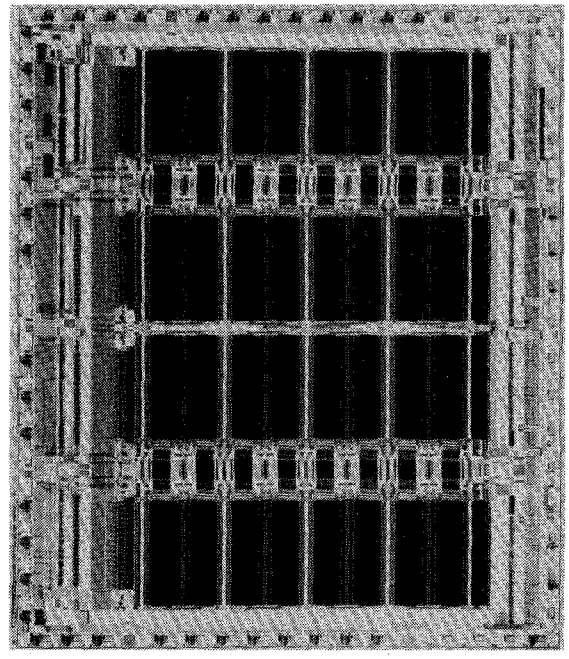

Fig. 11. Photomicrograph of 288-kb CAM.

When *HM*0 is "0" and *HM*1 is "1," only *SM*1 is activated. In this way, the outputs are decided based on the hit signal with the highest priority. Futhermore, an OR circuit used to generate a hit-signal *HMA*, which is transferred to an upper level circuit, is merged in the lookahead circuit. The number of transistors is very small compared with that of a circuit utilizing conventional logic gates. Therefore, the new circuit contributes to circuit area reduction.

VI. Circuit Simulation

Fig. 10 shows the simulation result of a search operation at 5 V of power supply. The generation time of a match address is 85 ns, from the time the search data is loaded on the bit lines. The encoding time of this new PE is 40 ns, and the typical cycle time is 150 ns. The maximum power dissipated in the PE is 52.2 mW at 6.7-MHz and 5-V operation, which is 20 times less than that of conventional PE architecture. The maximum power dissipation of the chip is 1.1 W at 6.7-MHz and 5-V operation.

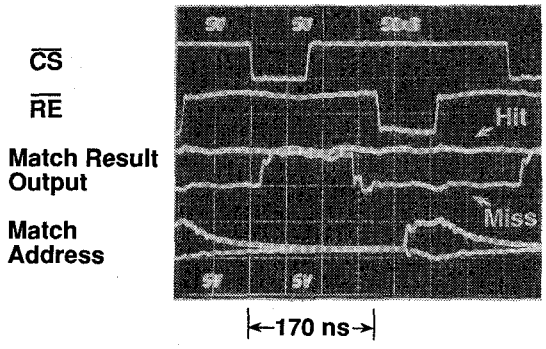

Fig. 12. Measured waveforms in search operation at V_{cc} = 5 V and T_a = 25°C.

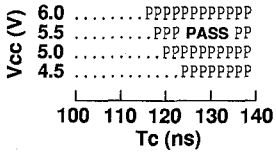

Fig. 13. Schmoo plot of V_{cc} versus cycle time T_c in read/write operation at T_a = 25°C.

VII. Experimental Results

An experimental 288-kb CAM chip has been fabricated using a 0.8-μm double-metal CMOS process technology. A photomicrograph of the CAM chip is shown in Fig. 11. The chip size is 10.3 × 12.0 mm^2. Fig. 12 shows waveforms measured in a search operation. The search operation starts from $\overline{CS}$ clock falling, and then the match result is output. Next, the match address is obtained from a match address register after $\overline{RE}$ clock falling. The waveforms indicate that a search operation is carried out within 170 ns at a supply voltage V_{cc} of 5 V and an ambient temperature T_a of 25°C. Fig. 13 shows a schmoo plot of V_{cc} versus cycle time T_c for read and write operations when T_a = 25°C. A cycle time of 120 ns has been achieved at a V_{cc} of 5 V. Furthermore, a data retention time of more than 2 s has been obtained in a search operation cycle when V_{cc} = 5 V and T_a = 25°C. This means that a refresh cycle time of 3.9 ms is required considering the 512 refresh architecture. This value is much longer than that of a dynamic RAM.

VIII. Conclusions

A 288-kb (8K words × 36 b) CAM with a fully parallel search operation has been successfully developed using a dynamic CAM cell with a stacked-capacitor structure and a novel hierarchical priority encoder. This CAM LSI is fabricated using 0.8-μm double-metal CMOS process technology. The chip measures 10.3 × 12.0 mm^2. The typical search cycle time and maximum power dissipation are 150 ns and 1.1 W, respectively, using circuit simulation. In fabricated CAM chips, we have verified the performance of a search operation at a 170-ns cycle and have obtained a read/write cycle time of 120 ns using a V_{cc} of 5 V. The features of the CAM are listed in Table II. This CAM LSI has possible broad applications to high-performance AI machines and data-base systems, which require high-speed for large-scale data searching.

TABLE II
Features of 288-kb CAM

Organization	8K words × 36 b
Cycle Time	150 ns (Typical)
Supply Voltage	5 V
Power Dissipation	1.1 W (Max.) at 6.7 MHz
I/O Interface	I/O Common, TTL Compatible
Number of Pins	68
Process Technology	0.8-μm twin-well CMOS 2 Al/3 Poly-Si/1 Polycide
Chip Size	10.3 × 12.0 mm^2
Cell Size	8.8 × 7.5 μm^2
Refresh Cycle	512

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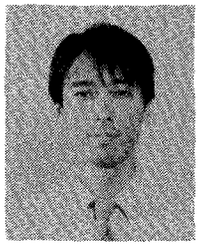

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Mr. Yamagata is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

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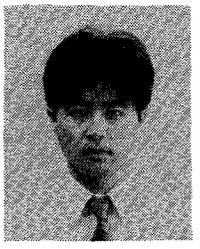
In 1986 he joined the LSI Research and Development Laboratory, Mitsubishi Electric Corporation, Hyogo, Japan.



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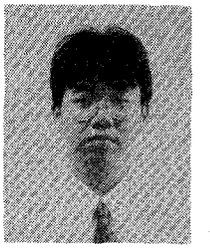
He joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in April 1987. Since then he has engaged in the design of ASIC memories and MOS dynamic RAM's.



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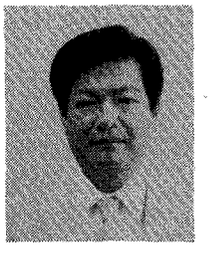

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Dr. Ozaki is a member of the Institute of Electronics, Information and Communication Engineers of Japan.