A 300-MHz 16-b BiCMOS Video Signal Processor

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Abstract— **A 300-MHz 16-b full-programmable parallel-pipelined video signal processor ULSI has been developed. With multifunctional arithmetic units to achieve parallel vector processing, and with a phase-locked-loop (PLL) type clock generator to help attain the 300-MHz internal operating speed, this ULSI is able to attain, with only one chip, 30-frame-per-second full-CIF video data coding based on CCITT H.261. Two different types of pass-transistor BinMOS circuits have been developed to help achieve an access time of 3 ns for a 146-kb SRAM and for data buses. Fabricated with a 0.5-m BiCMOS and triple-layer metallization process technology, the video signal processor ULSI contains 1.27-million transistors in a 16.5 × 17.0-mm^2 die area.**

I. Introduction

THE necessity of handling huge amounts of moving picture data with coding systems based on CCITT H.261 and MPEG resulted in the development of a number of high performance video signal processors (VSP's) over the last few years [1]–[3]. These VSP's, which handle video signal data at a rate of about 1.5 Mb/s, generally employ one of two approaches: 1) high speed circuits, which are able to achieve operating frequencies of a few hundred megahertz, or 2) highly parallel processing architectures, which operate at relatively low frequencies.

With the former approach, it is difficult to achieve low power dissipation or to design a low-skew clock distribution. In an attempt to overcome these disadvantages, we previously developed a 250-MHz super-high-speed video signal processor (S-VSP) which uses a BinMOS clock driver for driving a large capacitance and a clock generator with a phase-locked loop (PLL) for reducing interface power dissipation [1]. To meet the coding system recommendations of the CCITT H.261 at 30 frames per second, however, at least three of these S-VSP's would be required.

Parallel architecture, on the other hand, can improve VSP performance while maintaining a low operating frequency. One previously reported processor includes four arithmetic units operated in parallel at 25-MHz frequency [2]. Another processor employs a vector-pipelined architecture for processing of vector data at 60-MHz frequency [3]. Neither of these, however, is sufficient to implement the above-mentioned video data coding in a single chip.

In order to squeeze the entire processor necessary to the coding system onto a single chip, we have developed a 300-MHz 16-b full-programmable, parallel-pipelined video signal processor, hereafter referred to as VSP3. The key technologies used in the VSP3 are 1) a parallel vector processing architecture without resource conflicts, 2) an arithmetic unit configuration suited for use with a highly efficient, fast DCT algorithm and with moving vector detection based on the CCITT H.261, 3) a programmable phase-locked loop (PLL) circuit to generate a 300-MHz internal clock, and 4) two different types of pass-transistor BinMOS circuits to help achieve access times of 3 ns for a 146-kb SRAM and for data buses. Fabricated with 0.5-μm BiCMOS and triple-layer metallization process technology, the VSP3 contains 1.27-million transistors in a 16.5 × 17.0-mm^2 die area.

In this paper, we first introduce the VSP3 architecture in Section II. This is followed in Sections III and IV by a detailed description of vector processing techniques. In Section V, we discuss the arithmetic unit configuration which helps achieve efficient video signal processing, and in Section VI, we present the high-speed circuits used to attain 300-MHz operations. In Section VII, we present the operational results obtained for portions of an actual fabricated chip. In Section VIII, we discuss the significance of simulated performance results for the VSP3.

II. VSP3 Architecture

A block diagram of the VSP3 is shown in Fig. 1. It consists of four 1-port data SRAMs (512-word × 16-b RAM-A, 4-kword × 16b RAM-B, 512-word × 16-b RAM-F, and 512-word × 16-b FIFO) and three 8.5-kb (544-word × 16-b) 2-port data SRAM's (RAM-C, RAM-D, and RAM-E; one port for reading and the other for writing), seven memory address generation units (AGU's), a 16-b 6-stage variable-pipelined arithmetic logic unit (PAU), a 16-b 7-stage variable pipelined convolver unit (PCU), a sequence control unit (SCU) containing an instruction RAM (1-kword × 32-b IRAM), a host interface unit (HIU) with a 20-b input port and a 20-b output port, four 16-b data buses, and a 20-b control bus. The AGU's generate variable lengths of block scan addresses to access video data stored in the SRAM's. In addition to this, AGU-C and AGU-D generate zigzag scan addresses for efficient processing of inverse discrete cosine transforms and quantizations. Internal datapaths in the PAU and the PCU can be flexibly configured to cover various applications, from simple signal processing to the complex video data coding required for the CCITT H.261. The timing control unit (TCU) includes a programmable PLL-type clock generator circuit which generates an internal clock at anywhere from 2 to 16

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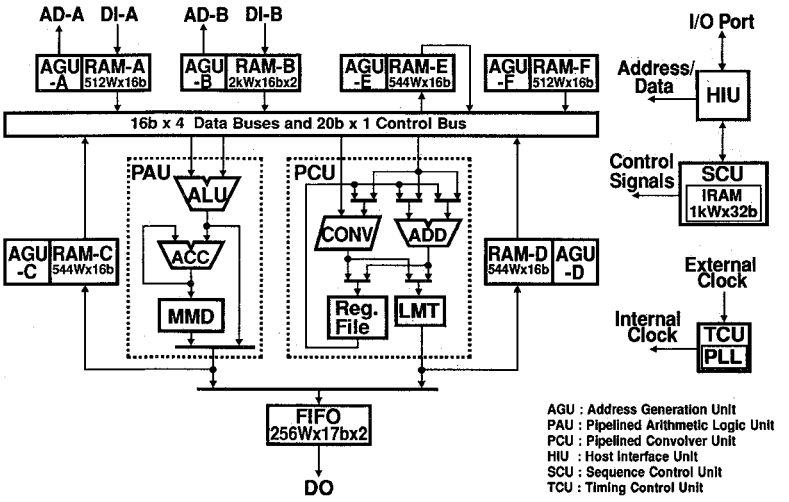

Fig. 1. Block diagram of the parallel-pipelined video signal processor (VSP3) ULSI.

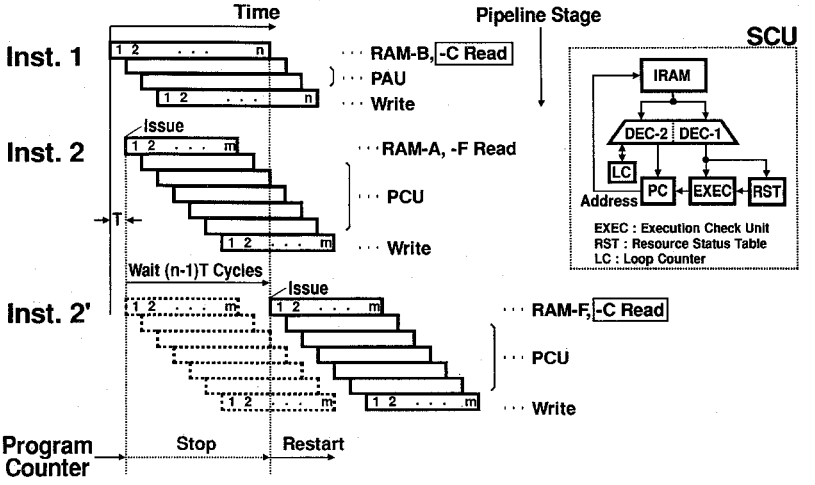

Fig. 2. Parallel-pipelined vector processing and timing control of executing instruction by the sequence control unit (SCU).

times the speed of the external clock, up to 300 MHz. To access external memories, the VSP3 has two 20-b address output ports (AD-A and AD-B), two 16-b data input ports (DI-A and DI-B) and one 16-b data output port (DO).

Table I summarizes the VSP3 instruction set, which includes scalar instructions (SET, SOP, and SMV) and vector instructions (LOAD, VOP, and VMV). SET instructions are used to write immediate data into registers of the AGU's, the PAU, and the PCU, as well as into registers corresponding to the respective upper 128-word addresses of the RAM-C and the RAM-D. LOAD instructions are used to transfer of pixel data stored in external memories into the RAM-A and the RAM-B. Arithmetic and transfer operations for word data are performed by executing SOP and SMV instructions, respectively, while those for vector data are performed by executing VOP and VMV instructions, respectively. Typical vector operations are performed as follows:

1) Specify addressing modes (block scan, zigzag scan, etc.) and address lengths, by issuing a SET instruction to write immediate data into 3 AGU's, one AGU to be used for a writing memory, as well as one for each of two reading memories.
2) Specify internal data paths and functions for the arithmetic units, either the PAU or the PCU by issuing a SET instruction to write immediate data into them.
3) Issue a VOP instruction to start the AGU's and one of the arithmetic units, either the PAU or the PCU.

Scalar and vector instructions can be executed in parallel as long as there are no conflicts among the memories, the arithmetic units, and the buses. Potential conflicts caused by parallel processing are predicted and avoided by the SCU, as is described below in detail.

III. Parallel-Pipelined Vector Processing

Fig. 2 shows a timing chart of parallel-pipelined vector processing. Horizontal and vertical axes indicate time and pipeline stages, respectively. The SCU contains instruction decoders (DEC-1 and DEC-2), a program counter (PC), a loop

TABLE I
INSTRUCTION SET SUMMARY OF THE VSP3

Instruction	Function
SET	Write immediate data into functional blocks
LOAD	Load vector data from outside to RAM-A and RAM-B
VOP	Vector operation and result store
SOP	Scalar operation and result store
VMV	Vector data transfer
SMV	Scalar data transfer
JUMP	Conditional/Unconditional jump
CALL	Conditional/Unconditional subroutine call
RETURN	Return from subroutine
NOP	No operation

TABLE II
ADDRESSING MODES OF THE ADDRESS GENERATION UNITS (AGU's)

Unit	Use	Addressing modes
AGU-A	RAM-A	Block
AGU-B	RAM-B	Block
AGU-C	RAM-C	Block, DCT, Zig-zag
AGU-D	RAM-D	Block, DCT, Zig-zag
AGU-E	RAM-E	Block, DCT
AGU-F	RAM-F	Block

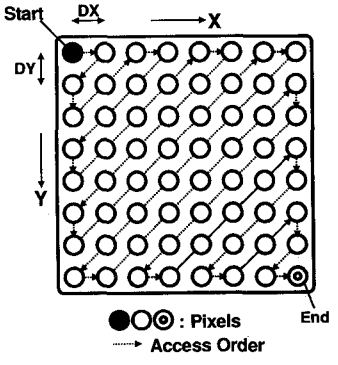

Fig. 3. Zigzag scan access to the data SRAM's.

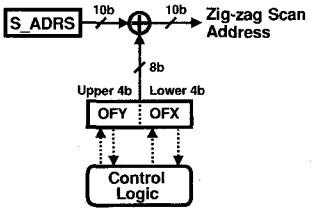

Fig. 4. Block diagram of the zigzag scan address generator.

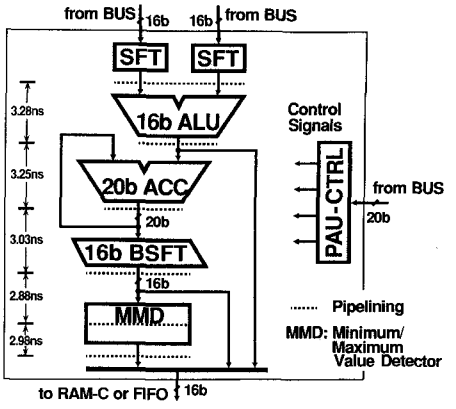

Fig. 5. Block diagram of the pipelined arithmetic logic unit (PAU).

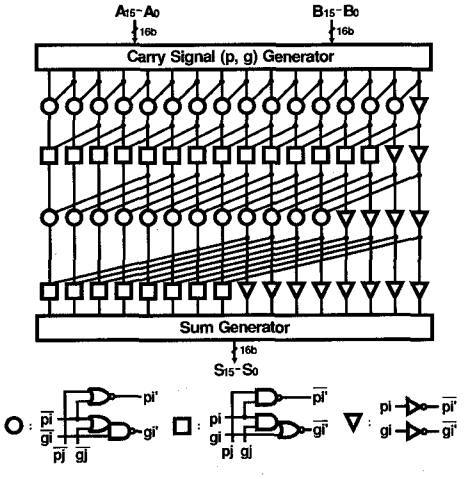

Fig. 6. Block diagram of the 16-b binary look-ahead carry (BLC) adder.

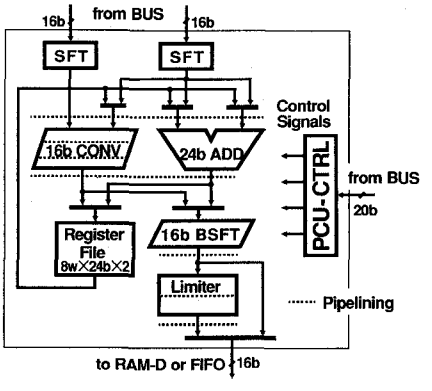

Fig. 7. Block diagram of the pipelined convolver unit (PCU).

counter (LC), a resource status table (RST), and an execution check unit (EXEC), as shown in Fig. 2. The PAU executes both arithmetic and logic (ALU) operations for n vector length data by instruction-1 (Inst.1), and the PCU executes a multiply or convolution (CONV) operation for m vector length data by instruction-2 (Inst.2) or instruction-2′(Inst.2′). When the Inst.2 is read from the IRAM and decoded by the DEC-1 one T cycle after the Inst. 1, resources required by the Inst.2 are compared with outputs of the RST, which maintains the condition of resources used in the Inst. 1 execution. Where no conflicts exist, the EXEC allows the DEC-2 to execute the Inst.2 in parallel with the Inst.1. Both the ALU and the CONV operations then run in parallel. On the other hand, when the Inst.2′ is decoded instead of the Inst.2, a conflict with regard to the RAM-C read is predicted. The EXEC then prohibits Inst.2′ execution one T cycle after the Inst.1 execution, and makes the PC restart after $(n-1)T$ cycles. Thus, parallel-pipelined vector processing can be achieved without conflicts. All potential conflicts among data SRAM's, data buses, arithmetic units, and address generators are predicted and avoided by the EXEC unit each time a successive instruction is decoded.

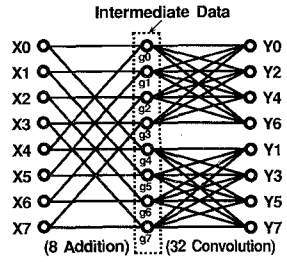

Fig. 8. Fast 1-dimensional 8-point DCT and inverse DCT algorithm.

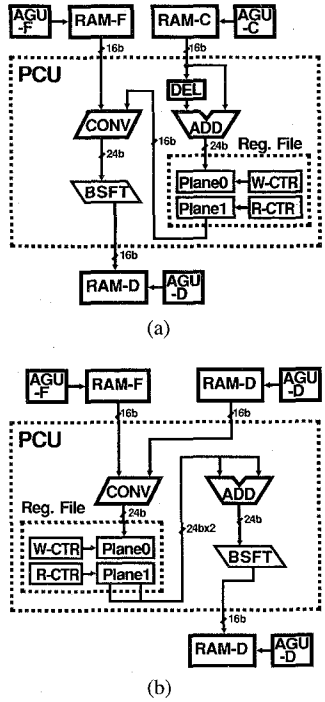

Fig. 9. Data path configurations using the PCU. (a) Discrete cosine transform (DCT) operation. (b) Inverse DCT operation.

IV. Address Generation Units

To enhance vector processing capability of the VSP3, we have designed the multifunctional AGU's. Table II lists the available addressing modes of the AGU's. Block scan is generally used in video signal processings [1]. DCT scan is provided for performing a fast DCT algorithm as described in Section V. Zigzag scan address is generated by a dedicated hardware in the AGU's. Fig. 3 shows an 8 × 8-pixel zigzag scan pattern. A block diagram of the 10-b 8 × 8-pixel zigzag scan address generator is shown in Fig. 4. It consists of a 10-b register (S_ADRS) to indicate start address, a 10-b adder, two 4-b offset registers (OFX and OFY) to be added to the S_ADRS, and a control logic to change values of the offset registers every clock cycle. The control logic operation can be summarized as follows:

1) To execute diagonal direction access, (OFY, OFX) is added by (DY, DX), where (DY, DX) is either (+1, −1) or (−1, +1).
2) In the top and the bottom boundaries of a scan area, (OFY, OFX) is added by (+1, 0) instead of (DY, DX).
3) In the right and the left boundaries of a scan area, (OFY, OFX) is added by (0, +1) instead of (DY, DX).

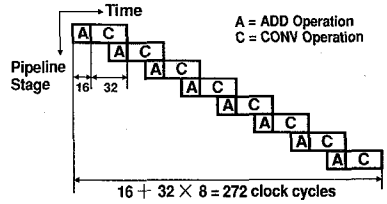

Fig. 10. Timing chart of the 1-dimensional 8 ×8-pixel fast DCT processing.

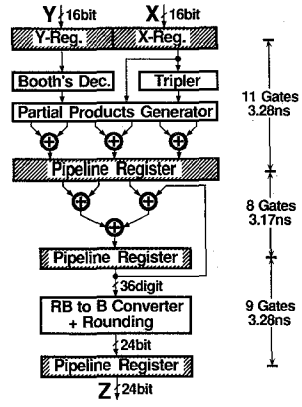

Fig. 11. Block diagram of the 16-b × 16-b redundant-binary convolver.

This control logic has been designed using 4-b adders, 4-b selectors, and 4-b comparators etc. An increasing hardware by expanding a scan area is smaller than that of the table-look-up manner.

V. Pipelined Arithmetic Units

A. Pipelined Arithmetic Logic Unit (PAU)

Fig. 5 shows a block diagram of a 6-stage variable pipelined arithmetic logic unit (PAU). Delay times of pipelined stages are also shown in the figure. The PAU consists of two 16-b shifters (SFT), a 16-b ALU, a 20-b accumulator (ACC), a 16-b barrel shifter (BSFT), a 16-b minimum and maximum value detector (MMD), and a controller (PAU-CTRL). Operations frequently used in video signal processings, such as an ALU operation, accumulation, and absolute difference operation ($|a_i - b_i|$) can be performed within a single clock period. Furthermore, pipelining of the ALU, the ACC and the MMD enables fast processing of moving vector detection based on the CCITT H.261 (searching a minimum and a maximum value among results of $\Sigma|a_i - b_i|$ operation). To efficiently perform vector operations and simplify the SCU, the PAU has its own controller. This controller generates series of control signal patterns for these arithmetic units every clock cycle. Since the controller starts by one cycle period of a decoded signal of a vector instruction, it is easier for the SCU to control the PAU and the PAU can perform more complex vector operations.

Fig. 6 shows a 16-b binary look-ahead carry (BLC) adder developed for the ALU. Here, (p_i, p_j) is a propagation signal, and (g_i, g_j) is a carry generation signal. Since the BLC adder generates carry signals for each bit in a binary tree carry look-ahead manner, the delay time along the critical path is kept within $O(\log_2 n)$. The rate of speed improvement

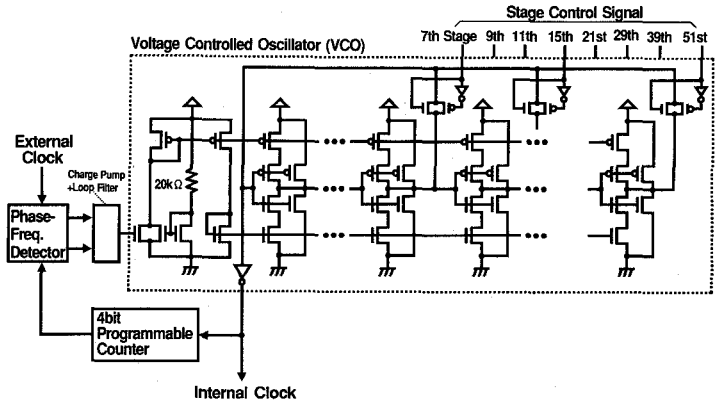

Fig. 12. Circuit diagram of the programmable phase-locked loop (PLL) type clock generator.

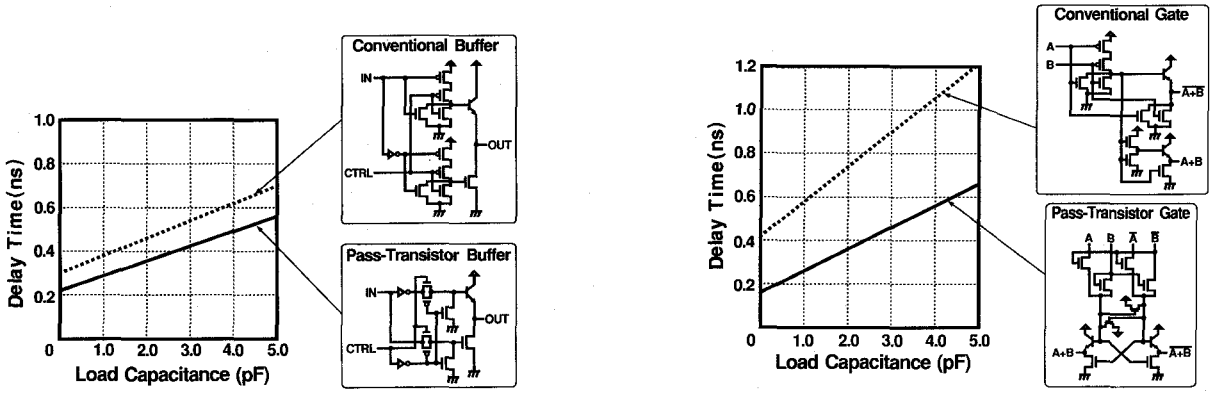

Fig. 13. Calculated delay time versus load capacitance of BinMOS circuits. (a) Tri-state buffers. (b) Logic gates.

accompanying increases in bit length is greater in the BLC adder than in conventional CLA adders. For 16-b addition, the BLC adder is 7% faster than the conventional CLA adder reported in [1].

B. Pipelined Convolver Unit (PCU)

Fig. 7 is a block diagram of a 7-stage variable pipelined convolver unit (PCU). The PCU consists of two 16-b shifters (SFT), a 16-b delay element (DEL) to delay input data for 1 internal clock cycle, a 16-b × 16-b redundant-binary convolver (CONV), a 24-b adder (ADD), a 3-port (2-read + 1-write) 8-word × 24-b × 2-plane register file, a 16-b barrel shifter (BSFT), a 16-b limiter for clipping input data, and a controller (PCU-CTRL) to control complex vector operations. In order to achieve high speed discrete cosine transform (DCT) and inverse DCT (DCT^{-1}) operations, which take up a large portion of processing time in efficient motion picture coding, we have employed a fast DCT algorithm [4]. Fig. 8 shows the signal flow of the 1-dimensional 8-point fast DCT algorithm to be performed by the PCU. X_i and Y_i are pixel data and g_i are intermediate data. A conventional algorithm consisting only of convolution operations would have to perform 8 convolutions to obtain one transformed datum $Y_i(X_i)$ [1]. Therefore, 64 operations would be required to transform 8-point data. On the other hand, the fast algorithm shown here, consisting of an 8-addition stage and a 32-convolution stage, transforms 8-point data in 40 operations, 1.6 times faster.

TABLE III
MAIN FEATURES OF THE VSP3 ULSI

Fabrication technology	0.5-μm BiCMOS triple-level Al
Chip size	16.5 mm × 17.0 mm
Number of transistors	1 267 838 (MOS: 1 259 760 Bip.: 8,078)
Data format	16-b fixed point
Peak performance	1500 MOPS at 300 MHz
Memory capacity	146 kb (Data: 114 kb Inst.: 32 kb)
Power dissipation	13 W at 300 MHz and 3.3-V power supply
Package	280-pin ceramic PGA (Signal: 151 Power: 126)

Figs. 9(a) and (b) indicate data paths for the DCT and the DCT^{-1} implementation, respectively. The register file consists of two 8-word × 24-b registers, a read controller (R-CTR), and a write controller (W-CTR). The R-CTR and the W-CTR generate addresses for reading and for writing, respectively.

DCT operations are performed as shown in Fig. 9(a): 1) pixel data (X_i) are read from the RAM-C and are added by the ADD every two clock cycles; 2) the addition results (intermediate data g_i) are stored in the register file; 3) the intermediate data and coefficient data read from RAM-F are

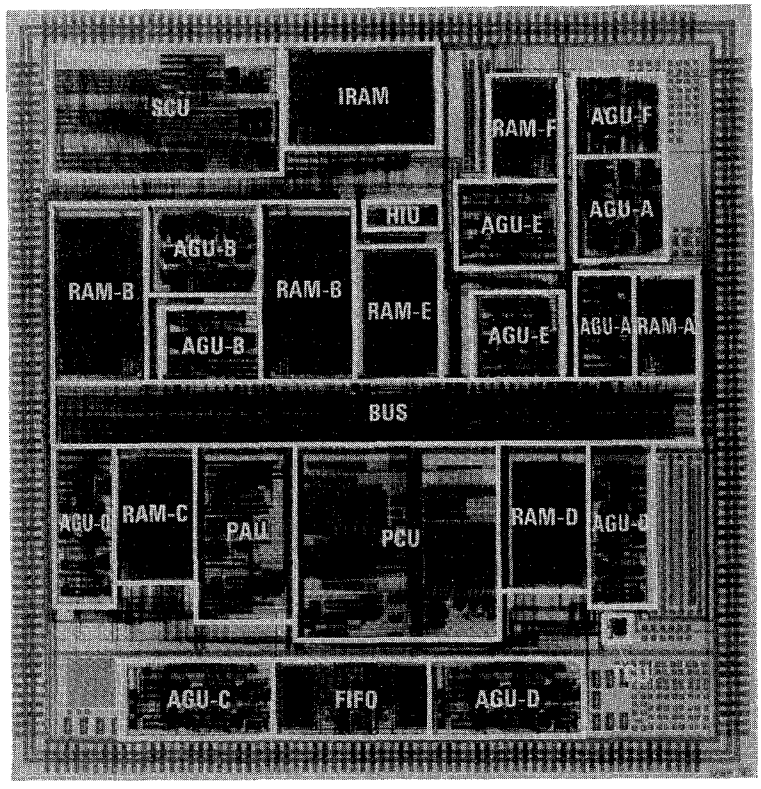

Fig. 14. Chip microphotograph of the VSP3 ULSI.

then multiplied and accumulated to obtain DCT data (Y_i); and 4) the DCT data are then finally stored in the RAM-D. DCT^{-1} operations can be performed by executing inverse operations from Y_i to X_i, as shown in Figs. 8 and 9(b).

In order to perform the fast DCT algorithm efficiently, both the CONV and the ADD are provided in the PCU to simultaneously execute convolution and addition with a register file for storing intermediate data. Fig. 10 shows a timing chart of 1-dimensional 8 × 8-pixel fast DCT processing. Each stage represents a processing time of the 8-point fast DCT algorithm. From Figs. 9(a) and 10, it takes 272 cycles to complete the 1-dimensional processing. Two-dimensional 8 × 8-pixel DCT processing, which can be done by executing Y-directional DCT after executing X-directional DCT, takes 544 clock cycles. On the other hand, the conventional DCT processing takes 1024 cycles. Thus, the fast DCT processing time of 2-dimensional 8-point data is 1.88 times faster than the conventional one.

Fig. 11 shows a block diagram of the CONV. Delay times for pipelined stages are also shown in the figure. The CONV features 1) the third Booth's algorithm which reduces the number of partial products to 6, and 2) the redundant binary (RB) adder with less than one digit carry propagation [1]. The tripler is provided to calculate $3X$, one of partial products generated according to the third-order Booth's algorithm ($\pm 3X, \pm 2X, \pm 1X$, and 0). Here X is multiplicand. The other partial products are generated by the partial products generator shown in Fig. 11. The tripler includes a redundant-binary adder in order to ensure that the $3X(= 4X - X)$ can be obtained within 3.3-ns cycle time. To further improve the CONV performance, we have developed a 37-b BLC adder for the RB to binary (B) converter, which is 1.6 times faster than a blocked carry look-ahead (CLA) adder.

TABLE IV
PROCESSING TIME OF THE VSP3 FOR ONE MACROBLOCK VIDEO DATA BASED ON CCITT H.261 (16 × 16-PIXEL LUMINANCE COMPONENT AND TWO 8 × 8-PIXEL CHROMINANCE COMPONENTS)

Process Time	(μs)
CIF conversion	6.4
Loop filtering	10.9
Interframe difference	1.3
Interframe addition	1.3
Discrete cosine transform	10.9
Inverse DCT	10.9
Quantization	2.6
Inverse Q	2.6
Moving vector detection	9.6

VI. HIGH-SPEED CIRCUITS FOR 300-MHz OPERATION

A. Programmable PLL-Type Clock Generator

To make 300-MHz clock signals from supplied external clock signals, we have developed a programmable PLL-type clock generator. A circuit diagram of the PLL-type clock generator is shown in Fig. 12. To attain a wide oscillating frequency range of a voltage controlled oscillator (VCO) from 50 to 300 MHz, 51 inverter stages in the ring oscillator are separated to eight parts by CMOS switches. Moreover, phase jitter at the frequency of 300 MHz is suppressed down to 6.3% by using a CMOS inverter of which delay time can be controlled by a control voltage, and a conventional CMOS inverter in parallel as one stage of the ring oscillator. For an application to the CCITT H.261 coding algorithm, the VCO

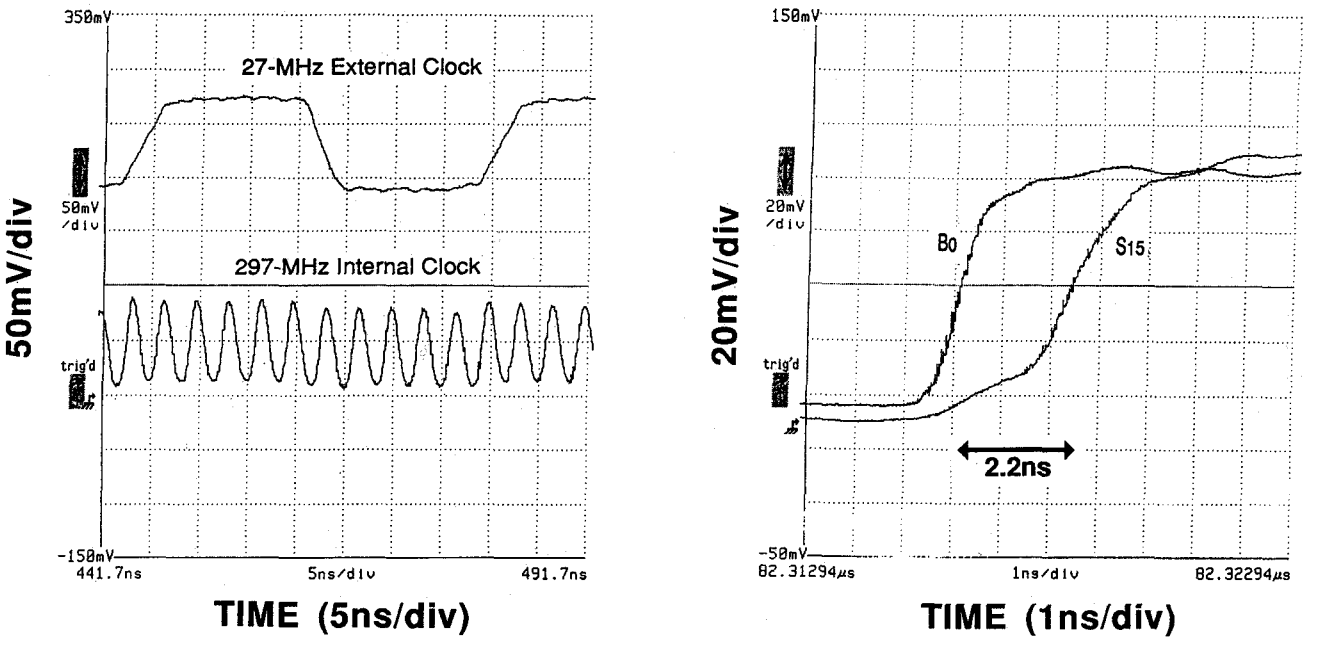

Fig. 15. Input and output measured waveforms. (a) PLL-type clock generator. (b) 16-b BLC adder.

is configured to seven stages to produce a 300-MHz internal clock from a 27.3-MHz external clock.

B. Pass-Transistor Type BinMOS Circuits

Fig. 13(a) shows both newly developed and conventional BinMOS tri-state buffer circuits and their delay times. The developed buffer circuit with a pass-transistor is 1.27 times faster than the conventional circuit at 5-pF load capacitance. This tri-state buffer is used in 300-MHz bus drivers driving large load capacitances.

Fig. 13(b) shows newly developed and conventional BinMOS logic circuits and their delay times. The developed pass-transistor logic circuit is 1.8 times faster than the conventional circuit at 5-pF load capacitance. The pass-transistor circuit can realize arbitral logics such as AND, NAND, exclusive-OR, etc., by changing pass-transistor logic structures [5]. This logic circuit is used in high-speed address decoders of the 300-MHz SRAM's.

VII. Chip Layout and Measurement

The VSP3 was fabricated using 0.5-μm BiCMOS triple-level Al wiring process technology. Fig. 14 is a chip microphotograph where 1.27-million transistors are integrated in a 16.5 $\times$ 17.0-mm^2 die area. The power dissipation is 13 W at 3.3-V power supply and 300-MHz operating frequency. Table III lists the VSP3 main features. Peak performance is 1500 MOPS at 300-MHz internal clock frequency, and internal operating frequency of maximum 300 MHz is generated at 2 to 16 times of external clock frequency. Moreover, an external clock signal can be supplied as an internal clock signal. 126 power supply and ground pads are provided to reduce the switching noise.

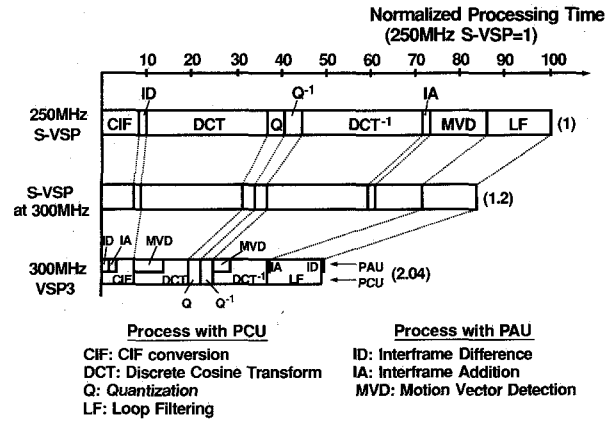

Fig. 16. Simulated performance comparison of the VSP3 with the 250-MHz [1] and the 300-MHz S-VSP.

Each functional block in the VSP3 is driven by a BinMOS balanced tree-structure clock driver to reduce the clock skew. Total load capacitance is 313 pF. Furthermore, signal delay of bus-lines and clock-lines caused by the resistance and capacitance of interconnections is reduced by using second and third-layer Al wirings. The power-line width is determined so that the voltage drop caused by dissipated current will be less than 0.1 V.

Fig. 15(a) shows measured results for the programmable PLL-type clock generator in the VSP3. A 297-MHz internal clock synchronized to 27-MHz external clock has been generated. Fig. 15(b) shows measured result for the 16-bit BLC adder in the ALU. The 15th addition result has been obtained in 2.2 ns.

VIII. Performance

The CCITT H.261 coding algorithm consists of NTSC-to-CIF (common intermediate format) conversion, discrete

cosine transform (DCT), inverse DCT (DCT^{-1}), loop filtering (LF), quantization (Q), and inverse Q (Q^{-1}), which are processed by the PCU, and interframe difference (ID), interframe addition (IA), and moving vector detection (MVD), which are processed by the PAU. The MVD is performed by applying a 3-step motion vector detection method [6] between an 8 × 8-pixel block in a present frame and a 45 × 45-pixel block in a previous frame. The first step selects one motion vector from 29 coarse motion vectors by L1-norm evaluations. Each of the second and the third steps then recursively determines one motion vector from 8 motion vectors in a similar manner, improving the accuracy of the vector. Table IV shows processing times of H.261 coding steps for one macroblock which contains a 16 × 16-pixel luminance component and two 8 × 8-pixel chrominance components. As shown in Section V, the fast DCT processing for one macroblock takes 3264 cycles, which corresponds to 10.9 μs at 300-MHz operating frequency. Fig. 16 shows a VSP3 processing time improvement due to 300-MHz operating frequency and parallel architecture. Compared with the 250-MHz S-VSP [1], the performance is improved by 20% due to 300-MHz operating frequency, and moreover, improved by 70% due to the fast DCT algorithm and parallel processing of the DCT and the MVD, the IA and the CIF, and so on. (The S-VSP serially performs these processes and employs the conventional DCT algorithm.) Thus, in total, the VSP3 is 2.04 times faster than the S-VSP. In order to perform the full-CIF video data coding in realtime, the processing time should be less than 84 μs (= 1/30 s / 396 macroblocks). On the other hand, from Table IV and Fig. 16, the VSP3 processing time of one macroblock is 45 μs. Thus, A single VSP3 has a performance sufficient for coding 30-frame-per-second full-CIF data in real time.

IX. Summary

The 300-MHz 16-b full-programmable, parallel-pipelined video signal processor ULSI has been developed. It features 1.27-million transistors integrated in a 16.5 × 17.0-mm^2 die area with 0.5-μm BiCMOS 3-layer aluminum wiring process technology. The parallel vector processing architecture without resource conflicts, the variable pipelined arithmetic units suited for efficient motion picture coding algorithms, and the two types of pass-transistor BinMOS circuits to achieve 3-ns operation time of the buses and the SRAM's, are newly developed to help achieve the processor performance of 1500-million arithmetic operations per second. The video signal processor is capable of processing motion picture coding based on the CCITT H.261 both in a single chip and in real time.

Acknowledgment

The authors wish to thank the many people involved in developing the video signal processor ULSI for their very valuable cooperation, assistance, and encouragement.

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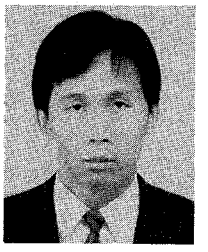

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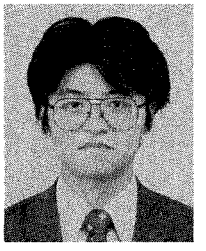
Mr. Inoue is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



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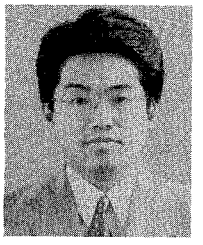

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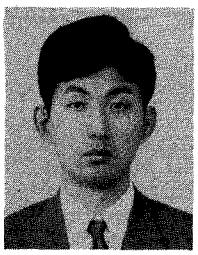

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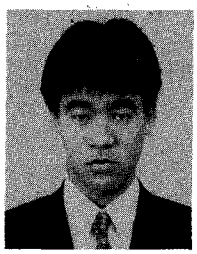

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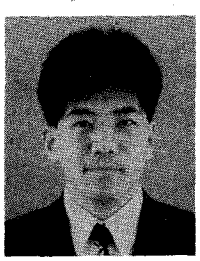

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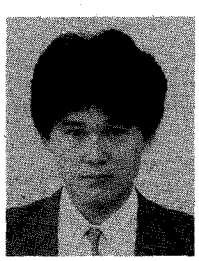

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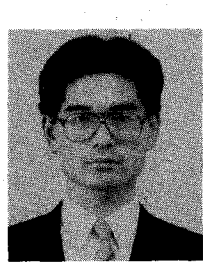

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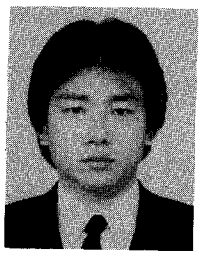

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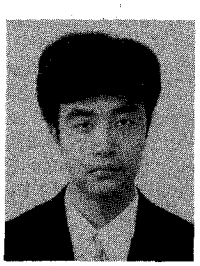
Mr. Horiuchi is a member of the Japan Society of Applied Physics.



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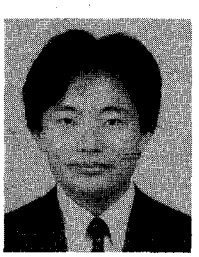

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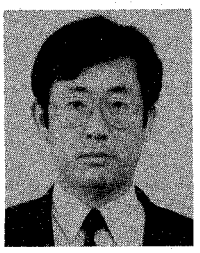

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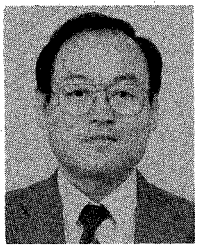

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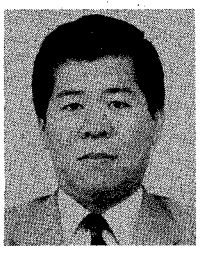

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