Freescale Semiconductor
Product Brief

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MPC8568E Integrated Processor Product Brief

This document provides an overview of features and functionality of the MPC8568E PowerQUICC III™ integrated communications processor. The MPC8568E combines a PowerPC™ processor core with system logic required for networking, telecommunications, and wireless infrastructure applications. The high level of integration helps simplify board design and offers significant bandwidth and performance benefits.

The MPC8568E offers an excellent combination of protocol and interface support including interworking, a high performance PowerPC CPU with a large L2 cache, a DDR memory controller, and high-speed interfaces such as serial RapidIO and PCI Express. This combination of features allows for replacement of separate control and data path processors with a single chip. The new QUICC Engine™ 2.0 block is also incorporated, which provides termination, interworking, and switching between a wide range of communication protocols including ATM, Ethernet, POS, and HDLC. The QUICC Engine block's enhanced interworking eases the transition from ATM to IP-based systems and reduces investment costs.

Contents

1 MPC8568E Overview

This section describes the features of the MPC8568E.

1.1 Block Diagram

Figure 1 shows the major functional units within the MPC8568E.

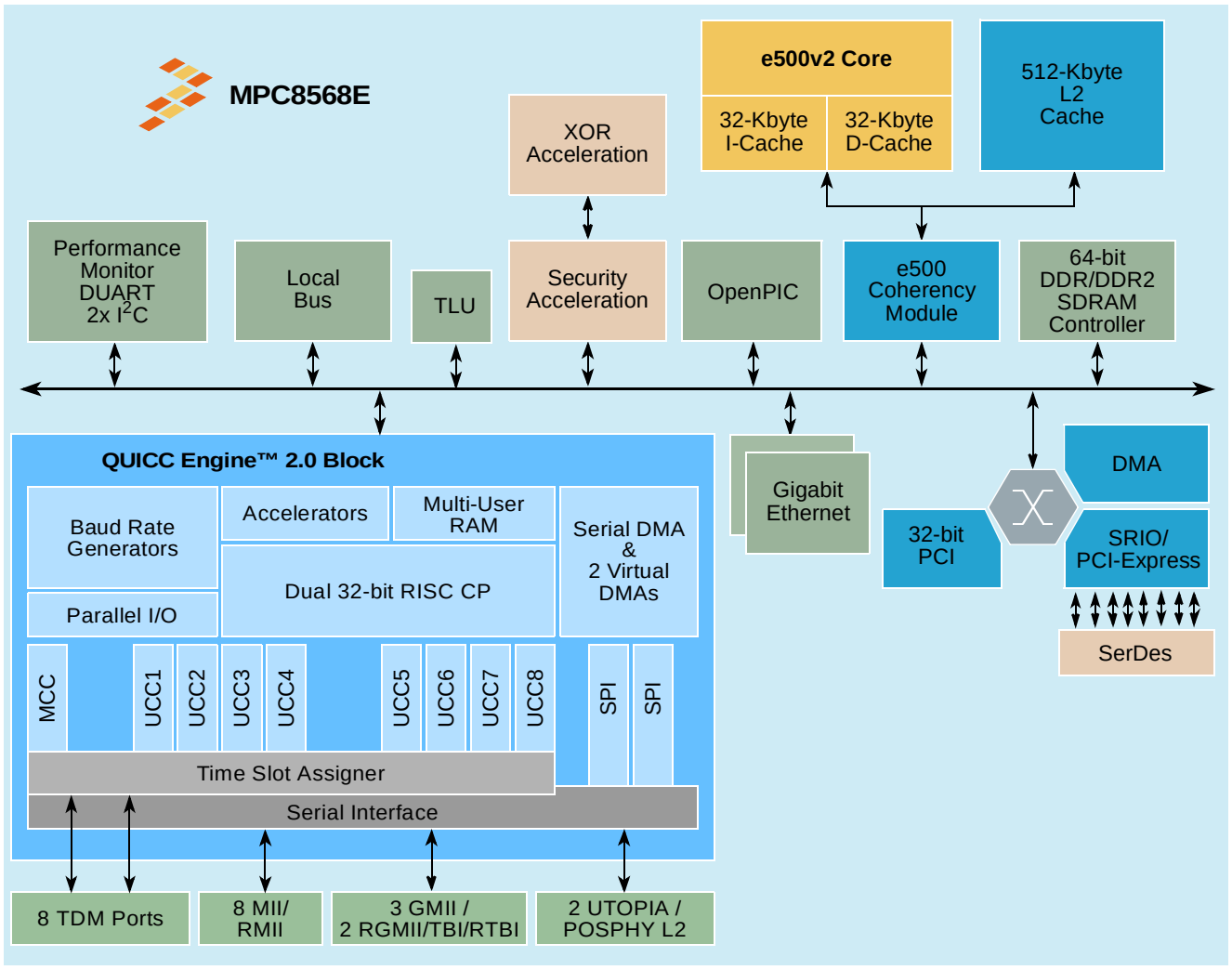

Figure 1. MPC8568E Block Diagram

1.2 Critical Performance Parameters

- Maximum e500v2 core frequency of 1.33 GHz
- Maximum memory bus frequency of 333 MHz for DDR, 533 MHz for DDR2
- Maximum QUICC Engine block frequency of 533 MHz
- Supply voltages:
  - Core: 1.1 V

  - PCI Express, serial RapidIO: 1.1 V
  - Ethernet: 3.3 or 2.5 V (subject to protocol)
  - Local bus: 3.3, 2.5 V, or 1.8 V
  - DDR: 2.5 V for DDR, 1.8 V for DDR2 (conforms to JEDEC standard)
- Operating junction temperature (T_j) range is -45–105 C.
- Package: 1023-pin FC-BGA (flip-chip ball grid array)

1.3 Chip-level Features

Key features of the MPC8568E include:

- High-performance PowerPC e500v2 core with 36-bit physical addressing
- 32-Kbyte level-1 instruction cache and 32-Kbyte level-1 data cache
- 512-Kbyte level-2 cache
- QUICC Engine block supporting Ethernet, ATM, POS, and T1/E1 along with associated interworking
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 SDRAM memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- Either a 1x/4x serial RapidIO or a x4/x2/x1 PCI Express interface (selectable at power on). A x8 PCI Express interface is also available; in this case, due to pin multiplexing limitations, serial RapidIO is not available.
- Programmable interrupt controller (PIC) compliant with Open-PIC standard
- Four-channel DMA controller
- Two I^2C controllers
- DUART
- Local bus controller (LBC)
- Eight general-purpose I/O signals

These features are described in greater detail in subsequent sections.

NOTE

The MPC8568E is also available without a security engine, in a configuration known as the MPC8568. All specifications other than those relating to security apply to the MPC8568 exactly as described in this document.

2 MPC8568E Application Examples

The following section provides block diagrams of different MPC8568E applications. The MPC8568E is a very flexible device and can be configured to meet many system application needs.

2.1 Base Station Network Interface Card

Figure 2 shows an application using the MPC8568E as a base station network interface card.

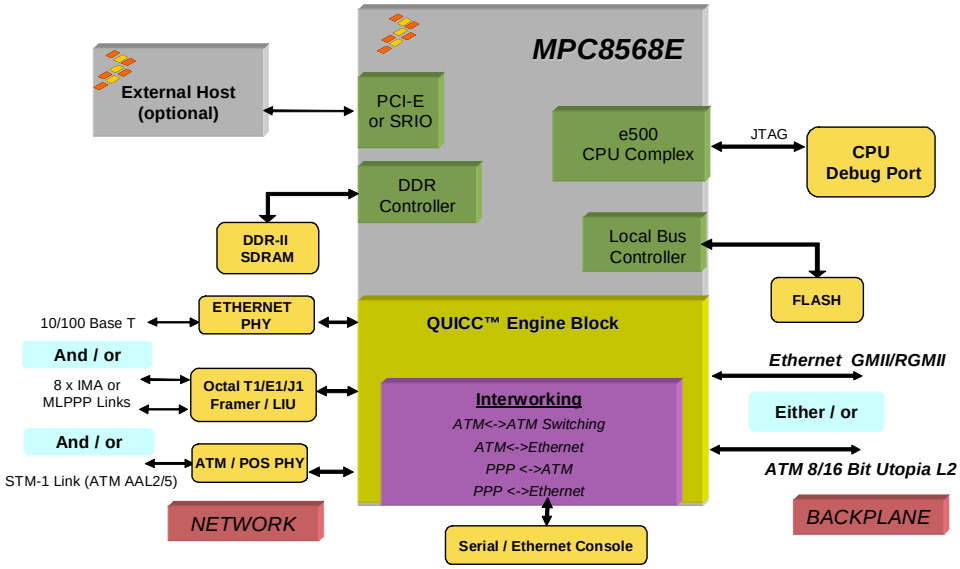

Figure 2. Base Station Network Interface Card Application

The MPC8568E enables glueless connection to an external host processor via PCI Express or serial RapidIO interconnect in applications where a separate processor is used for control processing.

On the network side, the QUICC Engine block is used to carry voice (AAL2), data, and video (AAL5) using ATM or IP over up to eight T1 /E1 TDM links bundled with IMA or MLPP terminated protocols between the Node Bs and the RNC. Using ATM, these links will migrate to higher data rates, such as OC-3/STM-1 (in order to aggregate the traffic of multiple Node Bs), with AAL2 to carry voice, AAL5 for data and AAL1. Alternatively, these links will migrate to 100 Mbps Ethernet.

For high bandwidth interfaces, where the traffic for multiple Node Bs is aggregated, 1xSTM-1 (second STM-1 for redundancy MSP 1+1 protection) interfaces or 100 Mbps Ethernet are more appropriate. This traffic is AAL2 up to 155 Mbps (STM-1) for the lub interface between the RNC and the UTOPIA or Gigabit Ethernet backplane.

In today's wireless solutions, ATM is predominantly also used as the switching layer on the UTOPIA backplane. For future IP ready solutions, alternative backplane concepts such as Ethernet are under consideration. However, ATM to ATM switching (AAL0, 2, 5), Ethernet to ATM switching or bridging with L3/L4 support and PPP inter-working are required.

A variety of physical implementations for the lub and lur interfaces and the back plane is required, making a flexible and programmable solution for the network interface highly desirable. To support the increase

in data plane processing for broadband wireless evolution the QUICC Engine block can be used as an offload engine for layer 2/3/4 processing.

2.2 UMTS Channel Card

Figure 3 shows the MPC8568E used as a UMTS channel card.

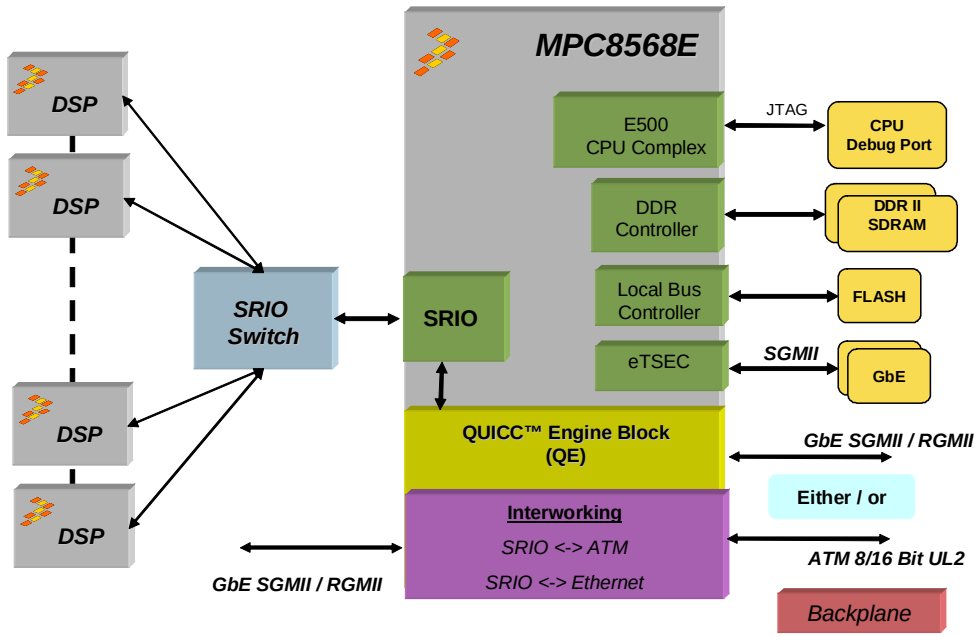

Figure 3. UMTS Channel Card Application

The QUICC Engine block is required for interfacing to data plane processing on the backplane, which includes ATM (for legacy reasons) and gigabit Ethernet (additional gigabit Ethernet port for redundancy) with ~100-120 Mbps sustained user data rate. Another gigabit Ethernet port is required for O&M handling (~800 Mbps with large packets for debug/trace data).

Serial RapidIO is required to interface to next generation DSPs for baseband processing. In addition, the option for serial RapidIO <-> gigabit Ethernet or serial RapidIO <-> ATM interworking off-load functionality on the QUICC engine block for message handling is very desirable for many channel card applications.

3 MPC8568E Architecture Overview

This section contains a high-level view of the MPC8568E architecture.

3.1 e500v2 Core and Memory Unit

The MPC8568E contains a high-performance 32-bit Book E–enhanced e500v2 core that implements the PowerPC architecture. In addition to 36-bit physical addressing, this version of the e500 core includes:

- Double-precision floating-point APU provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.

- Embedded vector and scalar single-precision floating-point APUs provide an instruction set for single-precision (32-bit) floating-point instructions.
- 32-Kbyte level-1 instruction cache and 32-Kbyte level-1 data cache with parity protection

The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.
  - Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

3.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500v2 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8568E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by ten local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8568E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8568E to be part of larger address maps such as the PCI or PCI Express 64-bit address environment and the RapidIO environment.

3.3 QUICC Engine Block

- Includes support for the following serial interfaces:
  - Two UL2/POS-PHY interfaces with 124 Multi-PHY addresses on UTOPIA and 31 Multi-PHY addresses on the POS interface
  - Three 1-Gbps Ethernet interfaces using GMII
    or Two 1-Gbps Ethernet interfaces using RGMII, TBI, or RTBI
  - Up to eight 10/100-Mbps Ethernet interfaces using MII or RMII
  - Up to eight T1/E1/J1/E3 or DS-3 serial interfaces
  - Dual UART, I^2C and SPI interfaces
- Includes support for the following protocols:

  - ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
  - ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
  - IMA and ATM Transmission convergence sub-layer
  - ATM OAM handling features compatible with ITU-T I.610
  - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
  - IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
  - ATM (AAL2/AAL5) to Ethernet (IP) interworking
  - Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
  - 256 channels of HDLC/Transparent or 128 channels of SS#7
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data

3.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8568E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Compatible with code written for the Freescale MPC8548E, MPC8555E, and MPC8541E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  - PKEU—public key execution unit
  - DEU—Data Encryption Standard execution unit
  - AESU—Advanced Encryption Standard unit
  - AFEU—ARC four execution unit
  - MDEU—message digest execution unit
  - KEU—Kasumi execution unit
  - RNG—Random number generator

3.5 Enhanced Three-Speed Ethernet Controllers

The MPC8568E has two on-chip enhanced three-speed Ethernet controllers (eTSECs). The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

The MPC8568E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with IEEE Std. 802.3™, 802.3u, 802.3x, 802.3z, 802.3ac, 802.3ab.

The buffer descriptors are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

Some of the key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 1. Supported eTSEC Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

NOTES:
1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):

  - IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std. 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

3.6 DDR SDRAM Controller

The MPC8568E supports DDR and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities from 64 Mbits to 4 Gbits. Four chip select signals support up to four banks of memory. The MPC8568E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes ($\overline{\text{MDM}}$[0:8]) are used to provide byte selection for memory bank writes.

The MPC8568E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8568E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8568E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The MPC8568E offers both hardware and software options to support battery-backed main memory. In addition, the DDR controller offers an initialization bypass feature which system designers may use to prevent re-initialization of main memory during system power-on following abnormal shutdown.

3.7 Table Lookup Unit (TLU)

The table lookup units (TLU) give access to application-defined routing topology, control, and statistics tables in external memory. Each TLU accesses external memory arrays attached either to the device DDR/DDR2 memory controller or to the enhanced local bus controller (eLBC). The cores and the TLUs communicate through messages passed among the memory-mapped configuration and status registers of each TLU. Each TLU uses a 64-bit wide data path for such register accesses.

The TLUs support several types of table lookup algorithms and provide resources for efficient generation of table entry addresses in memory, hash generation of addresses, and binary table searching algorithms for both exact-match and longest-prefix match strategies. Each TLU has 32 physical tables, PTBL[0–31],

each with an associated configuration register containing a physical table with a base table address configured by software.

3.8 PCI Controller

The MPC8568E supports one 32-bit PCI controller, which supports speeds of up to 66 MHz. Other features include:

- Compatible with the *PCI Local Bus Specification, Revision 2.2*, supporting 32- and 64-bit addressing
- Can function as host or agent bridge interface
- As a master, supports read and write operations to PCI memory space, PCI I/O space, and PCI configuration space
- Can generate PCI special-cycle and interrupt-acknowledge commands. As a target, it supports read and write operations to system memory as well as configuration accesses.
- Supports PCI-to-memory and memory-to-PCI streaming, memory prefetching of PCI read accesses, and posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible with selectable hardware-enforced coherency

3.9 High Speed I/O Interfaces

The MPC8568E supports two high-speed I/O interface standards: serial RapidIO and PCI Express. Due to pin multiplexing, however, if the user wishes to use x8 PCI Express, serial RapidIO is not available; otherwise, one 4x/1x serial RapidIO interface and one x4/x2/x1 PCI Express interface may be used simultaneously, provided that they use the same clock rate. Note that the serial RapidIO link can be either 1 or 4 bits wide, but cannot function as four 1-bit links.

3.9.1 Serial RapidIO

The serial RapidIO interface is based on the *RapidIO Interconnect Specification, Revision 1.2*. RapidIO is a high-performance, point-to-point, low-pin-count, packet-switched system-level interconnect that can be used in a variety of applications as an open standard. The RapidIO architecture has a rich variety of features including high data bandwidth, low-latency capability, and support for high-performance I/O devices, as well as support for message-passing and software-managed programming models. Key features of the serial RapidIO interface unit include:

- Support for *RapidIO Interconnect Specification, Revision 1.2* (all transaction flows and priorities)
- Both 1x and 4x LP-serial link interfaces, with transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
- Auto detection of 1x or 4x mode operation during port initialization
- 34-bit addressing and up to 256-byte data payload
- Receiver-controlled flow control
- Support for RapidIO error injection
- Internal LP-serial and application interface-level loopback modes

The RapidIO messaging unit supports two inbox/outbox mailboxes (queues) for data and one doorbell message structure. Both chaining and direct modes are provided for the outbox, and messages can hold up to 16 packets of 256 bytes, or a total of 4 Kbytes.

3.9.2 PCI Express Interface

The MPC8568E supports a PCI Express interface compliant with the *PCI Express Base Specification Revision 1.0a*. It is configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a 2.5-Gbaud data rate per lane. The theoretical unidirectional peak bandwidth is 8 Gbps. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 16 Gbps.

Other features of the PCI Express interface include:

- x8, x4, x2, and x1 link widths supported (Operating PCI Express in x8 link width mode prevents serial RapidIO operation.)
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

3.10 Programmable Interrupt Controller (PIC)

The MPC8568E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

3.11 DMA, I^2C, DUART, and Local Bus Controller

The MPC8568E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.
- To handle misaligned transfers as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. Both the transmitter and receiver support 16-byte FIFOs.

The MPC8568E local bus controller (LBC) port allows connection with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine

(GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at up to 166 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Supports zero-bus-turnaround (ZBT) RAM

3.12 Device Boot Locations

The MPC8568E may be configured to boot using one of the following interfaces:

- the DDR/DDR2 memory controller
- the serial RapidIO interface
- the PCI Express interface
- the local bus interface (via the GPCM)
- the I2C boot sequencer (I2C controller1)

3.13 Power Management

In addition to low-voltage operation and dynamic power management, which automatically minimizes power consumption of blocks when they are idle, four power consumption modes are supported: full on, doze, nap, and sleep.

3.14 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

4 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and the Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

4.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e500v2 PowerPC core.

4.2 Modular Development System (MDS)

Freescale provides an MDS board as a reference platform and programming development environment for the MPC8568E with a complete Linux board support package. The MDS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

4.3 Modular Software Building Blocks

The QUICC Engine block will be supported by a complete set of configurable device API drivers and initialization software. Table 2 shows the wealth of software protocols that the QUICC Engine block with the e500v2 PowerPC™ core supports.

Protocols • ATM AAL 0/1/2/5 • IMA over TDM/UTOPIA/Channelized • Serial ATM (ATM TC sublayer) • 10/100/1000 Ethernet and VLAN • Multi-ink PPP, Multi-Class PPP, PPP-Mux • HDLC • BISYNC • SS7 • Ethernet in the First Mile (EFM) • IP Header Compression	**Classification and Transformation** • Parsing for multi-field classification • Hierarchical lookups • Tables: Hash, Index, CAM Emulation, LPM • Flexible header manipulation
Interworking and Switching • ATM-to-TDM Interworking for AAL0/AAL1 • AAL2 CPS Switching • ATM to Ethernet Interworking • Ethernet to Ethernet Interworking • L2 Fast Ethernet Switch • PPP to Ethernet Switch • PPP to ATM Interworking • Enhanced Multi-Service Platform (EMSP)	**Quality of Service** • Ethernet / IP: – Combined strict priority and WFQ scheduling – Rate limiting / sharing – Lossless flow control – WRED • ATM Traffic Management – TM 4.1 UBR, CBR, GFR, VBR – Per-flow ATM scheduler for 64K VCs – Hierarchical frame and cell based scheduling – Policing – Congestion Control

Table 2. Standard QUICC Engine Block Supported Protocols, Royalty and NRE Free

5 Document Revision History

Table 3 provides a revision history for this product brief.

Table 3. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	09/06	Initial public release

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