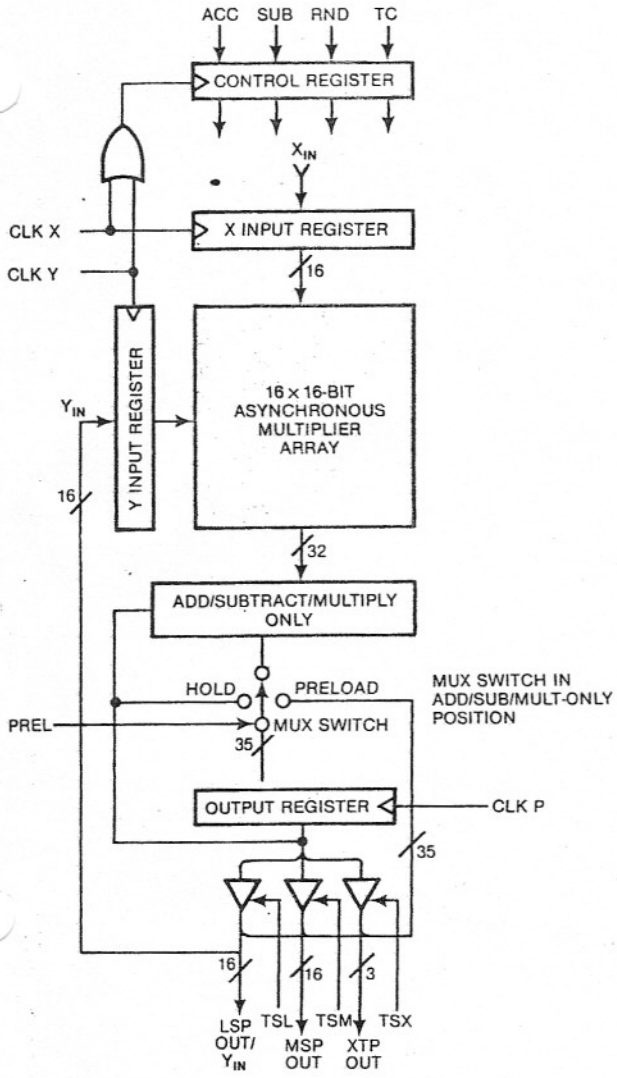

Fig 16—A Preload Control (PREL) line *in TRW/LSI Products' TDC1010J multiplier/accumulator turns off all output 3-state buffers when its value is ONE. With TSL, TSM and TSX also in the same state for the normal setup time before CLK P, any data put on the output lines from an external source gets loaded directly into the output register on the rising edge of CLK P. If either TSL, TSM or TSX is a ZERO, the corresponding LSP, MSP, or XTP bits of the output register are placed in a Hold state.*