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M320C50

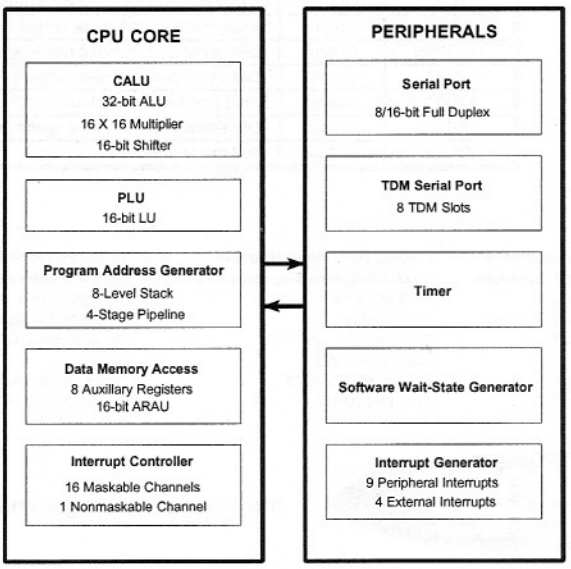
DIGITAL SIGNAL PROCESSOR

OVERVIEW

The M320C50 is a high-performance 16-bit digital signal processor with separate data and program memory. The central ALU has a 32-bit arithmetic logic unit, a 16-bit scaling shifter, and a 16 x 16 parallel multiplier. A separate parallel logic unit performs bit manipulations on any data memory location or control/status register. It uses a four stage instruction pipeline for speed of operation.

Peripherals are controlled through 28 memory-mapped registers and include: a timer, a serial port, a time-division-multiplexed serial port, a programmable wait-state generator, an interrupt controller and the I/O ports, 16 of which are memory mapped.

BLOCK DIAGRAM



KEY FEATURES

- Software compatible with the TI 320C50, 320C51, 320C52 and 320C53
- 32-bit ALU/accumulator
- 16-bit parallel logic unit
- Up to 64K words each of program memory and data memory
- 64K I/O space
- Instruction times fully compatible with industry standard 320C50
- Two circular buffers
- Interrupt controller
- TDM serial port
- Programmable wait-state generator
- Fully synthesizable

DELIVERABLES

- Verilog & VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test benches
- Reference technology netlist

SOFT CORES

MEMORY PROVISION

The M320C50 contains no RAM or ROM but provides functional interconnect signals for connecting three dual-port RAM blocks (two 512x16, one 32x16); a program RAM or ROM block of up to 32Kx16 and up to 16 single-port data RAM blocks up to a total of 32Kx16.

PROGRAM MEMORY: The M320C50 supports up to 64K words of program memory, which can be formed from a combination of up to 32K words of internal (on-chip) program memory, internal single-port RAM, and external program memory. In addition, a 256x16 block of internal data RAM may be configured as program memory.

DATA MEMORY: The M320C50 supports up to 64K words of data memory, which can be formed from a combination of up to 32K words of internal dual-port and single-port RAM, and external data memory.

The external data memory can be of three types: 'Loc al'; I/O selected; and 'Global'. Local memory is exclusive to the M320C50 but Global memory can be shared with other devices, allowing cooperative processing with other digital signal processors.

DESIGN FEATURES

CLOCK: The M320C50 uses a single clock input which is divided by two internally to provide the instruction cycle clock. There is no divide-by-one mode.

INTERNAL MEMORY SIZE: The size of the internal program memory and internal single-port RAM are configurable, in units of 1K words, up to a maximum of 32K words each. The size of the individual RAM blocks used to form the single-port RAM is also configurable.

POWER-DOWN MODES: The M320C50 supports two power-down modes; a power-down of the core CPU only (leaving peripherals running), and a complete power-down of the core CPU and peripherals. A CPU Core power-down can be exited by any interrupt. A complete power-down mode can be exited by an external interrupt.

REFERENCE TECHNOLOGY GATE COUNT: 40000

SIGNAL DESCRIPTION

The M320C50 has 55 DSP inputs and 79 DSP outputs, plus 238 functional interconnect signals that allow the end user to choose the appropriate memory blocks for each implementation and to configure internal program memory as RAM.

DSP INPUTS		
SIGNAL	**TYPE**	**DESCRIPTION**
AI[14:0]	Input	Address bus inputs, used during DMA
DI[15:0]	Input	Data bus inputs
READY	Input	Data ready
NHOLD	Input	Hold state select
RNWI	Input	Data bus direction indicator for DMA cycles
NBIO	Input	Branch control
NRS	Input	Reset
NCLKI	Input	Clock input = twice the instruction cycle rate
MPNMC	Input	Mode select
NBRI	Input	Bus request
NSTRBI	Input	Read or write single-port RAM during DMA
NNMI	Input	Non-maskable interrupt
NINT[4:1]	Input	Four external, maskable, interrupts
CLKR(XI)	Input	Serial port receive(transmit) clock
TCLKR(XI)	Input	TDM serial port receive(transmit) clock
DR(TDR)	Input	Serial port (TDM serial port) receive data input
FSR(XI)	Input	Serial port receive(transmit) frame synch
TFSR(XI)	Input	TDM port receive(transmit) frame/addr synch
DSP OUTPUTS		
OA[15:0]	Output	Address bus
IOD[15:0]	Output	Internal memory write data bus
OD[15:0]	Output	External write data bus
NDEN	Output	Data bus 3-state enable
NDS, NRS	Output	Data memory/Program memory select
NIS	Output	I/O select
RNWO	Output	Data bus direction indicator for external bus
NSTRBO	Output	External bus cycle strobe
NRD, NWR	Output	External memory read/write cycle indicator
NBR	Output	Bus request to access global memory
NIAQ	Output	Instruction acquisition
NHLDA	Output	Hold acknowledge
NIACK	Output	Interrupt acknowledge
XF	Output	External flag output
CLKO	Output	Instruction cycle clock output
NHOE	Output	3-state enable control signal
TOUT	Output	Timer output
DX	Output	Serial port transmit data output (+Enable)
TDX	Output	TDM serial port transmit data output (+Enable)
CLKXO	Output	Serial port transmit clock output (+Enable)
TCLKXO	Output	TDM serial port transmit clock output (+Enable)
TADD	Output	TDM serial port address output (+Enable)
FSXO	Output	Serial port frame synch output (+Enable)
TFSXO	Output	TDM serial port TX frame synch (+Enable)
IDLE2	Output	Idle2 mode indicator

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