

FUJITSU

# ADAPTIVE FILTER PROCESSOR

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## ADVANCE INFORMATION

### FEATURES

LEAST-MEAN-SQUARES ADAPTIVE FIR FILTER

FIXED COEFFICIENT FIR AND IIR FILTERS

MULTICHANNEL OPERATION

PARALLEL FILTER IMPLEMENTATION

CASCADEABLE TO PROVIDE INCREASED SYSTEM  
THROUGHPUT, HIGHER FILTER ORDERS, OR BOTH  
SIMULTANEOUSLY

POLYPHASE INTERPOLATOR/DECIMATOR

SUPPORTED BY A MENU DRIVEN DESIGN AND DE-  
VELOPMENT TOOL

16 bit x 16 bit multiplier = 26 bit product

32 bit accumulation

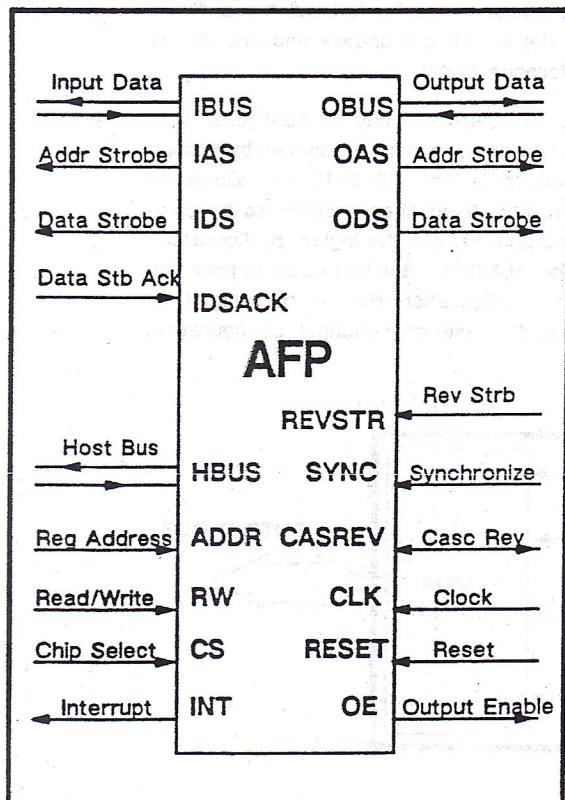
16 bit x 256 words of data RAM for FIR

24 bit x 256 words of coefficient RAM for FIR

24 bit x 256 words of data RAM for IIR

16 bit x 256 words of coefficient RAM for IIR

### PIN ASSIGNMENTS



AUGUST 1987

### INTRODUCTION

The MB86975 ADAPTIVE FILTER PROCESSOR (AFP) is a digital signal processing VLSI integrated circuit capable of implementing fixed coefficient FIR digital filters, IIR digital filters, and adaptive FIR digital filters using the least-mean-squares (LMS) technique. The MB86975 is designed to operate in a bus attached environment. A host processor provides the configuration data which determines the type and characteristics of the digital filter to be implemented. In addition to the host processor control bus, the AFP has separate data busses for the input and output data streams. The multiple bus configuration simplifies the use of the MB86975 in typical signal-flow applications. The MB86975 multiple bus signaling protocols allow the input and output data busses to interface with data conversion devices of varying performance.

The MB86975 supports a multichannel mode. This mode allows a single AFP to implement up to 32 independent digital filters. The input data stream can be independent and unique to each of the multichannel digital filters. Alternatively, the same data stream can be the input to groups of the filter channels. At the output, groups of channels may be summed together.

Multiple MB86975s may be connected in cascade. These devices may be operated as a cascade of multiple independent filter sections. Alternately, a single filter may be distributed across multiple intercommunicating devices. For a distributed filter, the number of AFPs used is a trade off between the component count and the throughput.

The MB86975 is fully supported by a high level, interactive software design tool. The support tool runs on IBM XT/AT computers. It provides a complete design, analysis, and implementation facility for digital filter development.

## GENERAL DESCRIPTION

The MB86975 Adaptive Filter Processor (AFP) is a digital signal processing component designed to implement FIR and IIR digital filters. The MB86975 integrates the storage, sequencing, control, and address computation resources required to implement fixed coefficient FIR filters, least - mean - squared adaptive FIR filters and fixed coefficient IIR filters. Figure 1 shows the top level organization of the MB86975.

The MB86975 can be configured to implement either fixed or adaptive filters. Fixed filters may be either the FIR type or the IIR type. In the fixed FIR case the filters are simple direct-form realizations. Each channel consists of a single unique filter. In the fixed IIR case the filters are implemented as cascaded second-order(biquad) sections. A single MB86975 can structure a channel as one to eight cascaded biquads.

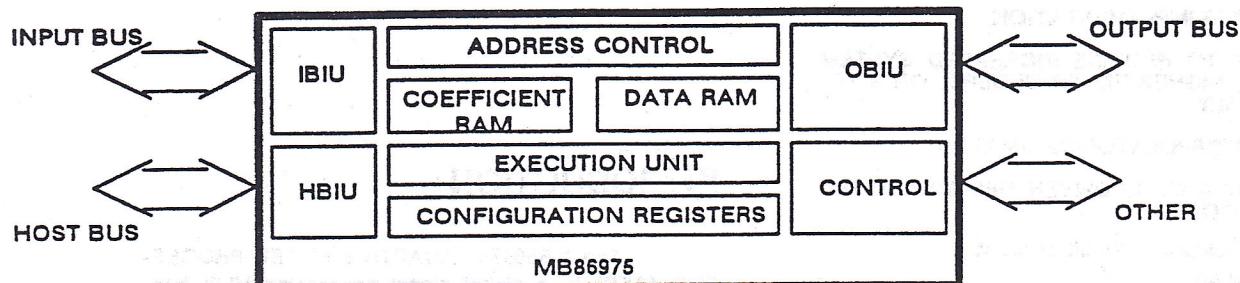


FIGURE 1

The MB86975 is designed for use in bus-attached environments in which a host microprocessor provides configuration and control information and monitors device operation. The communication between the host microprocessor and the MB86975 is through the HOST BUS.

A single MB86975 may be configured to process from 1 to 32 independent channels of signal data. Multichannel operation is achieved through time multiplexing of the signals onto the INPUT BUS, the complementary demultiplexing of the signals from the OUTPUT BUS, and the segmentation of the internal data and coefficient storage. Operationally, each channel processes a unique data stream through the MB86975. All channels share a common filter type and length (number of taps) but have separate coefficients. The basic multichannel model is shown in figure 2.

The MB86975 supports adaptive filtering applications. This is achieved through the internal execution of the LMS algorithm. The algorithm is completely self contained. The designer need only input the  $\mu$  factor which controls the coefficient update and provide the appropriate reference signal.

Fixed filter channels may be configured such that a single data stream may be processed by multiple parallel filter sections. The MB86975 also allows the outputs from multiple fixed filter sections to be combined. Figure 3 summarizes the logical configurations supported by the MB86975. It is important to note that the only logical configuration that is meaningful for adaptive filters is the basic multichannel configuration.

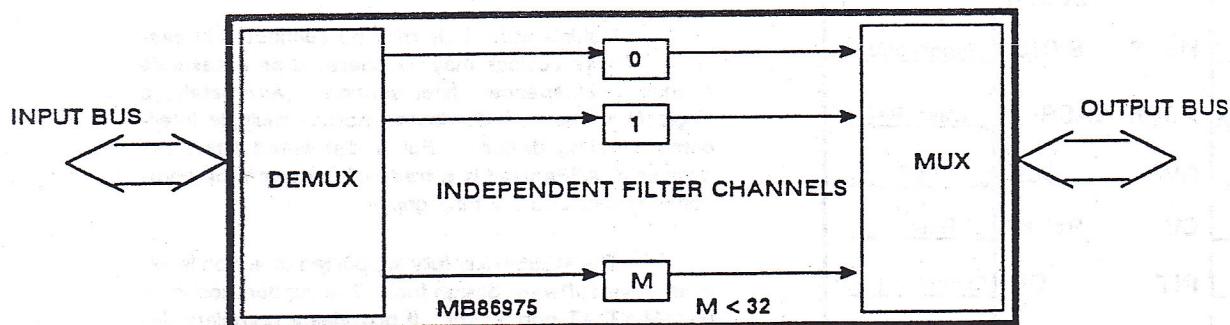


FIGURE 2

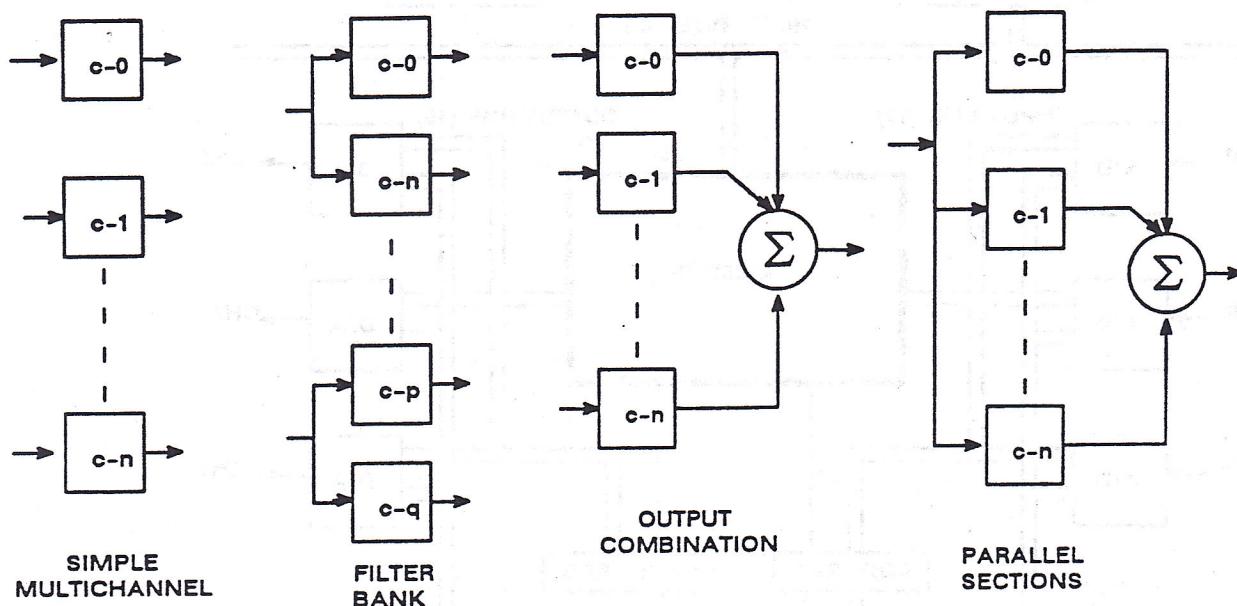


FIGURE 3 SINGLE MB86975 MULTICHANNEL CONFIGURATIONS

The multichannel parallel/combine capability of the MB86975 directly supports the implementation of polyphase interpolators and decimators. These configurations require each filter phase to be a separate channel.

The MB86975 includes three independent bus interfaces. One bus provides the interface to the host processor. The other two, the input bus and the output bus, provide the conduit by which the digital signal data enter and exit the MB86975. The separation of the input and output busses simplifies and optimizes the use of the MB86975 in signal-flow configurations. When multiple MB86975s are connected in cascade separate interchip-connection busses minimize the interconnection overhead.

The MB86975 supports direct connection of data conversion devices to the input bus and output bus. Multiple bus signaling protocols are provided to allow the use of converters which span a wide range of performance. In each performance class the appropriate bus-interface protocol allows for a minimum hardware implementation of the bus interface. Figure 4 shows the MB86975 system configuration.

Greater system throughput, higher filter orders, or both simultaneously, can be achieved by cascade connection of multiple MB86975 devices. Figures 5, 6, and 7 show the basic configurations for cascading AFP's. Note that cascade connected devices can implement filter configurations of two different types: cascaded filters or distributed filters.

In cascaded filters configuration (figure 5), each AFP operates independently of the other units in the cascade chain. Each AFP implements one or more autonomous filters sections. The response of this filter channel(s) is the composition of the responses of the individual filters sections. Synchronization of cascaded filters configurations must be externally controlled. In situations where the individual devices are configured with the same number of channels and the same filter orders, a simple, common start signal provides global system synchronization. Note that in this mode of operation, processing in the individual AFPs is fully overlapped. In IIR mode, the only cascade configuration allowed is cascaded filters.

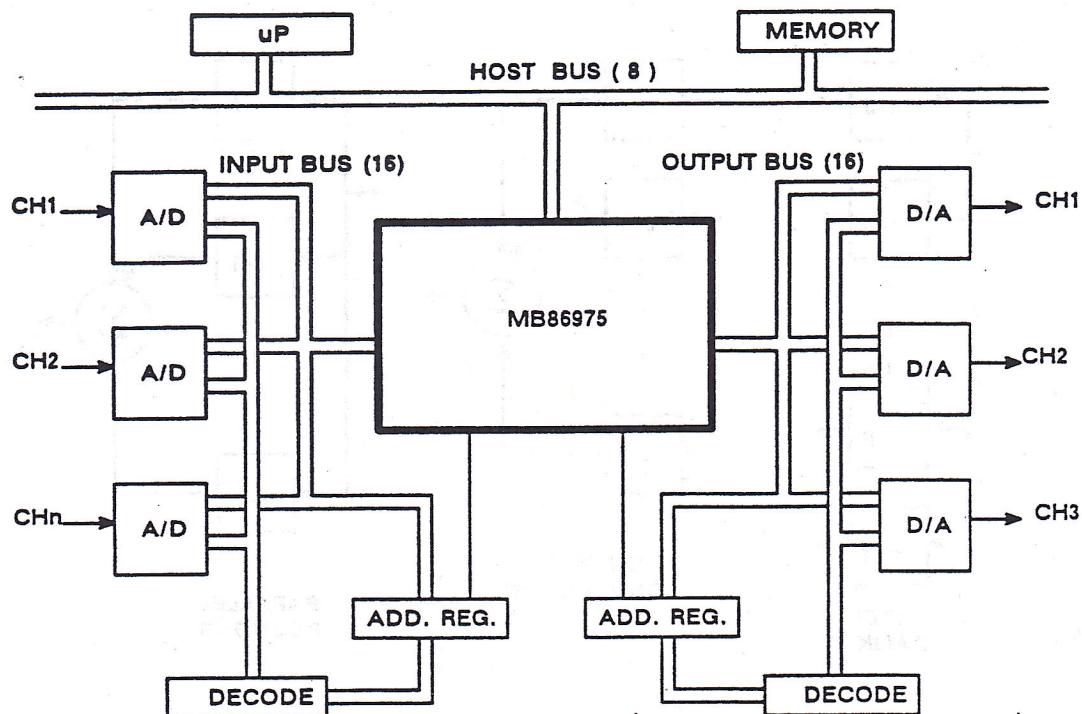


FIGURE 4 MB86975 SYSTEM CONFIGURATION

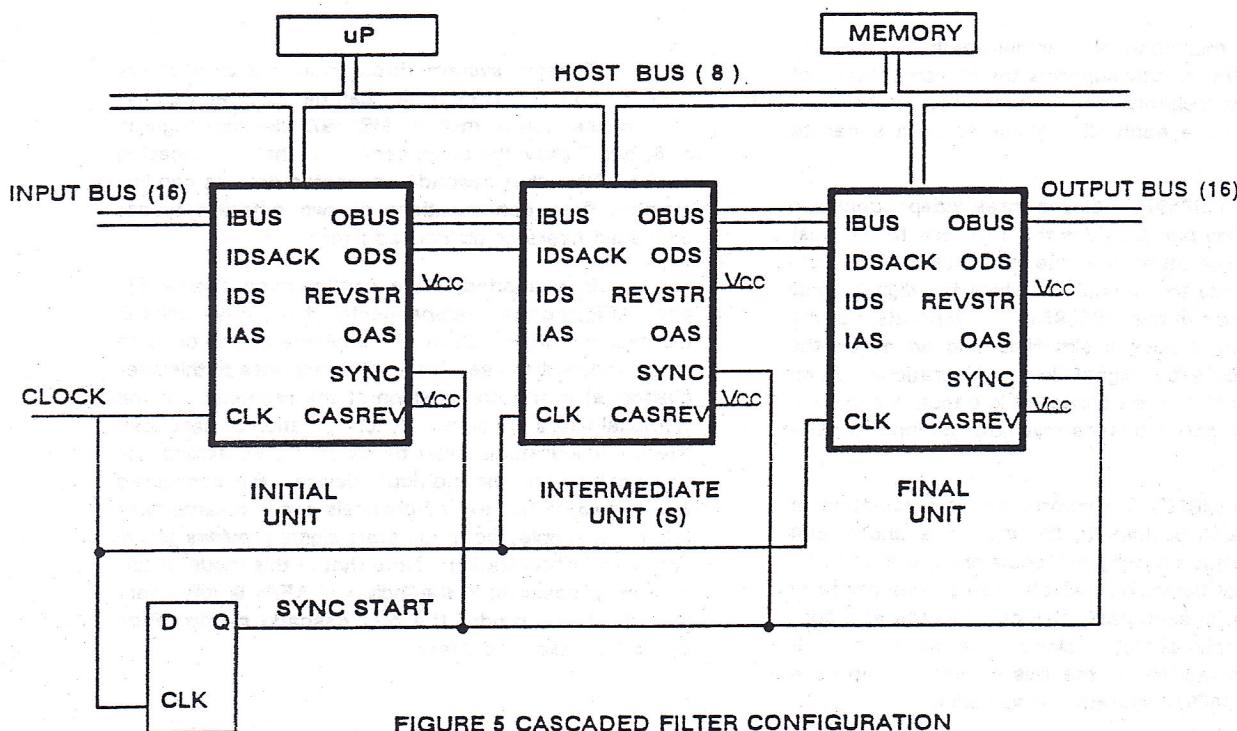


FIGURE 5 CASCADED FILTER CONFIGURATION

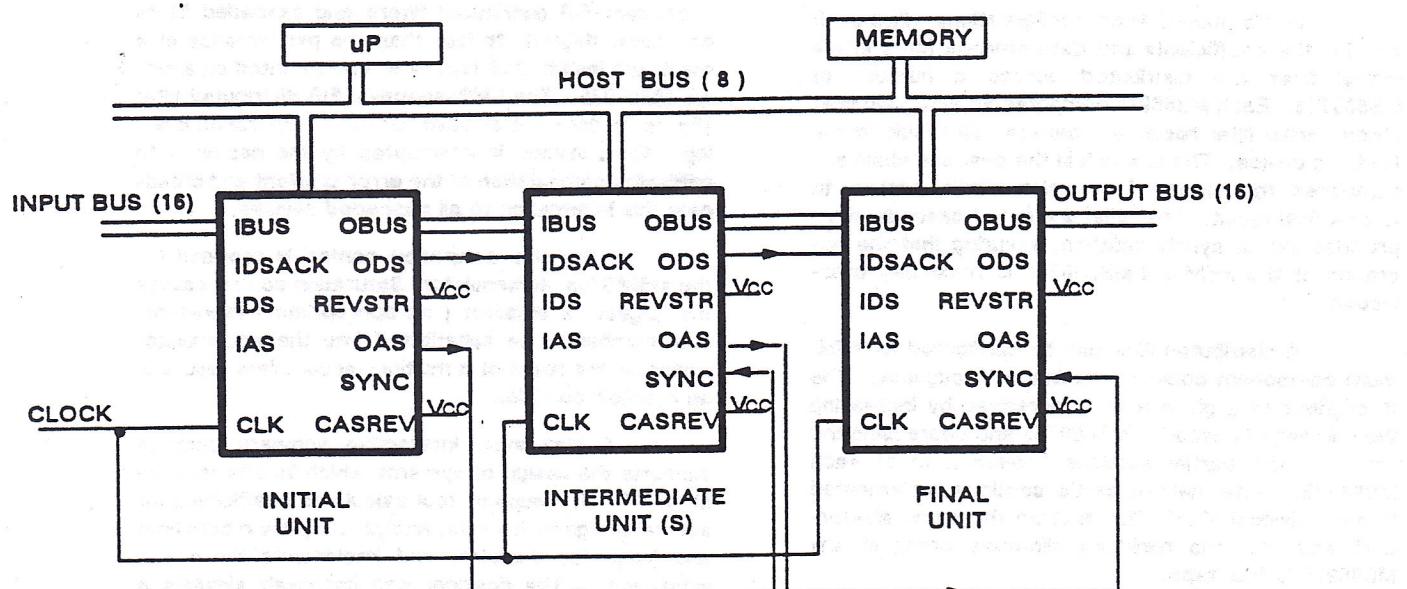


FIGURE 6 FIR DISTRIBUTED FILTER CONFIGURATION

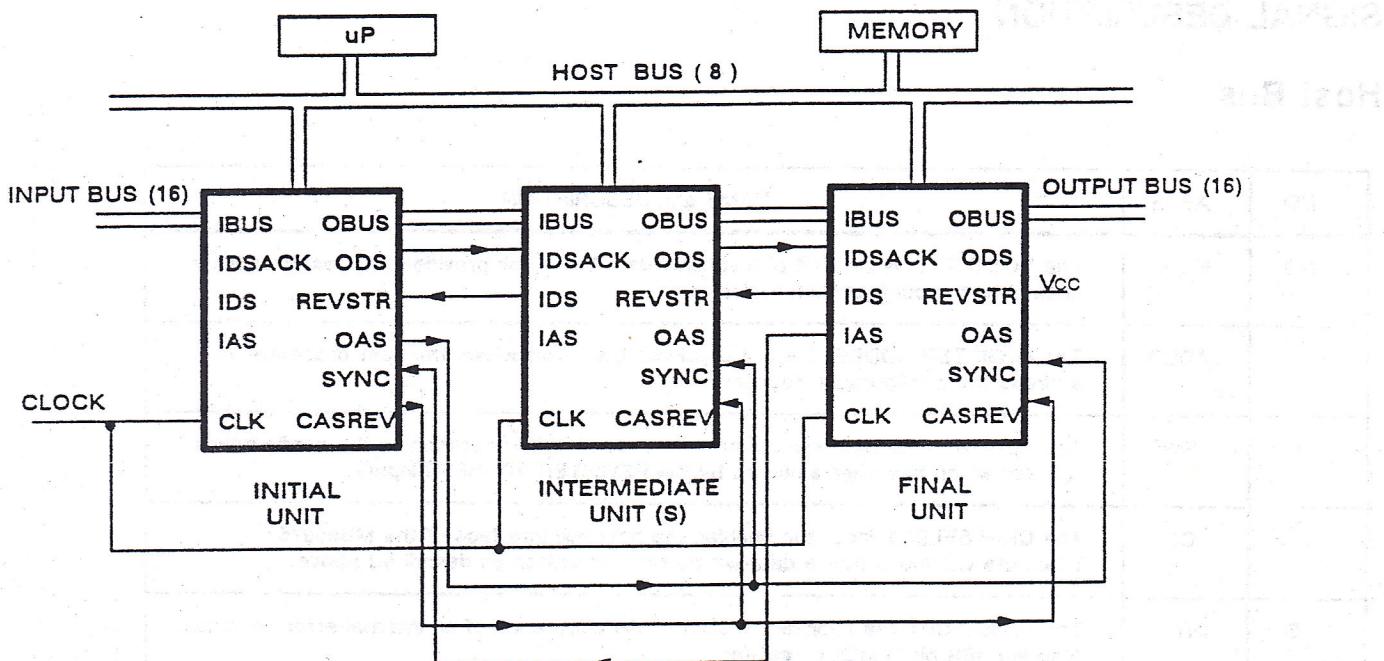


FIGURE 7 LMS DISTRIBUTED FILTER CONFIGURATION

In distributed filter configurations (figures 6 and 7), the coefficients and data storage for a single logical filter are distributed across a number of MB86975s. Each MB86975 computes an extended precision partial filter result and passes this result to the following device. The final unit in the cascade chain accumulates the extended precision partial results to form a final result. The initial unit in the cascade chain provides overall synchronization, assuring that the operation of the individual MB86975s is maximally overlapped.

A distributed filter can be configured for minimum component count or maximum throughput. The throughput of a given filter is increased by increasing the number of cascaded MB86975s and decreasing the order of the partial sections implemented in each MB86975. Note that the partial sections implemented in the individual MB86975s must be the same size (order) and that the minimum allowable order in any MB86975 is four taps.

Device operation in a fixed-coefficient-FIR distributed filter (figure 6) is fully overlapped, just as in the cascaded filters situation. Performance of fixed-

coefficient-FIR distributed filters and cascaded filters can never degrade to less than the performance of a maximum length (256 tap) filter implemented on a single MB86975. The LMS-adaptive-FIR distributed filter (figure 7) does not achieve full device operation overlap. Concurrency is interrupted by the necessity to centralize computation of the error gradient and broadcast this information to all cascaded devices.

Selectable saturation control is provided for the MB86975s accumulator. Saturation control causes the largest, or smallest (as appropriate) representable number to be substituted into the accumulator whenever the result of a multiply-accumulate results in an overflow condition.

A high-level, interactive software package supports the design of systems which incorporate the MB86975. The support tool calculates coefficients for several design techniques, analyzes signals in both time and frequency domains, and implements the device simulation. The designer can iteratively simulate a digital filter to quickly determine a suitable set of filter coefficients. The support tool is described in the Fujitsu document, the MB86975 Support Tool.

## SIGNAL DESCRIPTION

### Host Bus

I/O	ABBR.	NAME and DESCRIPTION
I/O	HBUS	The HOST BUS is an 8 bit bidirectional data bus which provides the host processor access to the configuration registers.
I	ADDR	The REGISTER ADDRESS is a 4 bits input line. This allows the host processor to address the configuration registers.
I	RW	The READ/WRITE input selects either a read or write operation to the configuration register which has been selected by the REGISTER ADDRESS inputs.
I	CS	The CHIP SELECT input line enables the host bus interface of the MB86975. When the CS line is active data will be read or written as described above.
O	INT	The INTERRUPT line informs the host of the occurrence of an internal error condition. Also see IER bit in MODE register
I	OE	The output enable line determine whether the AFP will output data or not. When OE is low, the AFP could output data to the Host bus. If OE is high, the AFP would not output data to the Host bus.

## Input Bus

The Input Bus is fully synchronous. All operations are timed by the CLOCK signal.

I/O	ABBR.	NAME and DESCRIPTION											
I/O	IBUS	<p>The IBUS is the channel by which signal-data enters the MB86975. The IBUS operates in two different modes: data acquisition and Interchip connections. In data acquisition mode the IBUS outputs channel addresses and accepts input data. In Interchip mode (used in distributed filter configurations) the IBUS is used to accept intermediate data points and partial filter results. In LMS distributed filters the IBUS is also used to propagate error gradient factor from the final unit to all preceding units in the cascade chain.</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td colspan="2" style="text-align: center;"><b>IBUS MODE</b></td> </tr> <tr> <td colspan="2" style="text-align: center;">DATA ACQ      INTERCHIP</td> </tr> <tr> <td rowspan="2" style="vertical-align: middle; text-align: center;">IBUS DIRECTION</td> <td style="text-align: center;">IN</td> <td style="text-align: center;">SIGNAL DATA</td> <td style="text-align: center;">SIGNAL DATA PARTIAL RESULTS</td> </tr> <tr> <td style="text-align: center;">OUT</td> <td style="text-align: center;">CHANNEL ADDRESSES</td> <td style="text-align: center;">LMS MODE ONLY ERROR GRADIENT FACTORS</td> </tr> </table> <p>Also see ICMODE register description.</p>	<b>IBUS MODE</b>		DATA ACQ      INTERCHIP		IBUS DIRECTION	IN	SIGNAL DATA	SIGNAL DATA PARTIAL RESULTS	OUT	CHANNEL ADDRESSES	LMS MODE ONLY ERROR GRADIENT FACTORS
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O	IAS	<p>The INPUT ADDRESS STROBE is an output line which indicates the presence of a channel address on the IBUS. When the MB86975 is used to form a LMS distributed filter the IAS is used to provide end-to-end synchronization between initial units and final units. In this situation the IAS of the final unit drives the SYNC input of the initial unit. (see figure 7)</p> <p>Also see IAC bit in IOMODE register</p>											
O	IDS	<p>The INPUT DATA STROBE indicates that the MB86975 is ready to accept data. There are two input modes which influence the behavior of the IDS.</p> <ol style="list-style-type: none"> <li>1. When in the INPUT STROBE mode a data source has a fixed amount of time to put its data onto the IBUS after IDS is detected to be asserted.</li> <li>2. In the HANDSHAKE mode the data source may enable data onto the IBUS after the data source detects the asserted IDS. The MB86975 will accept this input data after it receives an acknowledge (IDSACK) from the data source. In both of these cases the data source must continue to drive the IBUS until it detects the deassertion of IDS. IDS is also used in LMS distributed filter configurations to control passing of the error gradient terms. In that case IDS drives REVSTR pin of the immediate preceding unit (see figure 7).</li> </ol> <p>Also see IDC and IRC fields in IOMODE register</p>											
I	IDSACK	<p>The INPUT DATA STROBE ACKNOWLEDGE is an input signal generated by the data source. In the HANDSHAKE mode a data source will return the acknowledge after it has enabled data onto the IBUS in response to IDS. Upon the recognition of IDSACK the MB86975 will deassert IDS. The failure to return IDSACK when in the input HANDSHAKE mode will result in a data underrun and be flagged as an internal error. In cascade configurations IDSACK is driven by ODS to synchronize forward Interchip data transfer (see figures 5, 6, and 7).</p> <p>Also see IDC and IRC fields in IOMODE register</p>											

## Output Bus

I/O	ABBR.	NAME and DESCRIPTION										
I/O	OBUS	<p>The OBUS is the channel by which filtered signal-data exits the MB86975. The OBUS operates in two modes: data distribution and interchip connection. In data distribution mode the OBUS output channel addresses followed by the associated data. In interchip mode (used in distributed filter configurations) the OBUS is used to output intermediate data points and partial filter results. In LMS distributed filters, the OBUS reverses direction and is used to propagate error gradient factors from the final unit to all preceding units in a cascade chain.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2" style="text-align: center;">OBUS MODE</th> </tr> <tr> <th colspan="2" style="text-align: center;">DATA DISTR.                    INTERCHIP</th> </tr> <tr> <th rowspan="2" style="text-align: center;">OBUS DIRECTION</th> <th style="text-align: center;">IN</th> <td style="text-align: center;">LMS MODE ONLY ERROR GRADIENT FACTORS</td> </tr> </thead> <tbody> <tr> <th style="text-align: center;">OUT</th> <td style="text-align: center;">CHANNEL ADDRESSED, FILTERED SIGNAL DATA</td> <td style="text-align: center;">SIGNAL DATA, PARTIAL RESULTS</td> </tr> </tbody> </table> <p>Also see ICMODE register description.</p>	OBUS MODE		DATA DISTR.                    INTERCHIP		OBUS DIRECTION	IN	LMS MODE ONLY ERROR GRADIENT FACTORS	OUT	CHANNEL ADDRESSED, FILTERED SIGNAL DATA	SIGNAL DATA, PARTIAL RESULTS
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OBUS DIRECTION	IN	LMS MODE ONLY ERROR GRADIENT FACTORS										
	OUT	CHANNEL ADDRESSED, FILTERED SIGNAL DATA	SIGNAL DATA, PARTIAL RESULTS									
O	OAS	<p>The OUTPUT ADDRESS STROBE is an output line which normally indicates the presence of a channel address on the OBUS. In a distributed filter implementation OAS participates in system synchronization in the following ways:</p> <ol style="list-style-type: none"> <li>1. When the MB86975 is used to form a LMS distributed filter the OAS of the first unit provides the global synchronization by driving the SYNC inputs of all of the following devices (see figure 7).</li> <li>2. When the MB86975 is used to form a fixed FIR distributed filter each OAS drives the SYNC input of the immediately following MB87XXA FP in the cascade chain. This configuration automatically adjusts for the pipeline latency through the individual MB86975s (see figure 6).</li> </ol> <p>Also see OAC bit in IOMODE register.</p>										
O	ODS	<p>The OUTPUT DATA STROBE Indicates that the data on the output bus is valid. The output bus operates only in the output strobe mode. ODS is asserted for the number of clock cycles specified in the OBC field of the IOTIME register. In this mode the data destination has a fixed amount of time to capture data on the OBUS after ODS is detected asserted. When multiple MB86975s are cascaded each ODS drives the IDSACK input of the immediately following MB86975 in the cascade chain to the transfer of data and intermediate results between MB86975s (see figures 5, 6, 7).</p> <p>Also see ODC bit in IOMODE register.</p>										

## Cascade Control Signals

I/O	ABBR.	NAME and DESCRIPTION
I/O	CASREV	The CASCADE REVERSE line is used in LMS distributed filter configurations to control termination of the error gradient term passing process from the final unit back to the initial unit. CASREV is driven by the initial unit and is received by all other units in the cascade chain.
I	SYNC	<p>The SYNCHRONIZATION line is used to synchronize device operation when multiple MB86975s are used to form a cascade chain. The detailed signalling characteristics of SYNC depends upon the cascade configuration, the position of a particular device in the cascaded chain, and the algorithm implemented by the MB86975s.</p> <p>The four typical cases of SYNC usage are:</p> <ol style="list-style-type: none"> <li>1. Stand alone configuration; SYNC is not used</li> <li>2. Cascaded filters: the SYNC Inputs of all MB86975s are driven by an external synchronization signal.</li> <li>3. LMS distributed filter; OAS from the first MB86975 in the cascade chain drives the SYNC Inputs of all of the following units. IAS from the final unit drives the SYNC Input of the first unit.</li> <li>4. FIR distributed filter; OAS of the first unit drives SYNC of the following unit. SYNC input of the first unit is not used.</li> </ol>
I	REVSTR	The REVERSE STROBE is used in LMS distributed filter configurations to control the passing of the error gradient term computed in the final unit back to the preceding MB86975s in the cascade chain. REVSTR is driven by the IDS of the immediately following MB86975.

## Global Signals

I/O	ABBR.	NAME and DESCRIPTION
I	CLK	The CLOCK Input line is driven by the system clock to control all internal operations except Host Bus Interactions with the configuration registers.
I	RESET	The RESET forces selected configuration bits to a default state. In the default configuration, the execution unit is Idle, the Input Bus and Output Bus are tristate, and all output lines are in their respective deasserted states. The specific configuration control bits which are reset are SR(setup/run), DIAG(diagnostic mode), IER(interrupt on error), CRE and DRE(coefficient and data RAM enables).

## REGISTER DESCRIPTION

### Status Register

#### STATUS (address = 0 Read)

7	6	5	4	3	2	1	0
EF	RESERVED	CHE	OVR	IUN	HWE		

Bit 7 EF - ERROR FLAG

The error flag is set whenever an error condition is detected. This flag is a composite of the specific error condition flags found in the low half of the STATUS byte. EF and the specific error flags are cleared whenever the ICL(interrupt clear) bit is set, the MCL(master chip clear) bit is set, or the MB86975 is placed in the SETUP mode.

Bits 6,5,4 RESERVED

Bit 3 CHE - CASCADE HANDSHAKE ERROR

This bit is set if an erroneous handshake protocol is detected on either the Input Bus or the Output Bus in multidevice configurations. This error usually indicates improper setup of the device configuration control table in one or more of the cascaded chips.

Bit 2 OVR - OUTPUT OVERRUN

This bit is set if the internal computation unit generates a new output sample before the previous sample has been output from the device. This error usually indicates improper setup of the device configuration control table.

Bit 1 IUN - INPUT UNDERRUN

This bit is set if the internal computation unit requests a new input sample before such a sample has been acquired from the input bus. This error usually indicates improper setup of the device configuration control table.

Bit 0 HWE - HOST WRITE ERROR

This bit is set if the host processor attempts to alter any configuration control bits other than SR (setup/run), IER (interrupt on error), MCL (master clear), and ILC (interrupt clear) while the MB86975 is in the RUN mode.

### Status Register

#### STATUS (address = 0 Write)

7	6	5	4	3	2	1	0
		RESERVED		RWE	ICL	MCL	

Bits 7,6,5,4,3 RESERVED

Bit 2 RWE - RAM WRITE ENABLE

This bit is used to write into the 24 x 256 RAM and/or 16 x 256 RAM. If the CRE (coefficient RAM enable) bit or the DRE (data Ram enable) bit in the INTERNAL READ/WRITE CONTROL register is high, a 1 in the RWE bit will write data previously written into the DATA READ/WRITE registers (addresses 8,9,A) into the selected RAM. The address for the RAM is specified by the ORDER register. If both the CRE and DRE bits are high, RWE=1 will write data previously written into the the DATA READ/WRITE registers into both coefficient and data RAMs simultaneously. Note that the MB86975 must be in the SETUP mode and the NCH field in the SCNCH register must be set to zero for proper RAM write operation. At the end of each coefficient loading, the RWE bit will set to 0 by MB86975 automatically.

Bit 1 ICL - CLEAR INTERRUPT

This bit clears the MB86975 interrupt output. When ICL=1 the output is cleared. ICL can be asserted only if IER (Interrupt Error Condition) bit in MODE register. is high.

Bit 0 MCL - MASTER CHIP CLEAR

This bit is used to reset the MB86975. When MCL=1 the MB86975 behaves as if an external reset had been received.

### IBUS/OBUS Mode Control Register

#### IOMODE (address = 1)

7	6	5	4	3	2	1	0
IAC	IDC	ITC	IRC	OAC	ODC		

Bit 7 IAC - IBUS ADDRESS PHASE CONTROL

This bit determines whether the IBUS will output a channel address prior to reading the associated data. When IAC=1 the IBUS does not output channel addresses. When there is a single input channel, or when operation is externally synchronized, the IBUS is used to only read input data; IAC should =1. When

there are multiple input channels and bus source addressing is not externally synchronized and controlled, the IBUS must output channel addresses as well as input data. IAC should=0. The presence of a channel address on the IBUS is indicated by the assertion of IAS. The channel address specifies the data source. When IAC=0 the IBUS outputs the channel address prior to requesting data.

#### Bits 6,5 IDC - IBUS DATA WORD PHASE CONTROL

This two bit field determines how long the IDS is asserted during the data-word input phase on the IBUS. The four modes are :

MODE	IDC	IDS CONDITION
0	00	IDS is asserted until the IBUS COUNT expires (see IBC field in IOTIME register).
1	01	IDS is asserted for 2 clock cycles.
2	10	When the MB86975 detects the IDSACK, the timer starts and IDS is asserted until the timer expires.
3	11	IDS is asserted until the MB86975 detects IDSACK. IDSACK must meet the input sampling setup-time requirement for detection, IDS will be deasserted one clock cycle after the MB86975 detects the IDSACK (see Timing Diagram Figure 8).

#### Bit 4 ITC - IBUS TRANSITION PHASE CONTROL

The ITC bit applies only to the adaptive LMS algorithm. Each input cycle in LMS adaptive mode consists of two data transfers, one for data and one for the reference. This bit controls the duration of the inactive time between the data and reference transfers in the LMS adaptive mode input cycle. When ITC=0, IDS is deasserted for 1 cycle. When ITC=1, IDS is deasserted until the IBC timer expires (see IBC field in IOTIME register).

#### Bits 3,2 IRC - IBUS REFERENCE WORD PHASE CONTROL

This two bit field determines how long the IDS is asserted during the reference word phase. The IRC field is used only in the adaptive LMS mode to control acquisition of the reference signal. The reference word phase has the same modes as the data word phase described under IDC.

#### Bit 1 OAC - OBUS ADDRESS PHASE CONTROL

This bit determines whether the OBUS will output a channel address prior to writing the associated data. The OAC should be 1 when there is one output channel or when operation is externally synchronized operations. In these cases the OBUS is used only to write output data. The OAC should be 0 when there

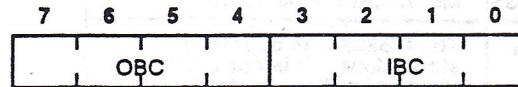
are multiple output channels and the bus source addressing is not externally synchronized and controlled. In these cases the OBUS must output channel addresses as well as data. The channel address specifies the data destination.

#### Bit 0 ODC - OBUS DATA HOLD PHASE CONTROL

This bit determines whether data will be held on the OBUS for one extra cycle after ODS is deasserted. When ODC=0, data on the OBUS will change and OBUS will be deasserted in the same cycle. When ODC=1, data on the OBUS will change one cycle after ODS is deasserted. This mode is provided to support peripheral devices requiring long data hold times.

### I/O Bus Data Strobe Times Register

#### IOTIME (address = 2)



#### Bits 7,6,5,4 OBC - OBUS COUNT

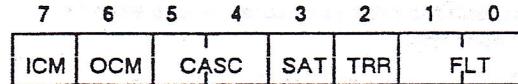
This field determines the number of cycles that ODS will be asserted during data output transfers on the OBUS. The four bit field ranges from 0000, 1 cycle, to 1111, 16 cycles.

#### Bits 3,2,1,0 IBC - IBUS COUNT

This field determines the number of cycles that the IDS will be asserted during the data word input in selected IBUS modes (see IDC, ITC, and IRC fields in IOMODE register). The four bit field ranges from 0000, 1 cycle, to 1111, 16 cycles.

### Algorithm Control Register

#### ALGCTRL (address = 3)



#### Bit 7 ICM - COMMON INPUT MODE

This bit controls the data source to the individual channels within a group. When ICM=0, each channel processes a unique input data stream. When ICM=1, filters in a group share a common input data stream.

**Bit 6 OCM - OUTPUT CONTROL/COMBINE MODE**

When in multichannel FIR or IIR grouped filter operation ( $NCH > GRPSZ \geq 1$ ), this bit controls the destination of data processed by the individual channels within a group. When OCM=0 each channel outputs a unique data stream. When OCM=1 the individual channel outputs within a given group are combined (summed) to form a single data stream which is the composite group output.

When in the LMS adaptive mode, this bit determines if the channel output will be the filtered signal or the error. When OCM=0 each channel sources the scaled output of the adaptive FIR filter. When OCM=1 each channel sources the difference (error) between the reference input and the scaled output of the adaptive FIR filter.

**Bits 5,6 CASC - CASCADE UNIT POSITION**

This two bit field specifies the position of the MB86975 in a cascade string. There are four modes.

MODE	CASS	MB87XXAOP POSITION
0	00	The MB86975 is operating stand alone. It is not a part of a distributed filter. Note that in cascaded filter configurations, each MB86975 performs separately. CASC must be set to 00 in each device.
1	01	The MB86975 is the first unit in a distributed filter configuration.
2	10	The MB86975 is ( one of ) the intermediate unit(s) in a distributed filter configuration.
3	11	The MB86975 is the final unit in a distributed filter configuration.

**Bit 3 SAT - SATURATION MODE**

This bit determines the contents of the accumulator after an overflow or an underflow occurs. When SAT=0 there is no saturation control. The contents of the accumulator is unpredictable after overflow or underflow occurs. When SAT=1 the accumulator will contain the maximum representable value in an overflow condition, and the minimum representable value in an underflow condition.

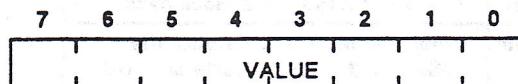
**Bit 2 TRR - TRUNCATION/ROUNDING CONTROL**

This bit controls the truncation or rounding of the end result of the arithmetic computation. When TRR=0 the MB86975 truncates the result of the computations. When TRR=1 the MB86975 adds a rounding constant to the result of the arithmetic computations to round the result to (n) significant bits.

**Bit 1,0 FLT - FILTER TYPE**

This two bit field selects the filter type to be implemented by the MB86975. There are four types.

TYPE	FLT	MB87XXAOP OPERATION
0	00	FIR filter
1	01	Adaptive FIR filter
2	10	IIR filter
3	11	Reserved

**Order Register****ORDER (address = 4)**

This register, in the setup mode, is used to address the coefficient and/or data RAMs. The contents of these RAMs may be read and written through the DATA READ/DATA WRITE registers (addresses 8,9,A), under the control of RWE bit of the STATUS register and the bits in the RWCTRL register. Both RAMs may be both read and written for testing and verification purposes. From an operational standpoint the user only accesses the RAM to load the coefficients for fixed FIR and IIR implementations.

In the FIR filter case, after the coefficient loading is complete, this field is programmed with the order of the filters to be implemented. Note that the maximum possible filter order per channel decreases as the number of channels increases. For a single device FIR filter, the maximum filter order is equal to 256 taps / the number of channels. For a single device adaptive FIR filter the maximum filter order is equal to (256 taps / the number of channels) minus 2.

In the IIR filter case, after the coefficient loading is complete, this field is programmed with the value: ( $4 * (\text{number of biquads}) - 1$ ). The maximum possible order of implementable IIR filters varies with the number of channels used as follows:

NUMBER OF CHANNELS	MAXIMUM FILTER ORDER
1	16 (8 cascaded biquads)
2	16 (8 cascaded biquads)
4	16 (8 cascaded biquads)
8	14 (7 cascaded biquads)
16	6 (3 cascaded biquads)
32	2 (1 cascaded biquad)

## Output Scaling/ Number of Channels Register

### SCNCH (address = 5)

7	6	5	4	3	2	1	0
SCALE				NCH			

#### Bits 7,6,5 SCALE - OUTPUT SCALE FACTOR

This field allows the user to control the final scaling on an internally accumulated value before it is output. The scale factors are as follows:

MODE	SCALE	SHIFT REGISTER
0	000	No shift
1	001	The contents of the accumulator are shifted left by 2 bits
2	010	The contents of the accumulator are shifted left by 4 bits
3	011	The contents of the accumulator are shifted left by 6 bits
4	100	Reserved
5	101	Reserved
6	110	Reserved
7	111	Reserved

#### Bits 4,3,2,1,0 NCH - NUMBER OF CHANNELS

This five bit field indicates the number of channels, to a maximum of 32, that is implemented. This field is offset by 1 as follows:

NCH	NUMBER of CHANNELS
00000	1
00001	2
00010	3
00011	4
00100	5
:	:
11100	30
11101	31
11111	32

## Leakage/Group Size Register

### LKGGRPSZ (address = 6)

7	6	5	4	3	2	1	0
LKGE				GRPSZ			

#### Bits 7,6,5 LKGE - LEAKAGE

This 3 bit field is used to specify a leakage constant. This constant is used in the adaptive FIR filter mode to push the coefficients toward zero. The constants are defined as follows:

LKGE	COEFFICIENT
000	No Leakage
001	$2^{-24}$
010	$2^{-23}$
011	$2^{-22}$
100	$2^{-21}$
101	$2^{-20}$
110	$2^{-19}$
111	$2^{-18}$

#### Bits 4,3,2,1,0 GRPSZ - GROUP SIZE

This five bit field indicates the number of channels that are grouped together to share a common input or summed output. Just as NCH, this field is offset by one. When 00000 in GRPSZ implies 1 channel per group; when 11111 in GRPSZ implies 32 channels per group.

## Number of Biquards/ Groups Register

### NBGPR (address = 7)

7	6	5	4	3	2	1	0
NBIQ				NGRP			

#### Bits 7,6,5 NBIQ - NUMBER of BIQUADS

This three bit field specifies the number of cascaded second order sections - biquads - may be implemented per channel in the IIR filter mode. This field is offset by one; a value of 0 implies 1 biquad.

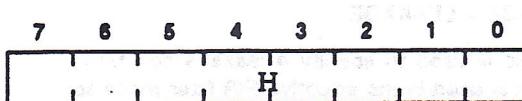
#### Bits 4,3,2,1,0 NGRP - NUMBER of GROUPS

This five bit field indicates the number of groups implemented. Note:  

$$\text{NGRP} = (\text{number of channels}/\text{channels per group}) = [(\text{NCH}+1)/(\text{GRPSZ}+1)] + 1$$

## Coefficient Read/Write Register, High Byte

### DATA.H (address = 8)

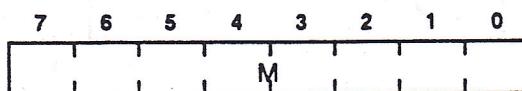


Bits 8,7,6,5,4,3,2,1,0 H - HIGH BYTE COEFFICIENT

This 8 bit register is used to access the most significant 8 bits of the 24 bit coefficient RAM, of the 16 bit data RAM, or the most significant byte of one half of the DOUT register. See RWCTRL register and RWE bit in STATUS(write) register.

### Coefficient Read/Write Register, Middle Byte

#### DATA.M (address = 9)

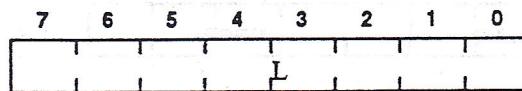


Bits 8,7,6,5,4,3,2,1,0 M - MIDDLE BYTE COEFFICIENT

This 8 bit register is used to access the middle 8 bits of the 24 bit coefficient RAM, the least significant 8 bits of the 16 bit Data RAM, or the least significant byte of one half of the DOUT Register. See RWCTRL register and RWE bit in STATUS(write) register.

### Coefficient Read/Write Register, Lower Byte

#### DATA.L (address = A)

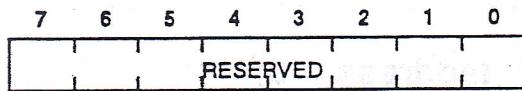


Bits 8,7,6,5,4,3,2,1,0 L - LOWER BYTE COEFFICIENTS

This 8 bit register is used to access the least significant 8 bits of the 24 bit coefficient RAM, or the least significant byte of the 16 bit Data Ram. See RWCTRL register and RWE bit in STATUS(write) register.

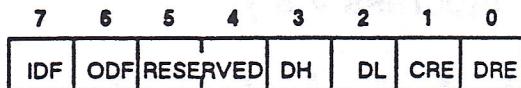
### Reserved

#### REV ( address =B)



### Internal R/W Control Register

#### RWCTRL (address = C)



This register allows the user to access the coefficient and Data RAMs and the data out register. In read mode, only one of these four bits should be on at a time. In the write mode, CRE and DRE may be on at the same time. This combination allows the user to write the same data into the coefficient and data RAMs simultaneously.

Bits 7,6,5,4 RESERVED

Bit 3 DH - DOUT HIGH WORD READ ENABLE

When this bit is set, DH=1, the user can read the left half of the 32 bit DOUT register. The upper byte of this half word is available in DATA.H. The lower byte is available in DATA.M. DOUT read back is provided to support diagnostic testing. See DIAG bit in MODE register.

Bit 2 DL - DOUT LOWER WORD READ ENABLE

When this bit is set, DL=1, the user can read the right half of the 32 DOUT register. The upper byte of this half word is available in DATA.M. The lower byte is available in DATA.L.

Bit 1 CRE - COEFFICIENT RAM ENABLE

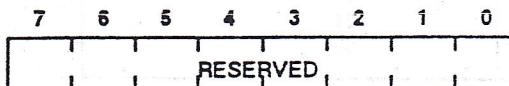
When this bit is set, CRE=1, the user can read or write into the coefficient RAM. A RAM write is initiated by the RWE bit in the STATUS register.

Bit 0 DRE - DATA RAM ENABLE

When this bit is set, DRE=1, the user can read or write into the data RAM. A RAM write is initiated by the RWE bit in the STATUS register.

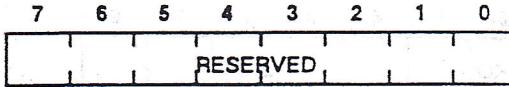
### Reserved

#### REV (address = D)



### Reserved

#### REV (address = E)



## Global Mode Register

### MODE (address = F)



#### Bit 7 IER - INTERRUPT ON ERROR CONDITION

This bit enables the MB86975 interrupt output. The INT can be asserted only if IER is high. The MB86975 generates interrupt signals when internal error conditions are detected.

#### Bits 6,5,4,3,2 RESERVED

#### Bit 1 DIAG - DIAGNOSE

This bit provides the system user with the ability to do a controlled test of the MB86975's internal control and configuration resources. If the MB86975 is placed in RUN mode, while DIAG is on it will execute one computation cycle and automatically return to the setup mode. The processing performed

during this single cycle is the same as in normal operation except that input and output requests are not made of the respective bus units. The result of the computation will be based entirely on state data provided by the user in the internal data and coefficient RAMs. This result is held in the DOUT register for user analysis. See the DH and DL bits in RWCTRL register.

#### Bit 0 SR - SETUP/RUN

This bit controls whether the MB86975 is in the SETUP or the RUN mode. SR is set only by direct write to the bit. SR is reset by an external device reset, reset pin, by a master clear, MCL bit, and by direct write. When the MB86975 is in the RUN mode the host can only write into selected bits of the coefficient registers without generating errors. The bits to which write access is allowed in the RUN mode are; the setup/run, interrupt on error enable, clear interrupt, and master clear. When SR=0 the MB86975 is in the SETUP MODE. When SR=1 the MB86975 is in the RUN mode. Note that in distributed filter configurations, the first unit in the cascade chain must be the last unit to leave its SR bit set to RUN mode. This guarantees proper synchronizations of the cascade chain.

REGISTER	ADDRESS	BIT POSITION							
		7	6	5	4	3	2	1	0
STATUS (read)	0	EF		RESERVED		CHE	OVR	IUN	HWE
STATUS (write)	0			RESERVED			RWE	ICL	MCL
IMODE	1	IAC		IDC		ITC		IRC	OAC
IOTIME	2			OBC				IBC	
ALGCTRL	3	ICM	OCM	CASC		SAT	TRR		FLT
ORDER	4					VALUE			
SCNCH	5			SCALE				NCH	
LKGRPSZ	6			LKGE				GRPSZ	
NBGRP	7			NBIQ				NGRP	
DATA	8					H			
DATA	9					M			
DATA	A					L			
RESERVED	B			RESERVED					
RWCTRL	C			RESERVED		DH	DL	CRE	DRE
RESERVED	D			RESERVED					
RESERVED	E			RESERVED					
MODE	F	IER		RESERVED			DIAG	SR	

REGISTER ASSIGNMENTS

## TIMING DIAGRAMS

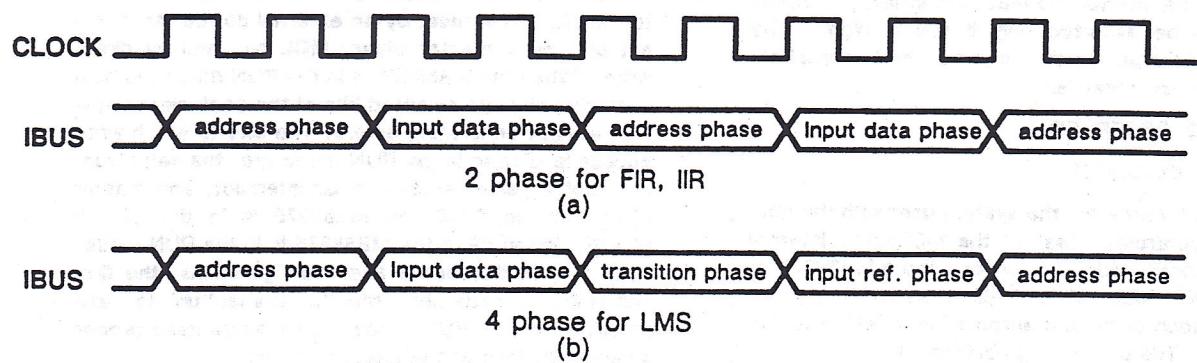


FIGURE 8 IBUS PROTOCOL

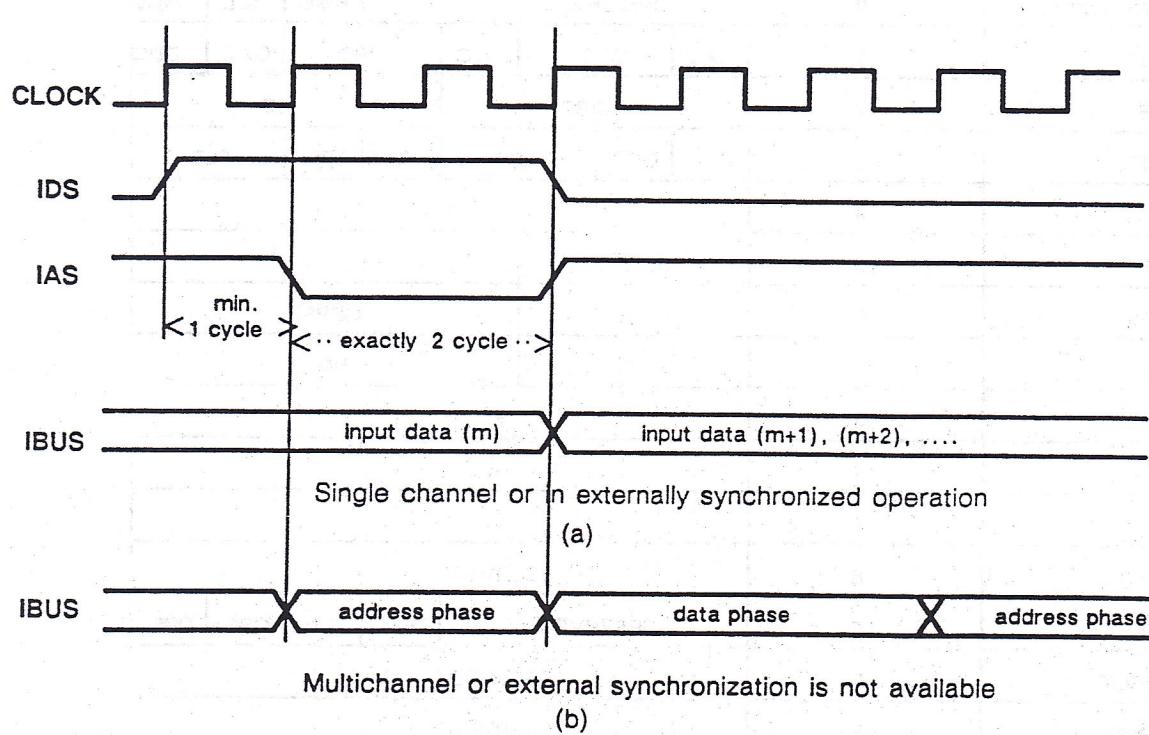


FIGURE 9 IBUS TIMING DIAGRAM

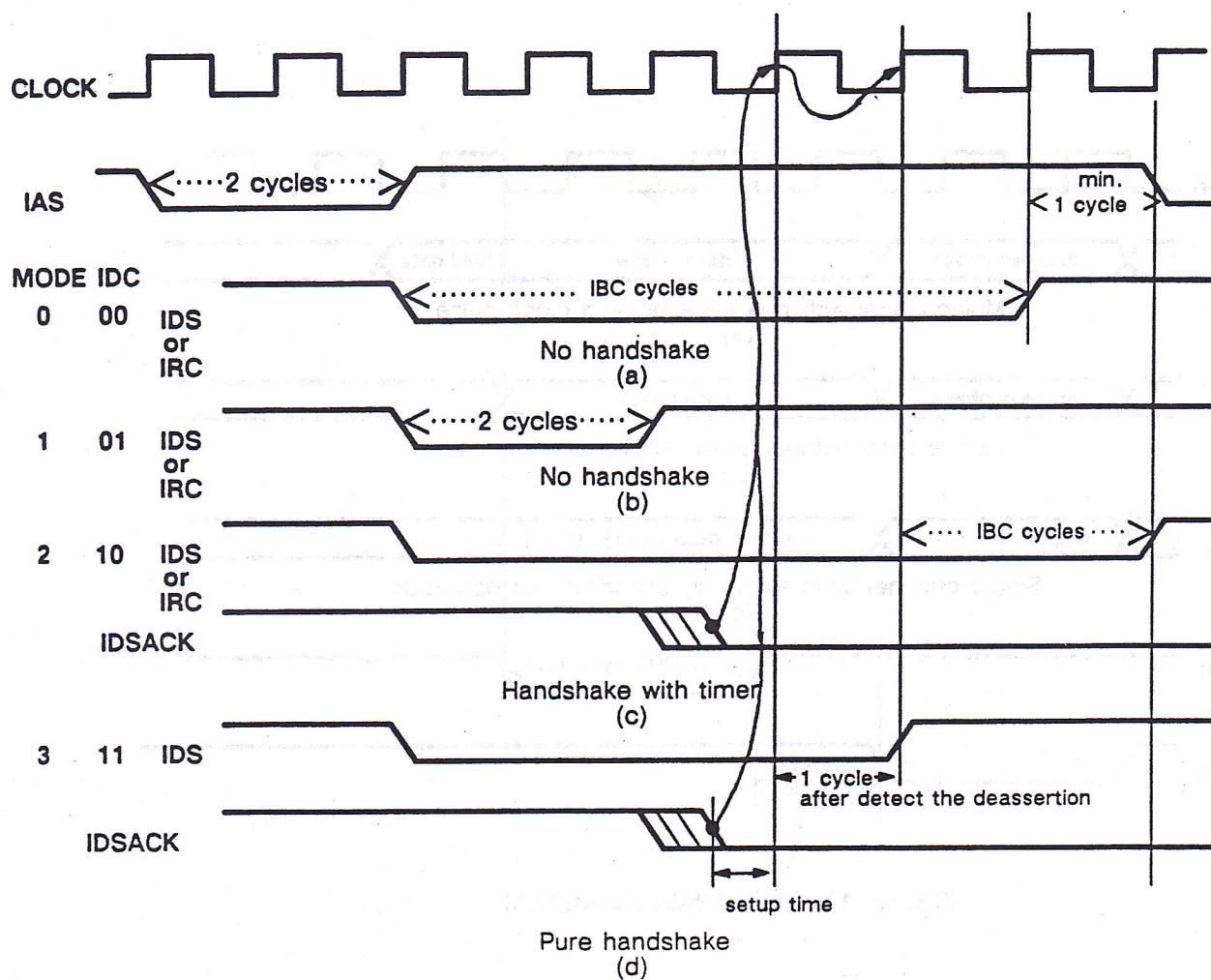


FIGURE 10 IDS TIMING DIAGRAM INPUT DATA PHASE OR INPUT REFERENCE PHASE

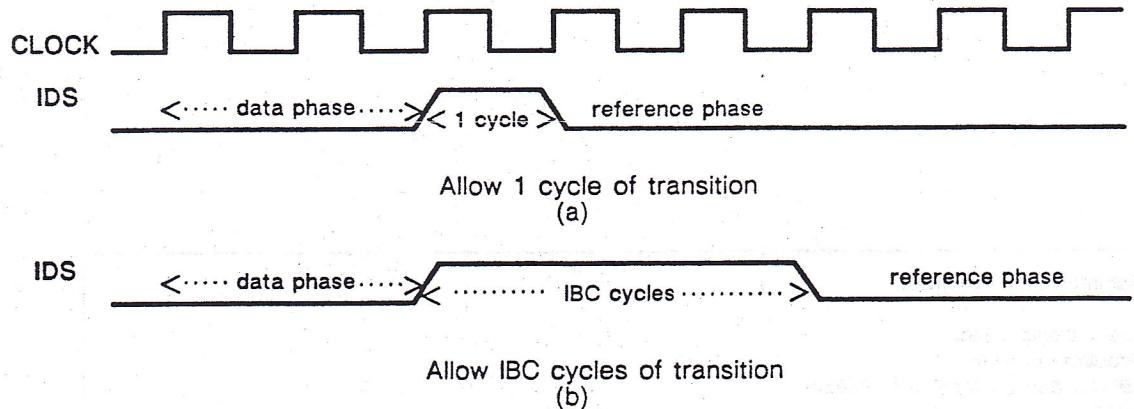


FIGURE 11 IDS TIMING DIAGRAM FOR INPUT TRANSITION PHASE

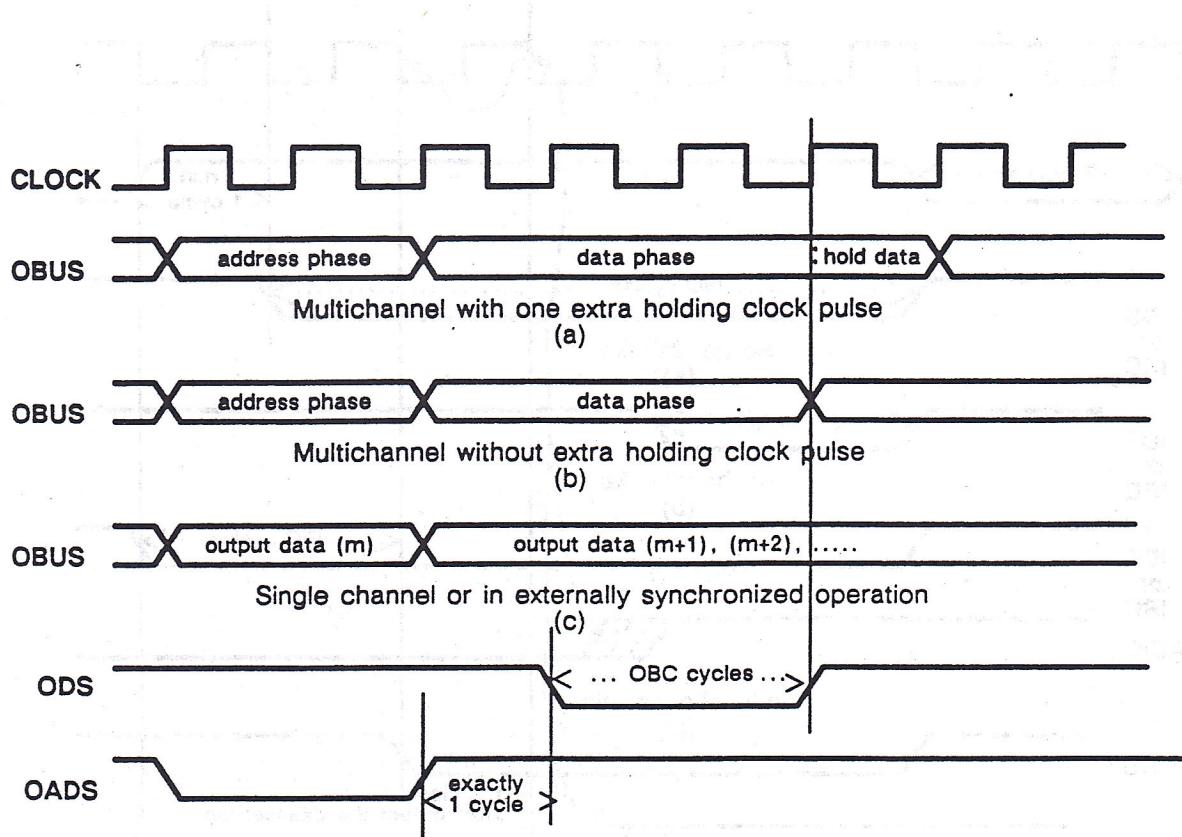


FIGURE 12 OBUS TIMING DIAGRAM

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