C32025TX
Digital Signal Processor Core

General Description

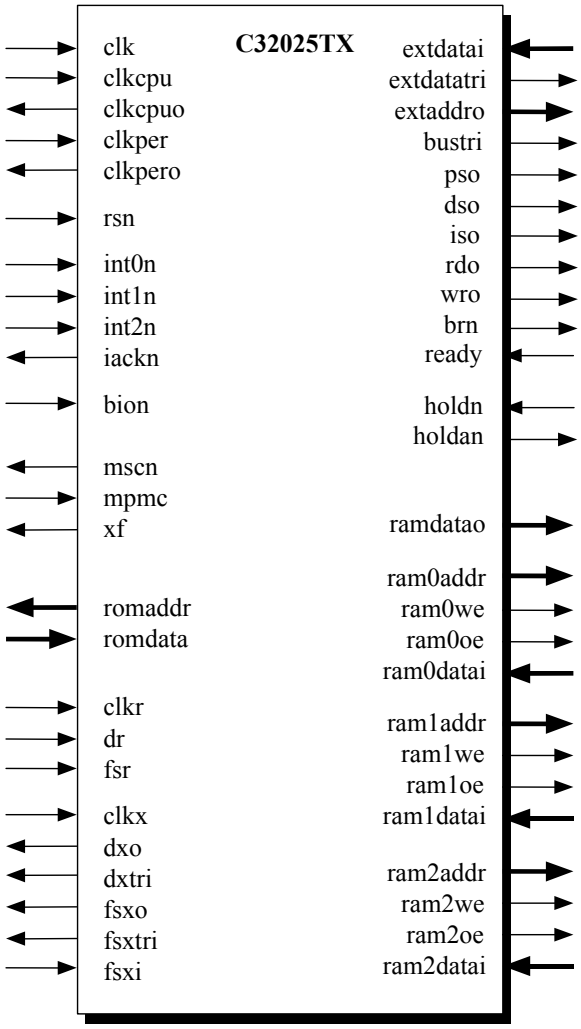
The C32025TX is a single-chip, high performance 16-bit fixed-point digital signal processor core. It implements the same instruction set as the TMS320C25 and provides the same interrupts, serial interface and timer, executing most of instructions in a single clock cycle.

The C32025TX is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is strictly synchronous with both-edge clocking, a synchronous reset, and no internal tri-states.

Features

- Control Unit
  - Single-clock per machine cycle operation
  - 16-bit instruction decoding
  - Repeat instructions for efficient use of program space
  - 8-level Hardware Stack
- Central Arithmetic-Logic Unit
  - 16-bit sign-extended parallel shifter
  - 32-bit arithmetic and logical operations
  - 16 x 16 bit parallel multiplier with a 32-bit product
  - 32-bit accumulator with output shifter
  - Single-cycle Multiply-and-Accumulate instructions
- Auxiliary Registers
  - 8 x 16-bit registers for indirect addressing or data storage
  - 16-bit Auxiliary Register Arithmetic Unit including operations with reversed-carry propagation
- 16-bit reload timer
- Memory addressing modes
  - Direct – using a 9-bit Page Pointer and 7 LSBs of instruction word
  - Indirect – using Auxiliary Register File
  - Immediate – less than 16-bit via instruction word or full 16-bit long immediate following the instruction word
  - Block moves for data/program management
- Interrupt Controller
  - 6 interrupt sources plus reset and one software interrupt
- Synchronous serial port for direct codec interface
- Program Memory organization
  - 4K-words of internal ROM
  - Internal 256-word RAM block configurable either as program or data space
  - 64K-word external program space
- Data Memory organization
  - 2 Internal 256-word and one 32-word RAM blocks
  - 64K-words of external data space
  - 6 memory mapped registers
- 16 Input and 16 Output channels
- Wait states for interfacing slower off-chip devices
- Configurable synchronous/asynchronous external / internal memory support
- Power Management Unit for low-power operation
- Concurrent DMA using an extended Hold operation
- Multiprocessing support
  - Global data memory interface

Symbol



Implementation

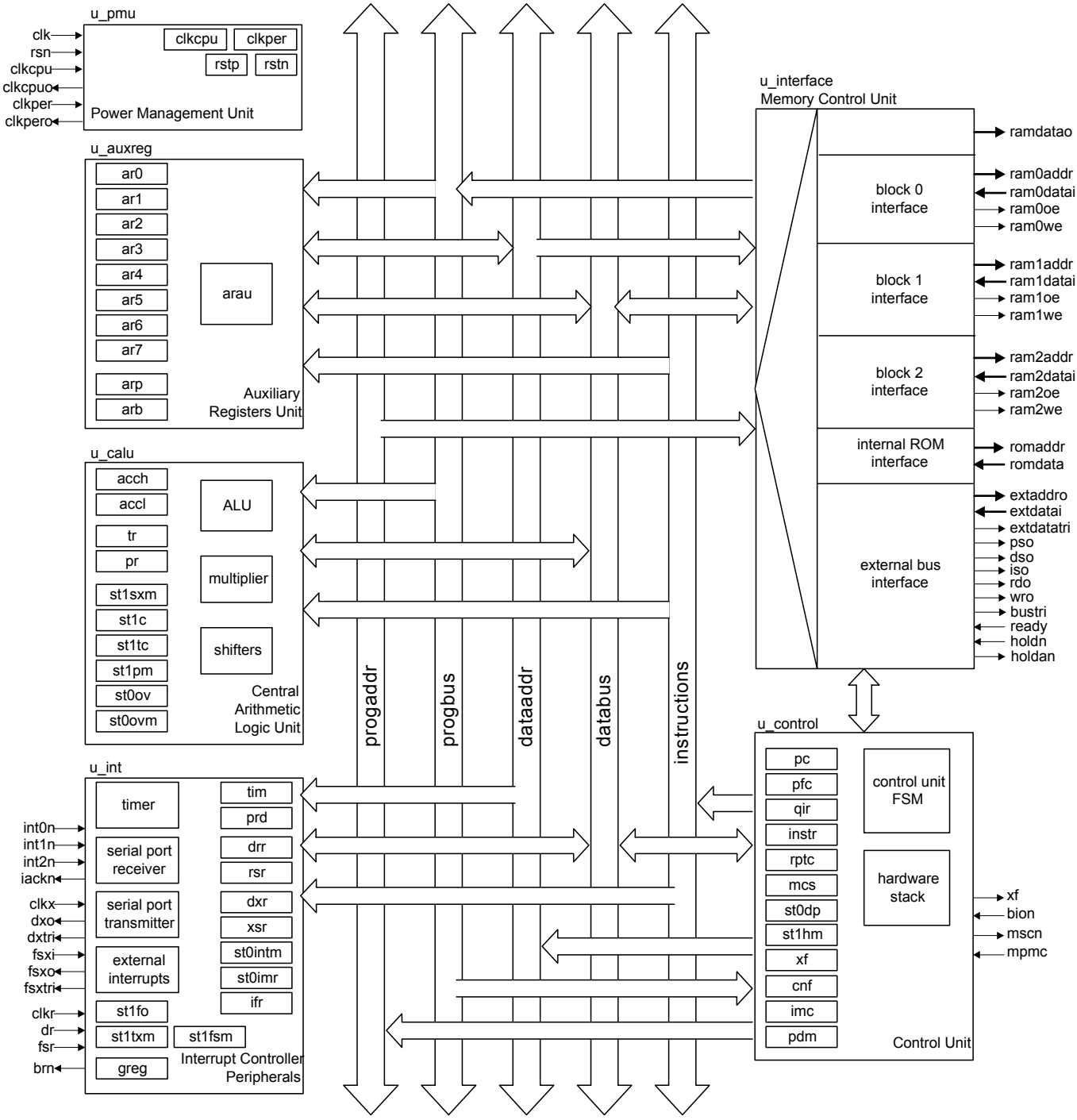
Device	Area	Speed
TSMC 0.25	24.000	53 MHz
Virtex II	2003 SLICEs	38 MHz
VirtexE	2223 SLICEs	29 MHz
Spartan2	2223 SLICEs	26 MHz
APEX20KE	4531 LCs	22 MHz
ACEX1KE	4979 LCs	18 MHz

Pin Description

Name	Type	Polarity	Description
clk	I	-	**Master clock input** Clock do all internal synchronous circuits
clkcpu	I	-	**Engine clock input** Pulse for internal circuits, which are stopped when the C32025TX is in IDLE or STOP mode
clkper	I	Rise	**Peripheral clock input** Pulse for timer, serial interface and interrupt circuits, which are stopped when the C32025TX is in STOP mode
clkcpuo	O	-	**Engine clock output** Gated clk clock. Clkcpuo stays low after the C32025TX enters into IDLE or STOP mode. The clkcpuo is dedicated to off-core connection to the clkcpu input.
clkpero	O	Rise	**Peripheral clock input** Gated clk clock. Clkpero remains low after the C32025TX enters into STOP mode. The clkpero is dedicated to off-core connection to the clkper input
mpmc	I	-	**Microprocessor / microcomputer mode** When Low the internal ROM is mapped into the program space

Name	Type	Polarity	Description
holdn	I	Low	**Hold input** Forces the processor to place the external bus into a high impedance state
holdan	O	Low	**Hold acknowledge output** Indicates that the processor is in the hold mode
int0n, int1n, int2n	I	Low/Fall	**External interrupt inputs**
iackn	I	Low	**Interrupt acknowledge** Indicates branch to interrupt vector
pso, dso, iso	O	Low	**Program, data and I/O space select signals**
rdo	O	Low	**External bus read**
wro	O	Low	**External bus write**
bustri	O	High	**External bus tri-state control** Enables external bus and control lines tri-state buffers
ready	I	High	**Data ready input** Indicates that the external device is prepared to complete a bus transfer
bion	I	Low	**Branch control input** Controls BIOZ branch effectiveness
brn	O	Low	**Bus request output** Asserted when the processor requires access to external global data memory
mscn	O	Low	**Microstate complete output** Indicates the beginning of a new memory operation
xf	O	-	**External flag output** General purpose output pin
clkr	I	Fall	**Receive clock input**
clkx	I	Rise	**Transmit clock input**
dr	I	-	**Serial data receive input** Data clocked by clkr
dxo	O	-	**Serial data transmit output**
dxtri	O	High	**Serial transmit tri-state control** - Active only while transmitting
fsr	I	Fall	**Frame synchronization pulse for receive input**
fsxi	I	Fall	**Frame synchronization pulse for transmit input**
fsxo	O	Fall	**Frame synchronization pulse for transmit output**
fsxtri	O	High	**Frame synchronization pulse for transmit tri-state control**
ramdatao	O	16	**Ram Data output** Data for all RAMs
			External Program/ Data/ IO interface
extaddro	O	16	Address bus output
extdatai	I	16	Data bus input
extdatatri	O	High	Data bus tri-state control
			Internal Program Memory interface
romdata	I	16	Data input
romaddr	O	12	Address output
			Internal RAM 0 interface
ram0datai	I	16	Data bus input
ram0addr	O	8	Data file address
ram0we	O	High	Data file write enable
ram0oe	O	High	Data file output enable
			Internal RAM 1 interface
ram1datai	I	16	Data bus input
ram1addr	O	8	Data file address
ram1we	O	High	Data file write enable
ram1oe	O	High	Data file output enable
			Internal RAM 2 interface
ram2datai	I	16	Data bus input
ram2addr	O	5	Data file address
ram2we	O	High	Data file write enable
ram2oe	O	High	Data file output enable

Block Diagram



Performance

The architecture of the C32025TX ensures overall system speed and flexibility in processor configurations. The instruction set and control signals provide block memory transfers, communication to slower off-chip devices and multiprocessing implementations. Single-clock multiply/accumulate instructions, two large on-chip RAM blocks, eight auxiliary registers with dedicated arithmetic unit, serial interface and hardware timer make the processor appropriate for data-intensive signal processing.

The C32025TX implements Harvard-type architecture to maximize processing power by maintaining two separate program and data buses for full-speed execution. The program bus carries instructions and immediate operands while data bus interconnects various components and carries data from/to any data memory space. Both buses can carry data for single-clock multiply & accumulate operations.

Instruction flow consists of three pipeline stages, essentially invisible to the user. The pre-fetch, decode and execute stages are independent, which allows instructions to overlap. Thus, three different instructions can be active during any given cycle.

Most instructions can be used in repeat mode, when they are executed a given number of times. This feature is at most useful with block moves, multiply/accumulates, I/O transfers and table read/writes.

The table below shows the speed ratio of the C32025TX over the standard TMS320C25 chip. A speed ratio of 4 means that the C32025TX performs the same instruction four times faster than the TMS320C25.

Instruction type	**Single**				**Repeated**			
	Fastest		**Average**		**Fastest**		**Average**	
	clk	ratio	clk	ratio	clk	ratio	clk	ratio
Memory reference	1	4	1.9	3.1	1	4	1.1	3.9
I/O	2	2	2.1	3.7	1	4	1.7	3.6
Block transfer	4	3	4.2	3.3	1	4	1.2	4
MAC	4	3	4	4.4	1	4	1.5	4
MAC with data move	4	3	4	4.4	2	2	2	3
Other	1	4	1.6	3.9	1	4	1	4
All	1	4	1.8	3.6	1	4	1.1	3.9

Deliverables

- VHDL or Verilog RTL source code
- Testbench (self checking)
- Example design showing how to connect memories
- Simulation script
- Synthesis script
- Documentation

Contact Information

CAST, Inc.
11 Stonewall Court
Woodcliff Lake, New Jersey 07677 USA
Phone: +1 201-391-8300
Fax: +1 201-391-8694
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

This core developed by the processor experts at Evatronix SA