SESSION 5: APPLICATION-SPECIFIC ICs

TAM 5.4: A 1.2-Million Transistor, 33MHz, 20-bit Dictionary Search Processor with a 160kb CAM

Masato Motomura, Jun Toyoura, Kazumi Hirata, Hideyuki Ooka, Hachiro Yamada, Tadayoshi Enomoto
NEC Corporation
Kanagawa, Japan

This 1.2-Million transistor, 32MHz, 20-bit dictionary search processor (DISP) design makes it practical to construct a 50,000-word dictionary search system using only 20 DISPs. Special features of the DISP are (1) an architecture that drastically increases capacity of the content addressable memory (CAM) which handles high-speed character searches, (2) logic that increases the speed of the cellular automation processor (CAP) which conducts word searches, and (3) architecture for reducing the size of CAP hardware.[1]

Figure 1 shows the DISP, which consists of a 160kb data CAM (DCAM), a CAP, a priority encoder, and a 1kb control code CAM (C^2CAM). The DCAM compares an input character with stored characters, and produces a match signal for each comparison. The CAP conducts both exact and approximate word searches using the match signals. A priority encoder encodes both the addresses and the degrees of mismatch for each searched word.

A conventional CAM cell requires a silicon area of about 4 SRAM cells because it consists of a SRAM cell and the match circuit for comparing input data with all CAM cell data. Here one match circuit is time-shared by each row, reducing silicon area to 1/5 of that of a conventional CAM designed with the same rules. Figure 2 shows the DCAM consisting of 20 CAM arrays. Each CAM array has 512 rows and 16 columns. A single match circuit is provided for each row. Figure 3 shows 16 SRAM cells and a read/match circuit (M1-M4) for a single row (a write circuit is not shown). The read/match circuit can be constructed from a conventional read circuit by adding an nMOSFET M4 and a match line.

For either read or write operation, 20 SRAM cells for one character are selected by column and row addresses. (See example marked in black in Figure 2). Data are either read or written through data lines. One column stores 512 characters forming up to 128 words. The length of each word can be arbitrarily chosen.

For the match operation, a column address selects 512 characters which are then simultaneously compared in read/match circuits with an input character loaded from data lines. Supposing in Figure 3, that a "1" is the stored datum at the selected cell and the input datum is "1" (i.e., bit line = "1" and data line = "1"). M1 is turned on and M2 and M4 are turned off, so that a precharged match line stay at "1". Similarly, when the input datum of "0" is applied, the match line is discharged and becomes "0". In order to obtain character match, all 20 input data and 20 stored data must be the same to keep the match line at "1". If one pair of data were mismatched, the precharged match line would be discharged, resulting in character mismatch. 512 match signals are produced at a time. This character search continues for all characters of the input word stream.

When words in the input word stream contain errors resulting from misspelling or failures in voice or character recognition, it is necessary to find the closest stored words. This is called an approximate search in which the degree of error (i.e., distance) must be calculated. This distance is defined as the minimum required number of character substitutions, deletions, and insertions[2]. A well-known algorithm for the calculating the distance is dynamic programming (DP), whose fundamental expression is:

$$d_j(k) = \mathrm{Min}\,[\, d_{j-1}(k-1) + \overline{M_j(k)},\ d_j(k-1)+1,\ d_{j-1}(k)+1 \,]. \tag{1}$$

Here, integer $d_j(k)$ is the distance between a substring up to the jth character for a stored word and a substring up to the kth character for an input word. $\overline{M_j(k)}$ is an inverse of the match signal mentioned above.

The problem with using a systolic processor (SP) to produce a DP algorithm is that hardware is extensive and complicated, because adders, minimum value detectors, etc. are required to calculate Equation 1. Now consider the distance vector, which may be express as $[\, d_{n,j}(k), \cdots, d_{i,j}(k), \cdots, d_{0,j}(k) \,]$, where $d_{i,j}(k) = 0$ for $i < d_j(k)$, $d_{i,j}(k) = 1$ for $i = d_j(k)$, and $d_j(k) = x$ for $i > d_j(k)$. Here x can be either 1 or 0. An increase of 1 in distance will result in a shift of all vector components to the left, i.e., [x, x, x, 1, 0, 0] is changed into [x, x, 1, 0, 0, 0]. Therefore, Equation 1 can be changed into the Boolean expression:

$$d_{i,j}(k) = d_{i,j-1}(k-1-)M_j(k) + d_{i-1,j-1}(k-1)\overline{M_j(k)} + d_{i-1,j}(k-1) + d_{i-1,j-1}(k). \tag{2}$$

The CAP consists of an array of processor elements (PEs). Each PE calculates Equation 2, as shown in Figure 4. PEs are simple so that a CAP is 20 times smaller and 3 times faster than the SP.

Figure 5 shows a CAP together with the DCAM and the priority endocer. Match signal $M_j(k)$ is supplied by the DCAM, and the distance vector is encoded by the priority encoder to give the distance. For example, the CAP shown here consists of 4x7 PEs, and the stored and input words are "MEMORY" and "MENORY". At k=1, "M" is loaded and $M_j(1)$ becomes "101000". Using these match signals, the CAP changes its state from k=0 to k=1, as shown in Figure 6. Similar transitions takes place for every k. When the last character "Y" is loaded at k=6, $[d_{i6}(6)]$ becomes [1, 1, 1, 0]. The priority endocer then produces a distance of 1, i.e., $d_6(6) = 1$. The present DISP contains a CAP consisting of 3x512 PEs to perform approximate searches with a maximum distance of 2.

Figure 7 shows a micrograph of a DISP whose main features are summarized in Table 1.

Acknowledgement

The authors thank all involved in developing the DISP.

[1] Yamada, H., et al., "A High-Speed String Search Engine", IEEE JSSC, Vol. SC-22, No. 5, p829-834, Oct., 1987.

[2] Hall, P.A., G. R. Dowling, "Approximate String Matching", Computing Surveys, Vol. 12, No. 4, Dec., 1980.

0193-6530/90/0000-0090$01.00 © 1990 IEEE

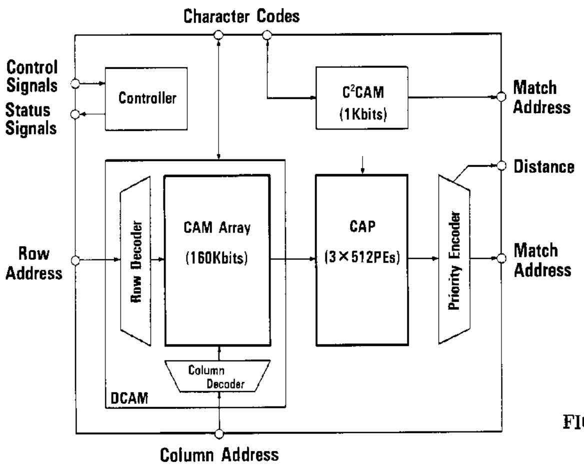

FIGURE 1 – Dictionary search processor

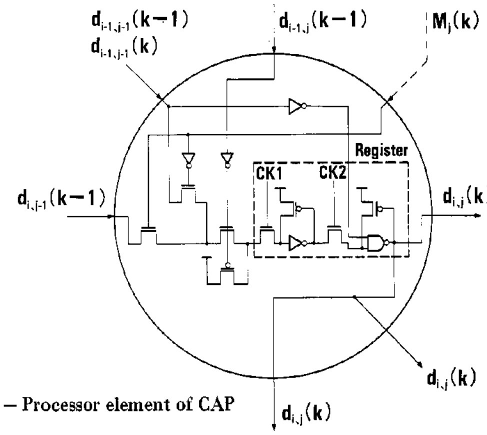

FIGURE 4 – Processor element of CAP

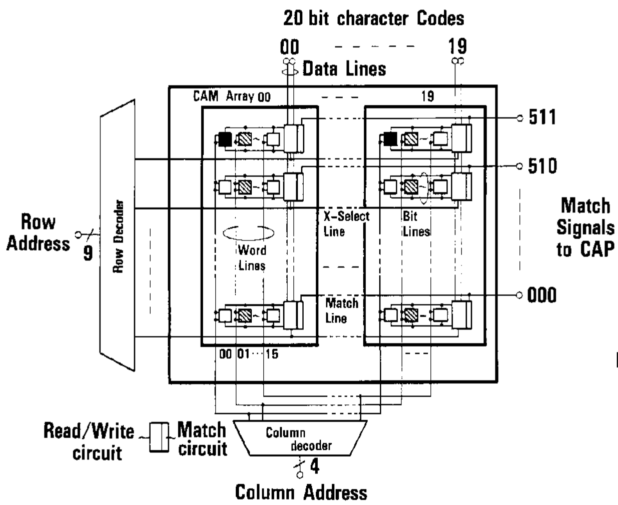

FIGURE 2 – Data CAM

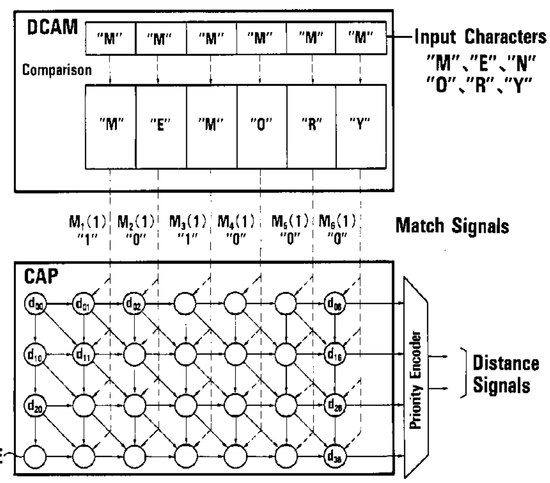

FIGURE 5 – CAP architecture

FIGURE 6 – *See page 271*

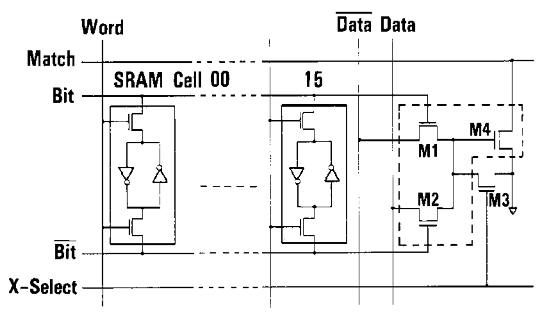

FIGURE 3 – Read/match circuit

DCAM	
Structure	160kb (= 16 column x 512 row x 16 array)
Clock Frequency	33MHz for 20-bit character search
Character input rate	33M characters/s
Number of search modes	12 basic search modes: 3 approximate search modes x 4 anchor modes 3 "don't care" search modes: Fixed length "don't care" Variable length "don't care" Grammatical construction
Power supply voltage	5V
Number of voltage	1,208,500
Die size	13.02 x 12.51mm
Fabrication technology	0.8μm, 3-Al-level, CMOS

TABLE 1 – Main features of the DISP

(Continued from page 91)

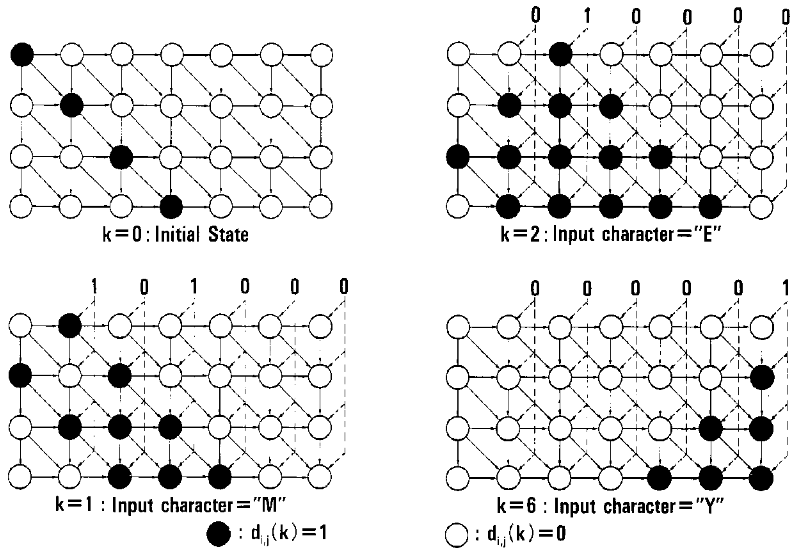

FIGURE 6 – CAP search process. Black (white) PE shows that the value equals 1 (0)

FIGURE 7 – DISP micrograph