AN EXPANDABLE SINGLE-IC DIGITAL FILTER/CORRELATOR

Frederick A. Williams
Sr. Applications Engineer

TRW LSI Products
La Jolla, California

ABSTRACT

The commercial success of single-integrated circuit multipliers and correlators has prompted the design of a new integrated circuit for video-speed digital convolution and correlation. This device is based on two concepts: 1.) the merging of delay and pipeline registers and 2.) "bit-slicing" the filter array in both the signal data word and coefficient dimensions. The device can update one coefficient per clock cycle. The result is an expandable "building block" which can be cascaded or paralleled to give the desired length, signal data word length, and coefficient data word length for any desired filter up to 20 MSPS.

INTRODUCTION

Digital finite impulse response (FIR) filters have a number of desirable properties: absolute stability, phase linearity (if symmetrical coefficients are used), ease of use in adaptive systems, an optimal computerized design methodology which is widely available, and conceptual simplicity. A canonical FIR filter comprises a tapped delay line, a means for weighting the outputs of those taps, and an adder to sum all the delayed and weighted signal samples. A block diagram is shown in Figure I.

In implementation, the canonical form has some severe drawbacks. A common number of taps is between 16 and 32. Despite the advent of single-IC multipliers, a 32-tap video-speed FIR filter is an impressively large and expensive unit. Such a 32-tap FIR filter could be made from 32 delay ICs, 32 multiplier ICs, 63 four-bit adders, 15 dual two-bit adders (this assumes 8-bit words), and as many pipeline registers as necessary to sustain the desired data rate. The number of such pipeline registers could easily reach 63 8-bit registers! This estimate does not include coefficient storage. It is capable of pipelined operation up to a sample rate of 1/Tmc, where Tmc is the multiplication time of the multiplier. This maximum sample rate is 16 MHz for the 8-bit TRW MPY008HJ-1, and 20 MHz for the 12-bit MPY112K. Even for 8-bit words, over 100 supporting MSI circuits are required.

In an effort to reduce the number of MSI circuits required, the circuit shown in Figure II was developed previous to the work reported here. Here, instead of shifting the incoming data through a shift-register type delay line, the hardware shifts the coefficients. The multipliers have been replace by multiplier-accumulators. The output is selected from the multiplier-accumulator which has summed a complete set of weighted samples. That multiplier-accumulator is then reset, and will start to accumulate a new set of weighted samples. For our example of 32 taps, only 36 supporting MSI chips are required (in addition, of course, to the 32 multiplier-accumulators). This configuration has the advantage that its chip count is rather insensitive to both coefficient and signal data word sizes. The design and construction of such a FIR filter is still an expensive and formidable undertaking, and there is a small speed penalty in the use of multiplier-accumulators instead of straight multipliers.

In short, previous implementations of video FIR filters have suffered from excessive circuit complexity and its attendant cost, both in money and engineering time.

A FIR FILTER METRIC

To compare implementations of FIR filters, a means of measuring computational complexity is required. To develop a suitable metric, consider the fact that the effects of word size in signal data words and coefficient words are different. The signal data word size determines the peak signal to noise ratio, whereas the coefficient word size affects only the accuracy of the approximation of the desired frequency response. Since LSI multiplier arrays are typically square, and multiplication time varies with the total number of bits in both the multiplier and the multiplicand, a time penalty is exacted for greater word size than necessary in either signal data or coefficients. This suggests that the number of bits in the signal data words ("m") and the number of bits in the coefficient words ("n") characterize the filter in addition to the filter length ("N"). The fact that (within limits) these three parameters are independent (determining SNR, approximation accuracy, and transition band widths) suggests that a suitable metric for a FIR filter is the product m x n x N. This is shown in Figure III.

In recent years a popular approach to the development of computer central processing units (CPUs) has been the so-called "bit-slice" approach, where a system is partitioned into sections which can be used in varying number to process data of different word length. This has permitted the use of a single device (such as the 2901) for multiple applications, and thus its production in high quantities at lower cost. Our metric suggests that this approach might be fruitful when applied to FIR filters. In fact, we have chosen to "slice" the filter in all three dimensions in producing the TDC1028.

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A REVISED ARCHITECTURE

The equation which describes the action of a FIR filter is

$$y(k)= \sum_{n=0}^{n} h(n)z^{-n}x(k-n)$$

where x(*) is the input sequence, h(*) the coefficient sequence, and y(*) the output sequence.

Although the canonical FIR filter delays the signal samples, and then multiplies the delayed samples by the impulse response coefficients, there is no reason that the multiplication must precede the delay. Reversing this order gives the signal flow diagram of Figure IV. Here, we note that to perform the additions which are required in any FIR filter at video rates, pipelined adders are needed. By merging the pipeline registers with the delay registers, the signal flow diagram of Figure V results.

THE TDC1028 FIR FILTER BUILDING BLOCK

We combined this merged register concept with the "bit-slice"format for signal data words, coefficient words, and length (number of taps) to develop a universal FIR filter "building block", functional up to 20 MSPS the TRW LSI Products TDC1028, as shown in Figure VI. This monolithic VLSI circuit is an 8-tap FIR filter with 4-bit signal data and coefficient words. The internal adders are 13 bits wide, and have a cascading input port. The user can cascade units up to 36 taps with absolutely no danger of overflow for any possible choice of coefficients. Actual choices for coefficients may sometimes allow cascading to greater lengths than 36. (In fact, a 4-bit two's complement data/4 bit coefficient 63 tap FIR filter can be built from cascaded TDC1028s, without external adders.)

Coefficients are held internally in registers which feed the multipliers. One coefficient can be written into the internal registers each clock cycle, even at the maximum clock rate. This is a restriction imposed by package pin count. Were an unlimited number of pins available, all coefficients could be written at the same time. This is a significant point in the design of adaptive filters, in that this design may not be suitable for all algorithms. The maximum wait for updating is eight clock cycles. If the coefficients are written in sequence from h(n) to h(0) synchronously with the incoming signal data, the filter can be changed "cleanly" - in other words, there will be no outputs which were computed with a mix of coefficients between the previous and present set of coefficients.

The use of a "bit-slice" format has implications for input formats. In general, signals may be either in two's complement or magnitude format, as may coefficients also. However, coefficients are generally in two's complement, as negative numbers are necessary for proper computations. When either the signal data or the coefficients are in two's complement with greater than 4 bits of precision, the least significant bits (LSBs) will have to be handled as magnitude numbers, whereas the most significant bits (MSBs) will have to be handled as two's complement numbers. Hence, the TDC1028 has two control pins, TCD and TCC, which respectively control whether the data or coefficients are two's complement or not. Sign extension is automatically provided by the internal adders.

We expect very few applications to fall within the limits imposed by the use of a single TDC1028. Thus, the device was designed for easy expansion. The 3-dimensional model for the metric intuitively communicates the proper way to connect the devices for longer signal data word length, coefficient word length, and filter length (i.e., number of taps). Figure VII shows how the provision of cascading connections simplifies increasing the number of taps.

The other major area of expansion is word sizes. The expansion of the design to 8-bit data words and 8-bit coefficients requires that the final sum outputs of four different strings of TDC1028s be added, with different weightings. One will handle the product of the LSBs and the LSBs, one will handle the product of the MSBs and the MSBs, and two will handle the cross-products. The addition necessary is shown in Figure VIII.

Ease of use has been a prime consideration in the design of the TDC1028. Even the pinout has been designed consciously to simplify the layout of printed circuit cards.

APPLICATIONS

Besides its use in educational applications, for which its ease of use commends it, the TDC1028 is expected to find use wherever reasonably high-speed FIR filters are encountered. Areas of application include noise reduction, picture enhancement, and standards conversion in broadcast television, matched filters for radar and sonar, and the real-time calculation of correlations.

Figure I.

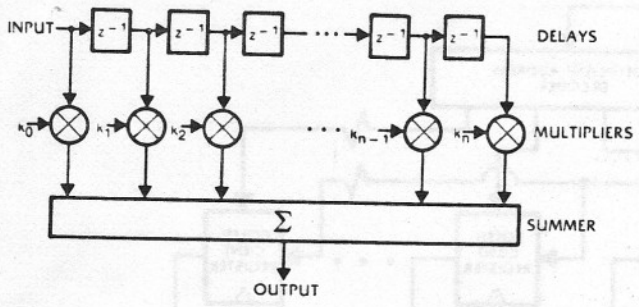

Figure II.

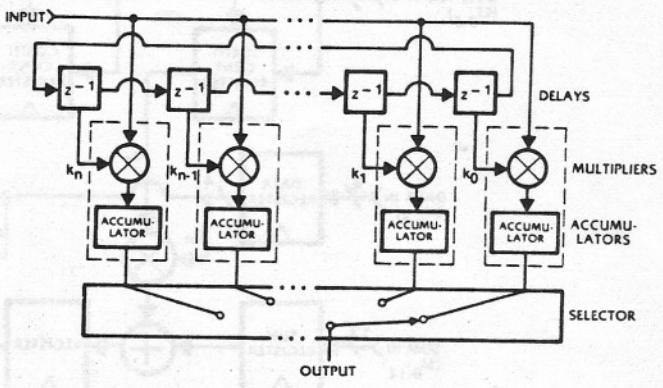

Figure III.

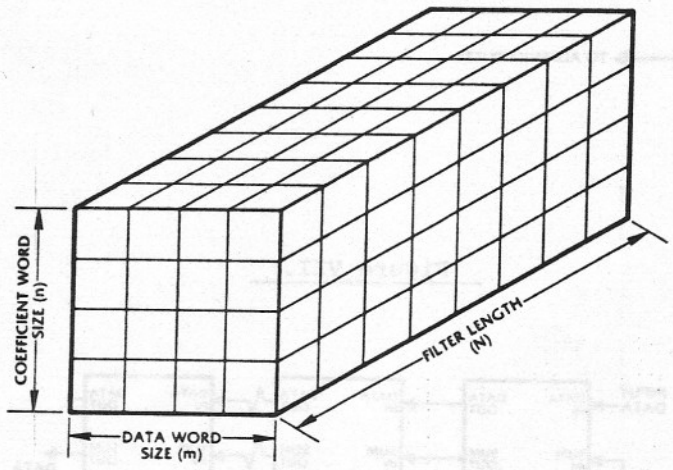

Figure IV.

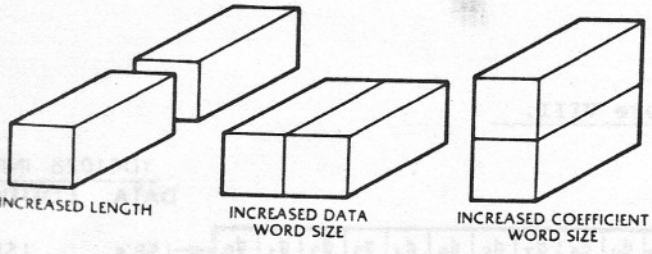

Figure V.

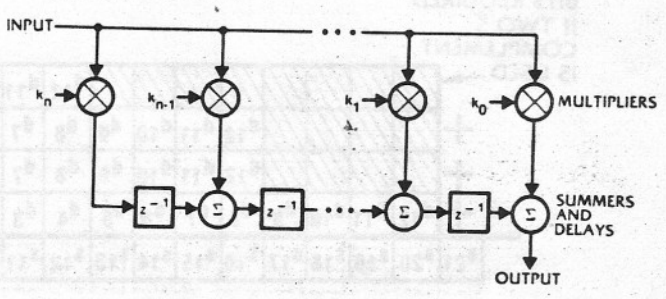

Figure VI.

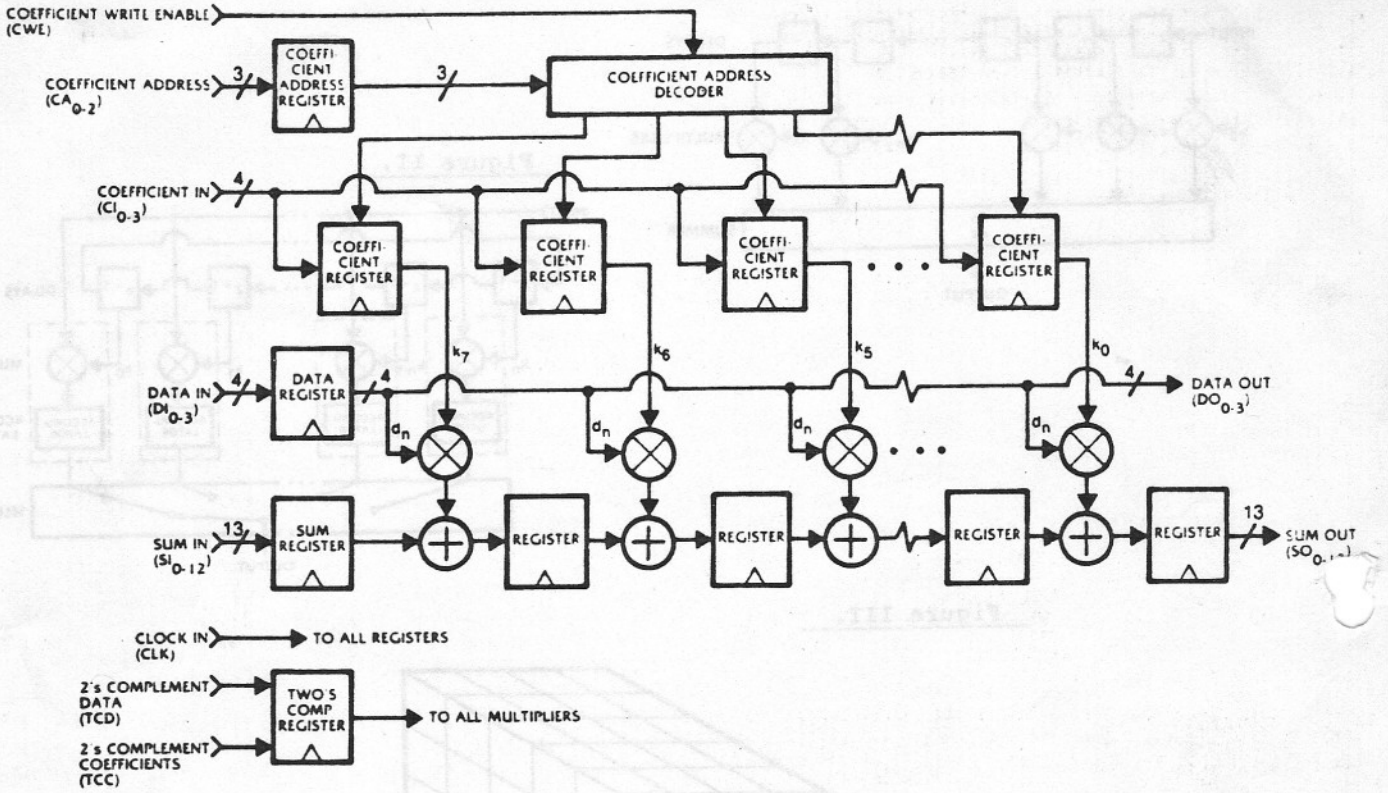

Figure VII.

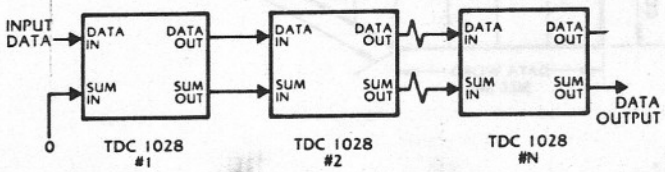

Figure VIII.