MP 4.4: A Digital 80Mb/s OFDM Transceiver IC for Wireless LAN in the 5GHz Band

Wolfgang Eberle, Mustafa Badaroglu, Veerle Derudder, Steven Thoen[1], Patrick Vandenameele[1], Liesbet Van der Perre, Mario Vergara, Bert Gyselinckx, Marc Engels, Ivo Bolsens

IMEC, Leuven, Belgium, [1]Also PhD student at KU Leuven.

W. Eberle

A programmable transceiver for up to 80Mb/s wireless LAN in the 5GHz band with 64/128/256 subcarriers encompasses (de)framing, (I)FFT, adaptive equalization and synchronization. The 14.6mm² 0.35µm 3.3V 50MHz CMOS IC, designed in a C++ flow, uses distributed control and clock gating to reduce power consumption.

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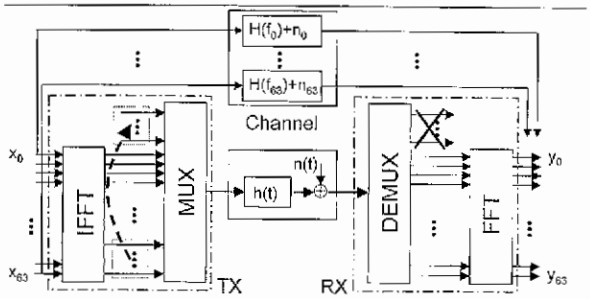
Outline

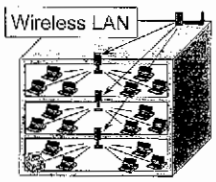
- High-speed wireless communications desirable!
- Datapath implementation aspects feasible?
- System integration, communication, and control flexible?
- Design flow and conclusions affordable? ... !

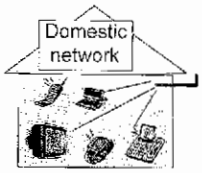
Beating the channel by changing the point of view



Orthogonal frequency division multiplex (OFDM) emerges
=> ADSL,VDSL,DAB,DVB-T,Hiperlan2,MMAC, IEEE 802.11a

Connecting 'everything' without a wire





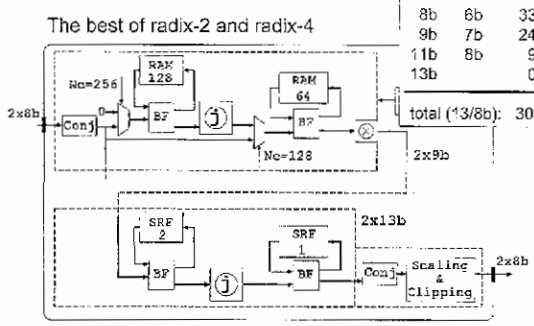
Wireless ~ 'hard'ware
(low-power, fast, fixed)

Networking ~ 'soft'ware
(configurable, on demand)

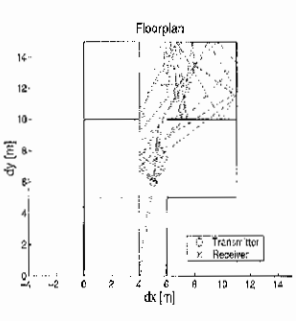
µP, RISC core, DSP, FPGA or a 'programmable' ASIC?

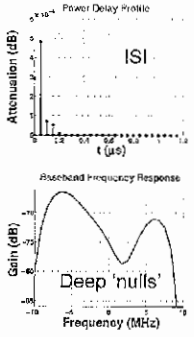
(I)FFT with optimum wordlength

Wordlength DP	coef	Gain in memory
8b	6b	33 %
9b	7b	24 %
11b	8b	9 %
13b		0 %
total (13/8b):		30 %

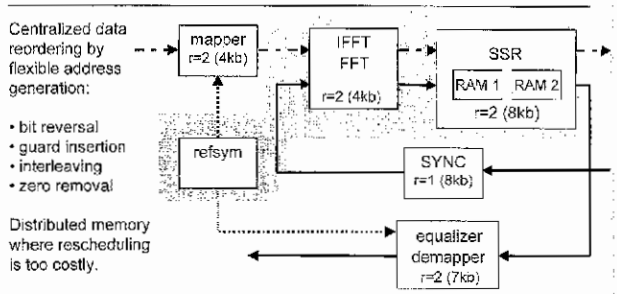


Challenges in a multipath indoor environment



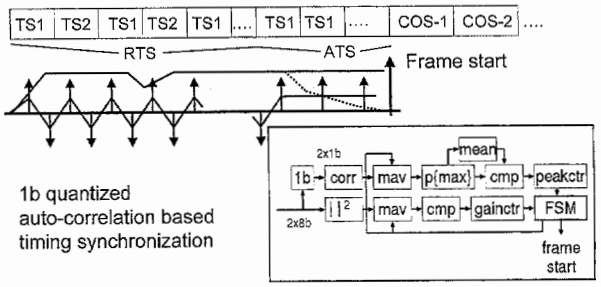


Resource sharing in half-duplex operation



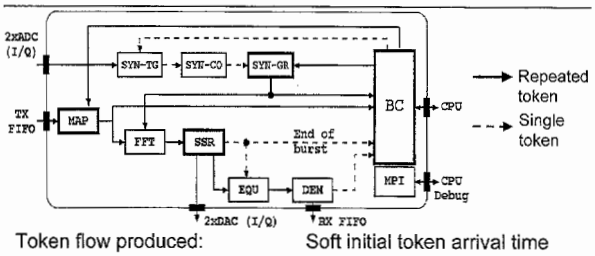
WLANs require fast burst synchronization

Acquisition process

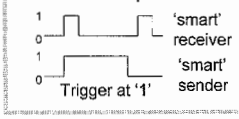


1b quantized auto-correlation based timing synchronization

Token flow control: integration = communication



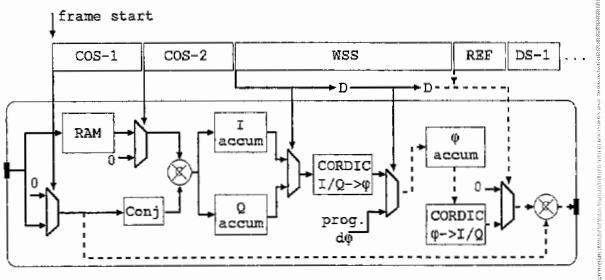
Token flow produced:



Soft initial token arrival time specification: $T_{min} < T < T_{max}$
=> boundary check only
=> supports IP block strategy

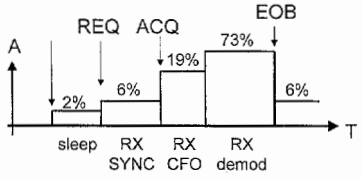
Limiting CFO to ensure FFT integrity

Required: 2-3 % of inter-carrier spacing to limit ICI
Approach: coarse pre-compensation in TD + fine tracking in FD

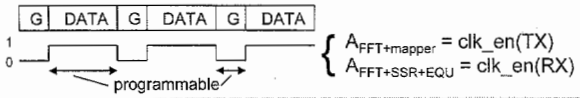


Clock gating as a companion for token semantics

Clock matches activity A => P_{avg}~A

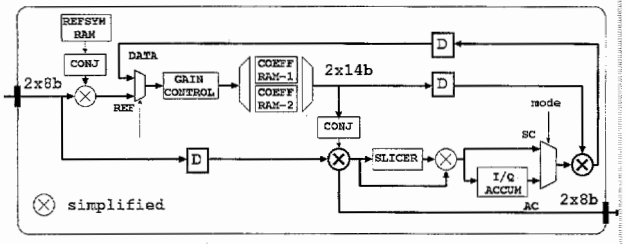


Avoids wait states in multi-rate processing: variable length guard insertion/removal



Adaptive equalization at low computational cost

Initial estimate: reference symbol ('pilots')
Short-term: decision-directed PLL with adaptive loop gain
Long-term: periodic reference symbol insertion



Benefit due to FD equalization: single-tap, single operator

The key question: why an ASIC?

Technology	3.3V CMOS 0.35 µm 5 LM
Maximum clock speed	50 MHz
Package	144 – PQFP
Die size	211500 equ. gates ~ 16.4 mm^2

'IEEE' mode @ 50 MHz	Power	GOPS	Memory #acc/s	Memory Gbit/s
– Transmission mode	670 mW	3.8	1.32 G	21.3
– Reception mode	570 mW	6.8	1.28 G	20.3
– Programming mode	400 mW	n/a	n/a	n/a
– Sleep mode *	150 mW	n/a	n/a	n/a

Configuration of the datapath building blocks

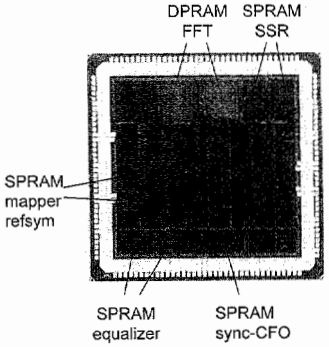
Parameter	Options
Number of carriers	64, 128, 256
Guard interval	0:4:28
Modulation	QPSK (BPSK)
Equalizer modes	REF-FF, SC-FB, AC-FB reference sequence
Spectral mask	Complex, per carrier
FFT clipping	5-8b, MSB or LSB aligned
Spreading	1, 2, 4, 8; code sequence
Acquisition	sequence, length, confidence factors
Number of zero carriers	Low: 0:1:3, left and right High: 0:2:30, left and right

It is a 'must' to handle channel, front-end, QoS requirements

and a challenge ... Parameters with global influence

with a consequence ... DP scheduling for all configurations
=> dynamic + 'hard'
=> data-driven
=> token semantics

Resource sharing with distributed memory



size in %	
FFT	34
CORDIC	26
Equalizer	18
SSR	8
Mapper	6
Acquisition	4
common	45
dedicated TX	6
dedicated RX	48

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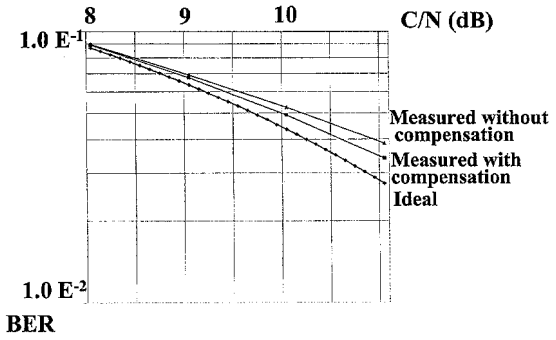
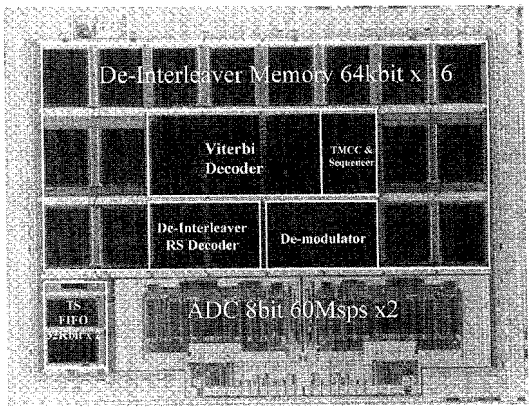
BER Performance



Characteristic Summary

Process Technology	**0.25um CMOS 1-Poly 3-Metal**
SRAM	**64kbit x 16, 32Kbit x 2, 3.25Kbit x 1**
ADC	**8bit 60Msps x 2ch**
Transistor Count	**8.8 million**
Power Supply	**2.5V (Internal), 3.3V (I/O)**
Chip Size	**72mm²**
Package	**100-pin Plastic QFP**



Conclusion

- **The Demodulator LSI for BS digital is developed**
  - **Demodulator , Error Correction &TS output**
  - **1Mbit SRAM, ADCx2, VCO,**
- **Dynamic multi-format demodulation is proposed**
  - **Pull-in range of ± 300 kHz**
  - **Frequency Offset ± 5MHz With scan circuit**
  - **Low BER**
- **The Two compensation circuit is realized**
  - **Improvement of 0.2 dB**

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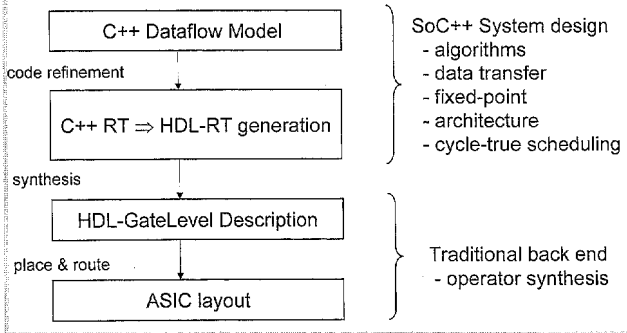
Merging algorithm and architecture design in C++



Conclusions

- wireless LAN at 80 Mbps with OFDM is feasible in 0.35 μm
  => 1/2 rate coded 155 Mbps will be available in 0.13 μm
- dedicated algorithmic solutions for fast burst synchronization, FFT and equalization lead to a low-cost implementation
- Token flow results in reusable IP and scalability
- Integrated design flow allows algorithm/architecture trade-offs
- > 6 Gops/s and > 20 Gbit/s memory transfer require a multi-processor architecture with distributed memory

  => 'Programmable' ASIC links wireless and networking