MASSANA

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FILU-50 ⇨ 50 MIPS 7000 gate DSP Coprocessor Core

Performance

- 50 MIPS in 0.35 μm
- 16-bit architecture, 40-bit accumulator
- Single 16-bit memory for lowest cost

Features

- Fully synthesizable Verilog – single clock design
- Technology independent
- Scan testable – high test coverage
- Enables efficient DSP on microcontrollers and RISCs
- Enables DSP development in C

Microcoded Functions

- FIR filters
- 1st, 2nd & Nth order IIR filters
- 256 point real FFT
- Correlation
- Matrix & Vector operations
- Taylor series

New microcoded functions can be added.

Applications

- Signal Conditioning / Analog Front-End Processing
- Engine Management / Knock Detection
- AC / DC Motor Control
- Disk Drive Servo Control

Introduction

The FILU-50 is an ultra-small 16-bit 50 MIPS DSP coprocessor core. At 7000 gates it is much less than ¼ the size of standard DSP cores. Tailored for medium complexity numerical operations, it is optimized for minimum area, bridging the gap between microcontrollers and DSPs. A single memory architecture yields the lowest system cost.

The FILU is capable of implementing various DSP functions which are microcoded and are invoked by a host processor (MCU or RISC) via a shared RAM. The Host has Master control of the RAM via control / status bits.

The microcoded kernel includes FIR and IIR filters, FFT, correlation, matrix operations and Taylor series. Extra DSP functions can be microcoded to suit particular applications.

The basic set of microcoded functions are hardwired but RAM based functions can extend the functionality after production.

It is expected that the user will develop their application entirely in C using an API to invoke FILU functions. To aid in the development process C and Verilog models are provided to allow system simulation.

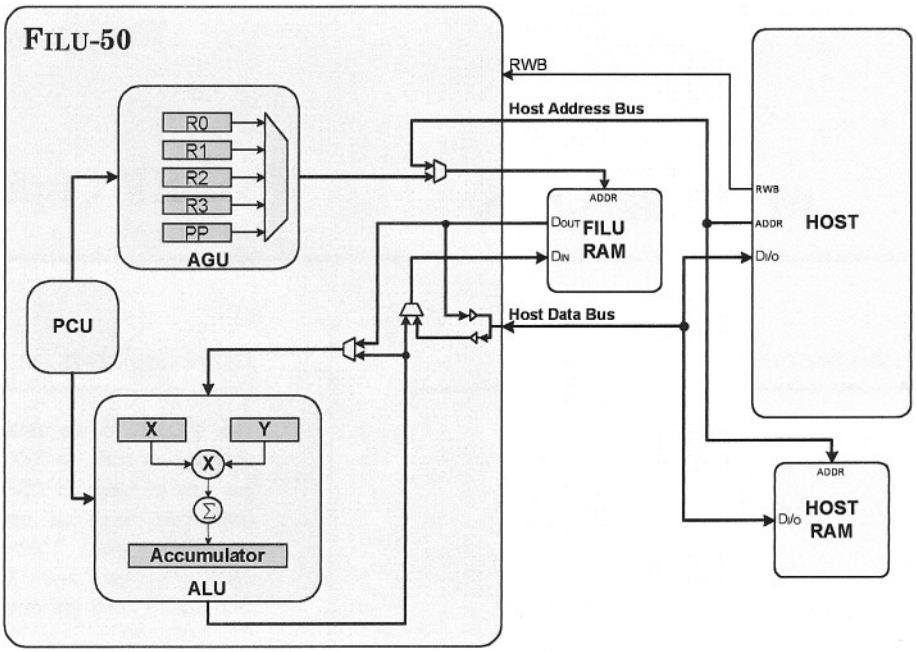

Figure 1 FILU-50 *block diagram and Host Interface.*

Benchmarks

The following benchmarks assume an 80 MHz clock.

Function	Data Points	Num of Coeff	Num of Cycles	Exec Time µs
Correlation	N =200	-	2N+8	5 µs
FIR	N =100	n = 20	N(2n+7)+5	59 µs
2nd Order IIR	N =100	4	12N+8	15 µs
M 2nd Order IIR	N = 100	M = 3	N(4+8M)+8	35 µs
Real FFT	N = 256	-	10368	130 µs

The FILU-50 has a MIPS capability competitive to standard 16-bit DSPs such as the TI 320C50, the DSP Group OakDspCore and the Motorola 56116.

Technical Specification

- Fully synthesizable – library independent
- FIR filter at 2 cycles per tap gives 50 MIPS with a 100 MHz clock
- 16-bit Architecture, 40-bit accumulation
- 7000 gates
- 0.35 mm^2 in 0.35 µm TLM.

Hardware & Software Interface

The FILU uses a very simple hardware and software interface. The FILU RAM is memory mapped into Host address space. An API allows the Host to use C function calls. These automatically generate the appropriate initialization vector for the RAM.

- Coefficients & data written as vectors in RAM, accessed with pointers
- A busy bit indicates start / end of processing
- Host has Master control of RAM via control / status bits in RAM

For More Information

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