

Figure 6. Quad MAC Single-Cycle Complex Multiply Architecture using Dual HCM-MACs

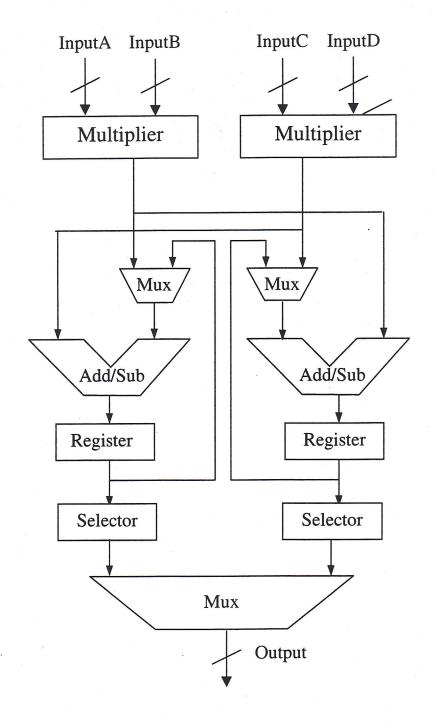


Figure 5. Dual Multiplier /
Dual Accumulator
(D/D-MAC) Execution Unit

ICSPAT 2000: Adam's Mark Hotel Dallas, Texas October 17-19, 2000 International Conference on Signal Processing Applications and Technology

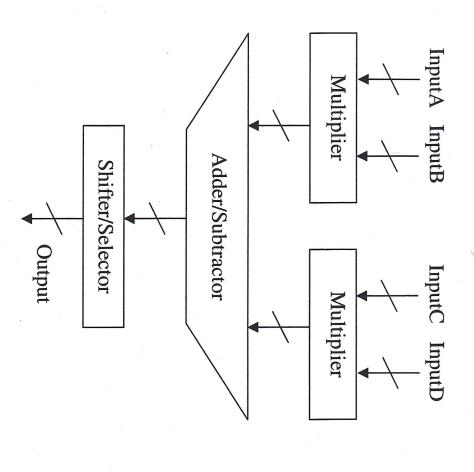


Figure 4. Half Complex Multiply (HCM-MAC) MAC Execution Unit

ICSPAT 2000: Adam's Mark Hotel Dallas, Texas October 17-19, 2000 International Conference on Signal Processing Applications and Technology