31 Asynchronous Sample Rate Converter (ASRC)

Sample rate converters (SRC) are frequently used in digital signal processing audio applications. The most frequently used sample rate conversions are off-loaded into hardware modules that are dedicated for filter processing and reduce the instruction processing load on the core, freeing it up for other tasks.

Features

The ASRC has the features shown in the list below.

- 4 Asynchronous stereo SRCs operating in slave mode are available in each DAI.
- Simple programming model.
- Controllable muting options (hardware, software and automatic).
- Automatically senses input and output sample frequencies.
- Supports left-justified, I^2S, right-justified (16-,18-, 20-, 24-bits), and TDM serial port modes.
- Daisy-chain configuration in TDM modes (including between DAI0 and DAI1) for input and output ports to create a serial frame.
- Different protocols on input/output port allow format conversions.
- De-emphasis filter for 32, 44.1 and 48 kHz sampling frequencies.
- Up to 192 kHz sample rate input/output continuous sample ratios from 7.5:1 to 1:8.
- Group delay (latency of interpolation filter) is 16 samples.
- SNR from 128 to 140 dB (depending on processor model).
- Matched phase mode available to compensate for group delays.
- Can be used to de-jitter clocks in systems.

ADSP-SC58x ASRC Register List

Sample Rate Converter Module

Table 1: ADSP-SC58x ASRC Register List

Name	Description
ASRC_CTL01	Control Register for ASRC 0 and 1
ASRC_CTL23	Control Register for ASRC 2 and 3
ASRC_MUTE	Mute Register
ASRC_RAT01	Ratio Register for ASRC 0 and 1
ASRC_RAT23	Ratio Register for ASRC 2 and 3

SRU Programming

The SRU (signal routing unit) needs to be programmed in order to connect the ASRCs to the output pins or any other peripherals.

Clocking

The ASRC module work on *SCLK0* clock domain. A internal divided version of *SCLK* clock is generated and used as fundamental clock for ASRC module.

Functional Description

Conceptually, the sample rate converter interpolates the serial input data at a rate of 220 and samples the interpolated data stream by the output sample rate. In practice, a 64-tap FIR filter with 220 polyphases, a FIFO, a digital servo loop that measures the time difference between the input and output samples within 5 ps, and a digital circuit to track the sample rate ratio are used to perform the interpolation and output sampling.

ASRC Block Diagram

The **ASRC Block Diagram** figure shows a top level block diagram of the ASRC module and the **Core Architecture** figure shows architecture details.

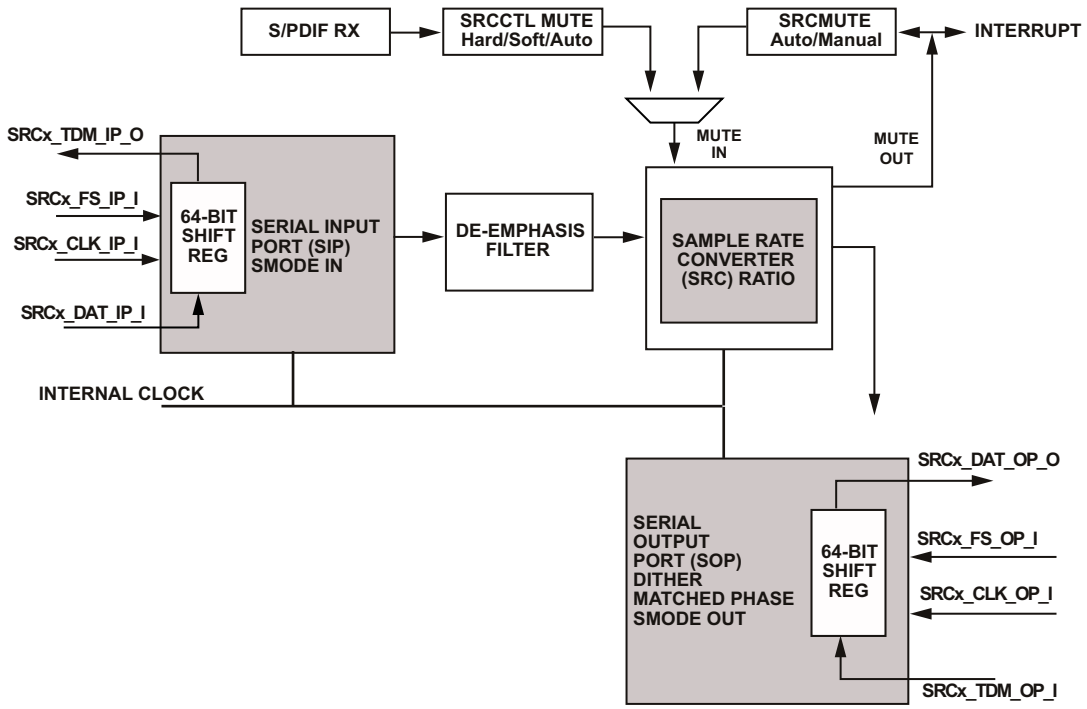

Figure 1: ASRC Block Diagram

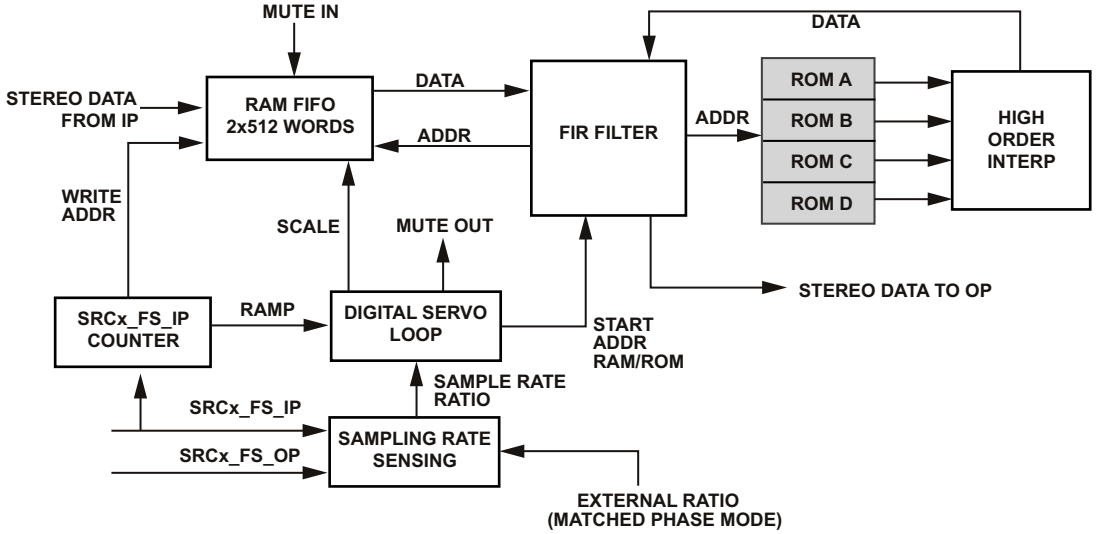

Figure 2: ASRC Core Architecture

I/O Ports

The I/O ports provide the interface through which data is transferred asynchronously into and out of the SRC modules. The SRC has a 3-wire interface for the serial input and output ports that supports left-justified, I^2S, and right-justified (16-, 18-, 20-, 24-bit) modes. Additionally, the serial interfaces support TDM mode for daisy-chaining multiple SRCs to form a frame. The serial output data is dithered down to 20, 18, or 16 bits when 20-, 18-, or 16-bit output data is selected.

NOTE: The SRC converts the data from the serial input port to the sample rate of the serial output port. The sample rate at the serial input port can be asynchronous with respect to the output sample rate of the output serial port.

De-Emphasis Filter

The de-emphasis filter is used to de-emphasize audio data that has been emphasized.

Mute Control

When either the SRC starts up (or there is a change in sample ratio), the mute out signal (SRCx_MUTEOUT) is asserted (=1). The mute out signal stays high until the SRC settles on the new sample rate(s). While mute out is asserted high, the mute in signal should be asserted high as well. The mute in signal performs a soft mute of the audio input data when asserted and un-mutes the input audio data softly when de-asserted.

Note that it takes 4096 input port FS samples until the audio input data is completely muted and 4096 FS samples until the audio input data is completely un-muted.

SRC Core

As shown in the **ASRC Core Architecture** figure, the sample rate converter's RAM FIFO block adjusts the left and right input samples and stores them for the FIR filter's convolution cycle. The ASRCx_FS_IP counter provides the write address (for scaling) to the FIFO block and the ramp input to the digital-servo loop. The ROM stores the coefficients for the FIR filter convolution and performs a high-order interpolation between the stored coefficients. The sample rate ratio block measures the sample rate by dynamically altering the ROM coefficients and scaling the FIR filter length and input data. The digital-servo loop automatically tracks the SRCx_FS_IP and SRCx_FS_OP sample rates and provides the RAM and ROM start addresses for the start of the FIR filter convolution.

NOTE: Unlike other peripherals, the sample rate converters own local memories (RAM and ROM) which are dedicated for the purpose of sample rate conversion only.

The sample rate converter only operates asynchronously and is always a slave to the input and output ports.

RAM FIFO

The RAM FIFO receives the left and right input data and adjusts the amplitude of the data for both the soft muting of the SRC and the scaling of the input data by the sample rate ratio before storing the samples in RAM. The input data is scaled by the sample rate ratio because as the FIR filter length of the convolution increases, so does the amplitude of the convolution output. To keep the output of the FIR filter from saturating, the input data is scaled down by multiplying it by (SRCx_FS_OP)/(SRCx_FS_IP) when SRCx_FS_OP<SRCx_FS_IP. The FIFO also scales the input data to mute and stop muting the SRC.

Digital Servo Loop

The digital-servo loop is essentially a ramp filter that provides the initial pointer to the address in RAM and ROM for the start of the FIR convolution. The RAM pointer is the integer output of the ramp filter while the ROM pointer is the fractional part. The digital-servo loop must be able to provide excellent rejection of jitter on the SRCx_FS_IP and SRCx_FS_OP clocks as well as measure the arrival of the SRCx_FS_OP clock within 5 ps. The digital-servo loop also divides the fractional part of the ramp output by the ratio of (SRCx_FS_IP)/(SRCx_FS_OP) for the case when SRCx_FS_IP> SRCx_FS_OP, to dynamically alter the ROM coefficients.

The digital-servo loop is implemented with a multi-rate filter. To settle the digital-servo loop filter quickly at startup or at a change in the sample rate, a fast mode has been added to the filter. When the digital-servo loop starts up or the sample rate is changed, the digital-servo loop kicks into fast mode to adjust and settle on the new sample rate. Upon sensing the digital-servo loop settling down to some reasonable value, the digital-servo loop kicks into normal or slow mode. During fast mode, the SRCx_MUTE_OUT bit of the ASRC is asserted to mute the ASRC input which avoids clicks and pops.

FIR Filter

The FIR filter is a 64-tap filter in the case of SRCx_FS_OP<SRCx_FS_IP and is (SRCx_FS_IP)/(SRCx_FS_OP) × 64 taps for the case when SRCx_FS_IP>SRCx_FS_OP. The FIR filter performs its convolution by loading in the starting address of the RAM address pointer and the ROM address pointer from the digital-servo loop at the start of the SRCx_FS_OP period. The FIR filter then steps through the RAM by decrementing its address by 1 for each tap, and the ROM pointer increments its address by the (SRCx_FS_OP/SRCx_FS_IP) × 2^{20} ratio for SRCx_FS_IP>SRCx_FS_OP or 2^{20} for SRCx_FS_OP<SRCx_FS_IP. Once the ROM address rolls over, the convolution is complete. The convolution is performed for both the left and right channels, and the multiply/accumulate circuit used for the convolution is shared between the channels.

Sample Rate Sensing

The (SRCx_FS_IP)/(SRCx_FS_OP) sample rate ratio circuit is used to dynamically alter the coefficients in the ROM for the case when SRCx_FS_IP>SRCx_FS_OP. The ratio is calculated by comparing the output of an SRCx_FS_OP counter to the output of an SRCx_FS_IP counter. If ASRCx_FS_OP>SRCx_FS_IP, the ratio is held at one. If SRCx_FS_IP>SRCx_FS_OP, the sample rate ratio is updated if it is different by more than two SRCx_FS_OP periods from the previous SRCx_FS_OP to SRCx_FS_IP comparison. This is done to provide some hysteresis to prevent the filter length from oscillating and causing distortion.

Digital Filter Group Delay

The RAM in the FIFO is 512 words deep for both left and right channels. An offset of 16 samples to the write address, provided by the SRCx_FS_IP counter, is added to prevent the RAM read pointer from overlapping the write address. The maximum decimation rate can be calculated from the RAM word is: depth = (512 - 16) ¸ 64 taps = 7.5:1.

The 64 samples effect latency in the interpolation filter. This latency (group delay) depends on interpolation or decimation ratio and is determined as follows:

Interpolation or Decimation Ratio (1): GDL = $16/f_{S\_IN} + 32/f_{S\_IN}$ seconds for SRC_FS_OP > SRC_FS_IP

Interpolation or Decimation Ratio (2): GDL = $16/f_{S\_IN} + 32/f_{S\_IN} \times f_{S\_IN}/f_{S\_OUT}$ seconds for SRC_FS_OP <SRC_FS_IP

Data Format

The **ASRC Data Frame Format by Protocol** figure shows the data input format for a frame (stereo data). The frame format is valid for all protocols. For models which do not support matched phase mode the 8-bit data field is ignored.

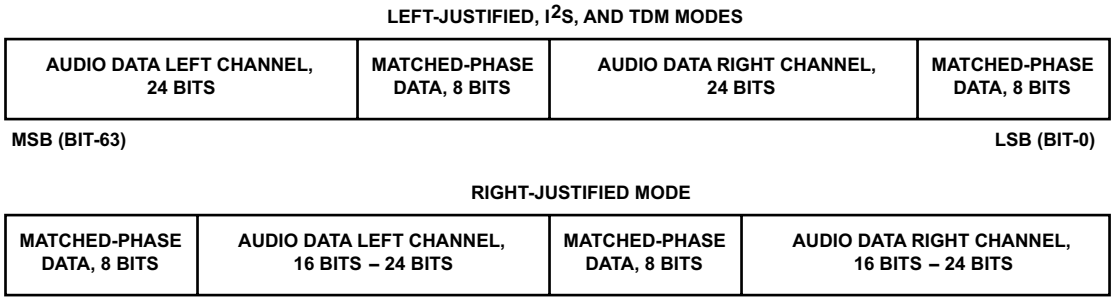

Figure 3: ASRC Data Frame Format by Protocol

Operating Modes

The ASRC can operate in TDM, I^2S, left-justified, right-justified, and bypass modes. The serial ports of the processor can be used for moving the ASRC data to/from the internal memory.

In I^2S, left-justified and right-justified modes, the ASRCs operate individually. The serial data provided in the input port is converted to the sample rate of the output port.

TDM Input Mode

In TDM input port, several ASRCs can be daisy-chained together and connected to the serial input port of a SHARC processor or other processor (see the **TDM Input/Output Modes** figure). The ASRC IP contains

a 64-bit parallel load shift register. When the SRCx_FS_IP_I pulse arrives, each ASRC parallel loads its left and right data into the 64-bit shift register. The input to the shift register is connected to SRCx_DATA_IP_I, while the output is connected to SRCx_TDM_IP_O. By connecting the SRCx_TDM_IP_O to the SRCx_DATA_IP_I of the next ASRC, a large shift register is created, which is clocked by SRCx_CLK_IP_I.

NOTE: The number of ASRCs that can be daisy-chained together is limited by the maximum frequency of SRCx_CLK_xx_I, refer to the data sheet for exact values. For example, if the maximum frequency of SRCx_CLK_xx_I is *x* MHz, and the output sample rate is *fS*, then number of ASRCs (n) that can be connected in daisy chained fashion is: n 64 FS <= *x* MHz.

TDM Output Mode

As shown in the **TDM Input/Output Modes** figure, using the TDM output port several ASRCs can be daisy-chained together and connected to the SPORT of this or another processor. The ASRC OP contains a 64-bit parallel load shift register. When the ASRCx_FS_OP_I pulse arrives, each ASRC loads its left and right data into the 64-bit shift register. The input to the shift register is connected to ASRCx_TDM_OP_I, and the output is connected to SRCx_DAT_OP_O. By connecting the SRCx_DAT_OP_O to the ASRCx_TDM_OP_I of the next ASRC, a large shift register is created, which is clocked by SRCx_CLK_OP_I.

As shown in **TDM Input/Output Modes**, with three ASRCs in a daisy-chain connection, the serial clock for input/or output port is defined as: *SCLK* = 3 × 64 FS = 192 FS

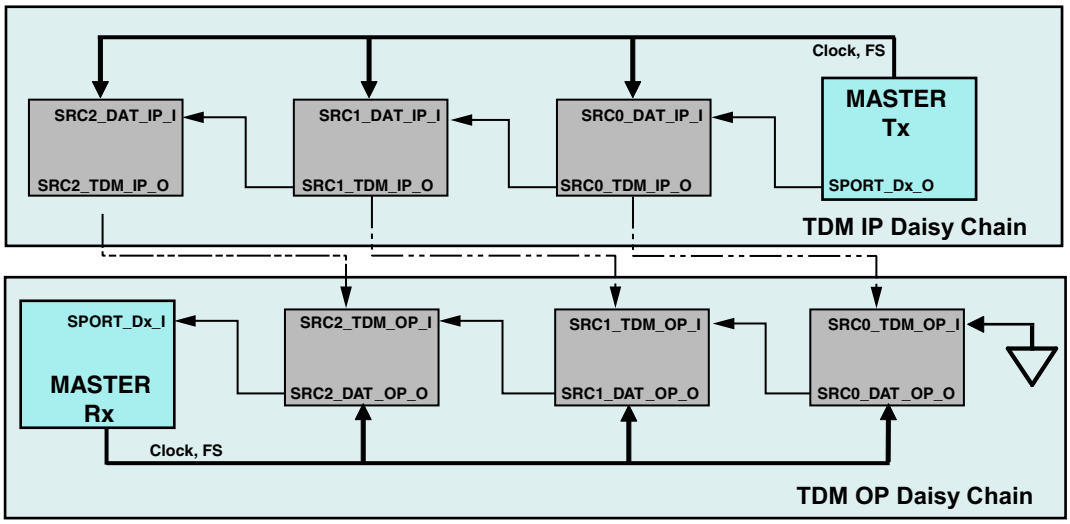

Figure 4: TDM Input/Output Modes

Matched-Phase Mode

The matched phase mode of the sample rate converter, shown in **Typical Configuration for Matched-Phase Mode Operation**, is enabled by the ASRC_CTL01.MPHASE1 through ASRC_CTL23.MPHASE3 bits. This mode is used to match the phase (group delay) between two or more adjacent sample rate converters that are operating with the same input and output clocks.

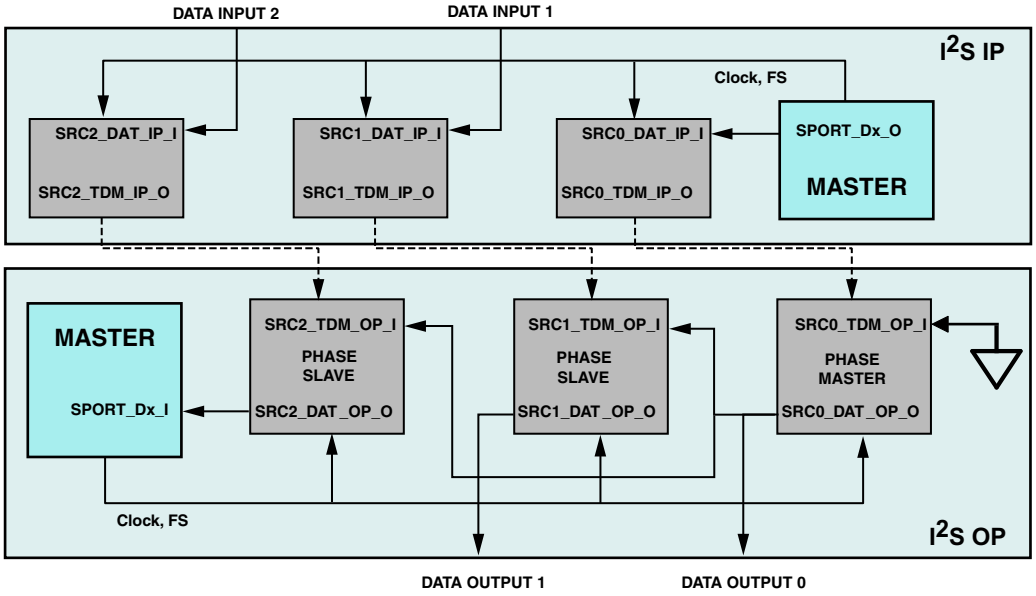

Figure 5: Typical Configuration for Matched-Phase Mode Operation

Hysteresis of the (SRCx_FS_OP)/(SRCx_FS_IP) ratio circuit can cause phase mismatching between two ASRCs operating with the same input and output clocks. Since the hysteresis requires a difference of more than two SRCx_FS_OP periods to update the SRCx_FS_OP and SRCx_FS_IP ratios, two ASRCs may have differences in their ratios from 0 to 4 SRCx_FS_OP period counts. The (SRCx_FS_OP)/(SRCx_FS_IP) ratio adjusts the filter length of the ASRC, which corresponds directly with the group delay. Thus, the magnitude in the phase difference depends upon the resolution of theSRCx_FS_OP and SRCx_FS_IPcounters. The greater the resolution of the counters, the smaller the phase difference error.

When the slave SRC MPHASE bit is set (=1), it accepts the sample rate ratio transmitted by another SRC, (the matched phase master) which has its MPHASE bit cleared (=0), through its serial output.

The phase master ASRC device transmits its SRCx_FS_OP/SRCx_FS_IP ratio through the data output pin (SRCx_DAT_OP_O) to the slave's ASRC's data input pins (SRCx_TDM_OP_I). The transmitted data (32-bit subframe) contains 24-bit data and 8-bits matched phase (see the **ASRC Data Frame Format by Protocol** figure).

The slave SRCs receive the 8-bit matched phase bits (instead of their own internally-derived ratio) if their SRCx_MPHASE bits set to 1, respectively. The SRCx_FS_IP and SRCx_FS_OP signals may be asynchronous with respect to each other in this mode. Note that there must be 64 SRCx_CLK_OP cycles per frame in matched-phase mode (2 24-bits data and 2 8-bits phase match).

NOTE: By default, matched phased data is sent on the SRCx_DAT_OP_O pin, but only if the SRCx_TDM_OP_I pin is tied low. The slaves simply ignore the matched phased data if their ASRC_CTL01.MPHASE1 through ASRC_CTL23.MPHASE3 bits are cleared (= 0).

Bypass Mode

When the ASRC_CTL01.BYP0 through ASRC_CTL23.BYP3 bits are set (=1), the input data bypasses the sample rate converter and is sent directly to the serial output port. Dithering is disabled. This mode is ideal when the input and output sample rates are the same and SRCx_FS_IP_I and SRCx_FS_OP_I are synchronous with respect to each other. In matched phase bypass mode, the SRCx_FS_OP_I should come at least one SRCx_CLK_xx_I period before SRCx_FS_IP_I. Cases where this is not met could result in data loss. For example, if internal SPORTS are used then SRCx_FS_OP_I and SRCx_FS_IP_I could be driven by different SPORTS so that the timing of these signals could be controlled by enabling them at different times. This mode can also be used for passing through non-audio data since no processing is performed on the input data.

De-Emphasis Mode

The ASRC_CTL01.DEEMPHASIS0 through ASRC_CTL23.DEEMPHASIS3 bits choose the type of de-emphasis filter based on the input sample rate for 32, 44.1 or 48 kHz sampling rates.

Dithering Mode

Serial output data is dithered[1]down to 20, 18, or 16 bits when 20-, 18-, or 16-bit output data is selected. In the case of 20-, 18- and 16-bit word lengths, the least significant bits of the 24-bit word coming from the SRC into the serial output port are truncated. The DITHER_EN signal (not user configurable) automatically adds dithering to the 24-bit word before truncating to the appropriate output word length. The 21BIT_DITHER signal is used for the consumer version of the SRC to reduce the dynamic range performance to approximately 128 dB.

Muting Modes

The mute feature of the ASRC can be controlled automatically in hardware using the MUTE_IN signal by connecting it to the MUTE_OUT signal. Automatic muting can be disabled by setting (=1) the ASRC_MUTE.MUTE0 throughASRC_MUTE.MUTE3 bits.

NOTE: Note that by default, the ASRC_MUTE register connects the MUTE_IN signal to the MUTE_OUT signal, but not vice versa.

Soft Mute

When the ASRC_CTL01.SOFTMUTE0 throughASRC_CTL23.SOFTMUTE3 bits are set, the MUTE_IN signal is asserted, and the ASRC performs a soft mute by linearly decreasing the input data to the ASRC FIFO to zero, (-144 dB) attenuation as described for automatic hardware muting.

1.The ASRC can be programmed to add triangular Probability Distribution Function (PDF) dither to the digital audio samples. It is advisable to add dither when the input word width exceeds the output word width, for example the input word is 20 bits and the output word is 16 bits. Triangular PDF is generally considered to create the most favorable noise shaping of the residual quantization noise.

A 12-bit counter, clocked by SRCx_FS_IP_I, is used to control the mute attenuation. Therefore, the time it takes from the assertion of MUTE_IN to -144 dB, full mute attenuation is 4096 FS cycles.Likewise, the time it takes to reach 0 dB mute attenuation from the deassertion of MUTE_IN is 4096 FS cycles.

Hard Mute

When the ASRC_CTL01.HARDMUTE0 through ASRC_CTL23.HARDMUTE3 bits are set, the ASRC immediately mutes the input data to the ASRC FIFO to zero, (-144 dB) attenuation.

Auto Mute

When the ASRC_CTL01.AUTOMUTE0 throughASRC_CTL23.AUTOMUTE3 bits are set, the ASRC communicates with the S/PDIF receiver peripheral to determine when the input should mute.

This mode is useful for automatic detection of non-PCM audio data received from the S/PDIF receiver.

Interrupts

The **Overview of ASRC Interrupts** table provides an overview of ASRC interrupts

Table 2: Overview of ASRC Interrupts

Default Programmable Interrupt	Sources	Masking	Service
INTR_DAI_IRQH INTR_DAI_IRQL	ASRC initialization ASRC sample rate change	DAIn_IMASK_x	ROC from DAIn_IRPTL_x + RTI instruction

Sources

Each ASRC module drives one interrupt signal (mute out asserted). All these signals are connected into the DAI_IRPTL_H or DAI_IRPTL_L latch registers. The ASRC ports generate interrupts as described below.

SRC Mute Out

The SRC mute-out signal can be used to generate interrupts on their rising edge, falling edge, or both, depending on how the DAI interrupt mask registers (DAI_IMSK_RE/DAI_IMSK_FE) are programmed. This allows the generation of DAI_IRPTL_H/DAI_IRPTL_L interrupts either entering mute, exiting muting or both. The SRCx_MUTE_OUT interrupt is generated only once when the SRC is locked (after 4096 FS input samples) and after changes to the sample ratio. Hard mute, soft mute, and auto mute only control the muting of the input data to the SRC.

Masking

The DAI_IMSK_FE, DAI_IMSK_RE, and DAI_IMSK_PRI registers must be unmasked accordingly. The DAI_IRQH and DAI_IRQL signals are routed to the system event controller (SEC) and general interrupt controller (GIC).

Service

The ISR reads the DAI_IRPTL_H and DAI_IRPTL_L registers to clear the interrupt request.

Effect Latency

The total effect latency is a combination of the write effect latency (core access) plus the peripheral effect latency (peripheral specific).

Programming Model

The following is basic information on programming the ASRC module.

1. Program the ASRC_CTL01 and ASRC_CTL23 registers and keep the ASRC_CTL01.EN0 through ASRC_CTL23.EN3 bits cleared.
2. Set the ASRC_CTL01.EN0 throughASRC_CTL23.EN3 bits. After 4096 input port FS cycles the ASRC has un-muted.

Debug Features

The asynchronous sample rate converter allow the bypass mode. When the ASRC_CTL01.BYP0 throughASRC_CTL23.BYP3 bits are set (=1), the input data bypasses the sample rate converter and is sent directly to the serial output port. This mode can be used for testing both ports when the input and output sample rates are at the same frequency, therefore both in- and output ports can be routed to the same serial clock and frame sync.

ADSP-SC58x ASRC Register Descriptions

Sample Rate Converter Module (ASRC) contains the following registers.

Table 3: ADSP-SC58x ASRC Register List

Name	Description
ASRC_CTL01	Control Register for ASRC 0 and 1
ASRC_CTL23	Control Register for ASRC 2 and 3
ASRC_MUTE	Mute Register
ASRC_RAT01	Ratio Register for ASRC 0 and 1
ASRC_RAT23	Ratio Register for ASRC 2 and 3

Control Register for ASRC 0 and 1

The ASRC_CTL01 register (read/write) controls the operating modes, filters, and data formats used in the ASRC modules 0 and 1.

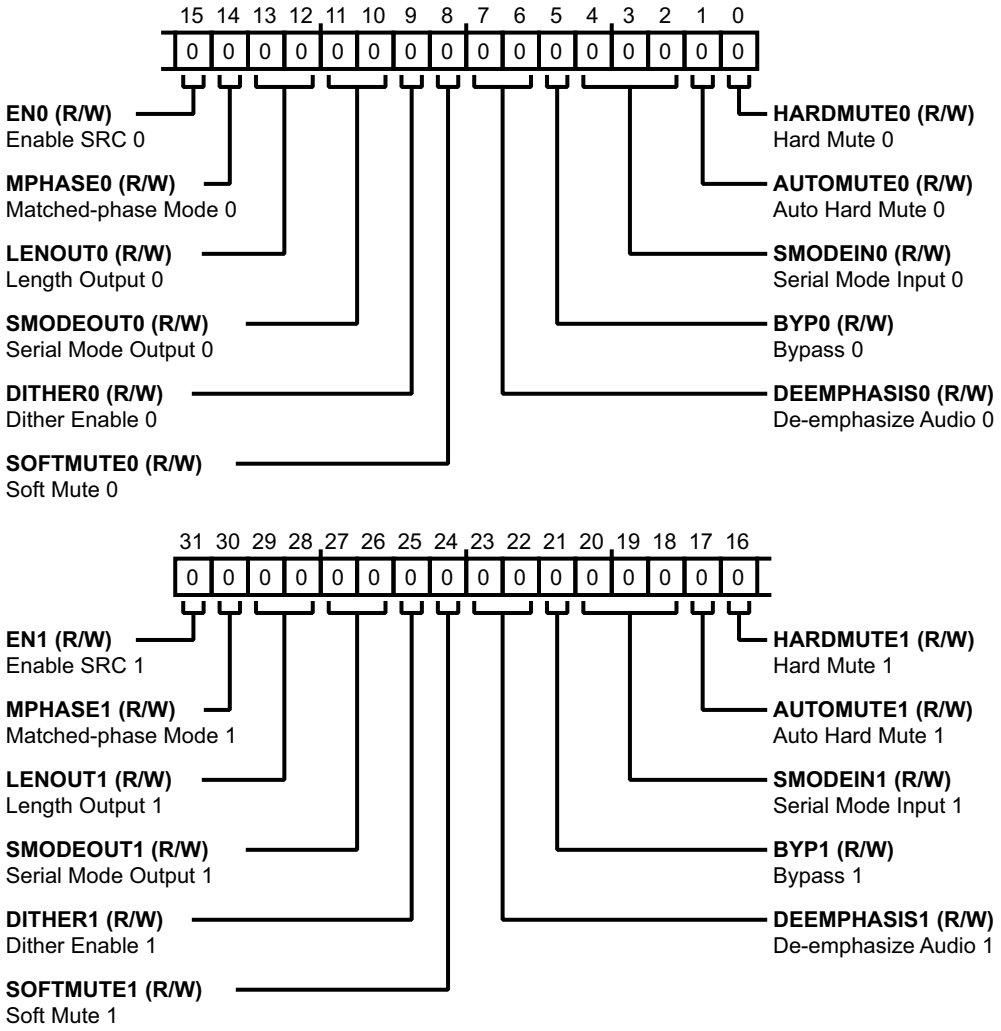

Figure 6: ASRC_CTL01 Register Diagram

Table 4: ASRC_CTL01 Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration
31 (R/W)	EN1	Enable SRC 1. The ASRC_CTL01.EN1 bit enables SRC 1. When (set = 1), or when the sample rate (frame sync) between the input and output changes, the SRC begins its initialization routine where; 1) MUTE_OUT is asserted, 2) soft mute control counter for input samples is set to maximum attenuation (144 dB). Note that SRC power-up completion is finished by clearing the ASRC_RAT01.MUTEOUT1 bit. Writes to the ASRC_CTL01 register should be at least one cycle before setting the ASRC_CTL01.EN1 bit. When setting and clearing this bit, it should be held low for a minimum of 5 SCLK cycles.

Table 4: ASRC_CTL01 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
30 (R/W)	MPHASE1	Matched-phase Mode 1. The ASRC_CTL01.MPHASE1 bit configures SRC1 to not use its own internally-generated sample rate ratio but use an externally-generated ratio. Used with TDM data.	
		0	Matched phase slave disabled
		1	Matched phase slave enabled
29:28 (R/W)	LENOUT1	Length Output 1. The ASRC_CTL01.LENOUT1 bit field selects the serial output word length on SRC1.	
		0	24 bits
		1	20 bits
		2	18 bits
		3	16 bits
27:26 (R/W)	SMODEOUT1	Serial Mode Output 1. The ASRC_CTL01.SMODEOUT1 bit field selects the serial output format on SRC1.	
		0	Left-justified
		1	I2S
		2	TDM
		3	Right-justified
25 (R/W)	DITHER1	Dither Enable 1. The ASRC_CTL01.DITHER1 bit enables dithering before truncation on SRC1 when a word length less than 24 bits is selected.	
		0	Truncation only
		1	Dithering before truncation
24 (R/W)	SOFTMUTE1	Soft Mute 1. The ASRC_CTL01.SOFTMUTE1 bit enables soft mute on SRC1.	
		0	Unmute
		1	Mute
23:22 (R/W)	DEEMPHASIS1	De-emphasize Audio 1. The ASRC_CTL01.DEEMPHASIS1 bits are used to de-emphasize audio data that has been emphasized. The type of de-emphasis filter is based on the input sample rate (SRCx_FS_IP_I signal).	
		0	No de-emphasis
		1	32 kHz
		2	44.1 kHz
		3	48 kHz
21 (R/W)	BYP1	Bypass 1. The ASRC_CTL01.BYP1 bit makes the output of SRC1 the same as the input.	

Table 4: ASRC_CTL01 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
20:18 (R/W)	SMODEIN1	Serial Mode Input 1. The ASRC_CTL01.SMODEIN1 bit field selects the serial input format for SRC1.	
		0	left-justified
		1	I2S
		2	TDM
		4	24-bit right-justified
		5	20-bit right-justified
		6	18-bit right-justified
		7	16-bit right-justified
17 (R/W)	AUTOMUTE1	Auto Hard Mute 1. The ASRC_CTL01.AUTOMUTE1 bit auto hard mutes SRC1 when non audio is asserted by the SPDIF receiver.	
		0	Unmute
		1	Mute
16 (R/W)	HARDMUTE1	Hard Mute 1. The ASRC_CTL01.HARDMUTE1 bit hard mutes SRC1.	
		0	Unmute
		1	Mute
15 (R/W)	EN0	Enable SRC 0. The ASRC_CTL01.EN0 bit enables SRC 0. When (set =1), or when the sample rate (frame sync) between the input and output changes, the SRC begins its initialization routine where; 1) MUTE_OUT is asserted, 2) soft mute control counter for input samples is set to maximum attenuation (144 dB). Note that SRC power-up completion is finished by clearing the ASRC_RAT01.MUTEOUT0 bit. Writes to the ASRC_CTL01 register should be at least one cycle before setting the ASRC_CTL01.EN0 bit. When setting and clearing this bit, it should be held low for a minimum of 5 CLK cycles.	
14 (R/W)	MPHASE0	Matched-phase Mode 0. The ASRC_CTL01.MPHASE0 bit configures SRC0 to not use its own internally-generated sample rate ratio but use an externally-generated ratio. Used with TDM data.	
		0	Matched phase slave disabled
		1	Matched phase slave enabled

Table 4: ASRC_CTL01 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
13:12 (R/W)	LENOUT0	Length Output 0. The ASRC_CTL01.LENOUT0 bit field selects the serial output word length on SRC0.	
		0	24 bits
		1	20 bits
		2	18 bits
		3	16 bits
11:10 (R/W)	SMODEOUT0	Serial Mode Output 0. The ASRC_CTL01.SMODEOUT0 bit field selects the serial output format on SRC0.	
		0	Left-justified
		1	I2S
		2	TDM
		3	Right-justified
9 (R/W)	DITHER0	Dither Enable 0. The ASRC_CTL01.DITHER0 bit enables dithering before truncation on SRC0 when a word length less than 24 bits is selected.	
		0	Truncation only
		1	Dithering before truncation
8 (R/W)	SOFTMUTE0	Soft Mute 0. The ASRC_CTL01.SOFTMUTE0 bit enables soft mute on SRC0.	
		0	Unmute
		1	Mute
7:6 (R/W)	DEEMPHASIS0	De-emphasize Audio 0. The ASRC_CTL01.DEEMPHASIS0 bits are used to de-emphasize audio data that has been emphasized. The type of de-emphasis filter is based on the input sample rate (SRCx_FS_IP_I signal).	
		0	No de-emphasis
		1	32 kHz
		2	44.1 kHz
		3	48 kHz
5 (R/W)	BYP0	Bypass 0. The ASRC_CTL01.BYP0 bit makes the output of SRC0 the same as the input.	

Table 4: ASRC_CTL01 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
4:2 (R/W)	SMODEIN0	Serial Mode Input 0. The ASRC_CTL01.SMODEIN0 bit field selects the serial input format for SRC0.	
		0	left-justified
		1	I2S
		2	TDM
		4	24-bit right-justified
		5	20-bit right-justified
		6	18-bit right-justified
		7	16-bit right-justified
1 (R/W)	AUTOMUTE0	Auto Hard Mute 0. The ASRC_CTL01.AUTOMUTE0 bit auto hard mutes SRC0 when non audio is asserted by the SPDIF receiver.	
		0	Unmute
		1	Mute
0 (R/W)	HARDMUTE0	Hard Mute 0. The ASRC_CTL01.HARDMUTE0 bit hard mutes SRC0.	
		0	Unmute
		1	Mute (default)

Control Register for ASRC 2 and 3

The ASRC_CTL23 register (read/write) controls the operating modes, filters, and data formats used in the sample rate converter modules 2 and 3.

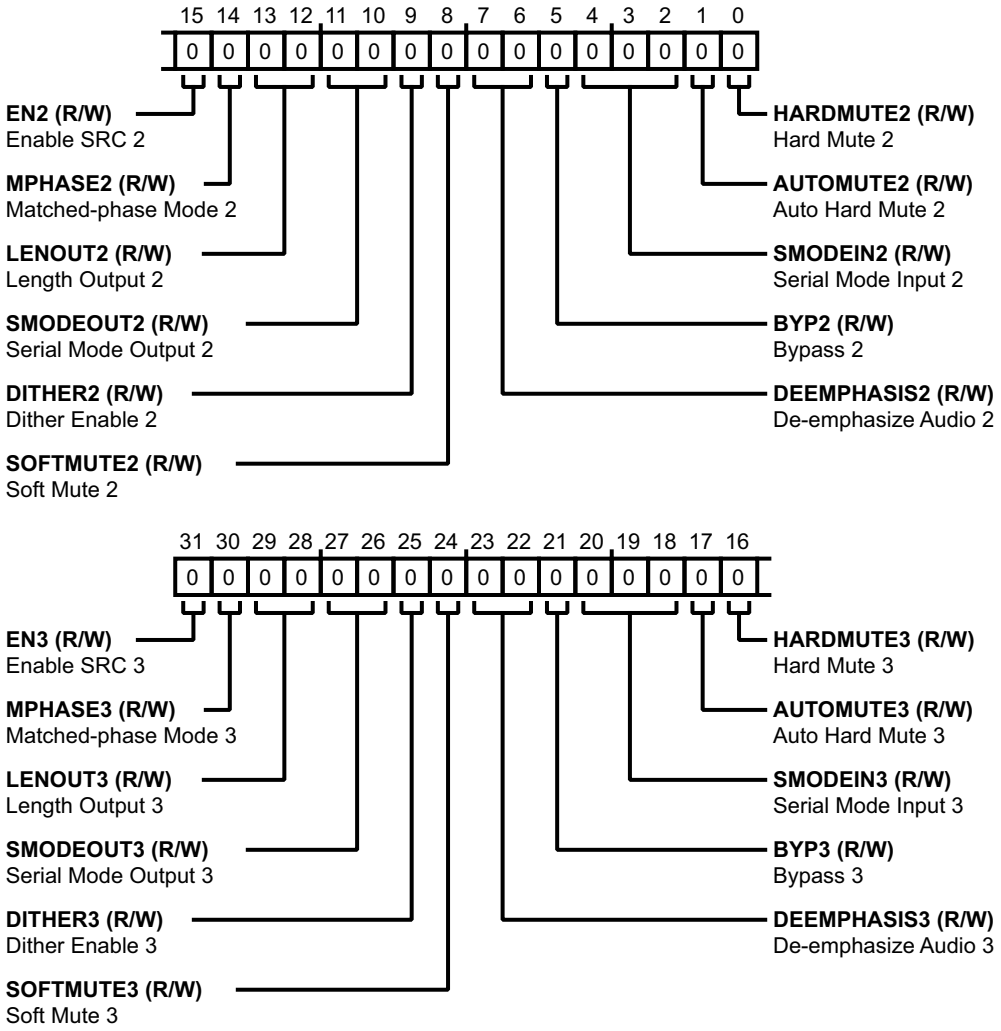

Figure 7: ASRC_CTL23 Register Diagram

Table 5: ASRC_CTL23 Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration
31 (R/W)	EN3	Enable SRC 3. The ASRC_CTL23.EN3 bit enables SRC 3. When (set =1), or when the sample rate (frame sync) between the input and output changes, the SRC begins its initialization routine where; 1) MUTE_OUT is asserted, 2) soft mute control counter for input samples is set to maximum attenuation (144 dB). Note that SRC power-up completion is finished by clearing the ASRC_RAT23.MUTEOUT3 bit. Writes to the ASRC_CTL23 register should be at least one cycle before setting the ASRC_CTL23.EN3 bit. When setting and clearing this bit, it should be held low for a minimum of 5 CLK cycles.

Table 5: ASRC_CTL23 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
30 (R/W)	MPHASE3	Matched-phase Mode 3. The ASRC_CTL23.MPHASE3 bit configures SRC3 to not use its own internally-generated sample rate ratio but use an externally-generated ratio. Used with TDM data.	
		0	Matched phase slave disabled
		1	Matched phase slave enabled
29:28 (R/W)	LENOUT3	Length Output 3. The ASRC_CTL23.LENOUT3 bit field selects the serial output word length on SRC3.	
		0	24 bits
		1	20 bits
		2	18 bits
		3	16 bits
27:26 (R/W)	SMODEOUT3	Serial Mode Output 3. The ASRC_CTL23.SMODEOUT3 bit field selects the serial output format on SRC3.	
		0	Left-justified
		1	I2S
		2	TDM
		3	Right-justified
25 (R/W)	DITHER3	Dither Enable 3. The ASRC_CTL23.DITHER3 bit enables dithering before truncation on SRC3 when a word length less than 24 bits is selected.	
		0	Truncation only
		1	Dithering before truncation
24 (R/W)	SOFTMUTE3	Soft Mute 3. The ASRC_CTL23.SOFTMUTE3 bit enables soft mute on SRC3.	
		0	Unmute
		1	Mute
23:22 (R/W)	DEEMPHASIS3	De-emphasize Audio 3. The ASRC_CTL23.DEEMPHASIS3 bits are used to de-emphasize audio data that has been emphasized. The type of de-emphasis filter is based on the input sample rate (SRCx_FS_IP_I signal).	
		0	No de-emphasis
		1	32 kHz
		2	44.1 kHz
		3	48 kHz
21 (R/W)	BYP3	Bypass 3. The ASRC_CTL23.BYP3 bit makes the output of SRC3 the same as the input.	

Table 5: ASRC_CTL23 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
20:18 (R/W)	SMODEIN3	Serial Mode Input 3. The ASRC_CTL23.SMODEIN3 bit field selects the serial input format for SRC3.	
		0	left-justified
		1	I2S
		2	TDM
		4	24-bit right-justified
		5	20-bit right-justified
		6	18-bit right-justified
		7	16-bit right-justified
17 (R/W)	AUTOMUTE3	Auto Hard Mute 3. The ASRC_CTL23.AUTOMUTE3 bit auto hard mutes SRC3 when non audio is asserted by the SPDIF receiver.	
		0	Unmute
		1	Mute
16 (R/W)	HARDMUTE3	Hard Mute 3. The ASRC_CTL23.HARDMUTE3 bit hard mutes SRC3.	
		0	Unmute
		1	Mute
15 (R/W)	EN2	Enable SRC 2. The ASRC_CTL23.EN2 bit enables SRC 2. When (set =1), or when the sample rate (frame sync) between the input and output changes, the SRC begins its initialization routine where; 1) MUTE_OUT is asserted, 2) soft mute control counter for input samples is set to maximum attenuation (144 dB). Note that SRC power-up completion is finished by clearing the ASRC_RAT23.MUTEOUT2 bit. Writes to the ASRC_CTL23 register should be at least one cycle before setting the ASRC_CTL23.EN2 bit. When setting and clearing this bit, it should be held low for a minimum of 5 CLK cycles.	
14 (R/W)	MPHASE2	Matched-phase Mode 2. The ASRC_CTL23.MPHASE2 bit configures SRC2 to not use its own internally-generated sample rate ratio but use an externally-generated ratio. Used with TDM data.	
		0	Matched phase slave disabled
		1	Matched phase slave enabled

Table 5: ASRC_CTL23 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
13:12 (R/W)	LENOUT2	Length Output 2. The ASRC_CTL23.LENOUT2 bit field selects the serial output word length on SRC2.	
		0	24 bits
		1	20 bits
		2	18 bits
		3	16 bits
11:10 (R/W)	SMODEOUT2	Serial Mode Output 2. The ASRC_CTL23.SMODEOUT2 bit field selects the serial output format on SRC2.	
		0	Left-justified
		1	I2S
		2	TDM
		3	Right-justified
9 (R/W)	DITHER2	Dither Enable 2. The ASRC_CTL23.DITHER2 bit enables dithering before truncation on SRC2 when a word length less than 24 bits is selected.	
		0	Truncation only
		1	Dithering before truncation
8 (R/W)	SOFTMUTE2	Soft Mute 2. The ASRC_CTL23.SOFTMUTE2 bit enables soft mute on SRC2.	
		0	Unmute
		1	Mute
7:6 (R/W)	DEEMPHASIS2	De-emphasize Audio 2. The ASRC_CTL23.DEEMPHASIS2 bits are used to de-emphasize audio data that has been emphasized. The type of de-emphasis filter is based on the input sample rate (SRCx_FS_IP_I signal).	
		0	No de-emphasis
		1	32 kHz
		2	44.1 kHz
		3	48 kHz
5 (R/W)	BYP2	Bypass 2. The ASRC_CTL23.BYP2 bit makes the output of SRC2 the same as the input.	

Table 5: ASRC_CTL23 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration	
4:2 (R/W)	SMODEIN2	Serial Mode Input 2. The ASRC_CTL23.SMODEIN2 bit field selects the serial input format for SRC2.	
		0	left-justified
		1	I2S
		2	TDM
		4	24-bit right-justified
		5	20-bit right-justified
		6	18-bit right-justified
		7	16-bit right-justified
1 (R/W)	AUTOMUTE2	Auto Hard Mute 2. The ASRC_CTL23.AUTOMUTE2 bit auto hard mutes SRC2 when non audio is asserted by the SPDIF receiver.	
		0	Unmute
		1	Mute
0 (R/W)	HARDMUTE2	Hard Mute 2. The ASRC_CTL23.HARDMUTE2 bit hard mutes SRC2.	
		0	Unmute
		1	Mute

Mute Register

This register connects an ASRCx mute input and output when the mute bit is cleared (=0). This allows ASRCx to automatically mute input while the ASRC is initializing (0 = automatic muting and 1 = manual muting). Bit 0 controls ASRC0, bit 1 controls ASRC1, bit 2 controls ASRC2, and bit 3 controls ASRC3.

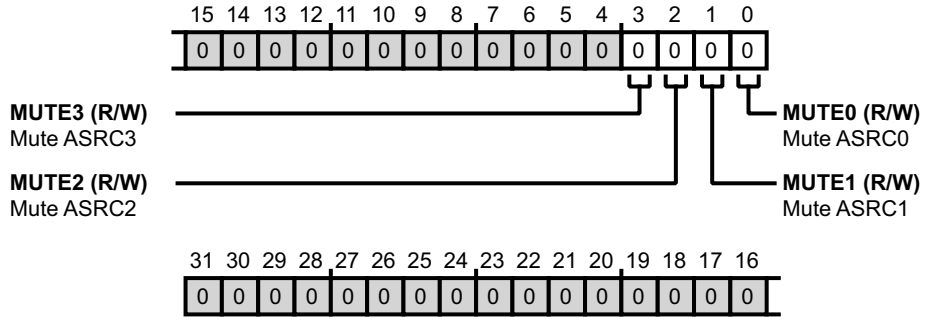

Figure 8: ASRC_MUTE Register Diagram

Table 6: ASRC_MUTE Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration
3 (R/W)	MUTE3	Mute ASRC3. The ASRC_MUTE.MUTE3 bit automatically mutes ASCR3 output when cleared (=0).
2 (R/W)	MUTE2	Mute ASRC2. The ASRC_MUTE.MUTE2 bit automatically mutes ASCR2 output when cleared (=0).
1 (R/W)	MUTE1	Mute ASRC1. The ASRC_MUTE.MUTE1 bit automatically mutes ASCR1 output when cleared (=0).
0 (R/W)	MUTE0	Mute ASRC0. The ASRC_MUTE.MUTE0 bit automatically mutes ASCR0 output when cleared (=0).

Ratio Register for ASRC 0 and 1

The ASRC_RAT01 register report the mute and I/O sample ratio for ASRC0 and ASRC1.

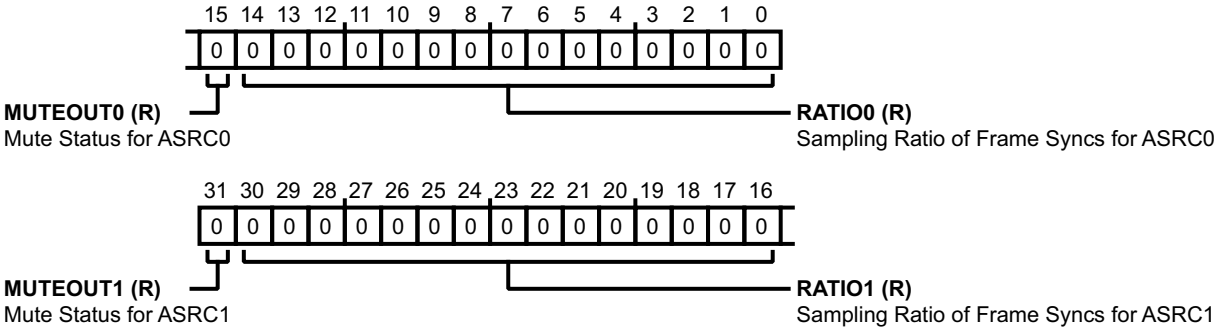

Figure 9: ASRC_RAT01 Register Diagram

Table 7: ASRC_RAT01 Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration
31 (R/NW)	MUTEOUT1	Mute Status for ASRC1. The ASRC_RAT01.MUTEOUT1 bit field reports the status of the MUTE_OUT signal. Once the SRCx_MUTEOUT signal is cleared, the ratio can be read. When ASRC1 is enabled or there is a change in the sample ratio, the MUTE_OUT signal is asserted. The MUTE_OUT signal remains asserted until the digital servo loops internal fast settling mode is complete. When the digital servo loop has switched to slow settling mode, the MUTE_OUT signal is deasserted.

Table 7: ASRC_RAT01 Register Fields (Continued)

Bit No. (Access)	Bit Name	Description/Enumeration
30:16 (R/NW)	RATIO1	Sampling Ratio of Frame Syncs for ASRC1. The ASRC_RAT01.RATIO1 bit field is read to find the ratio of output to input sampling frequency for ASRC1 (SRCx_FS_OP_I/SRCx_FS_IP_I). This ratio is reported in 4.11 (integer.fraction) format where the 15-bit value of the normal binary number is comprised of 4 bits for the integer and 11 bits for the fraction.
15 (R/NW)	MUTEOUT0	Mute Status for ASRC0. The ASRC_RAT01.MUTEOUT0 bit field reports the status of the MUTE_OUT signal. Once the SRCx_MUTEOUT signal is cleared, the ratio can be read. When ASRC0 is enabled or there is a change in the sample ratio, the MUTE_OUT signal is asserted. The MUTE_OUT signal remains asserted until the digital servo loops internal fast settling mode is complete. When the digital servo loop has switched to slow settling mode, the MUTE_OUT signal is deasserted.
14:0 (R/NW)	RATIO0	Sampling Ratio of Frame Syncs for ASRC0. The ASRC_RAT01.RATIO0 bit field is read to find the ratio of output to input sampling frequency for ASRC0 (SRCx_FS_OP_I/SRCx_FS_IP_I). This ratio is reported in 4.11 (integer.fraction) format where the 15-bit value of the normal binary number is comprised of 4 bits for the integer and 11 bits for the fraction.

Ratio Register for ASRC 2 and 3

The ASRC_RAT23 register report the mute and I/O sample ratio for ASRC0 and ASRC1.

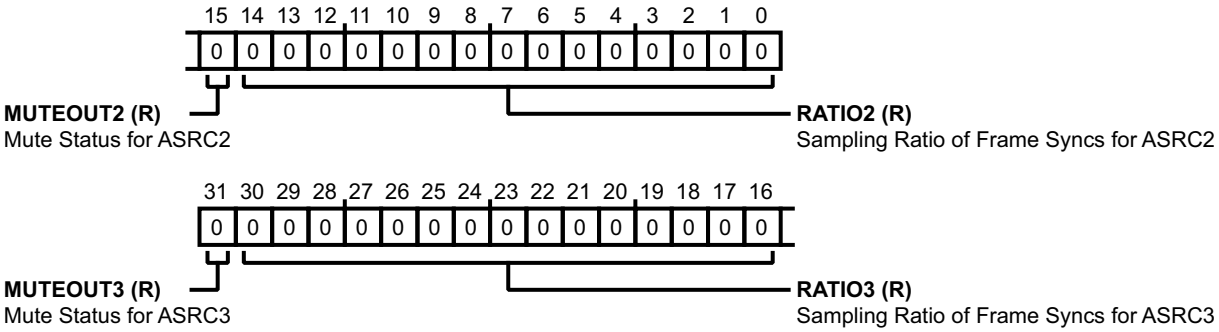

Figure 10: ASRC_RAT23 Register Diagram

Table 8: ASRC_RAT23 Register Fields

Bit No. (Access)	Bit Name	Description/Enumeration
31 (R/NW)	MUTEOUT3	Mute Status for ASRC3. The ASRC_RAT23.MUTEOUT3 bit field reports the status of the MUTE_OUT signal. Once the SRCx_MUTEOUT signal is cleared, the ratio can be read. When ASRC3 is enabled or there is a change in the sample ratio, the MUTE_OUT signal is asserted. The MUTE_OUT signal remains asserted until the digital servo loops internal fast settling mode is complete. When the digital servo loop has switched to slow settling mode, the MUTE_OUT signal is deasserted.
30:16 (R/NW)	RATIO3	Sampling Ratio of Frame Syncs for ASRC3. The ASRC_RAT23.RATIO3 bit field is read to find the ratio of output to input sampling frequency for ASRC3 (SRCx_FS_OP_I/SRCx_FS_IP_I). This ratio is reported in 4.11 (integer.fraction) format where the 15-bit value of the normal binary number is comprised of 4 bits for the integer and 11 bits for the fraction.
15 (R/NW)	MUTEOUT2	Mute Status for ASRC2. The ASRC_RAT23.MUTEOUT2 bit field reports the status of the MUTE_OUT signal. Once the SRCx_MUTEOUT signal is cleared, the ratio can be read. When ASRC2 is enabled or there is a change in the sample ratio, the MUTE_OUT signal is asserted. The MUTE_OUT signal remains asserted until the digital servo loops internal fast settling mode is complete. When the digital servo loop has switched to slow settling mode, the MUTE_OUT signal is deasserted.
14:0 (R/NW)	RATIO2	Sampling Ratio of Frame Syncs for ASRC2. The ASRC_RAT23.RATIO2 bit field is read to find the ratio of output to input sampling frequency for ASRC2 (SRCx_FS_OP_I/SRCx_FS_IP_I). This ratio is reported in 4.11 (integer.fraction) format where the 15-bit value of the normal binary number is comprised of 4 bits for the integer and 11 bits for the fraction.