TP 2.5: 2-Transistor-Cell 4-Valued Universal-Literal CAM for a Cellular Logic Image Processor

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In intelligent robot systems and real-time instrumentation and control systems, real-time cellular logic image processing requires highly-parallel template-matching with many templates. Some hardware accelerators are used for highly-parallel cellular logic image processing. However, cellular logic image processing requires complicated circuits, limiting application to smaller images. CAMs are used as hardware accelerators for highly-parallel processing with single-instruction multiple data streams. A multiple-valued (MV) CAM for highly-parallel magnitude comparisons is used as a hardware accelerator in several applications with numeric operations [1]. However, MVCAMs have not yet been proposed to perform highly-parallel non-numeric operations such as cellular logic image processing.

This non-volatile 4-valued CAM is for fully parallel cellular logic image processing. Since gray-level or colored pixel values are directly represented by multiple-valued (MV) data in cellular logic image processing, a template-matching operation with an NxN window is performed by multiple-valued logic operations, that is 'universal literals'. Since many templates are required in some image processing, several templates are compressed as shown in Figure 1. Universal literals are used to perform template-matching operations with MV compressed templates where a 4-valued universal literal is defined as

$$X^{\{a\}} = \begin{cases} 3 & \text{if } X \subset a \\ 0 & \text{otherwise} \end{cases}$$

where $a \subset L = \{0, 1, 2, 3\}$.

As shown in Figure 2(a), a universal literal can be expressed by a combination of 2 window functions. Figure 2(b) shows the realization of a window function using a threshold operation and a logic-value conversion (LVC) for a 4-valued input. Let (0, 1, 2, 3) be an input string of a 4-valued LVC f. Let $\left(p_0, p_1, p_2, p_3\right)$ be an output string of f corresponding to the input string. The LVC f is defined as

$$f = \left\langle p_0, p_1, p_2, p_3 \right\rangle$$

where $p_i (0 \le i \le 3) \in L$. To realize a 4-valued universal literal, it is necessary to prepare 4 LVCs, f_1, f_2, f_3, and f_4 as shown in Figure 2(b). A threshold operation $D_a(X)$ is defined as

$$D_a(X) = \begin{cases} 3 & \text{if } X < a \\ 0 & \text{otherwise.} \end{cases}$$

As shown in Figure 3(a), the proposed cellular logic image processing system is pipelined where a universal-literal 4-valued CAM is used as a hardware accelerator for parallel template-matching. 2-dimensional input image data are transformed into serial data according to line scanning. 9 pixels corresponding to a 3x3 window are picked up from the line-scanned image data simultaneously, and are entered into the CAM cellular array for parallel template-matching. Figures 3(b) and 3(c) show basic components of the image processor. 2 of 4-LVC output signals generated from an input signal are selected by mask programming in a CAM cell. A universal literal can be realized by a combination of 2 threshold operations with the selected 2-LVC output signals in each CAM cell.

Figure 4 shows circuit design and layout of a 4-valued universal-literal CAM cell. Since the threshold voltage of a floating-gate MOS transistor can be programmed by controlling the charge on its floating gate, a threshold operation with a one-digit 4-valued storage element can be performed simultaneously by using a floating-gate MOS transistor. Tables 1 and 2 show the relationship among 4-valued input logical values, 4-valued threshold values and the corresponding voltage levels. Since 4 LVCs are shared by every CAM cell in the same column of a CAM cellular array, the product of 2 threshold operations has only to be performed in a single CAM cell. Using the wired AND, the resulting CAM cell is implemented by 2 floating-gate MOS transistors. Use of the wired AND makes it possible to generate the product of many universal literals without additional circuits. Consequently, a MVCAM with powerful functionality is realized simply by the 2-transistor cell design.

Figure 5 shows a layout and its floor plan of the 1Mb 4-valued universal-literal CAM. Performance is summarized in Table 3. Since an LVC circuit is shared by many CAM cells, the LVC circuits are reduced to 12% of chip area.

Table 4 compares the template-matching circuits using CAM-based architectures with a 4-valued 3x3 template using 0.8μm standard EEPROM technology. Although a window is 3x3 in this evaluation, it can be extended to any size. Using a binary CAM, the limited cell functionality increases the number of CAM cells required to perform a universal literal. Moreover, a binary dynamic CAM cell is 5 transistors and 2 capacitors [2]. Consequently, binary CAM-based hardware requires more than 3.5-times the area than does the 4-valued universal-literal CAM.

The access time and the power dissipation of the CAM depend on total capacitance of the match line. Because the proposed hardware is compact compared with the binary CAM, the length of the match line is shorter and the capacitance is lower. In fact, the power dissipation and the access time of the CAM are 71% and about 67% respectively of those of a binary implementation.

It is impossible to perform highly-parallel template-matching operations in RAM-based hardware because of memory-access bottlenecks. Since 58.8k templates are performed simultaneously within 15.7ns single access time, processing performance is about 3.75TIPS with 6.0W.

Acknowledgments:

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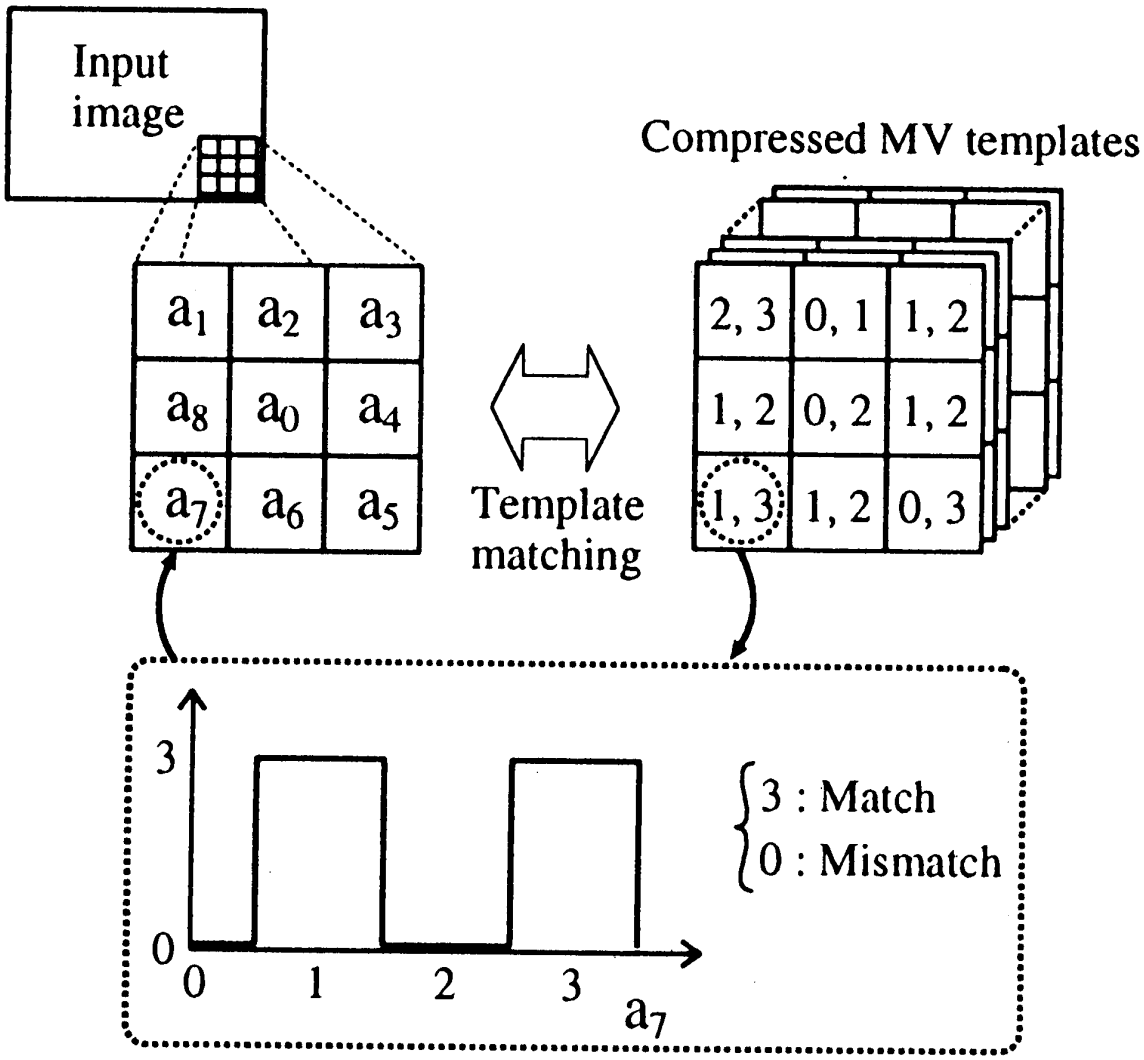
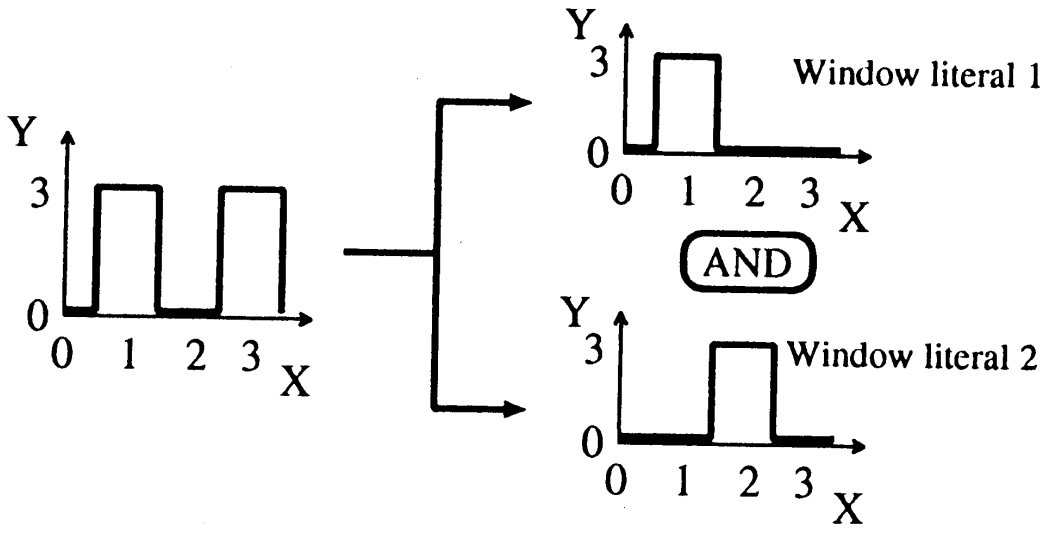
References:

[1] Hanyu, T., N. Kanagawa, M. Kameyama, "One-Transistor-Cell Multiple-Valued CAM for a Collision Detection VLSI Processor," ISSCC Digest of Technical Papers, pp. 264-265, Feb., 1996.

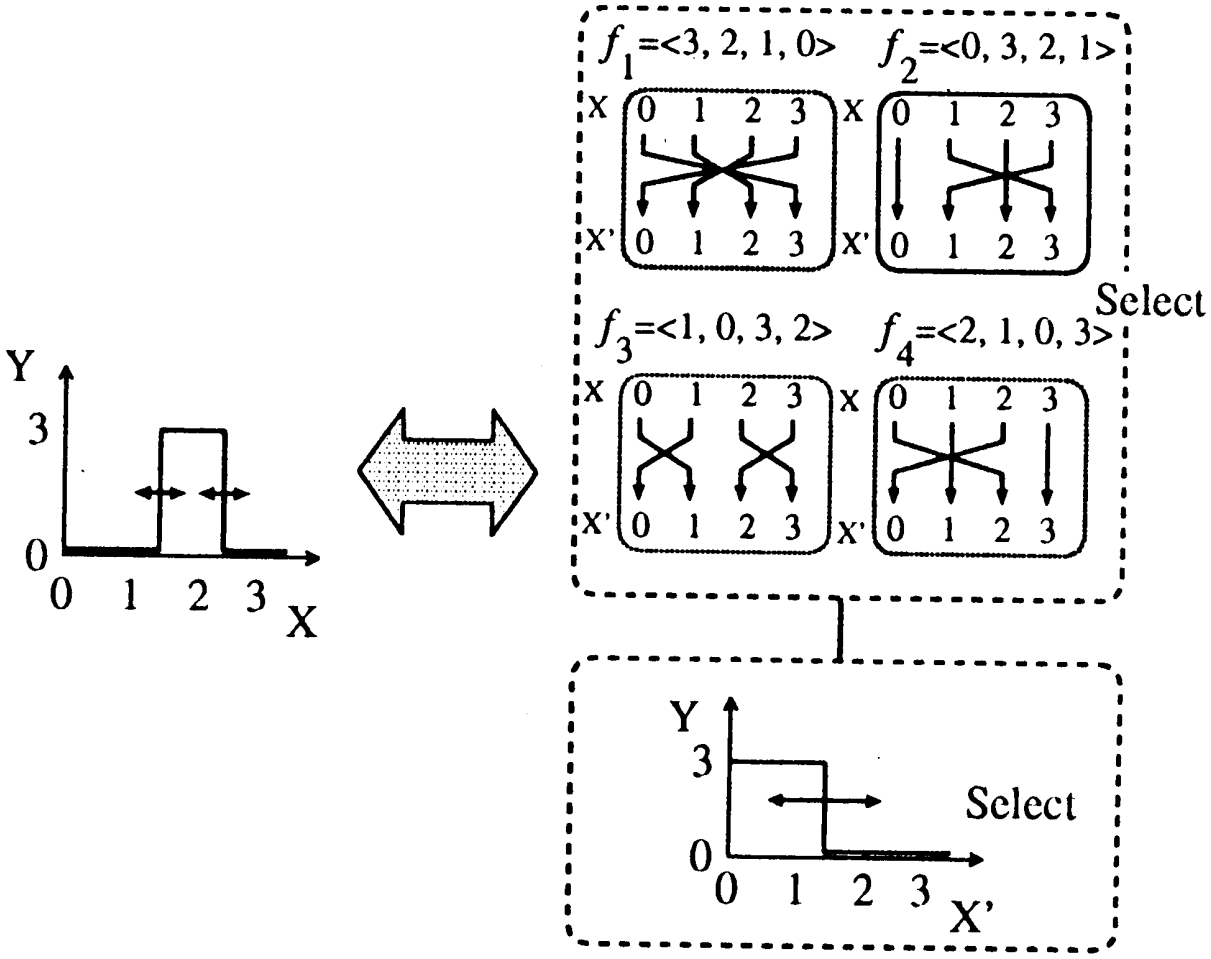
[2] Yamagata, T., et al., "A 288kb Fully Parallel Content Addressable Memory Using a Stacked-Capacitor Cell Structure," IEEE J. Solid-State Circuits, vol. 27, no. 12, pp. 1927—1933, Dec., 1992.



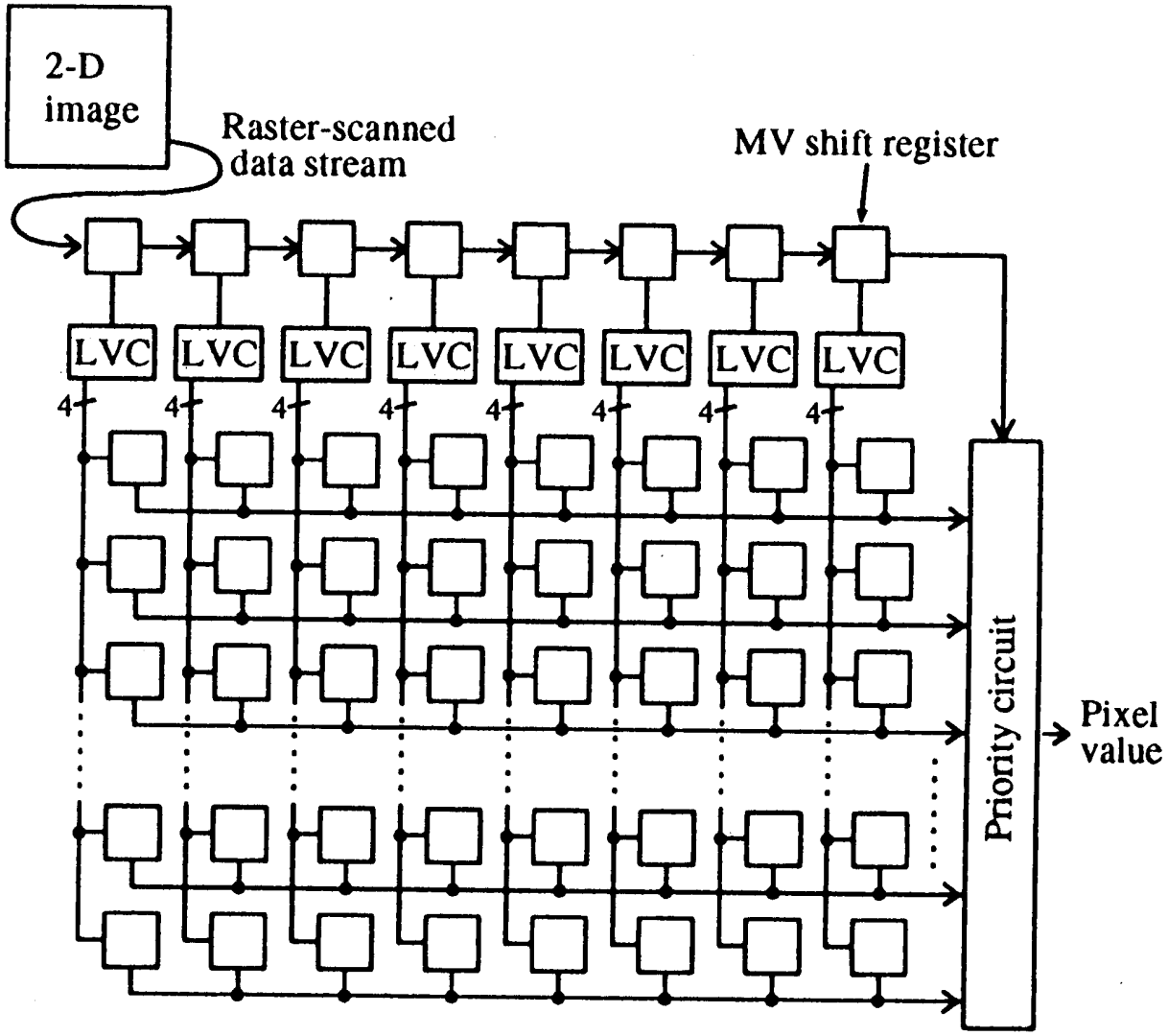
2-5-1: Template matching based on universal literals.



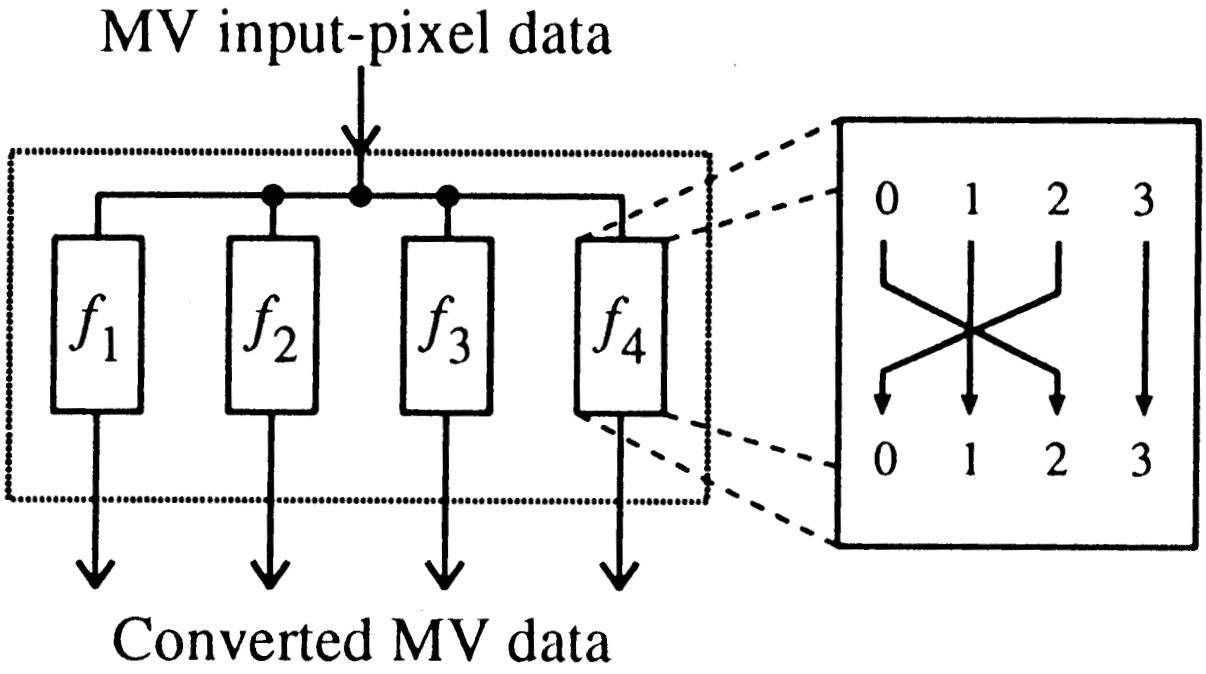
2-5-2: Realization of a universal literal with LVCs and threshold operations. (a) Decomposition of a universal literal



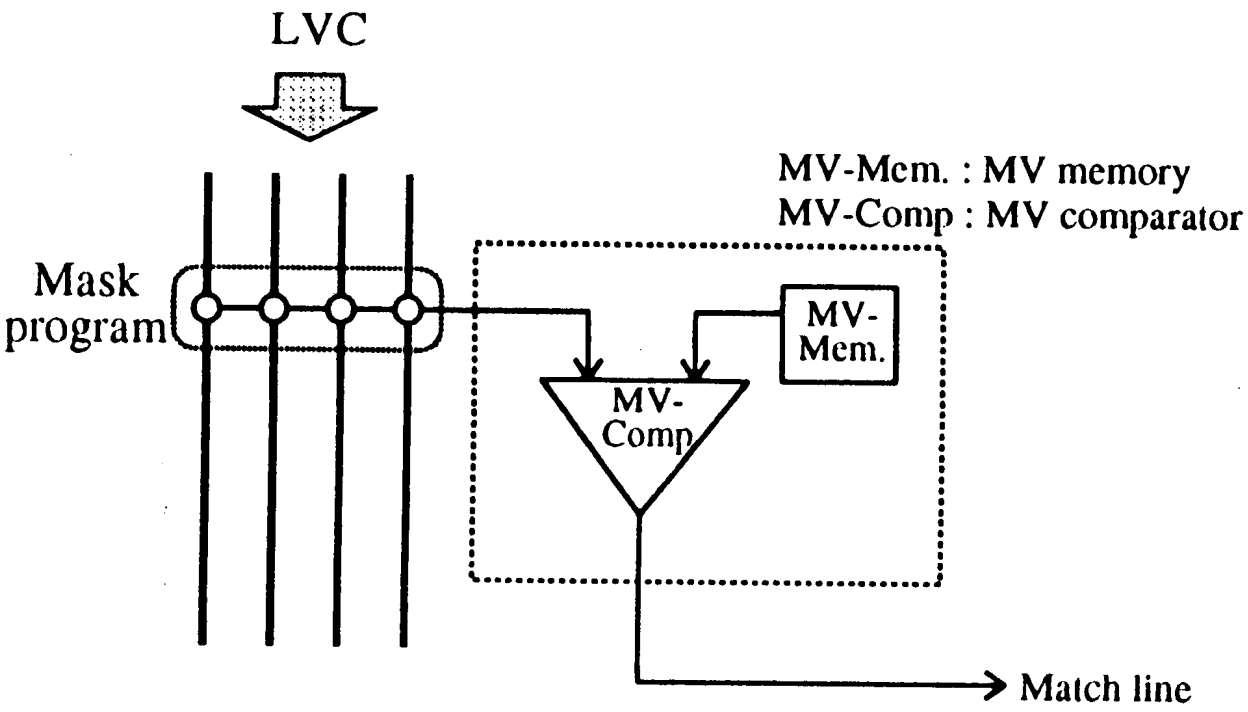
2-5-2: Realization of a universal literal with LVCs and threshold operations. (b) Realization of a window function.



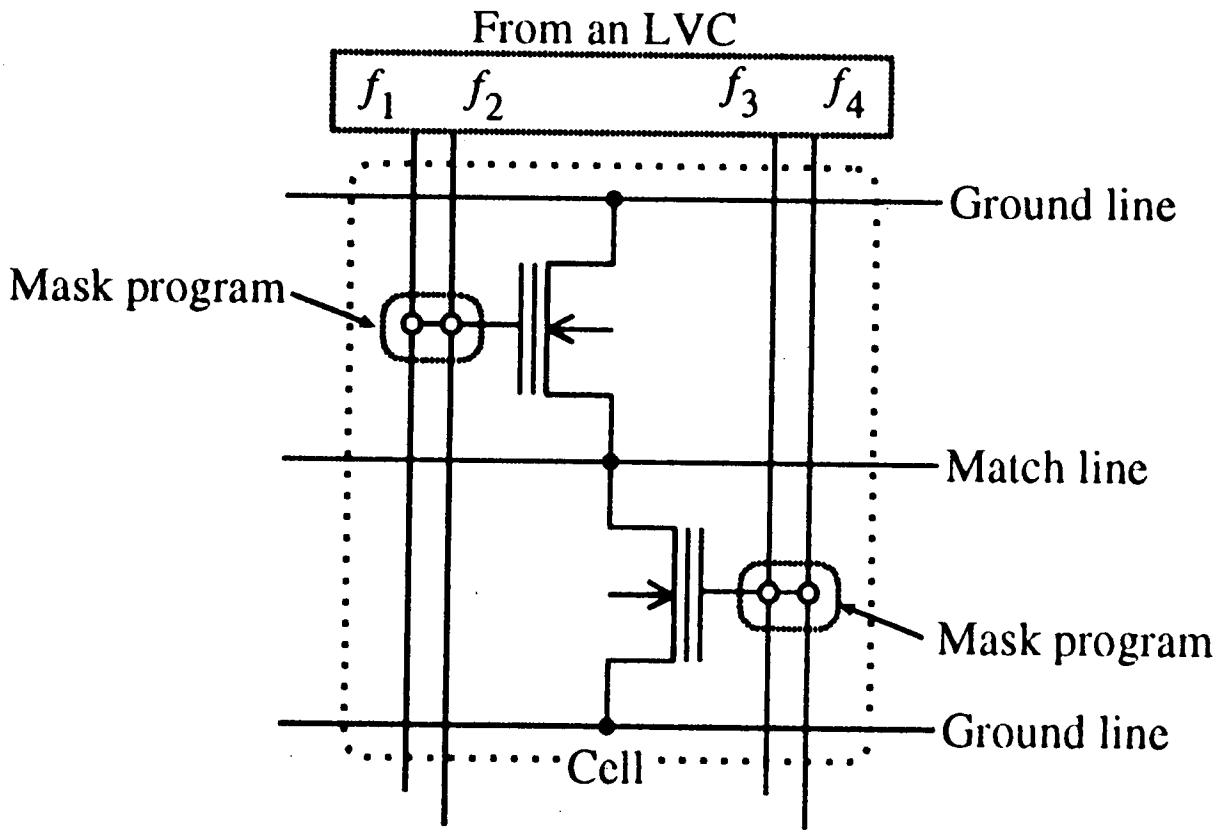
2-5-3: Proposed MV CAM (a) Overall structure.



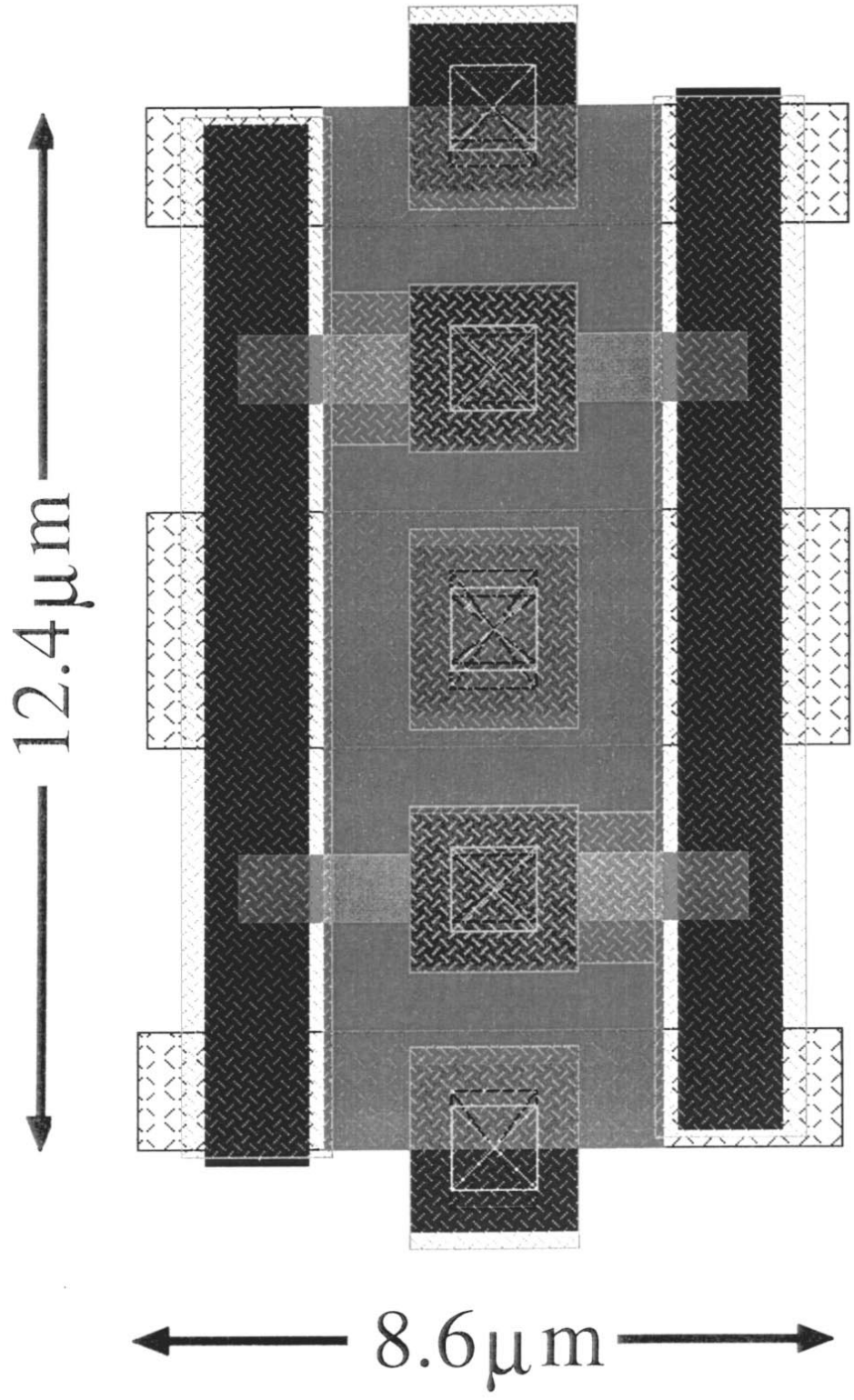
2-5-3: Proposed MV CAM (b) Structure of an LVC.



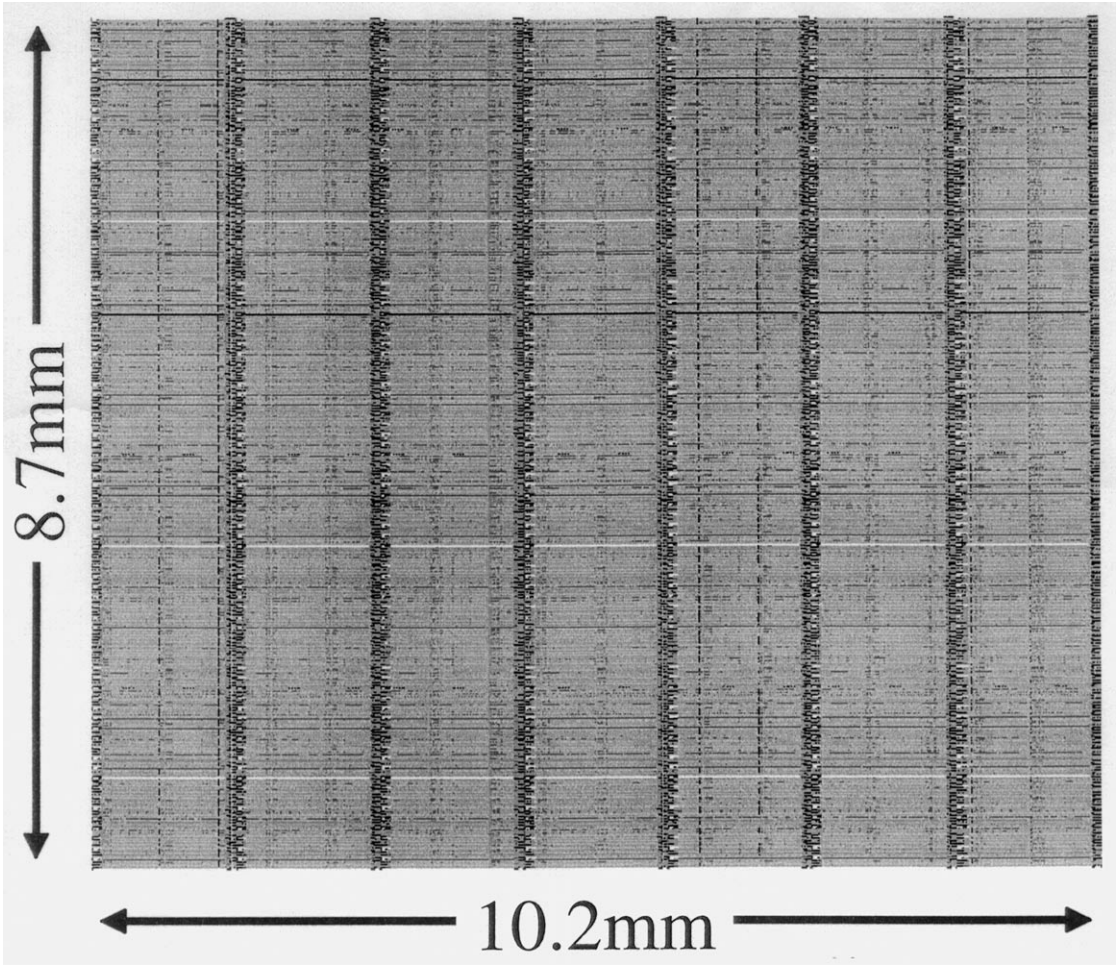
2-5-3: Proposed MV CAM (c) Structure of a CAM.



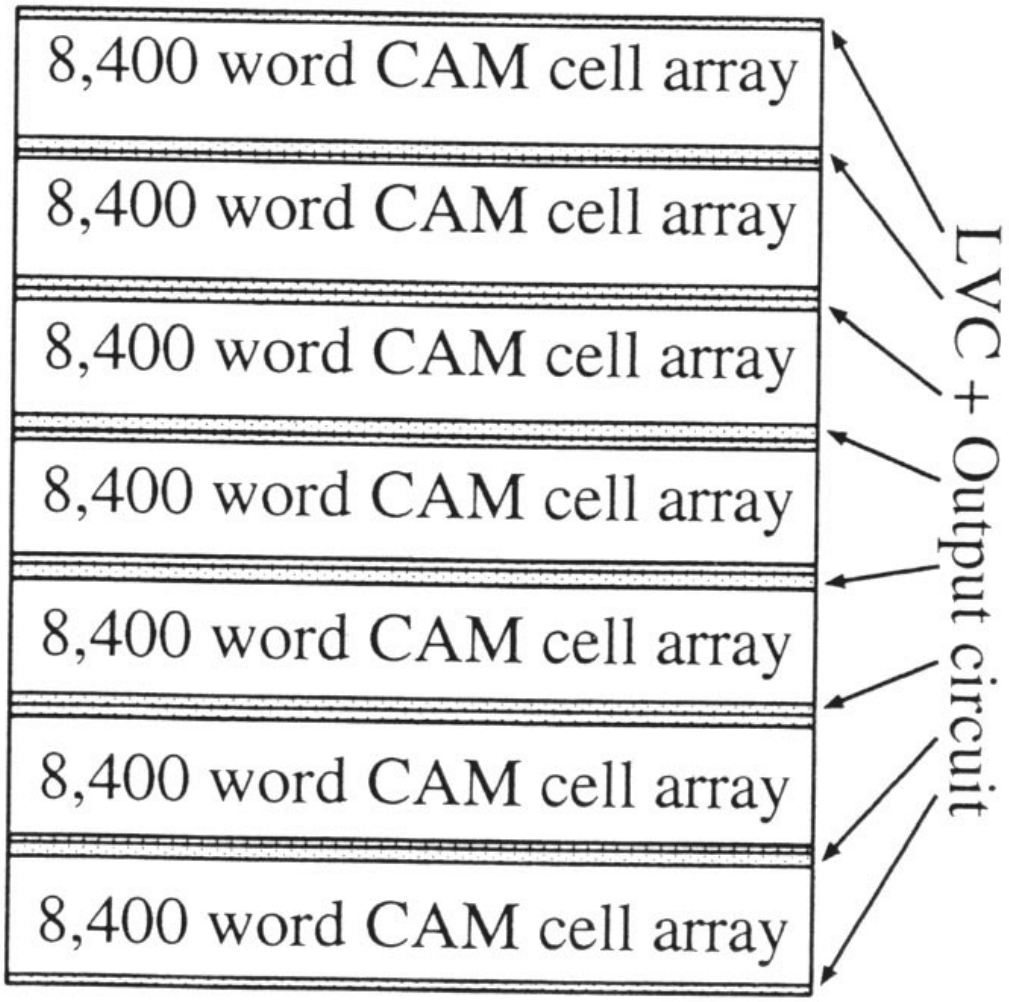
2-5-4: CAM cell, (a) Cell circuit,



2-5-4: CAM cell, (b) Cell layout.



2-5-5: 1Mb universal-literal CAM. (a) Chip layout.



2-5-5: 1Mb universal-literal CAM. (b) Floor plan.

Logic value	0	1	2	3
Voltage level (V)	0	1.7	3.4	5.0

2-5-Table 1: Relationship between logic values and voltage levels.

Logic threshold	0.5	1.5	2.5
Threshold level (V)	0.8	1.7	3.4

2-5-Table 2: Relationship between logical thresholds and threshold levels.

Process	0.8µm EEPROM double-polysi triple-metal
Number of templates	58.8k
Capacity	1Mb
Chip area	10.2x8.7mm²
(LVC area)	(12%)
Execution time	15.7ns
Power dissipation	6.0W

2-5-Table 3: Universal-literal CAM features.

	Binary CAM-based implementation	Proposed hardware
Layout area(μm²)	377	107
Power dissipation (W)	8.4	6.0
Execution time (ns)	23.6	15.7

2-5-Table 4: Performance comparison.