

APPLICATION NOTE

MULTICHANNEL OPERATIONS

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Digital Filter Implementation on MB86975

Most of the digital filters are based on the following difference equation.

$$y(n) = \sum_{i=0}^M a_i x(n-i) + \sum_{k=1}^N b_k y(n-k) \quad (1)$$

The length, also called the order or the number of taps, of the filters is M or N whichever is larger.

From this equation, we can get

1. Finite Impulse Response (FIR) filters, also called Nonrecursive digital filters, and
2. Infinite Impulse Response (IIR) filters, also called Recursive digital filters.

FIR Filters

If all the b_k in (1) are zero, (1) becomes

$$y(n) = \sum_{i=0}^M a_i x(n-i) \quad (2)$$

Taking the Z transform of (2), we get

$$Y(Z) = \sum_{i=0}^M a_i Z^{-i} X(Z) \quad (3)$$

From (3) we can get the transfer function

$$H(Z) = \frac{Y(Z)}{X(Z)} = \sum_{i=0}^M a_i Z^{-i} \quad (4)$$

The realization of this Mth - order nonrecursive filter is shown in Figure 1.

Setting up MB86975 for FIR

There are four steps to set up the MB86975 for FIR filters.

1. Set up the configuration registers for coefficient loading.
2. Input the FIR coefficients.
3. Set up the configuration registers.
4. Turn the MB86975 to the RUN mode.

Set up The Configuration Registers for coefficient loading:

Before loading coefficients, SR bit in the MODE register, IOMODE, ALGCTRL, SCNCH, LKGRPSZ, NBGRP, and RECTRL registers must be set to zero for proper coefficient loading.

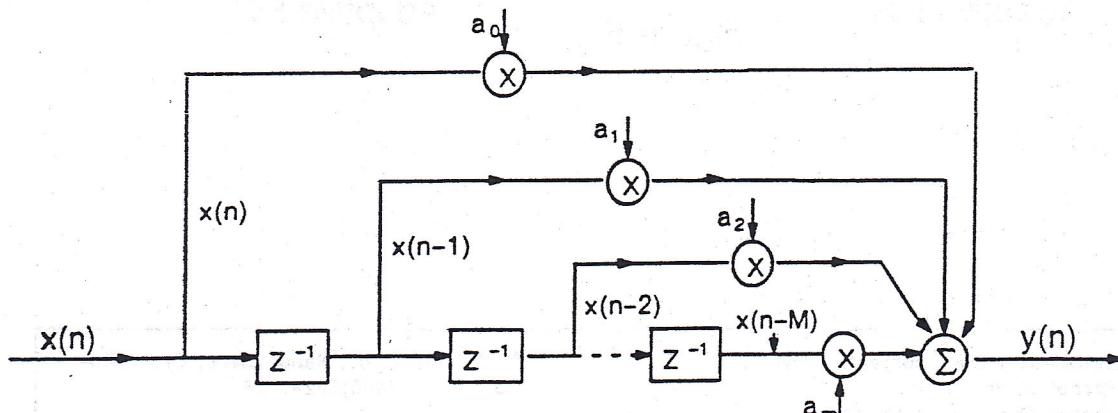


Figure 1

Input the FIR Coefficients:

A set of the coefficients specifies the characteristics of a filter. Designers use the Order register to specify the coefficient RAM address and load the coefficients into two Coefficient Read/Write registers(addr.=8,9) to load coefficients (16 bits total) into the proper coefficient RAM locations. The 24 bit RAM is used to update coefficients for the adaptive FIR filter. For regular FIR filters, only the most significant 16 bits will affect the result of FIR filters. See Figure 2 for coefficient loading consequence. Note that the RWE bit in the STATUS register will be set to 0 by AFP during the following DATA.H. loading. The coefficients must

be stored in coefficient RAM consecutively from the smallest address up.

For multichannel operations, each channel shares a common filter type and length but have separate coefficients. The 256 coefficient RAM will be divided into 2, 4, 8, 16, or 32 equal size blocks according to the number of channels. The coefficients must be stored consecutively. If the number of channels does not equal to 2, 4, 8, 16, or 32, the remainder blocks of RAM, that are not used should be left toward the highest coefficient RAM location (see Figure 4, b). Note that in the 4 channel case (Figure 4, a) that even if the filter length is less than 64, the coefficients for channel 2, 3, and 4 still begin at 40, 80, and C0.

AFP CLOCK 



Figure 2

I = information field U = user defined field IG = Ignored in this case

REGISTER	ADDRESS	BIT POSITION							
		7	6	5	4	3	2	1	0
STATUS (read)	0	I		IG		I	I	I	I
STATUS (write)	0			IG			1	IG	IG
IOMODE	1	0	U	IG		IG		0	U
IOTIME	2		U				U		
ALGCTRL	3	0	0	0	0	U	U	0	0
ORDER	4	VALUE							
SCNCH	5		U		1	1	1	1	1
LKGRLPSZ	6	0	0	0	0	0	0	0	0
NBGRP	7		IG		1	1	1	1	1
DATA	8	COEFFICIENT HIGH							
DATA	9	COEFFICIENT MIDDLE							
DATA	A	COEFFICIENT LOW							
RESERVED	B	IG							
RWCTRL	C	U	U	IG		IG	IG	1, 0	0, 1
RESERVED	D	IG							
RESERVED	E	IG							
MODE	F	I			IG		0	0, 1	

REGISTER ASSIGNMENTS

Figure 3

Set up The Configuration Registers:

To make the MB86975 run properly, designers need to set up the configuration registers to serve their specific applications. Designers use the Register Address lines and Host Bus to write into any particular configuration registers. Figure 3 is one of the possible register configurations for a single chip FIR filter without the leakage control. This configuration contains 32 channels, 1 channel per group, and 32 groups total. Each channel processes a unique input data stream, and outputs a unique data stream. In figure 3, the I stands for Information field. The MB86975 will provide certain information only if those situations ever occurred. The U stands for user define field. Designers can use those fields to define their specific applica-

tions. The IG stands for Ignored in the FIR filter operations. See the MB86975 data sheet for detail information about these registers. The next step is to write the filter coefficients into the coefficient RAM.

Turn MB86975 to the RUN mode:

Afterdesigners set up the configuration registers, designers need to write the filter order into the Order Register to specify the proper FIR filter order, write number of channels in NCH field (in our case it is 32 channels) in SCNCH register, set the CRE bit in the RWCTRL register to 0, and set the DRE bit in the RWCTRL register to 1 to accept input data. Lastly, designers need to turn the SR bit in the MODE register to 1, to start the MB86975.

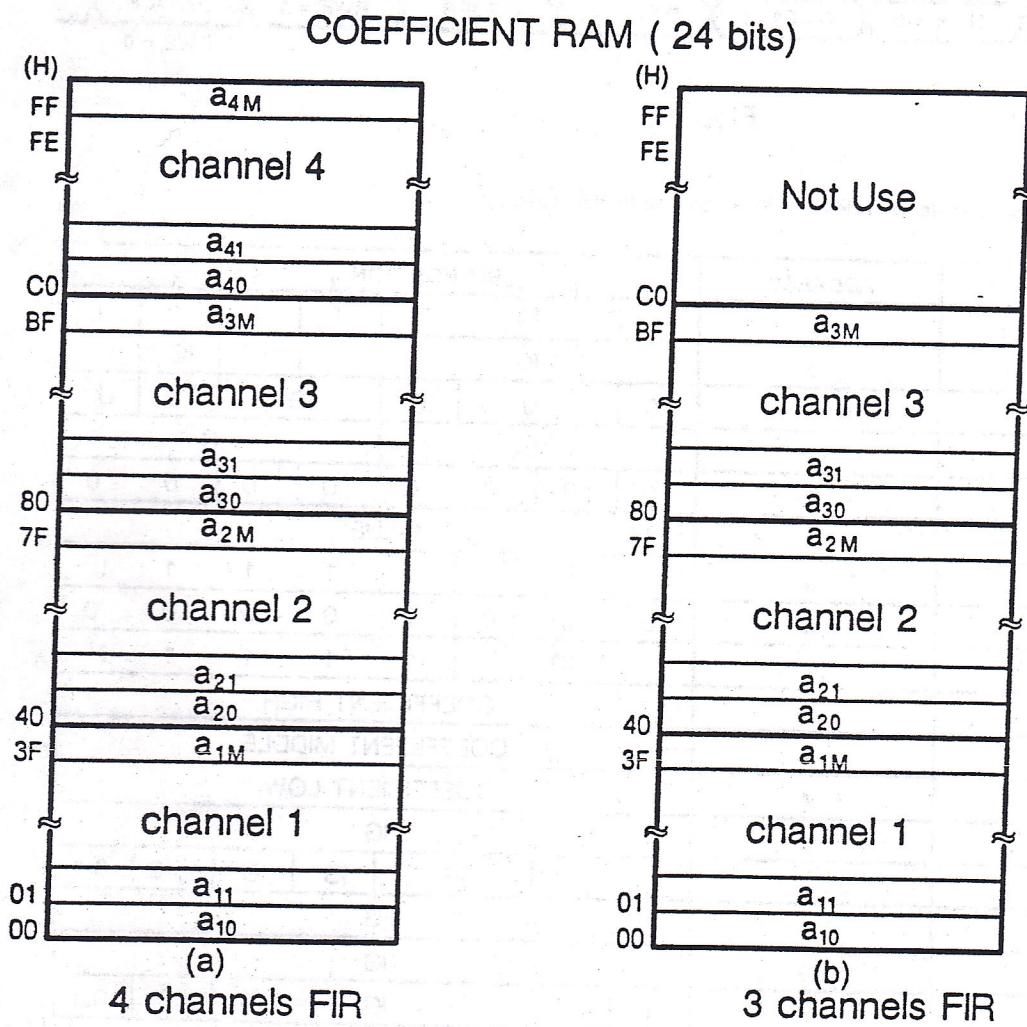


Figure 4

IIR Filters

Equation (1) with a_i and b_k nonzero, represents an IIR filter.

For simplification, $M = N$ and $i = k$ for IIR filters in the MB86975. (1) becomes

$$y(n) = \sum_{k=0}^M a_k x(n-k) + \sum_{k=1}^M b_k y(n-k) \quad (5)$$

Take Z transform of (5), we get

$$Y(Z) = \sum_{k=0}^M a_k Z^{-k} X(Z) + \sum_{k=1}^M b_k Z^{-k} Y(Z) \quad (6)$$

From (6) we can get the transfer function

$$H(Z) = \frac{Y(Z)}{X(Z)} = \frac{\sum_{k=0}^M a_k Z^{-k}}{1 - \sum_{k=1}^M b_k Z^{-k}} \quad (7)$$

In MB86975, the fixed IIR case are implemented as cascaded second - order (biquad) sections, $M \leq 16$. (7) becomes

$$H(Z) = A \prod_{k=1}^{M/2} \frac{1 + \alpha_{1k} Z^{-1} + \alpha_{2k} Z^{-2}}{1 - \beta_{1k} Z^{-1} - \beta_{2k} Z^{-2}} \quad (8)$$

The realization of Mth - order recursive filter is in figure 5.

Setting up MB86975 for IIR

There are four steps to set up the MB86975 for IIR filters.

1. Set up the configuration registers for coefficient loading.
2. Input the IIR coefficients.
3. Set up the configuration registers.
4. Turn the MB86975 to the RUN mode.

These four steps are similar to the FIR implementations.

Set up The Configuration Registers for coefficient loading:

Before loading coefficients, SR bit in the MODE register, IOMODE, ALGCTRL, SCNCH, LKGRPSZ, NBGRP, and RECTRL registers must be set to zero for proper coefficient loading.

Input the IIR Coefficients:

The coefficient RAM for IIR filters is 16 bit wide. Therefore, designers only use two Coefficient Read/Write registers (addr.=9,A) to load the IIR filter coefficients. The coefficients for each biquad must be stored in coefficient RAM consecutively, the Lowest coefficient RAM locations contains the coefficients for the last biquad. See figure 6 (a) for illustration. Since α_0 and β_0 are always 1, it is not necessary to input the coefficient for α_0 and β_0 . The A is located in the highest coefficient RAM location, and the second highest coefficient RAM is always not used.

For multichannel operation, the coefficient RAM will be divided into numbers of blocks in the same method as FIR filters. The biquad coefficients should be stored in the same method as single channel. The As should be stored in the last location of the next channel. The A for the last channel should be stored in the last location of the first channel. The second highest coefficient RAM location for each block is not used also (see figure 6, b).

Set up The Configuration Registers:

Designers use the Register Address lines and Host Bus to specify their particular applications. See description for FIR filters and the MB86975 data sheet for detail information.

Turn MB86975 to the RUN mode:

Afterdesigners set up the configuration registers, designers need to write the filter order into the Order Register to specify the proper IIR filter order. The maximum possible order of IIR filters varies with the number of channels used. The value in the Order Register is different than the actual IIR filter orders. See the following table:

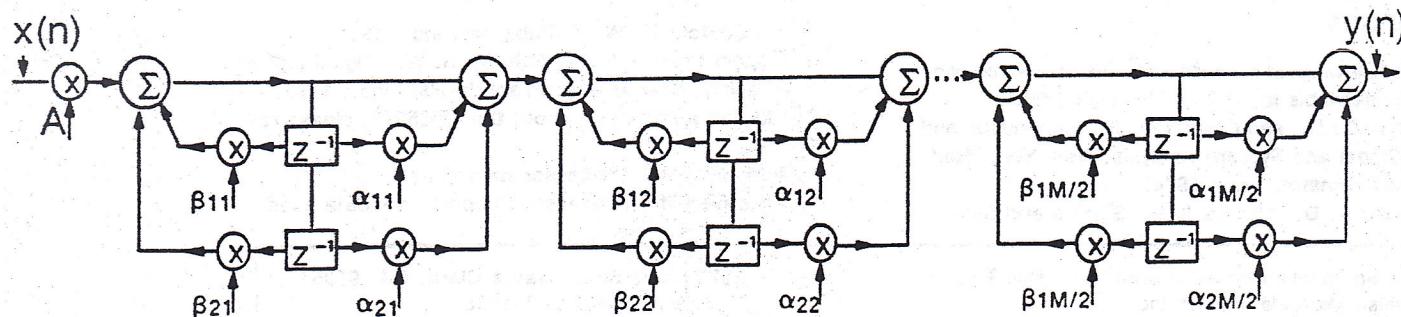
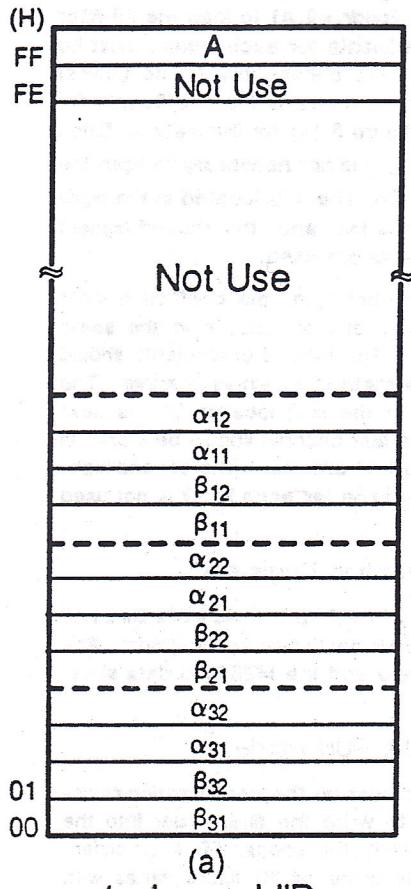


Figure 5

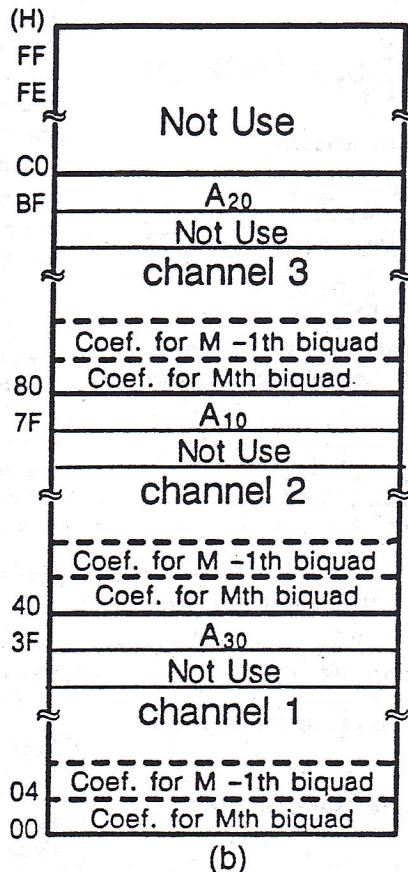
NUMBER of CHANNELS	MAXIMUM FILTER ORDER	VALUE IN THE ORDER REGISTER
1	16	31
2	16	31
4	16	31
8	14	27
16	6	11
32	2	3

Then designers need to write number of channels in NCH field in SCNCH register, set the CRE bit in the RWCTRL register to 0, and set the DRE bit in the RWCTRL register to 1 to accept input data. Lastly, designers need to turn the SR bit in the MODE register to 1, to start the MB86975.

COEFFICIENT RAM (16 bits)



(a)
1 channel IIR
3 biquads



(b)
3 channel IIR
M biquads

Figure 6

References

- The following list is representative of the common references available for FIR and IIR digital filters.
1. McGillem, C. D., and Cooper G. R., Continuous and Discrete Signal and System Analysis. New York: Holt, Rinehart and Winston, Inc., 1974.
 2. Pouliarihas A. D., and Seely S., Signals and Sys-

tems. Boston: P. W. S. Publisher, Inc., 1985.
3. Oppenheim A. V. and Schafer R. W., Digital Signal Processing. New Jersey: Prentice-Hall, Inc., 1975.
For further information about the MB86975, please refer to

1. Adaptive Filter Processor data sheet.
2. Adaptive Filter Processor Support Tool data sheet.

For additional information contact: Jinyi Tsai
Fujitsu Microelectronics Inc.
Advanced Product Division

3320 Scott Blvd., Santa Clara, CA 95054
Telephone: (408)562-1638