Low Power Parallel Digital Multipliers using 10 Transistor Adder Circuits

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Abstract:

In this paper we investigate the power and delay performance characteristics of parallel digital multipliers using recently developed 10 transistor static energy recovery full adder (SERF) circuit. For our comparative study we realized multipliers using two different algorithms and using three different input bit widths using SERF adders. The tradeoff between speed and power of these multipliers were compared to similar multipliers realized using regular static CMOS adder circuit. SPICE simulations were used for characterizing the building blocks as well as the multiplier circuits. Multipliers realized using the SERF adder circuit consumed considerably less power compared to static CMOS based multipliers in all the different multiplier configurations studied in this paper. Our simulation studies indicate that, in the case of 2x2 multipliers, SERF based multipliers are faster compared to static CMOS based multiplier configurations. While 4x4 SERF adder based multipliers are only slightly slower than the static CMOS based multipliers, 8x8 SERF based multipliers are considerably slower compared to its CMOS counterpart.

1. INTRODUCTION:

Until recently, the cost of VLSI chips was determined primarily by area, performance and testability parameters. Improvements in silicon processing technology have reduced these costs by a considerable degree. The resulting performance improvement and integration has increased the power dissipation of integrated circuits, leading to problems in packaging and in reliable operation of the circuits itself. Thus, it is essential in many applications to minimize the power dissipation in order to reduce the costs associated with the cooling of the chip. The increasing importance and growing popularity of mobile computing and communications systems have made power consumption a very critical design parameter. Concern over power has displaced silicon area as the principal design constraint in some of the application areas such as personal notebooks and wearable devices. Portable communication systems have wide spread applications such as Laptops, PDA's, Digital Camcorders and Cellular Phones, making them a key component of daily routine. The battery life is one among the pivotal factors in portable-applications, which underlines the need for low power consumption and high throughput. It therefore becomes imperative to design circuits with low power dissipation.

Multipliers are used in digital signal processors (DSPs), media processors, as well as general purpose processors. Digital multipliers are often needed in many applications, including digital filters, correlators, Fast Fourier Transforms, neural networks, and audio and video processing. Many microprocessors and digital signal processors now have fast multipliers in them. There are different types of multipliers with different speed, area, and circuit configurations. Multipliers can be implemented using different algorithms. Depending on the algorithm used, the performance characteristics of the multipliers vary. In most of the digital multiplier implementations binary adders are an essential component.

The performance characteristics of the digital multiplier depends to certain extent, on the performance characteristics of the adder circuit used to realize it for a given multiplication algorithm. There have been tremendous research efforts in the design and characterization of low power adders [1,2,3,4,]. Recently our research group developed a new low power static energy recovering full (SERF) adder cell, which requires only 10 transistors to realize the complete function of a full adder [3]. The basic idea in the SERF adder is the reuse of charge stored in the load capacitance during the high output to drive the control logic. The elimination of direct paths to ground also reduced power consumption. To the best of our knowledge, this 10 transistor adder has the best power performance among all low power adder circuits published

to-date and is second only to the Dual Value Logic (DVL) full adder [4] circuit in delay performance. The DVL adder needs 23 transistors for the realization of the adder function and hence consumes more energy. The low power performance characteristics and the low transistor count make the new SERF adder circuit an ideal candidate for the realization of low power digital multipliers.

In this paper we investigate the power and delay performance characteristics of parallel digital multipliers using the 10 transistor static energy recovery full adder (SERF) circuit. For our comparative study we realized multipliers using two different algorithms, bit array multiplier and carry save multiplier, using SERF adder circuits. The tradeoff between speed and power of these multipliers were compared to similar multipliers realized using regular static CMOS adder circuit. In Section 2 we describe the background and related research. Section 3 describes the SERF adder circuit in detail. Section 4 describes the multiplier design, and simulation methodology used. In Section 5 the results of simulation study are presented and Section 6 presents summary of the paper and the concluding remarks.

2. BACKGROUND AND MOTIVATION:

In any digital processor architecture, data path is the core of the processor. The data path consists of an interconnection of basic arithmetic operators like Adders, Multipliers and Shifters. Hence optimization of these circuits would enhance performance of the arithmetic processors. The adder is the most commonly used component and hence is also the most deterministic component. Henceforth using an efficient and optimum power usage adder is mandatory for any processor. The recent trends toward energy efficient circuitry have proven to be useful for power optimization. The idea behind energy recovering logic is to be able to recover and reuse most of the system's energy from one cycle to the next, rather than dissipating all or a large fraction of it on each cycle. That is, a system is reversible if there is no loss of information in its path. In VLSI circuits it implies that all the power that is lost in combinational logic should be within the system rather than being dissipated.

Power optimizations for multipliers can be done at different levels. New architecture and circuit technologies have been proposed by various research groups to reduce the power consumption of parallel multipliers [5,6,7,8,9]. In this paper we use the low power 10 transistor SERF adder cells for the realization of low power multipliers.

3. SERF ADDER:

The Static Energy Recovery Full Adder (SERF adder) circuit was developed implementing energy recovery logic and reduced number of transistors. The power dissipated in a CMOS circuit can be classified as static power and dynamic power dissipation. The total power, P_{total}, dissipated by a CMOS combinational circuit can be expressed by the well-known formula [10,11]

$$P_{total} = P.\,(C_{Load} V_{dd}^2 f_{clk}) + I_{sc} V_{dd} + I_{leakage} V_{dd}$$

Where C_{Load} is the load capacitance, V_{dd} is the power supply voltage, f_{clk} is the clock frequency and p is the probability that a power consuming transition occurs (activity factor). The second term is due to short-circuit current I_{SC}, which arises when a direct path from supply to ground occurs. The last term is the leakage current $I_{leakage}$, which can arise from substrate injection and sub threshold effects. Curtailing any of the factors would lead to a low power design.

Figure 1. shows the schematic of the 10 transistor SERF adder [3]. The basic idea in the SERF adder is the reuse of charge stored in the load capacitance during the high output to drive the control logic. The elimination of direct paths to ground also reduced power consumption. The SERF adder is not only energy efficient but also area efficient due to its low transistor count. The main drawback of the SERF adder is the threshold voltage drop at the output voltage for certain input combinations. A detailed comparative study of SERF adder with other low power adders can be found in [3].

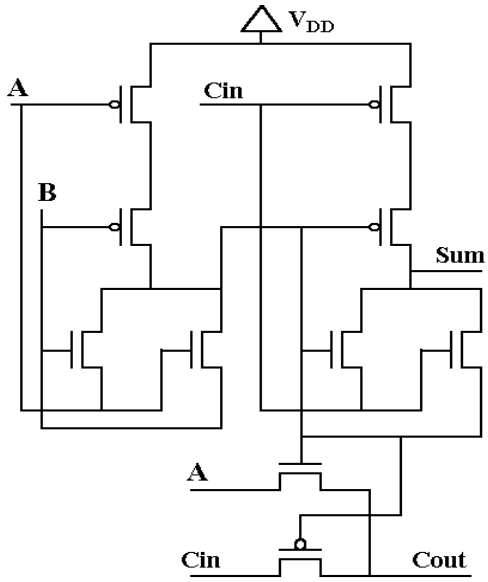

Figure 1: Static Energy-Recovery Full (SERF) Adder

4. MULTIPLIERS:

Multipliers are in fact complex adder arrays. This is an operation common to a large number of applications, and the complexity of this function has lead to a large amount of research directed at speeding up its execution. Multipliers can be implemented using different algorithms. Depending on the algorithm used, the performance characteristics of the multipliers vary. In the implementation of digital multipliers binary adders are an essential component. With the inception of power as a design consideration, speed is not the only criterion by which various implementations are judged. Designing multipliers with low power, energy efficient adders reduce the power consumption and efficiency of multipliers. In this paper we have concentrated on the design and characterization of two popular multipliers, viz. the Carry-Save Multiplier and the Bit-Array Multiplier. For power dissipation and speed comparative study we implemented these two multipliers based on SERF adder circuit and the static CMOS adder circuit. We further implemented these multipliers for operands of sizes 2, 4 and 8.

4.1 Carry-Save Multipliers:

Carry Save Array Multipliers have a very regular structure, which makes it amenable to automation. It uses only short wires to the nearest neighboring cells. It can also be easily pipelined. In the carry-save multiplier, the carry bits of each stage are not immediately added but are rather "saved" for the next adder stage. This results in a more efficient multiplier structure by reducing the time spent on the critical path of the operation. An added bonus is that there is only one critical path rather than the several identical critical paths found in the generic array multiplier. Figure 2 shows the general structure of a Carry-Save Multiplier.

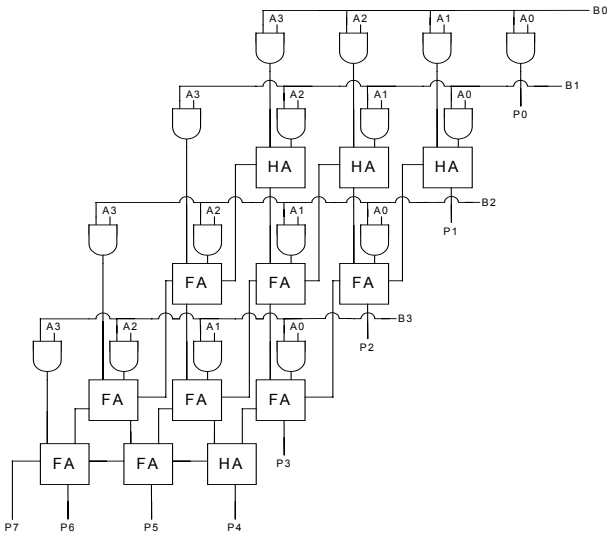

Figure 2: 4x 4 Carry-Save Multiplier

4.2 Bit-Array Multipliers:

Bit Array Multipliers are another structure with regularity that is simple to expand. The structure is similar to the previously discussed Carry-Save multiplier but propagates the carry bits from the full adders in a different fashion. A simple diagram of a 4x4 multiplier is shown in Figure 3.

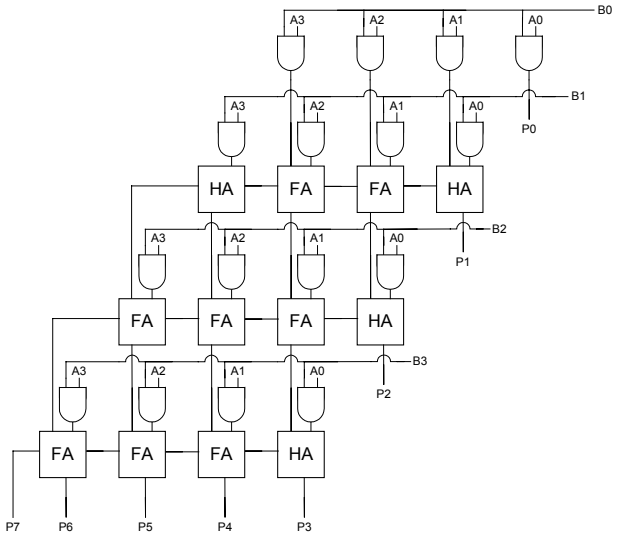

Figure 3: 4 x 4 Bit-Array Multiplier

5. SIMULATIONS AND RESULTS:

Two bit, four bit and eight bit carry-save and array multipliers using the SERF and CMOS adders were designed and simulated in PSPICE with 1.2-micron transistors. The simulations were run at 100MHz for 1 microsecond and consisted of multiplying either the vector F or FF by itself and then a zero vector and then by F or FF depending on the multiplier size. The simulation continued toggling the second vector for the duration of the run. Buffers were placed on all the input and output signals.

These simulations were used to gather data on the energy consumption of the circuits as well as the delays of the circuits. The energy consumption is determined by the following equation.

$$P_{TOTAL} = \int_0^T V_{DD} \cdot I_{INSTANTANEOUS}$$

Table1 gives the energy consumption for all the multipliers that were investigated. As expected the SERF adder based multipliers consumed considerably less energy compared to the CMOS adder based multipliers. Since more and more adder cells are used for larger multipliers, as the multiplier size increases the percentage power savings also increases.

Table 1. Circuit Energy Consumption

ENERGY CONSUMPTION (nJ)		
	w/SERF Adder	**w/CMOS Adder**
2x2 Cell	0.555	0.814
4x4 Bit-Array	2.103	4.579
4x4 Carry-Save	2.748	4.411
8x8 Bit-Array	8.748	21.876
8x8 Carry-Save	12.067	20.861

The results clearly show that under any circumstance, the SERF adder based multipliers consumed less energy than a traditional CMOS adder based multiplier. In fact, the SERF based multiplier performed at least thirty-two percent better than any CMOS based version. The SERF based 8x8 Bit-Array multiplier proved to have the greatest advantage over its CMOS counterpart with a sixty percent improvement.

Tables 2 and 3 give the delay performance characteristics of various multipliers used for the study in this paper. From the tables it can be seen that SERF adder based 2x2 multipliers are faster than the CMOS adder based 2x2 multipliers. Unfortunately, as the size of the multiplier rises, the performance of the SERF adder based circuits with respect to the CMOS adder based circuit decreases. For both tables the 2x2 cell is identical because of the simplicity of the design at such a small size.

Table 2. Circuit Delay of Bit-Array Multipliers

ARRAY MULT. TIME DELAY (ns)		
	w/SERF Adder	**w/CMOS Adder**
2x2 Cell	0.259	0.454
4x4 Bit-Array	1.035	0.674
8x8 Bit-Array	4.708	1.700

In the 2-bit Array multiplier arrangement, the SERF adder allowed for over forty percent increase in speed. This dropped for the next size in which the CMOS adder based design performed approximately thirty-five percent better and even more so for the larger circuit.

Table 3. Circuit Delay of Carry-Save Multipliers

CARRY-SAVE MULT. TIME DELAY (ns)		
	w/SERF Adder	**w/CMOS Adder**
2x2 Cell	0.259	0.454
4x4 Carry-Save	0.816	0.861
8x8 Carry-Save	6.009	1.590

The SERF adder proves to aid the performance of the Carry-Save multiplier circuit in the 2- and 4-bit circuits. The performance drops drastically for the 8-bit model and would probably continue to drop for larger models.

6. CONCLUSION:

In this paper we presented the power and speed performance characteristics of two different multipliers realized using 10 transistor SERF adders and CMOS static adders. For our comparative study we realized 2x2, 4x4 and 8x8 carry-save and bit-array multipliers. In all the studied multiplier configurations, the SERF adder based multipliers exhibited superior power performance compared to CMOS adder based multipliers. However our simulation studies clearly show that CMOS adder based multipliers are faster for higher input bit width multipliers than the SERF adder based multipliers. In digital signal processing systems where power is the foremost design constraint, SERF based multipliers are expected to be valuable building blocks.

Acknowledgement: The authors would like to thank Vijay Nair of Intel Corporation for useful discussions.

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This research was supported in part by the National Science Foundation under Grant Number ECS-0219338