C49402 16-Bit Microprocessor Slice

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CAST, Inc.

IP Center:
75 N. Broadway
Nyack, New York 10960 USA

Phone: +1 845-353-6160
Fax: +1 845-727-7607
E-Mail: info@cast-inc.com
URL : www.cast-inc.com

Features

- Eight function ALU
- Expandable – Any number of devices can be connected for wider bus structures
- Support for all original 2901 source, function and destination codes
- Additional destination codes for performance improvement allowing Direct (external) data to be directly loaded into register file and Q register
- 64-word register file with Input Shifter
- Functionality based on the IDT and Cypress 49C402

AllianceCORE™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core specification, Instruction set details, tests set details
Design File Formats	.ngo, EDIF Netlist, or VHDL Source RTL available at extra cost
Constraints File	C49402.ucf
Verification Tool	VHDL Testbench
Instantiation Templates	VHDL, Verilog
Reference designs & Application notes	Example design, assembler programs
Additional Items	Simulation and synthesis scripts
Simulation Tool Used	
1076-Compliant VHDL Simulator,	
Support	
Support provided by CAST, Inc.	

Table 1: Core Implementation Data

Supported Family	Device Tested	Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (MHz)	XILINX Tools
Spartan-II	2S150-6	670	1	73	37	M3.3i
Virtex	V150-6	670	1	73	37	M3.3i
Virtex-E	V200E-8	670	1	73	45	M3.3i

Notes:
1.Optimized for speed
2.Assuming all core I/O is routed off-chip

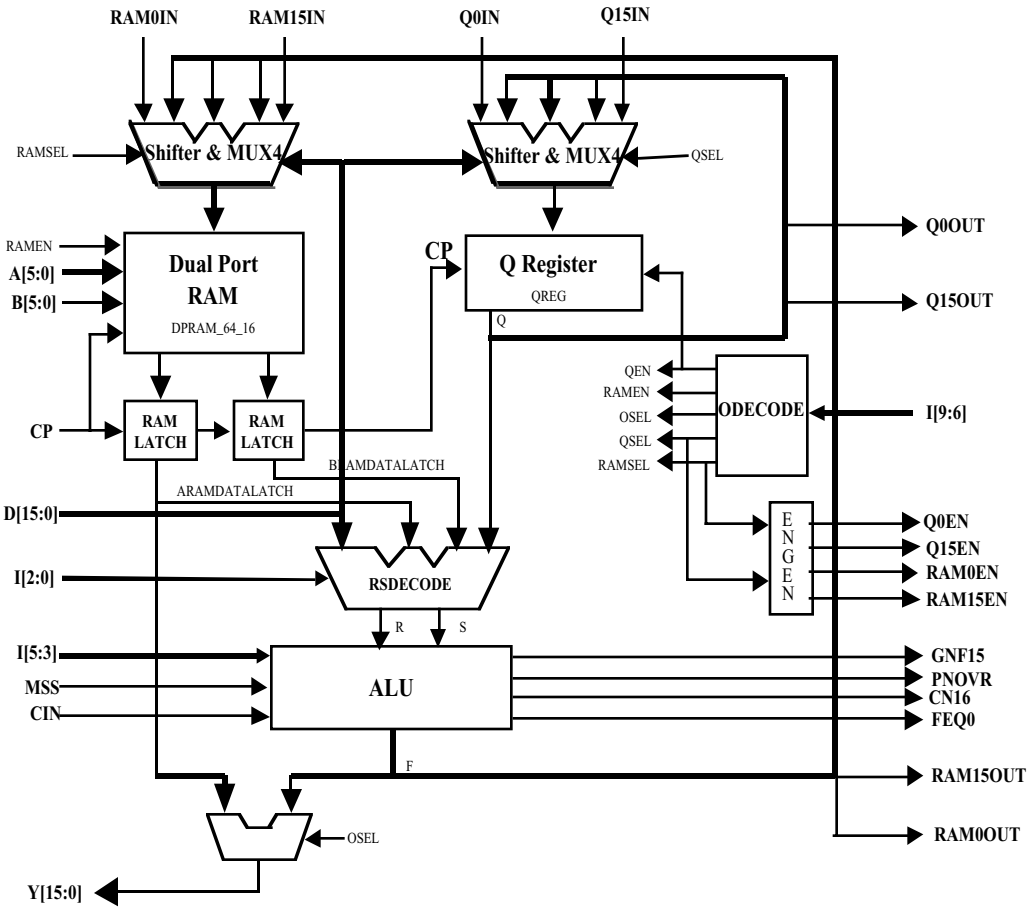

Figure 1: C49402 16-Bit Microprocessor Slice Block Diagram

Applications

The C49402 core is used where simple micro-programmable controllers are required.

General Description

The C49402 16-bit microprocessor slice core is a cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The core includes a dual-port RAM, ALU, shifter, register and multiplexer. The micro-instructions of the C49402 allow for easy modeling of various microcontrollers.

Functional Description

The C49402 core is partitioned into sections as shown in figure 1 and described below:

Dual Port RAM

The internal memory is a 16-bit by 64 deep Dual Port RAM. It is addressed for writing by the B Port and for reading by both the A and B Ports. The input data is defined by a microinstruction decoded from 4 bits of the 10-bit I Port.

RAM Latch

These latches store the outputs of the Dual Port RAM. They are clocked using the CP input. This eliminates any possible race conditions that could occur while new data is being written into the RAM

Q Register

The Q register is enabled by the internal signal qen, which is generated by the Instruction input (I) and clocked on the rising edge of CP.

ALU

The ALU accepts input from either RAM Port, the Q Register and cascaded inputs from previous stages. It has basic functions including most logic and arithmetic operations including such functions as shifting, adding and subtracting.

ODecode

The Odecode block takes bits 6 – 9 of MicroInstruction Bus and uses them to control the internal output enables and selects of the other blocks.

RSDecode

The RSDecode block takes bits 0 – 2 of the MicroInstruction Bus and uses them to control the 16-bit R and S buses. These buses get loaded with the outputs of the other blocks, routing various results back through the ALU block.

ENGEN

This block takes the select bits for the ram and q register and decodes the enable pins for the bi-directional RAM and Q bits.

Pinout

The pinout of the C49402 core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

All bi-directional pins have been split to have input, output and enable pins associated with them. This is done to be in compliance with VSIA.

Table 2. Core Signal Pinout

Signal	Signal Direction	Description
CP	In	Clock
MSS	In	Most Significant Slice
I[9:0]	In	Instruction/Microcode
D[15:0]	In	Data Input
A[5:0]	In	A-port Address
B[5:0]	In	B-port Address
OEN	In	Output Enable
CIN	In	Carry In
Q0IN	In	Shift Line — Q Registe
RAM0IN	In	Shift Line — RAM Stack
Q15IN	In	Shift Line — Q Registe
RAM15IN	In	Shift Line — RAM Stack
Q0OUT	Out	Q0 Output
RAM0OUT	Out	RAM0 Output
Q15OUT	Out	Q15 Output
RAM15OUT	Out	RAM15 Output
Q0ENB	Out	Q0 Output Enable
RAM0ENB	Out	RAM0 Output Enable
Q15ENB	Out	Q15 Output Enable
RAM15ENB	Out	RAM15 Output Enable
Y[15:0]	Out	Data Output
GNF15	Out	Carry Generate / ALU MSB
PNOVR	Out	Carry Propagate / Overflow
FEQ0	Out	ALU outputs are zero
CN16	Out	Carry out

Verification Methods

The C49402 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model, which contained the original IDT49C402 chip, and the results compared with the core's simulation outputs.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

The C49402 core is licensed from Evatronix SA.

Related Information

IDT49C402 16-Bit CMOS Microprocessor Slice Datasheets, December 1987

Xilinx Programmable Logic

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Xillinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: 408-559-7778
Fax: 408-559-7114
URL: www.xilinx.com

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