NEW CMOS CHIP FACILITATES MULTIBIT CORRELATION

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ABSTRACT

Although correlation is a simple mathematical function, its implementation in digital hardware is cumbersome and complex. During the past few years, both digital and analog correlator integrated circuits have helped reduce the cost and size of correlation hardware. Unfortunately, the analog correlators exhibit noise and calibration problems, while the digital devices are generally limited to single-bit resolution, requiring the parallel use of many devices or the use of very coarse signal quantization levels.

In response to these objections and to the need for low power correlators, TRW LSI Products is developing the TMC2220, a four-channel, 32-word CMOS digital correlator chip. This paper outlines the architecture of this versatile chip and illustrates some of its advantages in multibit and dual-channel (in phase and quadrature) applications. Potential noise performance of the four-bit correlator is compared to that of similar single-bit and ideal analog devices. A few applications which might best exploit the TMC2220's architecture are also discussed.

BACKGROUND

The TMC2220 is a sophisticated correlator integrated circuit, comprising four 1-bit, 32 tap individual correlator modules. The user can interconnect the four modules to serve a variety of applications, including 1, 2, or 4-bit single-channel or 1 or 2-bit dual-channel (quadrature) matched filtering. This paper compares the performances of 1, 2, and 4-bit correlators, describes the chip's architecture and sketches a few applications.

SIGNAL DETECTION SIMULATIONS

The most novel feature of the TMC2220 is its 4-channel architecture, which supports 1, 2, or 4-bit quantization of the incoming signal (Figure 1). Several simulations were performed to quantify and illustrate the impact of signal quantization on the accuracy and signal detection powers of a benchmark 1023-tap correlator. The modeling technique used can be easily modified to simulate a correlator of any length (number of taps or words) or width (number of bits per data word). In each test, noise uniformly and randomly distributed over the full scale input voltage was added to a binary (one unit positive or negative) signal of an assigned amplitude. Signal amplitudes used in the study ranged from 0 to 20% of peak noise level, in increments of 2%. Thus, the "signal present" tests involved (peak) signal-to-noise ratios (SNR's) of -34 dB (20log 0.02) to -14 dB (20log0.2). Since the standard deviation of a uniform 2-unit-wide distribution is 1/1.73 = 0.58, all RMS SNR's are 4.6 db less negative than the respective peak values given in this paper. In each case, the peak value of (signal + noise) was normalized to a nominal "full scale" reading of 1.0, to simulate the action of a slow automatic gain control (AGC) loop.

Four different quantization levels were modeled at each noise level (Figure 2):

a. "Analog": The incoming signal was used directly in the analysis, to the accuracy of the computer.
b. "4-Bit": The incoming signal was quantized into 16 levels, ranging from full scale negative to full scale positive.
c. "2-Bit": The incoming signal was quantized into 4 levels, two each positive and negative.
d. "1-Bit": Just the polarity (sign) of the signal was retained in the analysis.

To obtain statistically robust distributions of correlation scores, 1000 replicate trials were performed for each combination of noise and quantization levels. At each quantization level, the score distributions with and without the signal present determine the part's signal detection abilities, as discussed below.

A signal detection correlator is a matched filter, whose programmed impulse response is the signal of interest. Given only the desired signal, the correlation score will be very high; with only random noise, it will tend to be much lower. In use, each correlation score is compared to a user-selected threshold. When the score exceeds this threshold, the desired signal is deemed to have been detected. Conversely, below-threshold scores are assumed to signify "no signal."

In signal detection, a correlator's figures of merit are its false alarm rate (FAR, the "detection" of a nonexistent signal), and its missed event rate (MER, the failure to detect an existing signal). In applications requiring a low MER, it is customary to set the threshold fairly low, raising the FAR. The correlation score distribution charts (Figure 3) illustrate the tradeoff between FAR and MER for each quantization level, given a SNR of 0.1. The percentage of "signal present" cases below a reader-selected threshold is the MER; the percentage of "no-signal" cases above it is the FAR.

Figure 4 summarizes the relationship among quantization level, SNR, and FAR. In this study, each detection theshold was set at the 0.5%th percentile of signal-present correlation scores, thereby forcing the MER to 0.5%. For each quantization, the corresponding FAR's were plotted as a function of SNR. For the signals and noise conditions studied here, Figure 4 demonstrates that 4-bit quantization performs almost as well as analog correlation. As anticipated, two and one-bit correlators require stronger signals for a given FAR. The results obtained in this study are consistent with the various theoretical analyses reported elsewhere [1, 2, 3].

HARDWARE DESCRIPTION

Classically, correlators are used to detect weak signals buried in strong noise. In a signal detection application, the correlator's reference register is loaded with the desired (one-bit) coded signal. A pseudo-noise (PN) signal is employed if minimal chance of unauthorized detection is desired and/or if minimal transmitted power is required.

The TMC2220 chip is designed to support one, two, and four-bit quantization of incoming data. Furthermore, N chips can be stacked in parallel for 4N-bit quantization.

Since many applications will require reference patterns of less than 32 taps, the TMC2220 is provided with a masking function, which permits the user to decide which of the 32 taps in each channel shall be ignored by the chip's adder (Figure 5).

The TMC2220's two basic arithmetic modes are:

a. Unipolar, in which correlation scores run from 0 (a perfect anticorrelation of -1.0) to 32 (a perfect correlation of +1.0).
b. Two's complement, in which correlation scores run from -16 to +16.

This chip directly supports four-bit, single channel correlation, with a wide choice of relative weighting factors among the four data bits. Standard binary arithmetic 8:4: 2:1, is included among the options. The final output (via the main output port) is the properly weighted sum of the correlation sums of the four individual channels. This single value is very useful in numerous applications, including clipped autocorrelation, in which a multibit quantized version of a signal is correlated against a "hard-limited" (single bit) version of the same.

The TMC2220 also offers 1:1:1:1 weighting, essential for single-bit, 128-word correlation. In this mode, the sums of the individual channels are added directly, and the final sum is output. The individual reference and data registers of the four correlator modules are catenated serially, to store the required 128-word long patterns.

The TMC2220 includes a "MAX + 0.5 MIN" circuit, which estimates the vector magnitude of a quadrature signal from its two orthogonal components, $|I|$ and $|Q|$. This approximation of the Pythagorean function was selected for its economical hardware realization. Figure 6 demonstrates that the worst-case error is under 12%, with an average error below 9%. The user can reduce these errors to 6% and 4% by multiplying its vector magnitude output by 15/16, which requires only a 12-bit subtractor. If greater accuracy is required, Reference [4] catalogues more sophisticated Pythagorean approximations.

REAL WORLD APPLICATIONS AND ADVANTAGES

Over the past four decades, extensive theoretical work has been done to motivate the use of both single-bit and multibit digital correlators. As systems are designed and built for more sophisticated, higher speed, and lower power applications in a variety of noise environments, the desirability of a multibit CMOS correlator will continue to grow. The most obvious advantages of the TMC2220 over the TDC1023 are its low power and its on-chip parallel expansion into 4-bit resolution. Four-bit applications require at least four TDC1023's and six 4-bit adders per 64-tap section. These ten chips can now be replaced with a single TMC2220 for each 32-tap section, or two TMC2220's and two 4-bit adders for 64 taps. Despite its five-fold power advantage over the TDC1023, the TMC2220 actually offers a higher operating speed, supporting digital signal sampling rates up to a full 20 MHz.

With the availability of the TMC2220, system architectures and hardware tradeoffs need to be reexamined. Its multibit resolution is particularly advantageous in RADAR systems, when jamming may be present. Our simple statistical analysis assumed a benign environment with uniform noise and a constant signal. However, deliberate jamming can present a much greater challenge to the correlator. The use of long PN sequences with very sharply peaked, unambiguous autocorrelation functions is helpful, since the high integration gain will tend to cancel out the effects of uncorrelated noise. Where adaptive, intelligent jammers are used, the PN code can be changed each cycle, with the added benefit of further improving system performance by decorrelating "second time around" echoes. The multibit correlator can further enhance the performance of such a system, by reducing arithmetic quantization noise. As the simulations demonstrated, a correlator's ability to extract weak signals buried in noise increases with its resolution, at least up to 4-bits. With a digital correlator, changing the PN code, its length, or the relative weighting of its bits is simply a matter of loading the new values from RAM or ROM. The variations can be implemented automatically and adaptively, as needed.

The increasing use of satellite data communication links provides additional demand for multibit correlators. As millimeter wave links are established and gallium arsenide makes higher modulation bandwidths possible, it becomes feasible to trade effective bandwidth against error rate, by varying the amount of redundancy in the information transmitted. Just as military or space shuttle data traffic is less tolerant of error than TV sitcom reruns, extra error correction and sync detection can be designed into the more critical systems only, permitting economical transfer of data in the less critical channels. Given a satellite's very limited high-frequency power output, this sort of error rate tradeoff becomes critical. The system designer can interleave data for burst error tolerance, then code both sync and data with long orthogonal PN sequences. Selecting longer PN sequences lowers both the effective communication data rate and the error rate. The same tradeoffs apply to high bandwidth fiberoptic data links. Again, as in our RADAR example, simply by changing the length of the codes, the user can easily and cheaply adapt the system to its noise environment and error immunity requirements.

Sophisticated image processing often involves correlation in the frequency domain. Here, the "data" points are spectral line intensities in frequency space instead of in the time domain, but the correlator doesn't care. The expected results of a 32-point FFT could be correlated in a single TMC2220, with one frequency bin per correlator tap. Here, the chip's four-bit resolution is needed to accommodate the dynamic range of the frequency-transformed data. In this frequency domain application, uninteresting bands may be masked off, to concentrate the analysis on the most critical bands only. (The TDC1023 has taught us that the uses of a digital correlator are limited only by the user's creativity.)

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[3] Chang, K.Y., Modified Digital Correlator and Its Estimation Errors, IEEE TRANS INFO THEORY Vol IT-16, No.6, November, 1970.

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[5] Golomb, S., Shift Register Sequences, Holden Day, 1967.

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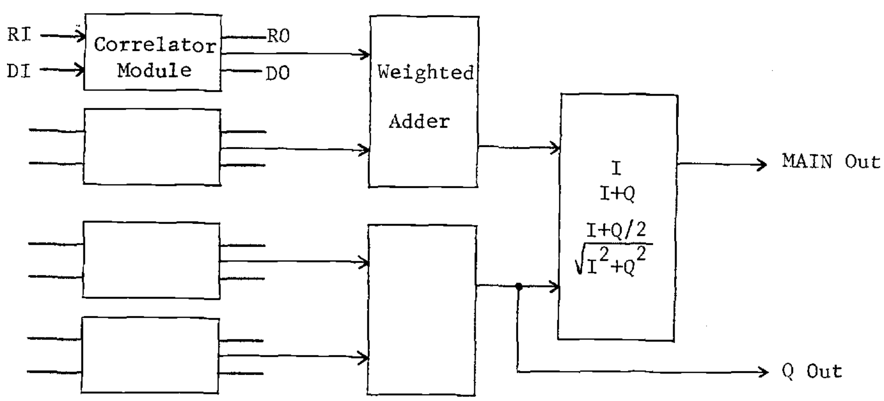

Figure 1. Block Diagram

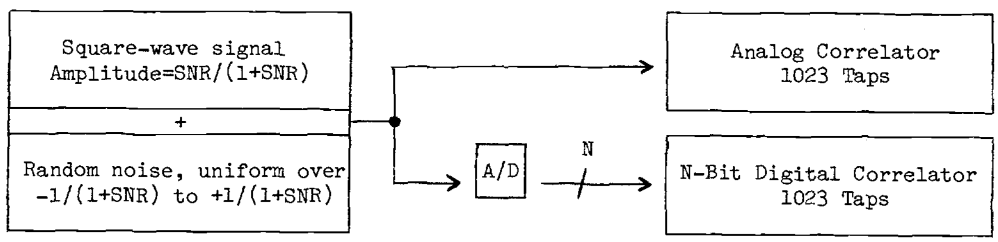

Figure 2. Conceptual Structure of Model

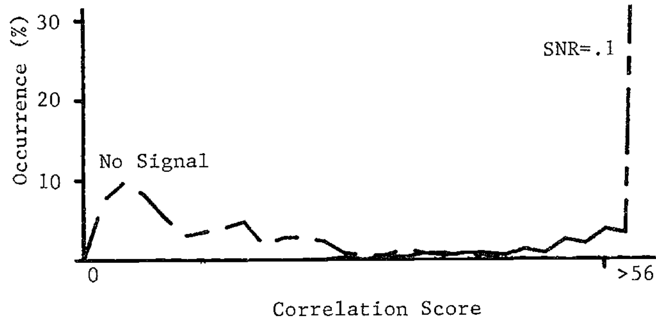

Figure 3A. Analog Correlator, 1023 Taps

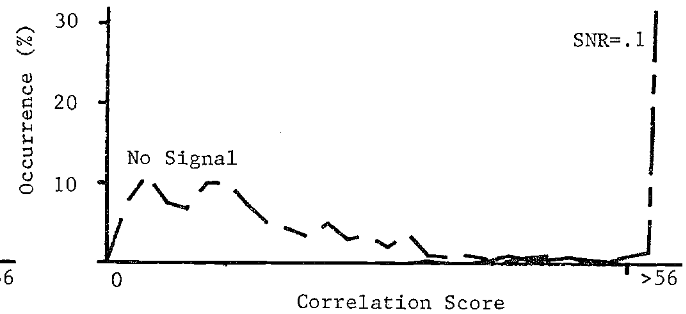

Figure 3B. Four-Bit Correlator, 1023 Taps

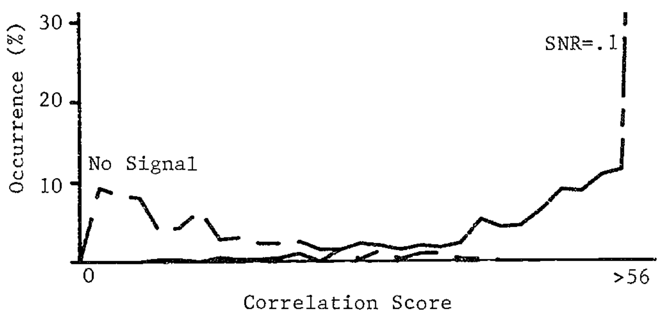

Figure 3C. Two-Bit Correlator, 1023 Taps

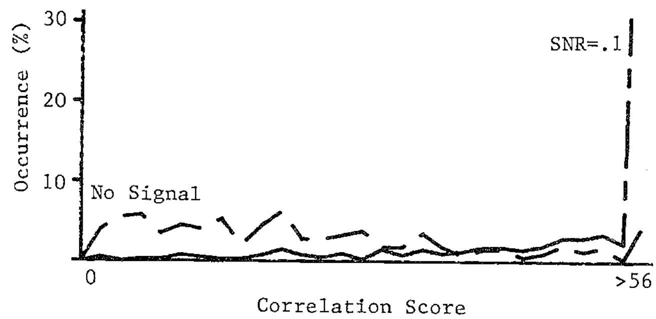

Figure 3D. One-Bit Correlator, 1023 Taps

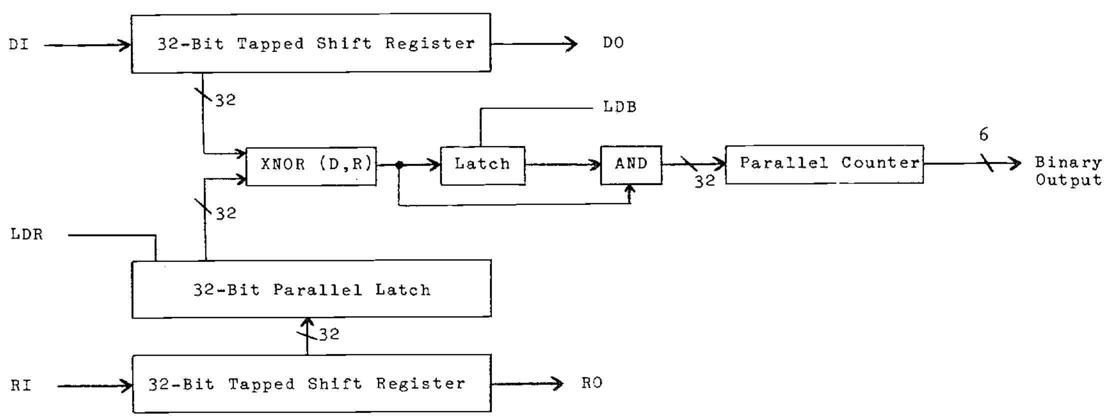

Figure 5. Correlator Module

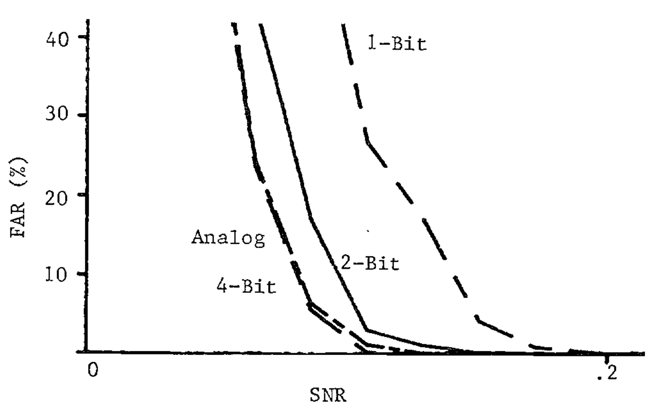

Figure 4. FAR For MER=0.5%

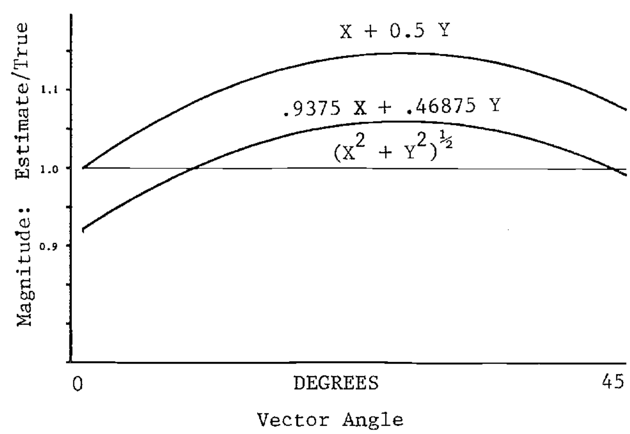

Figure 6. Pythagorean Approximations