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M320C25

DIGITAL SIGNAL PROCESSOR

OVERVIEW

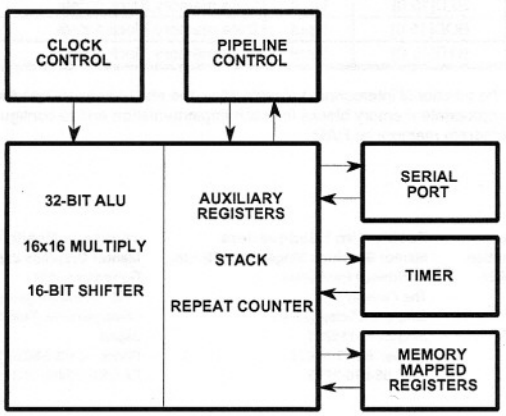
The M320C25 is a highly-efficient 16-bit digital signal processor with separate Data and Program memory, each of which may be up to 64K words. It has a 16 -bit shifter, a 16 x 16 bit parallel multiplier and a 32-bit ALU/accumulator. It also offers a 16-bit timer, eight auxiliary registers, an eight-level hardware stack, sixteen I/O addresses, and a 8/16-bit serial port.

The design is pipelined for speed of operation. It also offers an Idle mode in which internal clocks are disabled to reduce power consumption.

KEY FEATURES

- Software compatible with TI 320C25
- 32-bit ALU/Accumulator
- 16 x 16 Parallel Multiplier
- 16-bit Shifter
- Up to 64K words each of Program memory and Data memory
- Up to 16 I/O addresses
- Instruction times fully compatible with industry standard 320C25
- 16-bit Timer
- Serial Port

BLOCK DIAGRAM



DELIVERABLES

- Verilog source code
- VHDL source code
- Synthesis script for Design Compiler
- Verilog & VHDL test vectors
- Reference technology netlist

SOFT CORES

PERFORMANCE

The M320C25 offers high performance digital signal processing through features such as single-cycle multiply and accumulate instructions, an eight-level hardware stack, eight auxiliary registers and a dedicated arithmetic unit.

The M320C25 has been proven to wo rk at clock rates of up to 60MHz in 1 µ technology, with the serial controller working at over 7MHz.

PROGRAM MEMORY

The M320C25 supports up to 4K words of internal (on-chip) program memory and up to 64K words of external program memory.

The M320C25 contains no RAM or ROM but provides functional interconnect signals for connecting to RAM blocks. If internal program memory is required, a single port RAM (or ROM) block of up to 4K x 16 may be connected to the M320C25. Alternatively, a 256x16 block of internal data RAM may be configured as program memory.

The use of RAM rather than ROM allows the user to download program code from slow external ROM. The use of internal data RAM as program memory will give fast context switching.

DATA MEMORY

The M320C25 supports up to 544 words of internal data memory and up to 64K words of external data memory.

If internal data memory is required, this can be provided by adding 1, 2 or 3 blocks of dual port RAM may be connected to the M320C25. Blocks 0 and 1 can be up to 256 x 16; Block 2 can be up to 32 x 16.

The external data memory can be of three types: 'Local'; I/O selected; and 'Global'. Local memory is exclusive to the M320C25 but Global memory can be shared with other devices, allowing cooperative processing with other digital signal processors.

POWER-SAVING MODES

The M320C25 offers two power-saving modes, Idle and Hold. In Idle mode, all internal states are maintained. In Hold mode, the address bus and control signals are all 3 -stated.

For very low power use, LOWPOW may be used during Idle mode to disable the external clocks CKQ1-4. The control lines and the address bus remain active, but the data bus is high impedance.

SIGNAL DESCRIPTION

The M320C25 has 205 external signals; 102 inputs and 103 outputs.

SIGNAL	TYPE	DESCRIPTION
DSP INPUTS		
CKQ[4:1]	Input	4-phase clock which is stopped in Idle mode
CCKQ[4:1]	Input	4-phase clock that runs continuously
NRS	Input	Reset, active low
DI[15:0]	Input	Data bus inputs
READY	Input	Data ready
NHOLD	Input	Select Hold mode
NBIO	Input	Branch control
NINT[2:0]	Input	Three external interrupts, active low
NTEST	Input	Only used during scan test
MPNMC	Input	Mode select
CLKR, CLKX	Input	Serial port receive/transmit
DR	Input	Serial port receive data input
FSR, FSXI	Input	Serial port receive/transmit synchronisation
DSP OUTPUTS		
A[15:0]	Output	Address bus
NDS	Output	Data memory select, active low
NPS	Output	Program memory select, active low
NIS	Output	I/O select, active low
RNW	Output	Read Not Write select
NSTRB	Output	External bus cycle strobe, active low
NHLZ	Output	Control signal 3-state enable, active low
OD[15:0]	Output	Data bus output
NDEN	Output	Data bus 3-state enable, active low
NBR	Output	Bus request, active low
NHLDA	Output	Hold acknowledge, active low
NIACK	Output	Interrupt acknowledge, active low
NMSC	Output	Microstate complete, active low
XF	Output	External flag
CLKOUT1,2	Output	Instruction cycle phase indicators
DX	Output	Serial port transmit data output (+Enable)
FSXO	Output	Serial port transmit synch output (+Enable)
LOWPOW	Output	Used in Idle mode to disable CKQ1-4
FUNCTIONAL INTERCONNECT SIGNALS		
MD[15:0]	Input	Program memory data
MA[11:0]	Output	Program memory address
NMOE	Output	Program memory output enable, active low
NMWE	Output	Program memory write strobe, active low
NRDB[2:0]	Output	Data memory block enables, active low
NWRB[2:0]	Output	Data memory block write strobes, active low
RA[7:0],WA[7:0]	Output	Data memory read/write address
BZRA[7:0]	Output	Data memory Block 0 read address
BZWA[7:0]	Output	Data memory Block 0 write address
BZD[15:0]	Input	Data memory Block 0 data
BOD[15:0]	Input	Data memory Block 1 data
BTD[15:0]	Input	Data memory Block 2 data

The functional interconnect signals allow the end user to choose the appropriate memory blocks for each implementation and to configure internal program memory as RAM.

REFERENCE TECHNOLOGY GATE COUNT: 25000

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