A 1-Mb 2-Tr/b Nonvolatile CAM Based on Flash Memory Technologies

Tohru Miwa, Hachiro Yamada, Yoshinori Hirota, Toshiya Satoh, and Hideki Hara

***Abstract*—This paper describes the circuit technologies and the experimental results for a 1 Mb flash CAM, a content addressable memory LSI based on flash memory technologies.**

Each memory cell in the flash CAM consists of a pair of flash memory cell transistors. Additionally, four new circuit technologies have been developed: a small-size search sense amplifier; a highly parallel search management circuit; a high-speed priority encoder; and word line/bit line redundancy circuits for higher production yields.

A cell size of 10.34 μm^2 and a die size of 42.9 mm^2 have been achieved with 0.8 μm design rules. Read access time and search access time are 115 ns and 145 ns, respectively, with a 5 V supply voltage. Power dissipation in 3.3 MHz operations is 210 mW in read and 140 mW in search access.

I. Introduction

A CONTENT addressable memory (CAM) is a functional memory in which large amounts of stored data are simultaneously compared with input data, and the addresses of any matches are then output. CAM LSI's are utilized in data flow computers to search for executable data [1], in LAN packet routers as terminal address tables for searching out destination addresses [2], etc. A number of SRAM-based and DRAM-based CAM LSI's have been developed for such applications, and their memory cells each consist of a normal SRAM or DRAM cell and a comparator [3]–[5]. Because of the large number of transistors in such memory cells, CAM capacity has been limited to 20 Kb SRAM-based [3] and 288 Kb DRAM-based [4]. Further, these are volatile memories, which means that systems employing them require time overheads for loading data into them.

What are needed are higher capacity, nonvolatile CAM LSI's, and our approach has been to develop a high-capacity, flash-memory-based CAM (flash CAM) LSI. Though each of its memory cells consists of only two floating gate transistors, it can be searched for masked binary data. This structure stands in strong contrast to the structure of cells in SRAM-based CAM's (17 transistors: two six-transistor SRAM cells and a five-transistor comparator) or in DRAM-based CAM's (five transistors and two capacitors: two one-transistor/one-capacitor DRAM cells and a three-transistor comparator), as shown in Figs. 1 and 2. In addition to the important fact that flash CAM's are nonvolatile, they also feature on-board programmable/erasable memory storage.

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T. Miwa, H. Yamada, and Y. Hirota are with the Microelectronics Research Laboratories, NEC Corporation, Sagamihara, Kanagawa 229, Japan.

T. Satoh and H. Hara are with the LSI Memory Division, NEC Corporation, Sagamihara, Kanagawa 229, Japan.

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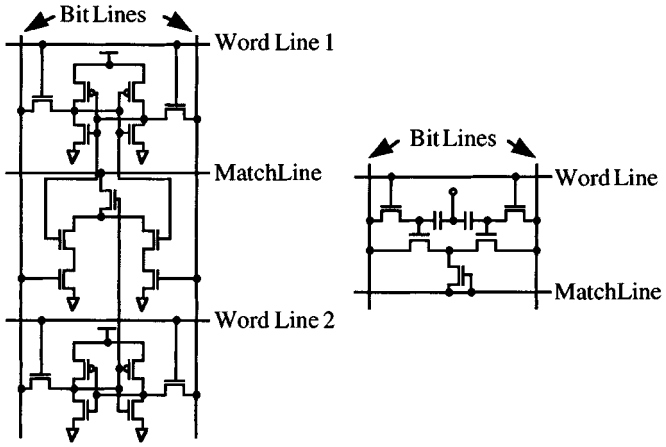

Fig. 1. Conventional CAM cell configurations.

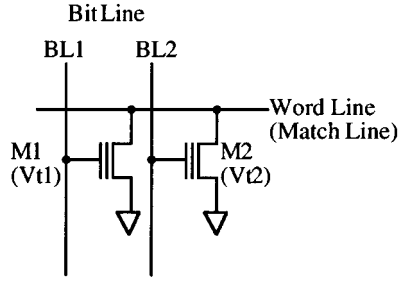

Fig. 2. Flash CAM cell configuration.

Our design also stands in contrast to the CAM cell array using floating gate transistors described by T. Hanyu *et al.* in [6] and [7]. While LSI's based on such multivalued arrays have the great advantage of higher density, they would be hard to implement: the complicated multivalued logic they require would mean that their active operational margins would be smaller than normal binary flash memories and insufficient for stable operations. Our flash CAM is based on binary logic, and its active margin is fully sufficient in this respect.

In addition to a new cell structure, four new circuit technologies have made particular contributions to the development of our high performance flash CAM LSI: 1) a small-area, low-power, current differential sense amplifier for highly parallel search operations; 2) a search management circuit for on-chip result management and extra long word searching; 3) a high-speed priority encoder provided with inhibit signal bypasses; and 4) word line/bit line redundancy circuits for higher production yields.

TABLE I
MEMORY CELL TRANSISTOR ACTIONS

Stored Data (Vt1, Vt2)	Search Data (VBL1, VBL2) "1" (5V, 0V)	"0" (0V, 5V)	"masked" (0V, 0V)
"1" (>7V, <3V)	OFF, OFF match	OFF, *ON* *non-match*	OFF, OFF match
"0" (<3V, >7V)	*ON*, OFF *non-match*	OFF, OFF match	OFF, OFF match
"don't care" (>7V, >7V)	OFF, OFF match	OFF, OFF match	OFF, OFF match

II. FLASH CAM CELL ARRAY

As illustrated in Fig. 2, each flash CAM cell consists of a pair of floating gate transistors (M1, M2). In a flash CAM cell, a word line is also used as a match line. The threshold voltage of each floating gate transistor is programmed to become either under 3 V or over 7 V, depending on the value of the data item stored in the cell. For a search operation, each bit line is set at 0 V or 5 V, depending on the value of the data item being searched for along that line. Threshold voltages for individual stored data items and bit line voltages for individual search data items are shown in Table I.

Table I also shows the memory cell transistor actions performed for all the various possible combinations of stored and search data values. As may be seen in the table, where the search data item is a "nonmatch" with the stored data, one of the transistors is ON; both transistors are OFF only when the search data item is a "match" with the stored data item. For example, when the search data item is "1" and the stored data item is "1" ("match" condition), M1 ($V_{t1} > 7$ V) is OFF with BL1 at 5 V, and M2 ($V_{t2} < 3$ V) is also OFF with BL2 at 0 V. On the other hand, when the search data item is "1" and the stored data item is "0" ("nonmatch" condition), M2 ($V_{t2} < 3$ V) turns ON with BL2 at 5 V. The stored data item "don't care" can be used to fill in the unused bits in memory words, and the search data item "masked" can be used to ignore irrelevant bits in a search operation.

A flash CAM cell consisting simply of two floating gate transistors is naturally much smaller than a RAM-based CAM cell, which consists of a RAM cell and a comparator, but it is still able to perform the same functions of memory storage and comparison.

For bit-parallel search operations, flash CAM cells in individual words are arranged in parallel. This means that if even one cell in a word represents a "nonmatch," the entire word is a "nonmatch." For word-parallel search operations, bit lines are shared by some number of words. In this way, the memory cell array of the flash CAM is a matrix of floating gate transistors, as shown in Fig. 3, and resembles a NOR-type flash memory cell array. The flash CAM cell array has the same layout image as a NOR-type flash memory cell array. The drain nodes of each individual row are connected to a word line, and the gate nodes of each individual column are connected to a bit line. The flash CAM's word lines are drain lines, and its bit lines are gate lines. This is the only difference between the flash CAM cell array and that of a conventional flash memory, in which word lines are not drain lines but gate lines, and bit lines are not gate lines but drain lines.

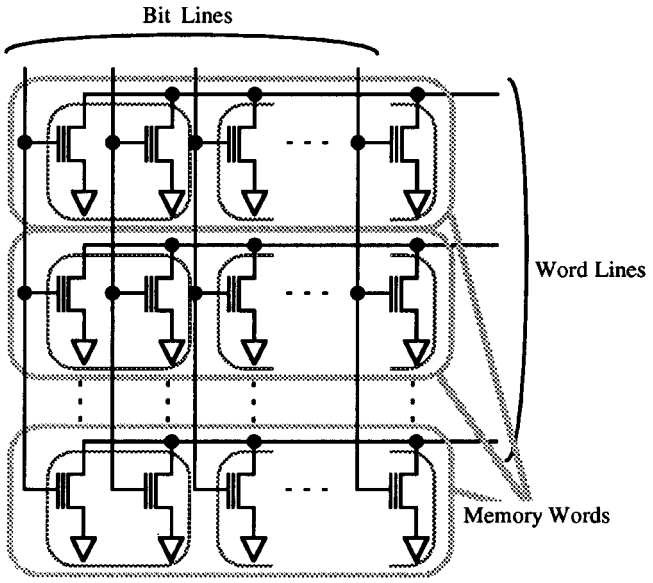

Fig. 3. Flash CAM cell array configuration.

Because flash CAM cells in a memory word share one drain line, bit-parallel read/write accesses are impossible. Thus, in the flash CAM, read/write accesses are carried out bit-serially.

III. FLASH CAM CIRCUIT TECHNOLOGIES

In addition to circuits in NOR-type flash memories, our newly developed flash CAM, shown in Fig. 4, consists of two shift registers and circuits of four newly developed designs: 1) small-area low-power search sense amplifiers; 2) search management circuits for on-chip result processing; 3) a high-speed priority encoder provided with inhibit signal bypasses; and 4) word line/bit line redundancy circuits for higher production yields.

For search operations, each bit line is set at 0 V or 5 V depending on the data stored in the shift registers, as shown in Fig. 5. Each search sense amplifier detects whether its word line leaks or not, and it outputs the results. Search results are operated on by the search management circuits, and the priority encoder generates the highest priority address of any "matched" words. New redundancy circuits are effective in improving the yields both of word-line and of bit-line defects.

A. Search Sense Amplifier

We have developed the small-area, low-power, nine-transistor sense amplifier shown in Fig. 6 for highly parallel search operations. In contrast to commonly used sense amplifiers, which consist of two current-voltage converters and a voltage-differential amplifier [8], ours is a latch-type current-differential amplifier. Because it contains no current mirror amplifier, power dissipation is quite low.

For search operations, each search sense amplifier detects whether its word line leaks or not. If there is no ON cell transistor in the word line, the search sense amplifier senses a "match." If there is at least one ON cell transistor, the search sense amplifier senses a "nonmatch."

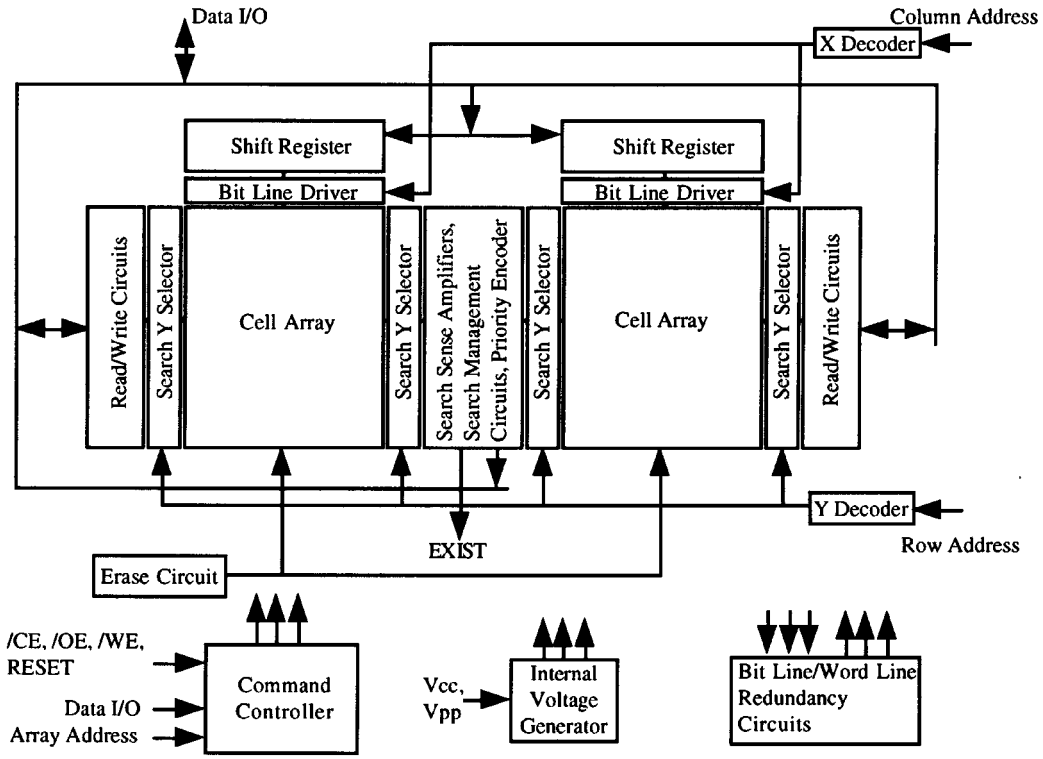

Fig. 4. Flash CAM block diagram.

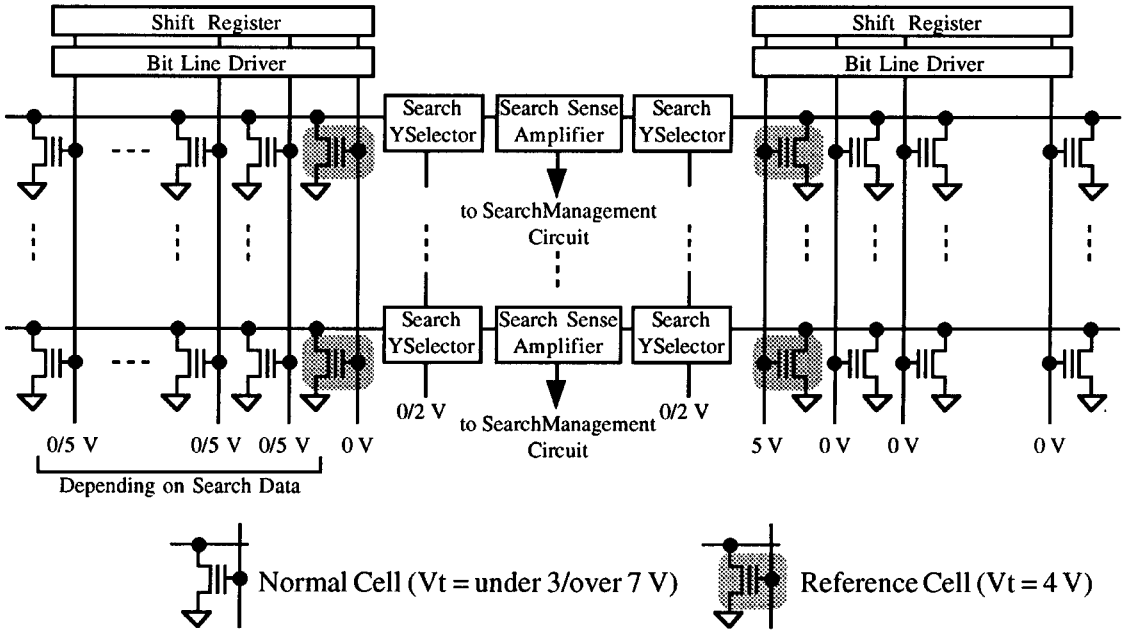

Fig. 5. Search operation on the left cell array.

In the flash CAM, we employ an open word line sensing scheme. The search sense amplifiers are laid out between the two memory cell arrays. In search operations in the left array, as shown in Fig. 5, each search sense amplifier compares the current in the left word line with the reference current in the right word line. Each word line has a reference memory cell which drives half the amount of current that an ON cell transistor drives. Reference cells are the same size as normal cells and are laid out in the cell arrays. In wafer testing, the threshold voltages of the reference cells are set at 4 V by means of read/write circuits.

Since each word line has its own reference cell, the longest read disturb time of reference cells is the same as that of normal cells, i.e., read disturbance is not a problem in reference cells. The source nodes of reference cells are separated from the source nodes of normal cells, and in an erase operation on normal cells, the threshold voltages of reference memory cells are not lowered.

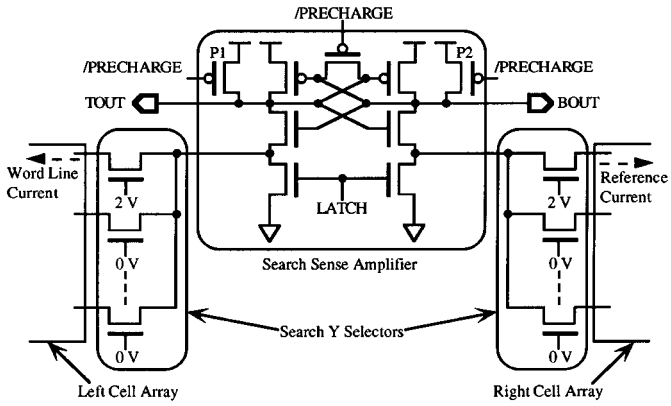

Fig. 6. Search sense amplifier circuit configuration.

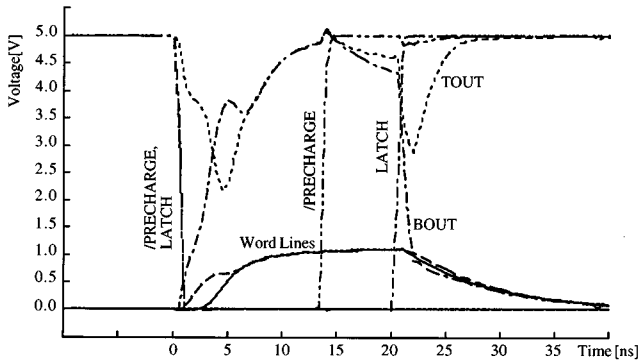

Fig. 7. Simulated waveforms of search sense amplifier.

In search operations, the amplifier detects the difference between the word line current and the reference current in the following way. First, a low level /PRECHARGE signal precharges the word lines. Word line voltage is kept under 1 V ($2V - V_{tn}$) by a search Y selector to avoid read disturbance, and the active current is limited by the saturation currents of precharge PMOS transistors (P1, P2). This active current is independent of the number of ON memory cell transistors in the word line. Next, after the /PRECHARGE signal returns to a high level, the difference between the word line current and the reference current makes the output nodes' (TOUT, BOUT) voltages different. Finally, the LATCH signal at a high level amplifies the output nodes' voltages. After current detection, the sense amplifier holds the result and does not dissipate any more power until time for the next detection.

Fig. 7 shows simulated waveforms for the search sense amplifier in a search operation on the left cell array. In this simulation, each word line has 1024 normal cells and one reference cell. All of the normal cells in both word lines are OFF ("match" condition), and only the right reference cell is ON. Peak power in the search sense amplifier is limited to 4 mW.

B. Search Management Circuit

On-chip parallel executions of logic functions upon search results (search management) are effective in improving CAM performance. With search management, CAM's can perform on-chip retrieval formula processing and extra long word

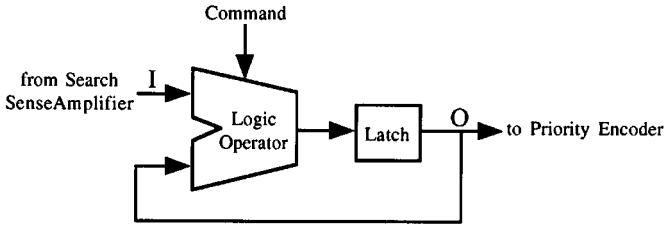

Fig. 8. Basic idea of search management circuit.

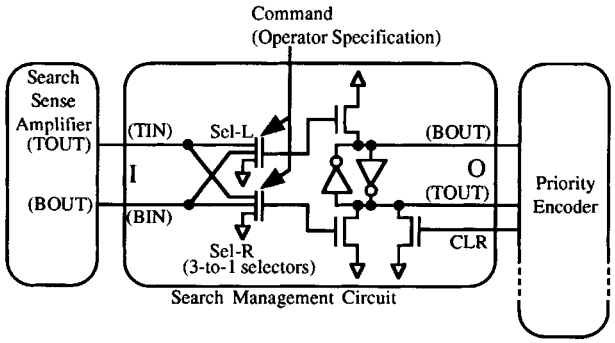

Fig. 9. Search management circuit diagram.

search operations. There are two main advantages of on-chip search management operations. First, on-chip operations are generally faster than off-chip operations because they are highly parallel and have no need for search result transportation. Second, on-chip operations reduce the load of the CPU, which computes off-chip operations. In order not to spoil the parallelism of the flash CAM's search sense amplifier, the search management circuit should also be small and use very little power. Fig. 8 illustrates its basic concept of our design in this regard, and Fig. 9 is a circuit diagram. Each search management circuit is connected to its own individual search sense amplifier, which detects the leakage of its memory words. The search management circuit accumulates search results and generates an operation result.

As may be seen in Fig. 8, the search management circuit performs a logic function on the output of search sense amplifier (I) and previous operation result (O) (which it has retained). It then retains the result of this operation as a new operation result (O′).

CAM's can perform complicated retrieval formula operations by using the search management circuits to process the search results for particular memory words. They can also search for extra long words by calculating logical-AND for word search results.

In order to maintain a low power dissipation and a small circuit area, we designed our search management circuit to consist simply of one SRAM-cell-like flip flop and two three-input selectors (Sel-L, Sel-R). The circuit has two complemental input signals, TIN (active high) and BIN (active low), and two complemental output signals, TOUT (active high) and BOUT (active low). The selectors normally output at ground level, and the flip flop holds the result of the previous logical operation. In search operations, the selectors select appropriate signals depending on the input commands, and the output

TABLE II
LOGIC OPERATIONS OF SEARCH MANAGEMENT CIRCUIT

Output of Sel-L	Output of Sel-R	Logic Operation	
BIN	TIN	THROUGH	O′ = I
TIN	BIN	NOT	O′ = *not*(I)
BIN	GND	AND	O′ = *and*(O, I)
GND	TIN	OR	O′ = *or*(O, I)
TIN	GND	SUB	O′ = *and*(O, *not*(I))
GND	BIN	—	O′ = *or*(O, *not*(I))
GND	GND	HOLD	O′ = O

of the flip flop is modified. The search management circuit operates six different logic functions and a hold function, as shown in Table II. For example, when Sel-L selects BIN (active low input signal) and Sel-R selects ground level, if BIN = 1 (TIN = 0), the output node TOUT is connected to ground node and TOUT will be zero. On the other hand, if BIN = 0 (TIN = 1), TOUT will keep its previous value. Therefore, the new operation result becomes *and* (old operation result, search result).

The seven operations shown in Table II cover all two-input (I, O) logical operations, which are unate (positive or negative) in "I" and positive in "O." These are enough to operate perform retrieval formula operations and searches for extra long words.

An input signal CLR at a high level resets the operation result. After a search operation, the flash CAM outputs all of the "matched" addresses in the following sequence [5], [9]. First, the priority encoder generates the address of the highest priority "matched" word and outputs it. Second, the priority encoder sets the CLR signal of the highest priority "matched" word at high level to reset its search management circuit. Then the priority encoder generates the address of the second highest "matched" word. The last two steps are repeated to generate all of the "matched" addresses in the priority order, until there is no "match" in the search management circuits.

C. Priority Encoder

As a search operation becomes more highly parallelized, delay in the priority encoder, which arbitrates among multiple "matched" words, occupies a larger part of total search operation delay, and for this reason, we have developed a high-speed priority encoder which consists of a priority selector with bypasses and an address encoder (ROM) and which is a modification of the priority encoder reported in [5]. If at least one input signal is "match," a priority selector sets an EXIST output at high level, selects the highest priority "match" in input "match" signals and sets its individual output signal at a high level, and an address encoder generates the highest priority "match" address. On the other hand, if any input signal is not "match," the priority selector sets the EXIST output at low level. In order to speed the priority selector operations, it is designed to consist of a global high speed ripple chain (EXIST chain) and local priority selectors (INHIBIT chains), as shown in Fig. 10. The priority selector selects the highest priority "match" input and outputs the EXIST signal in the following way. When an input is "match," its stage of the EXIST chain generates an EXIST signal at a high level. The

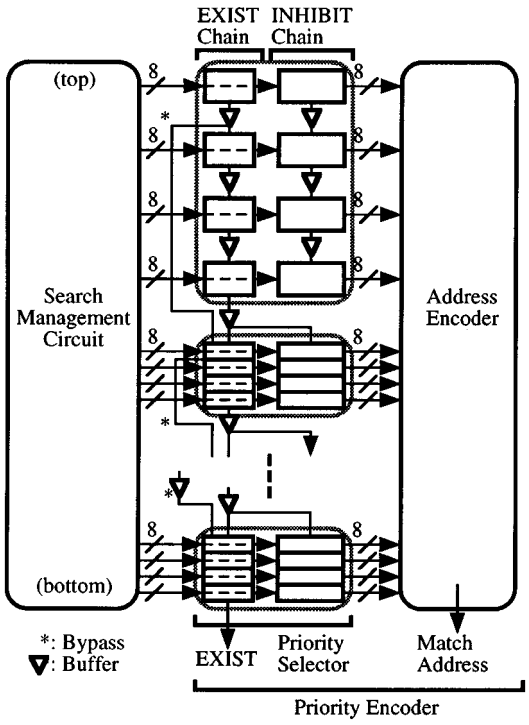

Fig. 10. Block diagram of the priority encoder.

EXIST signal at a high level is propagated through the EXIST chain to the lower priority stages. The EXIST chain outputs the EXIST signal from its bottom stage. The EXIST signal at a high level signifies that there is at least one "match" input. When at least one input of an INHIBIT chain is "match" and there is no "match" input in higher priority INHIBIT chains (known from the EXIST chain), the INHIBIT chain selects the highest priority "match" in its "match" inputs, and sets the individual output at a high level.

To speed our priority selector, we have made two modifications. First, to minimize delay through local inhibit chains, we use a low threshold voltage NMOS transistor ($V_t = 0$ V) as a transfer gate. Fig. 11 shows the circuit diagram of a bit slice of the priory selector. Second, to speed the EXIST chain, we use EXIST signal bypasses in addition to a conventional sequential path. The block diagram of the priority selector is shown in Fig. 10. In simulation, the addition of these bypasses helps to improve encoding delay, from 34 ns to 19 ns, where a priority selector (258-input) consisted of 33 serially assigned inhibit chains (32 eight-input and one two-input). The priority selector was provided with eight four-INHIBIT-chain-skip bypasses in addition to the sequential path.

D. Word Line/Bit Line Redundancy Circuits

To overcome reliability problems associated with increasingly dense large memory LSI's, redundancy circuits are essential. This has not been a problem for content addressable memories because of their small capacities, but in large capacity flash CAM's, word line and bit line redundancy circuits are necessary.

Both types of redundancy circuits present difficulties, however. In a word line redundancy circuit, we must maintain

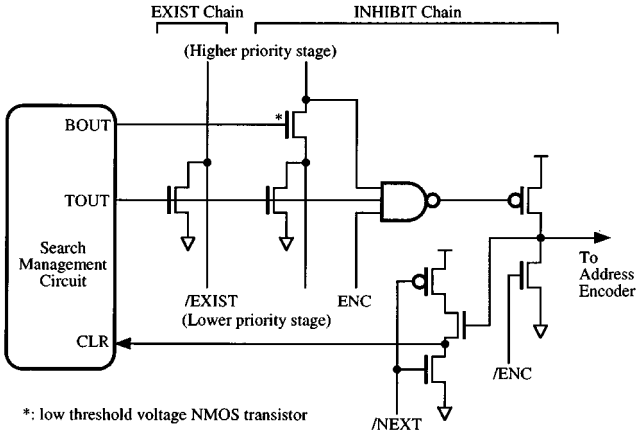

Fig. 11. Circuit diagram of a bit slice of the priority selector.

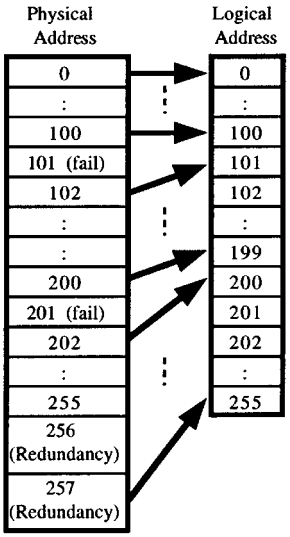

Fig. 12. Physical addresses and logical addresses of the search sense amplifiers.

consistency between the address order and the priority order, and in a bit line redundancy circuit, we must prevent failure due to "over-erasure" in unused bit lines [10].

In our flash CAM, search sense amplifiers are laid out in a line from the top of the chip to the bottom, and physical addresses are assigned to each, as shown in Fig. 12. In an ordinary redundancy scheme, when a failed word-line is detected, the amplifier connected to it will be replaced by one of the bottom-most (redundancy) amplifiers. This could create a logical inconsistency, however, in the case in which "multiple" matches are detected; if, for example, one of the matches were a replacement (redundancy) amplifier [R] and another match were an amplifier [X] located below the amplifier for which the replacement had originally been made, since a priority encoder always generates the physical address of the "upper-most" amplifier for any multiple match, in this case it would generate the address for [X] when in fact it should generate the address for [R], which actually represents a higher position.

In order to avoid the creation of such inconsistencies, we employ a newly developed word line redundancy circuit, which consists of two converters, shown in Figs. 13 and

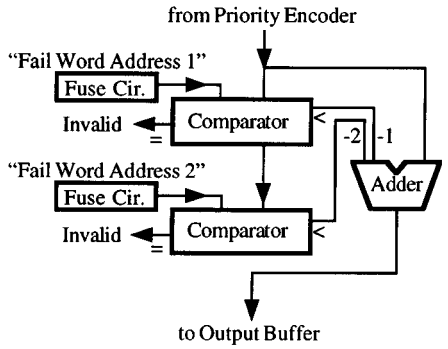

Fig. 13. Block diagram of the physical-to-logical converter.

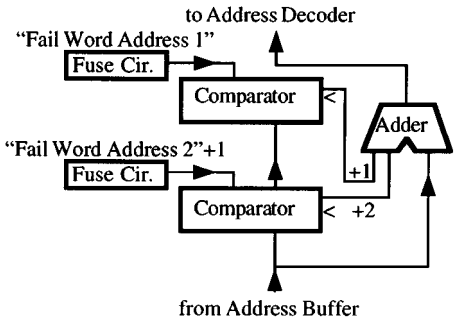

Fig. 14. Block diagram of the logical-to-physical converter.

14, used in combination. The converter shown in Fig. 13 generates logical addresses on the basis of the physical addresses in the sense amplifiers. When a failed word line has been detected, it simply subtracts one or two (as appropriate) from subsequent physical addresses to create logical addresses. This has the effect of covering a failure simply by shifting all amplifiers below it up one position (Fig. 12), thus maintaining proper order and avoiding any inconsistency. The converter shown in Fig. 14 operates as a decoder to reverse this process by adding one or two (as appropriate) to logical addresses; it recreates the correct physical address from the adjusted logical address that it has received.

The physical-to-logical converter (Fig. 13) and the logical-to-physical converter (Fig. 14) can share an adder, comparators, and fuse circuits.

While the word line redundancy circuit formed by these two converters can repair at most two word line failures, more can be repaired if we increase the size of the converters.

We have also developed a bit line redundancy circuit with small delay overhead. In erase operations, this circuit loads shift registers with the proper data needed to select all unused bit lines. Then, when the cell source node is at high voltage, all unused bit lines will be at 5 V. This prevents over-erasure of unused cells. The loading time of this bit line redundancy circuit is much shorter than the preprogramming time of the gate line redundancy circuits utilized in normal flash memories.

IV. Experimental Results

Fig. 15 is a chip micrograph of our 1-Mb flash CAM, fabricated using 0.8-μm CMOS flash memory technologies with double polysilicon and double metal wiring.

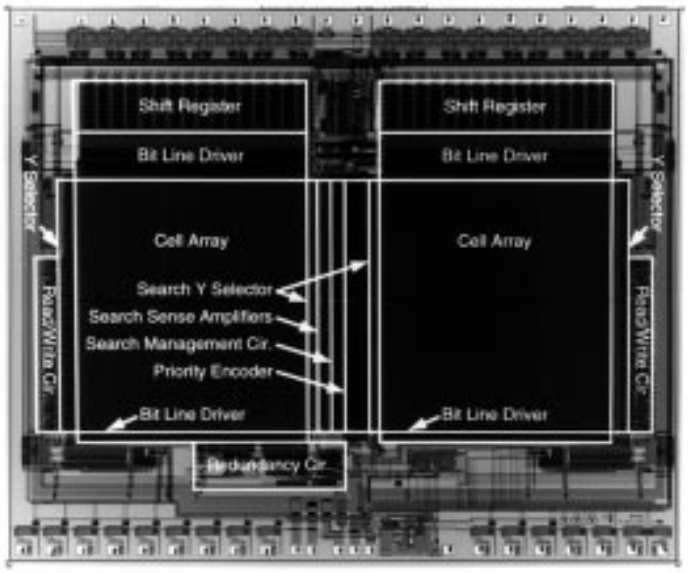

Fig. 15. Chip micrograph of the 1-Mb flash CAM.

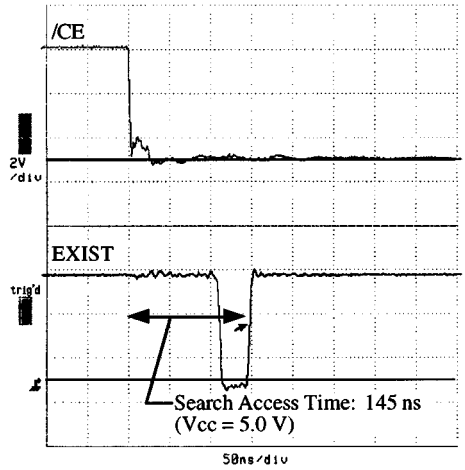

Fig. 16. Measured search operation waveforms.

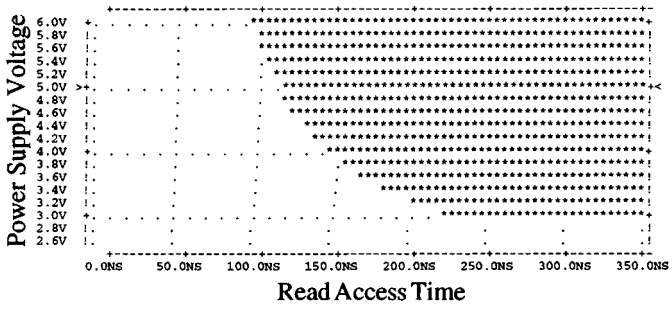

Fig. 17. Read access time versus power supply voltage.

Word organization is 128 b $\times$ 8 K words, and arrays are organized in 1 K word lines$\times$ 1 Kb lines$\times$ 2 planes. Each word line has 512 + 4 (redundancy) cells (1 K + 8 normal cell transistors) and one reference cell transistor, and is shared by four 128-bit (256-transistor) memory words. Every four bit lines at the same position of each memory word are laid out side-by-side and connected to one output node of the shift register through a bit line driver. The bit line drivers work as 4-to-1 selectors as well as level shifters. In search operations, the bit lines at the selected column and array address are set at 0 V or 5 V depending on the data stored in the shift register, and the others are set at 0 V, which means search data "masked." Thus, the search sense amplifiers detect whether the selected memory words are "match" or "nonmatch."

In the flash CAM LSI, 256 + 2 (redundancy) search sense amplifiers are located between two cell arrays. They occupy 0.7% of the die area, and each of them is laid out in a 10.55 μm (four-word-line space) $\times$ 110 μm area. Each search Y selector selects one word line out of four according to row address. This means that the flash CAM performs a search operation on 1/32 of its memory words.

The 256 + 2 (redundancy) search management circuits and a priority encoder are laid out next to the search sense amplifiers. Each plane is divided into 256 bit line units, each of which consists of four bit lines sharing a bit line driver, and is provided with two redundancy bit line units. By means of the bit line redundancy circuit, any combination of two defective bit lines in a plane can be repaired.

In the flash CAM, 18 sense amplifiers and 18 write circuits for read/write operations are provided in the left and right extremities of the chip. Since the cell transistors for a word are arranged in a drain line (word line), read/write access for a word is processed in bit serial. However, in chip programming and verifying preceding erase pulses, erase verifying, and wafer testing, the 18 read/write circuits work in parallel for fast operations.

Fifty-thousand peripheral transistors and 2 million floating gate transistors have been integrated onto a 7.14 mm $\times$ 6.01 mm die area. Memory cell size is 2.35 μm (bit line pitch) $\times$ 2.2 μm (gate line pitch) $\times$ 2, and gate width and gate length in the memory cell transistor are 1.0 μm and 0.75 μm, respectively. The minimum gate lengths of the peripheral transistors are $L_n = 1.0$ μm and $L_p = 1.2$ μm. The flash CAM operates with two supply voltages, $V_{\rm cc}$ (5 V) and $V_{\rm pp}$ (12 V) $V_{\rm pp}$ is used in erase and write operations.

Fig. 16 shows measured waveforms of a search operation, and Figs. 17 and 18 show, respectively, Shmoo plots of read access time and of search access time versus power supply voltage ($V_{\rm cc}$). Read access time is 115 ns, and search access time is 145 ns. Search access time includes the operation times of the search management circuits and the priority encoder. Output signal EXIST at a high level signifies that there is at least one "match" search management circuit. If EXIST is at high level, the "matched" address which has the highest priority can be read out in the subsequent sequence. As can be seen in Figs. 17 and 18, the minimum supply voltage ($V_{\rm cc\,min}$) in search operations is 0.6 V higher than that in read operations. The reason for this difference is that $V_{\rm cc\,min}$ in read operations depends on the V_t distribution of the normal memory cell transistors, while $V_{\rm cc\,min}$ in search operations depends on the V_t of the reference cell transistors.

Read power dissipation is 50 mW + 160 mW (I/O buffers) for 300 ns cycle operations at a 5 V supply voltage, and search

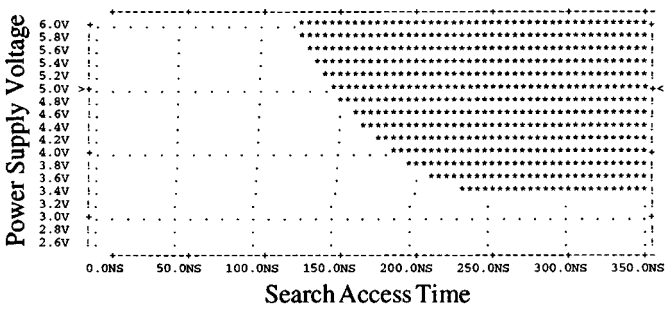

Fig. 18. Search access time versus power supply voltage.

TABLE III
FLASH CAM CHARACTERISTICS

Organization	1 Mbit (128 bit × 8 Kword)
Supply Voltages	Vcc (5V), Vpp (12V)
Technology	0.8 μm CMOS flash memory with double poly and double metal
Die Size	7.14 mm × 6.01 mm
Cell Size	4.7 μm(2 bit line pitches) × 2.2 μm(1 word line pitch), W/L = 1.0 μm/0.75 μm
Read Access Time	115 ns (Vcc = 5.0V)
Read Active Power	50 mW + 160 mW(I/O) (300 ns cycle)
Search Access Time	145 ns (Vcc = 5.0V)
Search Active Power	140 mW (300 ns cycle)

power dissipation is 140 mW under the same conditions. Chip characteristics are summarized in Table III.

V. SUMMARY

A new flash CAM (content addressable memory based on flash memory technologies) has been developed. High array density is achieved by using two-floating-gate-transistor CAM cells. The flash CAM cell array has the same basic layout as a conventional NOR-type flash memory, which means we can easily fabricate one of mega-bit-class.

We have developed four new circuit designs for the flash CAM. A new small-area, low-power search sense amplifier achieves highly parallel search operations, and a new search management circuit performs the on-chip parallel operations on search results. A new priority encoder provided with inhibit signal bypasses speeds search access time in the flash CAM, and new word line/bit line redundancy circuits significantly improve production yields. Any multiple fail word lines or multiple fail bit lines can be repaired by the redundancy circuits.

To test the ability of the flash CAM, we fabricated a 1-Mb flash CAM LSI. A cell size of 10.34 μm^2 and a die size of 42.9 mm^2 have been achieved with 0.8 μm design rules. Read access time and search access time are 115 ns and 145 ns, respectively, with a 5 V supply voltage. Power dissipation in 3.3 MHz operations is 210 mW in read and 140 mW in search access.

Our 1 Mb flash CAM achieves 20 times greater capacity than previously reported SRAM-based CAM's. We expect future progress in flash memory technology to improve its potential even further.

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Tohru Miwa was born in Tokyo, Japan, on October 26, 1967. He received the B.S. and M.S. degrees in information science from Kyoto University, Kyoto, Japan, in 1990 and 1992, respectively.

In 1992, he joined the System ULSI Research Laboratory, Microelectronics Research Laboratories, NEC Corporation, Kanagawa, Japan, where he has been engaged in the research and development of flash memory LSI's. His current research interests include flash memory circuit techniques and content addressable memory architecture.

Mr. Miwa is a member of the Information Processing Society of Japan.

Hachiro Yamada was born in Shizuoka, Japan, on June 6, 1949. He graduated from Shizuoka Technical High School in 1968 and the Nippon Electric Institute of Technology in 1973.

In 1968 he joined NEC Corporation, Kawasaki, Japan, where he was engaged in the research and development of memory hierarchy systems and magnetic bubble memory systems. Since 1985 he has been engaged in the development of content addressable memories, DSP's, vector processor LSI's, high-speed circuit technologies, and VLSI architecture. He is presently a research manager at Microelectronics Research Laboratories, NEC Corporation.

Mr. Yamada received the 1992 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award from IEEE (with M. Motomura and T. Enomoto) and the 1995 Achievement Award from the Institute of Electronics, Information and Communication Engineers of Japan (with T. Enomoto). Mr. Yamada is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

Yoshinori Hirota was born in Hokkaido, Japan, in 1957.

In 1980 he joined NEC Corporation, Kanagawa, Japan, where he has been engaged in the research and development of LSI's. He belongs to the Microelectronics Research Laboratories.

Toshiya Satoh was born in Ibaragi, Japan, in 1964. He received his B.S. degree in technology from Ibaragi University in 1988.

In 1988 he joined NEC Corporation, Kanagawa, Japan, where he has been engaged in the circuit development of PROM's and flash memories. He belongs to the LSI Memory Division.

Hideki Hara was born in Gifu, Japan, in 1967. He received his B.S. degree in electrical engineering from Hosei University in 1989.

In 1989 he joined NEC Corporation, Kanagawa, Japan, where he has been engaged in the process development of flash memory LSI's. He belongs to the LSI Memory Division.