Model 4954-401,-404 GateFlow IP Cores

GateFlow 1k and 4k Quad FFT Library IP Cores

For more information and free IP core evaluation go to:
pentek.com/fpga

Features

- Ultra-high-speed, high-performance 1024- and 4096-point complex FFTs
- Supports Virtex-II™ and Virtex-II Pro™ FPGAs
- Four input and output points per clock cycle performance
- Flexible input stage accepts one, two or four input streams
- Four 4k-point FFT calculations in 4096 clock periods
- Four 1k-point FFT calculations in 256 clock periods
- Highly distributed arithmetic
- 16-bit complex or real input data
- Selectable 16-bit complex or unsigned power output data
- Supports continuous input and output data
- Selectable Hanning window function
- Naturally ordered input and output data
- Operates in continuous output or triggered "one-shot" mode
- Test bench included
- Downloadable simulation models available
- Compatible with Xilinx Foundation ISE Tools

Ordering Information

Model	Description
4954-401	1k-point Quad FFT Library IP Core
4954-404	4k-point Quad FFT Library IP Core

Licensing of these cores follows the Xilinx SignOnce Project License. Simulation models can be downloaded for evaluation.

General Information

The Pentek Model 4954 GateFlow Library IP Cores 401 and 404 are ultra-high-speed, pipelined 1024- and 4096-point complex FFT engines designed specifically for Xilinx Virtex-II and Virtex-II Pro FPGAs.

Both cores are optimized for demanding applications that require real-time, sustained FFT calculations for one, two or four input channels at aggregate input data sample rates up to 560 MHz.

The quad architecture supports four parallel processing streams so that four input and output sample streams are accepted and delivered per clock cycle.

Input Data

Continuous input and output data streams are supported with zero data loss. Input data can be either 16-bit real or 16-bit I & Q complex values. Input overlap processing is available for fewer than four streams according the following schemes:

- One input data stream producing four FFT outputs computed from input blocks consisting of 25% new data and 75% previous data (75% input overlap)
- Two simultaneous input data streams producing two FFT outputs with 50% input overlap
- Four simultaneous input data streams and four FFT output streams with no overlap

Additionally, the input data streams may be optionally windowed with a built-in Hanning window function. Alternate custom window functions are supported for special applications.

FFT Engine

This implementation of the 1024-point (Core 401) and 4096-point (Core 404) complex FFTs both employ a highly distributed Cooley-Tukey radix-4 decimation-in-frequency (DIF) algorithm.

The basic FFT building blocks are multiple stages that each compute 1024 radix-4 butterfly operations. The 4096-point FFT requires six stages and the 1024-point FFT requires five stages.

This architecture takes advantage of the wealth of block RAM in the Virtex™ II devices to form the delay lines. Dedicated hardware multipliers allow all butterfly calculations to occur in parallel for continuous input and output flow. Each stage operates simultaneously to minimize the time for the overall calculation. The dynamic range is 90 dB for complex inputs and 84 dB for real inputs. The Hanning window reduces dynamic range by 6 dB.

Output Data

At the output of the FFT, a digit-reversal reordering presents the output points in natural frequency order. The output of the FFT may be presented either in complex form with 16-bit I and Q components, or in power ($I^2 + Q^2$) as a 32-bit unsigned integer.

Speed Performance

Four 1024-point FFTs (Core 401) and four 4096-point FFTs (Core 404) are computed in 1024 clocks and 4096 clocks, respectively. FFT calculation time is inversely proportional to the clock frequency, whose maximum value depends on the FPGA speed grade.

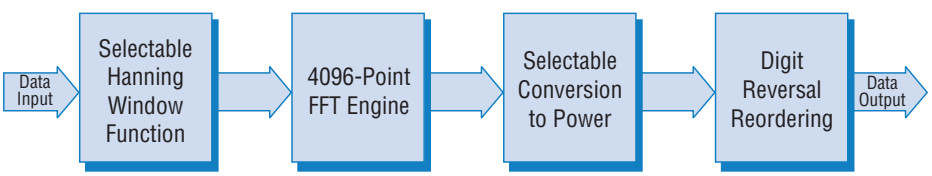
The chart below shows the aggregate input rate for four parallel channels and the effective time for each of the four FFTs.

Xilinx Speed Grade	Max Clock Rate	Max Input Rate	401 1k FFT Time	404 4k FFT Time
-6	140 MHz	560 MHz	1.83 µs	7.31 µs
-5	126 MHz	504 MHz	2.03 µs	8.10 µs
-4	110 MHz	440 MHz	2.33 µs	9.31 µs

FPGA Resource Utilization

Cores 401 and 404 will fit into the Xilinx Virtex-II XC2V3000 or larger devices. The chart below shows the utilization of FPGA resources:

Resources	Core 401	Core 404
Slice LUTs	12,702	13,184
Slice Flip-Flops	11,410	14,590
Block RAM	40	90
Block Multipliers	64	76
Global Clocks	1	1



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