

Design of High-Speed Digital Filters Suitable for Multi-DSP Implementation

KATSUHIKO HAYASHI, KAUSHAL K. DHAR, KAZUNORI SUGAHARA, MEMBER, IEEE, AND
KOTARO HIRANO, SENIOR MEMBER, IEEE

Abstract—A multipath signal processing scheme is proposed to overcome the limitation on the throughput rate of present day available LSI devices which is specifically suitable for implementation using a number of Digital Signal Processors (DSP). Two methods are proposed to realize a given transfer function $H(z)$ of digital filter, with a throughput rate speed up factor of N , over the conventional methods.

The first method, called Delayed Multipath Approach here, uses an N -path structure as a building element. These N elements are connected successively with increasing delay units to realize a given transfer function. The second method preprocesses the input signal sequence by an FFT processor and follows it up by N of constituent transfer functions derived from $H(z)$ having real coefficients. The output of these N constituent transfer functions are finally postprocessed by inverse FFT processor to obtain the desired output signal. The number of the constituent transfer functions are double for a special case when the transfer function to be implemented has complex valued coefficients. These two methods serve as complementary approaches, because the first method is better suited for small values of the speed-up factor N and the second one has distinct advantage for larger values of N .

The discussion of the first design method is organized in two parts: FIR filter design and IIR filter design, for each of which 2-path and N -path structures are separately explained. The second design method is discussed under the headings of real transfer function and complex transfer function. Design examples are also given to illustrate both of these two methods. Finally, a multi-DSP hardware system is outlined which is specifically designed for implementing the multipath structures discussed here.

I. INTRODUCTION

IN RECENT YEARS Digital Signal Processor (DSP) chips [1]–[3] are getting to be used more and more to realize the digital signal processing system replacing the more conventional hardware elements like discrete digital components or a general purpose microprocessor based systems. The DSP chip, apart from having many similarities to a microprocessor, also has on chip hardwired multiplier as well as instruction and data memories. Due to the on chip pipelined architecture and a wide data bus width, typically 16 bits, these chips can implement the signal processing algorithms with high speed and precision, without having to use an arithmetic coprocessor which is essential for a microprocessor based system used for the purpose of digital signal processing.

The different DSP chips have own assembly languages

associated to them and so the signal processing algorithms can be implemented by their software programs. The execution times of single instruction for different chips vary between 150–200 ns and tend to be limited by the device technology used to fabricate the chip. For a given processor, the signal throughput rate achieved, is governed by the number of the instruction steps in a given signal processing program and thus is directly related to the complexity of the algorithm. Hence a signal processing structure which suggests improving the throughput rate considerably beyond the limits imposed by the device technology, employed to fabricate the DSP chip, is quite useful.

The digital filter systems containing N -path digital element are proposed in this paper, to process the signals containing frequency components higher than the maximum frequency which can be processed to a reasonable degree of complexity by a single DSP chip. Section II discusses some of the general aspects of an N -path digital element [4], which is used to develop two design methods in the following sections. Section III proposes the first of the structures of multipath system suitable for low values of N , and outlines the procedure to design FIR and IIR digital filters from a given specifications. Section IV discusses the second of the multipath scheme suitable for larger values of N . At the end of Sections III and IV, the proposed approach is illustrated using several examples. The hardware implementation of the proposed structure by a multi-DSP architecture is discussed in Section V.

II. DIGITAL N -PATH ELEMENT

This section discusses the properties of an N -path digital element and its limitations when it is applied to implement a high speed digital filter. Fig. 1 shows an N -path digital element which has two N position switches, S_i and S_o , one each at the input and the output, respectively. The successive samples of the input signal arrive every T seconds. These samples are sequentially fed to each of the N identical filter blocks, all having a transfer function $H(z)$. The outputs of the component filter blocks are combined by the N position switch at the output which retains the same sequential switching order of that of the input switch.

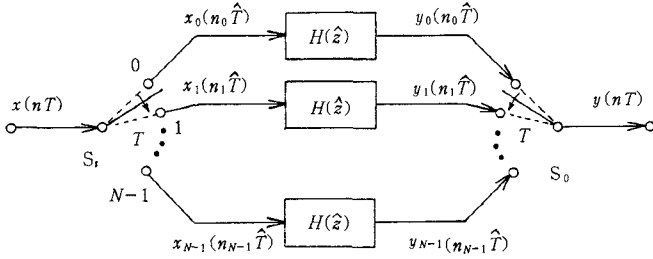
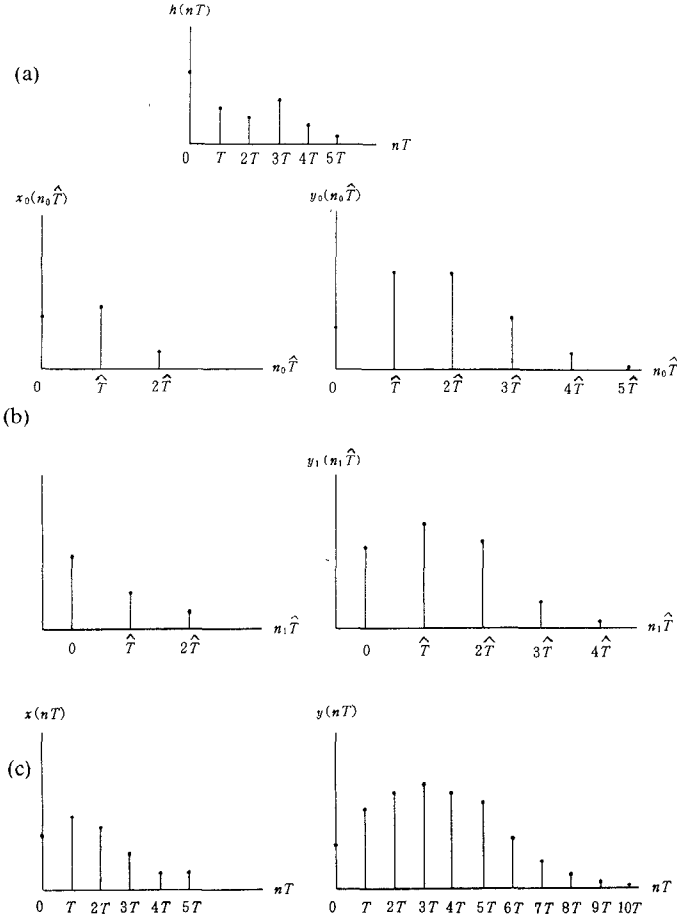
For an example the impulse response of the component filter is shown in Fig. 2(a). Using this component filter in a 2-path system, the outputs are $y_0(n_0\hat{T})$ and $y_1(n_1\hat{T})$, as shown in Fig. 2(b), corresponding to inputs $x_0(n_0\hat{T})$ and

Manuscript received May 20, 1985; revised September 30, 1985.

K. Hayashi, K. K. Dhar, and K. Hirano are with the Department of Electronic Engineering, The Faculty of Engineering, Kobe University, Kobe 657, Japan.

K. Sugahara is with the Department of Electrical Engineering, Kobe Technical College, Kobe, Japan.

IEEE Log Number 8406490.

Fig. 1. N -path digital element.Fig. 2. (a) Impulse response of component filter. (b) Responses of the component filter to the input signal samples $x_0(n_0\hat{T})$ and $x_1(n_1\hat{T})$, respectively. (c) Response of a 2-path composite digital element to input signal $x(nT)$.

$x_1(n_1\hat{T})$, respectively, where $\hat{T} = 2T$. Finally, the composite response of the 2-path system as a whole is shown in Fig. 2(c). Each component filter is allowed to process the signal, available to it as an input, at a sampling interval of \hat{T} . However, the input signal samples are given to the overall system at a sampling interval of T which implies that composite filter signal throughput rate is two times that of the component filter.

Extending this idea, an N -path element can process input signals at a rate which is N times faster. The z -transform

$$X(z) = \sum_{n=0}^{\infty} x(nT)z^{-n}. \quad (1)$$

can be organized as

$$X(z) = \sum_{i=0}^{N-1} X_i(z^N)z^{-i} \quad (2)$$

where

$$X_i(z^N) = \sum_{n=0}^{\infty} x(nNT + iT)z^{-nN}. \quad (3)$$

The N position switch S_i on the input side sequentially routes the input signal samples to each of the N parallel paths. The signal samples which are selected to be given to the i th path are $x(iT), x(NT + iT), \dots, x(nNT + iT), \dots$. The z -transform of the signal which is given to the i -th path is $X_i(z^N)$. The successive samples along any path arrive at the intervals NT apart.

Since the transform variable z corresponds to the sample time interval T , the transfer function of each path is represented by $H(z^N)$ to conform to the same variable z even though the signal sample arrival rate has slowed down by a factor N . Hence the equation

$$Y_i(z^N) = H(z^N)X_i(z^N) \quad (4)$$

represents, in z -domain, relation between the input/output signal samples corresponding to i th path. The output switch S_o determines the z -transform $Y(z)$ of the output signal from the component transform $Y_i(z^N)$ by the relation

$$Y(z) = \sum_{i=0}^{N-1} Y_i(z^N)z^{-i} \quad (5)$$

which implies

$$Y(z) = \sum_{i=0}^{N-1} H(z^N)X_i(z^N)z^{-i} = H(z^N)X(z). \quad (6)$$

Equation (6) represents that the composite transfer function of an N -path digital element constructed from N identical filters is $H(z^N)$, where $H(z)$ is the transfer function of the component filter. Generally speaking, the frequency response of an N -path filter is an N -times scaled version, along the frequency axis, of the concerned component filter.

The process of frequency scaling creates unwanted passbands in the realized filter, transferred from the frequency region greater than $1/2T$ in the component filter, to the frequency range of less than $1/2T$. The upper part of Fig. 3 is the typical example of magnitude response of the individual filter component $H(z)$. Obviously it is a low-pass filter with cutoff angular frequency ω_c . This component when used in a 2-path structure gives the composite transfer function $H(z^2)$ whose magnitude response is shown in the bottom part of Fig. 3. As indicated by the dotted lines, connecting the two figures, the passband of the individual component filter, beyond $\omega T = \pi$, lying in the region $(2\pi - \omega_c, 2\pi)$ is transferred to the region $(\pi - \omega_c/2, \pi)$ in the composite response. This transfer of the passband from one region to another is an unwanted feature. This can be attributed to nonrealizability of the terms of the type

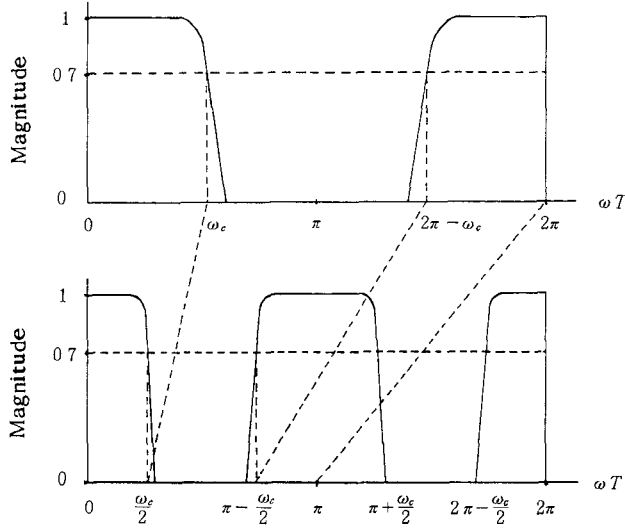


Fig. 3. Component and composite magnitude responses of 2-path element.

z^{-nN+i} for an integer value of n and $i=1,2,\dots,N-1$ in the N -path filter structure.

If the transfer function of the component filter block of the system is given in polynomials of z^{-1} , that of the 2-path system will be given by polynomials of z^{-2} . This implies that odd power terms of z^{-1} will vanish out in the transfer function of the composite 2-path structure. If the desired filter to be implemented has odd degree terms, the 2-path structure by itself can not realize that.

One way to eliminate these unwanted passbands is by cascading several N -path filters [5]. However, the specifications possible to be achieved are highly limited. The following section will propose a structure which realizes the given transfer function $H(z)$, derived from arbitrary specification, by using several N -path elements in a modified sort of parallel configuration.

III. DIGITAL DELAYED MULTIPATH STRUCTURES

A. FIR Digital Filter

(i) 2-Path Structure:

In order to overcome the disadvantage discussed above, first introduce the FIR filter structure containing two 2-path elements. A dual 2-path filter structure is shown in Fig. 4 that can realize any given transfer function as well as retain the advantage of doubled throughput rate of 2-path digital element. The transfer function of an FIR filter is derived to be generally in the form

$$H(z) = \sum_{k=0}^M \alpha_k z^{-k} \quad (7)$$

by using the methods available elsewhere. Equation (7) can be split into two parts: the terms consisting of odd powers of z^{-1} and those consisting of the even powers of z^{-1} as

$$H(z) = H_0(z^2) + z^{-1}H_1(z^2). \quad (8)$$

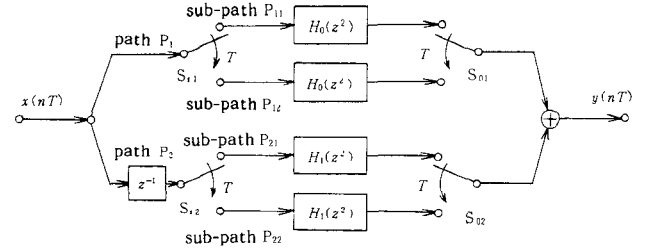


Fig. 4. Dual 2-path filter configuration.

The transfer function $H_0(z^2)$ and $H_1(z^2)$ are determined by the expressions

$$H_0(z) = \sum_{k=0}^{M/2} \alpha_{2k} z^{-k} \quad (9)$$

$$H_1(z) = \sum_{k=0}^{(M/2)-1} \alpha_{2k+1} z^{-k}$$

for even value of M , and

$$H_0(z) = \sum_{k=0}^{(M-1)/2} \alpha_{2k} z^{-k} \quad (10)$$

$$H_1(z) = \sum_{k=0}^{(M-1)/2} \alpha_{2k+1} z^{-k}$$

for odd value of M .

since $H_0(z^2)$ and $H_1(z^2)$ of (8) are polynomials in z^{-2} , each of these can be realized by using 2-path digital elements. The whole desired transfer function $H(z)$, in turn, can be realized by the structure shown in Fig. 4.

(ii) N -Path Structure:

Along the lines similar of the logic developed above, a transfer function $H(z)$ of FIR filter given by (7) can also be expressed in general as

$$H(z) = \sum_{i=0}^{N-1} H_i(z^N) z^{-i}. \quad (11)$$

The expressions for $H_i(z)$ for $i=0,1,\dots,N-1$ are governed by

$$H_i(z) = \begin{cases} \sum_{k=0}^{I+1} \alpha_{Nk+i} z^{-k}, & i=0,1,\dots,J-1 \\ \sum_{k=0}^I \alpha_{Nk+i} z^{-k}, & i=J,J+1,\dots,N-1 \end{cases} \quad (12)$$

where $I = \{(M+1)\text{div}N\} - 1$ and $J = (M+1)\text{mod}N$. Since $(M+1)$ terms of the given transfer function $H(z)$, in (7), have to be divided into N blocks, each of $H_i(z)$ $i=0,1,\dots,N-1$, has at least $(M+1)\text{div}N$ terms. This implies that the minimum order of $H_i(z)$ is I . The remaining J terms are assigned one each to those $H_i(z)$, for which $i=0,1,\dots,J-1$, which results in the corresponding filter blocks having the order of $I+1$. Obviously the remaining $H_i(z)$ for $i=J,J+1,\dots,N-1$ have an order I each.

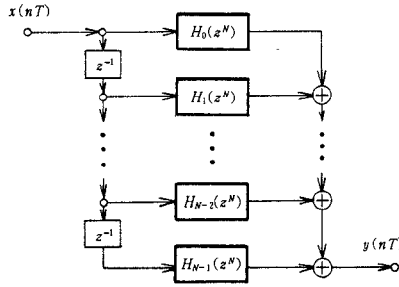


Fig. 5. Delayed multipath digital filter structure.

The filter structure to implement desired $H(z)$, using an N -path element, is shown in Fig. 5. Here filter block of each path is a pure N -path digital element. Each of the $H_i(z)$ in Fig. 5 is obtained by using (12).

B. IIR Digital Filter

(i) 2-Path Structure:

First, the design approach to realize a given $H(z)$ is outlined by using a 2-path structure. The transfer function derived by using available method is mathematically manipulated, so that the denominator is the function of z^{-2} only. Subsequently, the numerator is split into two separate parts of even and odd powers of z^{-1} as in (8). Hence we manage to get an equation of the type (8) in which $H_0(z^2)$ and $H_1(z^2)$ are both functions of z^{-2} only and both parts can be implemented by 2-path digital elements. In general the transfer function of an IIR filter can be expressed as

$$H(z) = \prod_{m=1}^L \frac{a_{0m} + a_{1m}z^{-1} + a_{2m}z^{-2}}{1 - b_{1m}z^{-1} + b_{2m}z^{-2}}. \quad (13)$$

One of the factors in (13) can be selected to be

$$H_m(z) = \frac{a_0 + a_1z^{-1} + a_2z^{-2}}{(1 - bz^{-1})(1 - b^*z^{-1})} \quad (14)$$

where b and b^* are mutually complex-conjugate numbers represented as $b = re^{j\theta}$ and $b^* = re^{-j\theta}$.

The denominator of (14) can be converted into a function of z^{-2} only by the arithmetic manipulation

$$\begin{aligned} H_m(z) &= \frac{(a_0 + a_1z^{-1} + a_2z^{-2})(1 + bz^{-1})(1 + b^*z^{-1})}{(1 - b^2z^{-2})(1 - b^{*2}z^{-2})} \\ &= \frac{A(z)}{B(z^2)} \end{aligned} \quad (15)$$

where

$$\begin{aligned} A(z) &= a_0 + (a_1 + a_0b_1)z^{-1} + (a_2 + a_1b_1 + a_0b_2)z^{-2} \\ &\quad + (a_2b_1 + a_1b_2)z^{-3} + a_2b_2z^{-4} \\ &= \sum_{k=0}^4 \alpha_k z^{-k} \end{aligned} \quad (16)$$

with $b_1 = 2r \cos \theta$ and $b_2 = r^2$. The expression for the modified denominator is given by

$$B(z) = 1 - 2r^2 \cos 2\theta z^{-1} + r^4 z^{-2}. \quad (17)$$

The two component transfer functions $H_{m0}(z)$ and $H_{m1}(z)$ such that

$$H_m(z) = H_{m0}(z^2) + z^{-1}H_{m1}(z^2) \quad (18)$$

are given as

$$H_{m0}(z) = \frac{\alpha_0 + \alpha_2 z^{-1} + \alpha_4 z^{-2}}{B(z)} \quad H_{m1}(z) = \frac{\alpha_1 + \alpha_3 z^{-1}}{B(z)} \quad (19)$$

respectively. Each of two transfer functions $H_{m0}(z^2)$ and $H_{m1}(z^2)$ can be implemented by 2-path digital elements.

Arguing along the same lines, each factor of (13) with the similar type of expressions (14) can thus be realized by a suitable pair of 2-path elements $H_{m0}(z^2)$ and $H_{m1}(z^2)$. The complete system can be realized by the structure of Fig. 6.

(ii) N -Path Structure:

The logic used above will be extended to the case where an N -path IIR filter structure is to be used as a building element to realize a given transfer function $H(z)$. The given transfer function is mathematically manipulated such that denominator of each term of the form (14) of the IIR filter transfer function (13) is converted to a factor $(1 - b^N z^{-N})(1 - b^{*N} z^{-N})$, a function of z^{-N} only. The necessary mathematical transformation is such that

$$\frac{1}{(1 - bz^{-1})(1 - b^*z^{-1})} = \frac{C(z)}{(1 - b^N z^{-N})(1 - b^{*N} z^{-N})} \quad (20)$$

where

$$C(z) = \prod_{l=1}^{N-1} \{1 - 2r \cos(2\pi l/N + \theta) z^{-1} + r^2 z^{-2}\}. \quad (21)$$

The terms r , θ , and l are defined by the roots of equations

$$1 - b^N z^{-N} = 0 \quad 1 - b^{*N} z^{-N} = 0 \quad (22)$$

and are governed by

$$z = z_l = re^{\pm j(\theta + 2\pi l/N)}, \quad l = 0, 1, 2, \dots, N-1. \quad (23)$$

These mathematical manipulations convert the $H_m(z)$ of (14) to

$$H_m(z) = \frac{A(z)}{B(z^N)} \quad (24)$$

where

$$\begin{aligned} A(z) &= (a_0 + a_1 z^{-1} + a_2 z^{-2})C(z) = \sum_{k=0}^{2N} \alpha_k z^{-k} \\ B(z) &= 1 - 2r^N \cos N\theta z^{-1} + r^{2N} z^{-2}. \end{aligned} \quad (25)$$

Each factor $H_m(z)$ of (13) is similarly manipulated. The complete system is implemented by cascading of individual structures obtained after such manipulations. The resulting numerator can be treated as an FIR filter equation and can be conveniently split into several parts along the lines of (12) to give the filter structure of the Fig. 5.

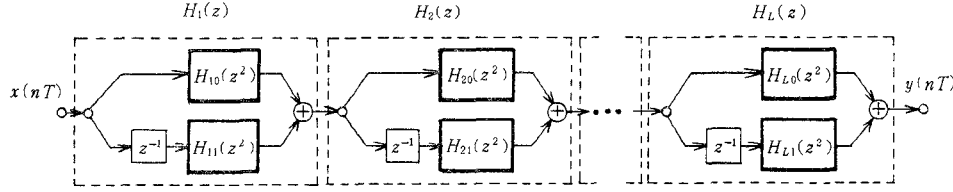


Fig. 6. A general realization of IIR filter using 2-path filter elements in tandem.

TABLE I
VALUES OF α_i AND β_{ij} OF IIR LOW-PASS FILTER IN EXAMPLE 1 OF
SECTION III

coefficients	values	coefficients	values
α_0	0.00483378	α_1	0.0307845
α_2	0.0859787	α_3	0.137839
α_4	0.138983	α_5	0.0903461
α_6	0.0369833	α_7	0.00871341
α_8	0.00090488	—	—
β_{11}	-0.478425	β_{12}	0.400176
β_{21}	-0.506797	β_{22}	0.0875692

C. Illustrative Examples

Two simple examples are presented here which illustrate the procedure of designing delayed multipath structure clearly. The general approach followed here consists of first obtaining the transfer function of an FIR or IIR filter satisfying the given specifications by any of the conventional methods available in the literature. Subsequently, the $H(z)$ obtained by such method is used to derive transfer functions of the constituent filter blocks of delayed N -path structure, for a suitable N , by the mathematical manipulations outlined in Sections III-A and B. The value of N is decided from the considerations of the largest frequency component in the input signal.

(i) Example 1: Low-Pass Filter

First, consider the realization of a delayed 2-path IIR lowpass filter satisfying the following set of specifications:

$$\begin{aligned} \omega_c T &= 0.2\pi & \alpha_{\max} &= 3 \text{ dB} \\ \omega_{\min} T &= 0.35\pi & \alpha_{\min} &= 20 \text{ dB} \end{aligned}$$

where α_{\max} is the maximum attenuation at the 3-dB cutoff angular frequency, ω_c and α_{\min} is the minimum attenuation in the stopband beyond the angular frequency ω_{\min} . Using the design method outlined in [6], the Butterworth transfer function $H(z)$ satisfying the specifications is obtained to be

$$H(z) = \frac{c(1+z^{-1})^2}{1-a_{21}z^{-1}+a_{31}z^{-2}} \cdot \frac{(1+z^{-1})^2}{1-a_{22}z^{-1}+a_{32}z^{-2}} \quad (26)$$

where $c = 0.00483378$, $a_{21} = 1.32046$, $a_{22} = 1.04816$, $a_{31} = 0.632596$, and $a_{32} = 0.295921$. Using the arithmetic manipulations of (15), the expression

$$H(z) = \frac{\sum_{k=0}^8 \alpha_k z^{-k}}{B(z^2)} \quad (27)$$

where

$$B(z) = (1 + \beta_{11}z^{-1} + \beta_{12}z^{-2})(1 + \beta_{21}z^{-1} + \beta_{22}z^{-2}) \quad (28)$$

is obtained, corresponding to which the values of α_k for $i = 0, 1, 2, \dots, 8$ and β_{ij} , for $i, j = 1, 2$ are given in Table I. The two component transfer functions such that numerator is expressed along the same lines as (8), are given by

$$\begin{aligned} H_0(z) &= \frac{\alpha_0 + \alpha_2 z^{-1} + \alpha_4 z^{-2} + \alpha_6 z^{-3} + \alpha_8 z^{-4}}{B(z)} \\ H_1(z) &= \frac{\alpha_1 + \alpha_3 z^{-1} + \alpha_5 z^{-2} + \alpha_7 z^{-3}}{B(z)}. \end{aligned} \quad (29)$$

Fig. 7 shows the plot of the magnitude response of the filter so designed where the points marked with cross indicate the actual values obtained by implementing the example on the hardware system of Section V.

(ii) Example 2: Bandpass Filter

A bandpass filter is designed here in a delayed 2-path IIR structural form with the specification

$$\begin{aligned} \omega_1 T &= 0.4\pi & \omega_2 T &= 0.5\pi & \alpha_{\max} &= 3 \text{ dB} \\ \omega_{\min 1} T &= 0.25\pi & \omega_{\min 2} T &= 0.65\pi & \alpha_{\min} &= 20 \text{ dB} \end{aligned}$$

where ω_1 and ω_2 are two cutoff angular frequencies of the passband with α_{\max} as the maximum attenuation in it. The angular frequency ranges $\omega < \omega_{\min 1}$ and $\omega > \omega_{\min 2}$ form the stopband with a minimum attenuation α_{\min} . A transfer function $H(z)$, satisfying the given specifications, is obtained by [6] to be

$$H(z) = c \cdot \frac{(1-z^{-2})}{1-a_{21}z^{-1}+a_{31}z^{-2}} \cdot \frac{(1-z^{-2})}{1-a_{22}z^{-1}+a_{32}z^{-2}} \quad (30)$$

where $c = 0.0201737$, $a_{21} = 0.0820591$, $a_{31} = 0.797415$, $a_{22} = 0.481871$, and $a_{32} = 0.803871$.

Using the mathematical manipulation as (15), $H(z)$ is broken into two component transfer functions $H_0(z)$ and

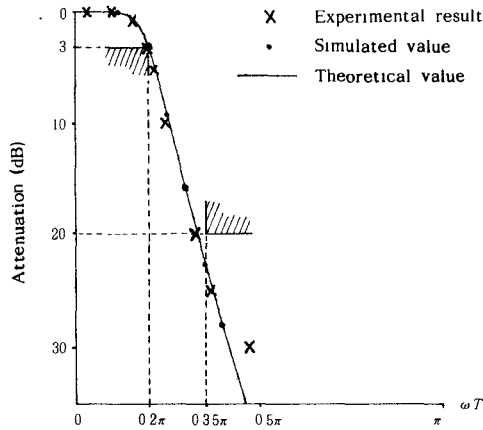


Fig. 7. Magnitude response of the low-pass filter in Example 1 of Section III.

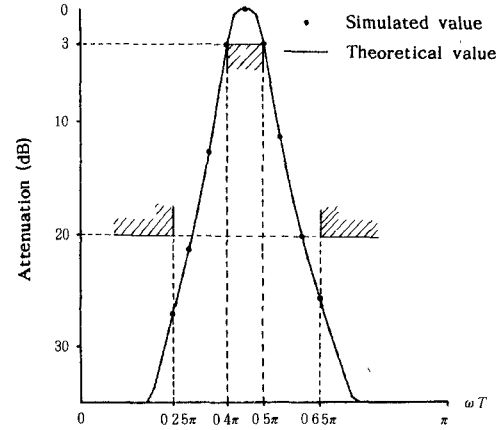


Fig. 8. Magnitude response of the bandpass filter in Example 2 of Section III.

TABLE II
VALUES OF α_i AND β_{ij} OF IIR BAND-PASS FILTER IN EXAMPLE 2 OF SECTION III

coefficients	values	coefficients	values
α_0	0.0201737	α_1	0.0113766
α_2	0.0331016	α_3	0.00908252
α_4	0.0129317	—	—
β_{11}	1.58810	β_{12}	0.635871
β_{21}	1.37554	β_{22}	0.646209

$H_1(z)$ similar to (18), as

$$\left. \begin{aligned} H_0(z) &= \frac{(\alpha_0 + \alpha_2 z^{-1} + \alpha_4 z^{-2})(1 - 2z^{-1} + z^{-2})}{B(z)} \\ H_1(z) &= \frac{(\alpha_1 + \alpha_3 z^{-1})(1 - 2z^{-1} + z^{-2})}{B(z)} \end{aligned} \right\} \quad (31)$$

and

$$B(z) = (1 + \beta_{11}z^{-1} + \beta_{12}z^{-2})(1 + \beta_{21}z^{-1} + \beta_{22}z^{-2})$$

where the values α_i for $i=0,1,2,3,4$ and that of β_{ij} for $i, j=1,2$ are given in the Table II. Fig. 8 shows the plot of the magnitude response of the designed filter.

IV. PRE- AND POST-PROCESSED MULTIPATH STRUCTURE

According to the delayed multipath filters discussed in Section III, the overall signal throughput rate can be made N times by using N -path structures. All of the paths consist of N transfer functions each, which causes a total of N^2 constituent transfer functions in the composite system. In case one DSP is assigned to implement one transfer function each, a total of N^2 DSP's are needed to realize such a system. Obviously, even for a modest value of N , a very complex hardware structure results which may offset the advantages of speed-up in the signal throughput rate. Moreover, for a large N the processing time of the adder units at the output may further limit the improvement in the throughput rate achieved and may be the reason for asymptotic levelling off of the throughput rate with the increase in the value of N . The discussed scheme may be tolerable for a low value of N being 2 or 3.

In this section, a scheme which needs only N constituent transfer functions, instead of N^2 is introduced. For a special case when some of the coefficients of the given transfer function $H(z)$, to be implemented, are complex valued, a total of $2N$ constituent transfer function blocks are needed.

A. Real Transfer Function

First, realization of a transfer function with real coefficients is discussed. Consider again a 2-path system of Fig. 4. The input sequence $x(nT)$ can be split to be composed of two sequences $x_0(n\hat{T})$ and $x_1(n\hat{T})$ defined as

$$x_0(n\hat{T}) = x(2nT) \quad \text{and} \quad x_1(n\hat{T}) = x(2nT + T) \quad (32)$$

using the equivalent sampling period $\hat{T} = 2T$. Fig. 9(a) and (b) show the two states of the system of Fig. 4, depending on the two different positions of two-way switches, respectively. The input/output equations governing the system during the two states are written as

$$\begin{aligned} Y_0(\hat{z}) &= H_0(\hat{z})X_0(\hat{z}) + \hat{z}^{-1}H_1(\hat{z})X_1(\hat{z}) \\ Y_1(\hat{z}) &= H_1(\hat{z})X_0(\hat{z}) + H_0(\hat{z})X_1(\hat{z}). \end{aligned} \quad (33)$$

where $\hat{z} = z^2$. Putting (33) in matrix yields $\mathbf{Y}(\hat{z}) = \mathbf{H}(\hat{z})\mathbf{X}(\hat{z})$, where

$$\begin{aligned} \mathbf{Y}(\hat{z}) &= \begin{bmatrix} Y_0(\hat{z}) \\ Y_1(\hat{z}) \end{bmatrix}, \quad \mathbf{X}(\hat{z}) = \begin{bmatrix} X_0(\hat{z}) \\ X_1(\hat{z}) \end{bmatrix} \\ \mathbf{H}_1 &= \begin{bmatrix} H_0(\hat{z}) & \hat{z}^{-1}H_1(\hat{z}) \\ H_1(\hat{z}) & H_0(\hat{z}) \end{bmatrix}. \end{aligned} \quad (34)$$

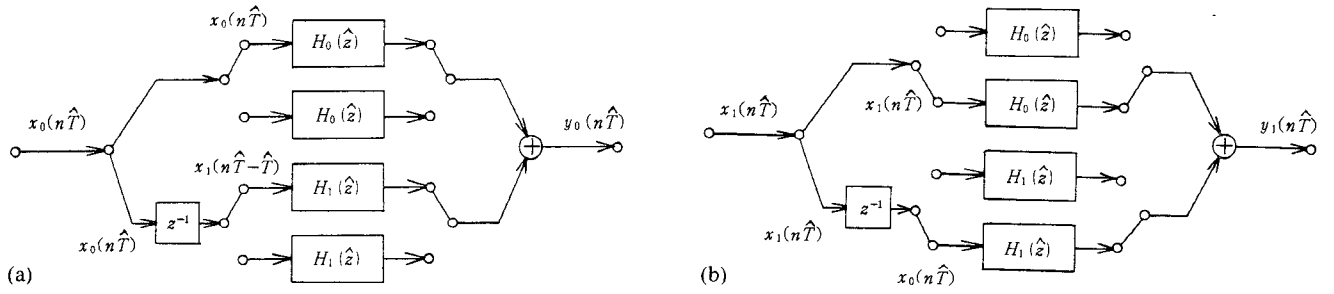


Fig. 9. (a) The output sequence $y_0(n\hat{T})$ corresponding to the input sequence $x_0(n\hat{T})$ for the first state of switches. (b) The output sequence $y_1(n\hat{T})$ corresponding to the input sequence $x_1(n\hat{T})$ for the second state of switches.

Extending the above argument for the delayed multipath digital filter structure of Fig. 5, the input and output signal sample sequence is broken down into N sequences whose z -transform is represented by $X_i(\hat{z})$ and $Y_i(\hat{z})$, and are given by (2) and (5), respectively, for $i = 0, 1, \dots, N-1$ and $\hat{z} = z^N$.

The concerned transfer function is given, in terms of its components as (11). The relation between the input and the output can be represented by a matrix equation $\mathbf{Y}(\hat{z}) = \mathbf{H}(\hat{z})\mathbf{X}(\hat{z})$, where

The equation

$$\mathbf{Y}(\hat{z}) = 1/2 [\mathbf{H}_Q(\hat{z}) + \mathbf{H}_R(\hat{z}) - \hat{z}^{-1} \{ \mathbf{H}_Q(\hat{z}) - \mathbf{H}_R(\hat{z}) \}] \mathbf{X}(\hat{z}) \\ = 1/2 [\mathbf{Y}_Q(\hat{z}) + \mathbf{Y}_R(\hat{z}) - \hat{z}^{-1} \{ \mathbf{Y}_Q(\hat{z}) - \mathbf{Y}_R(\hat{z}) \}] \quad (38)$$

represents another form of expression for $\mathbf{Y}(\hat{z})$ in terms of the partial matrices. Thus $\mathbf{Y}(\hat{z})$ can be obtained by calculating $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$ instead of direct calculation.

Let us define another vector $\bar{\mathbf{Y}}(\hat{z})$ associated to $\mathbf{Y}_Q(\hat{z})$

$$\mathbf{Y}(\hat{z}) = [Y_0(\hat{z}), Y_1(\hat{z}), \dots, Y_{N-1}(\hat{z})]^T \\ \mathbf{X}(\hat{z}) = [X_0(\hat{z}), X_1(\hat{z}), \dots, X_{N-1}(\hat{z})]^T \\ \mathbf{H}(\hat{z}) = \begin{bmatrix} H_0(\hat{z}) & \hat{z}^{-1}H_{N-1}(\hat{z}) & \hat{z}^{-1}H_{N-2}(\hat{z}) & \dots & \hat{z}^{-1}H_1(\hat{z}) \\ H_1(\hat{z}) & H_0(\hat{z}) & \hat{z}^{-1}H_{N-1}(\hat{z}) & \dots & \hat{z}^{-1}H_2(\hat{z}) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{N-1}(\hat{z}) & H_{N-2}(\hat{z}) & H_{N-3}(\hat{z}) & \dots & H_0(\hat{z}) \end{bmatrix} \quad (35)$$

Let us define component matrices $\mathbf{H}_Q(\hat{z})$ and $\mathbf{H}_R(\hat{z})$, which when appropriately used in mathematical manipulations produce $\mathbf{Y}(\hat{z})$, in terms of partial vectors $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$:

$$\mathbf{Y}_Q(\hat{z}) = \mathbf{H}_Q(\hat{z})\mathbf{X}(\hat{z}) \\ = [Y_{Q,0}(\hat{z}), Y_{Q,1}(\hat{z}), \dots, Y_{Q,N-1}(\hat{z})]^T \\ \mathbf{Y}_R(\hat{z}) = \mathbf{H}_R(\hat{z})\mathbf{X}(\hat{z}) \\ = [Y_{R,0}(\hat{z}), Y_{R,1}(\hat{z}), \dots, Y_{R,N-1}(\hat{z})]^T \quad (36)$$

where

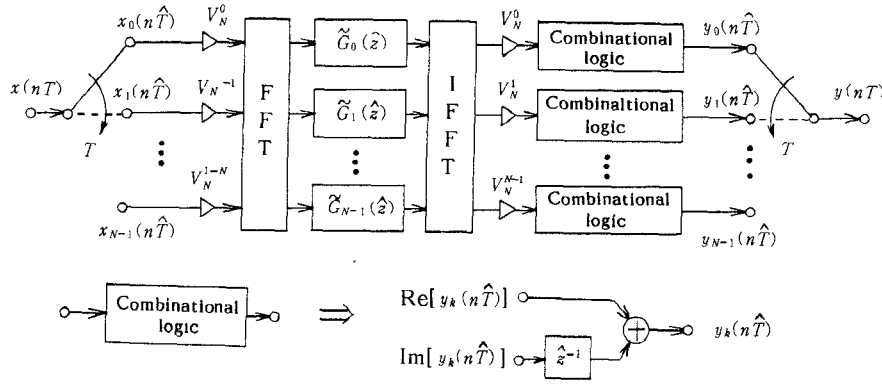
$$\mathbf{H}_Q(\hat{z}) = \begin{bmatrix} H_0(\hat{z}) & -H_{N-1}(\hat{z}) & -H_{N-2}(\hat{z}) & \dots & -H_1(\hat{z}) \\ H_1(\hat{z}) & H_0(\hat{z}) & -H_{N-1}(\hat{z}) & \dots & -H_2(\hat{z}) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{N-1}(\hat{z}) & H_{N-2}(\hat{z}) & H_{N-3}(\hat{z}) & \dots & H_0(\hat{z}) \end{bmatrix} \\ \mathbf{H}_R(\hat{z}) = \begin{bmatrix} H_0(\hat{z}) & H_{N-1}(\hat{z}) & H_{N-2}(\hat{z}) & \dots & H_1(\hat{z}) \\ H_1(\hat{z}) & H_0(\hat{z}) & H_{N-1}(\hat{z}) & \dots & H_2(\hat{z}) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{N-1}(\hat{z}) & H_{N-2}(\hat{z}) & H_{N-3}(\hat{z}) & \dots & H_0(\hat{z}) \end{bmatrix} \quad (37)$$

and $\mathbf{Y}_R(\hat{z})$ by the relation

$$\bar{\mathbf{Y}}(\hat{z}) = 1/2 [\mathbf{Y}_Q(\hat{z}) + \mathbf{Y}_R(\hat{z}) - j \{ \mathbf{Y}_Q(\hat{z}) - \mathbf{Y}_R(\hat{z}) \}] \\ = [\bar{Y}_0(\hat{z}), \bar{Y}_1(\hat{z}), \dots, \bar{Y}_{N-1}(\hat{z})]^T \quad (39)$$

Simplifying (39) and using the fact that $\mathbf{Y}(\hat{z})$ has only real valued elements, it becomes

$$2 \operatorname{Re} \{ \bar{Y}_k(\hat{z}) \} = Y_{Q,k}(\hat{z}) + Y_{R,k}(\hat{z}) \\ 2 \operatorname{Im} \{ \bar{Y}_k(\hat{z}) \} = Y_{R,k}(\hat{z}) - Y_{Q,k}(\hat{z}). \quad (40)$$

Fig. 10. High speed implementation of an $H(z)$ having all real coefficients.

Using (40), the k th element of $\mathbf{Y}(\hat{z})$ is found to be

$$Y_k(\hat{z}) = \text{Re}\{\bar{Y}_k(\hat{z})\} + \hat{z}^{-1} \text{Im}\{\bar{Y}_k(\hat{z})\}. \quad (41)$$

Equation (41) calculates the elements of desired output vector $\mathbf{Y}(\hat{z})$ in terms of those of $\bar{\mathbf{Y}}(\hat{z})$. From (36) it is obvious that vectors $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$ contain the vector $\mathbf{X}(\hat{z})$ as a common entity. By taking it out (39) is further simplified to be

$$\bar{\mathbf{Y}}(\hat{z}) = 1/2\{\mathbf{Y}_R(\hat{z}) - j\mathbf{Y}_Q(\hat{z})\}(1+j) = \mathbf{G}(\hat{z})\mathbf{X}(\hat{z}). \quad (42)$$

Here the newly defined transfer function matrix $\mathbf{G}(\hat{z})$, which when subjected to the input vector $\mathbf{X}(\hat{z})$, produces an output vector $\bar{\mathbf{Y}}(\hat{z})$ related to the desired output vector $\mathbf{Y}(\hat{z})$ through (41) is given by

$$\begin{aligned} \mathbf{G}(\hat{z}) &= 1/2\{\mathbf{H}_R(\hat{z}) - j\mathbf{H}_Q(\hat{z})\}(1+j) \\ &= \begin{bmatrix} H_0(\hat{z}) & jH_{N-1}(\hat{z}) & jH_{N-2}(\hat{z}) & \cdots & jH_1(\hat{z}) \\ H_1(\hat{z}) & H_0(\hat{z}) & jH_{N-1}(\hat{z}) & \cdots & jH_2(\hat{z}) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ H_{N-1}(\hat{z}) & H_{N-2}(\hat{z}) & H_{N-3}(\hat{z}) & \cdots & H_0(\hat{z}) \end{bmatrix}. \end{aligned} \quad (43)$$

It is proposed to convert the transfer function matrix $\mathbf{G}(\hat{z})$ into a diagonal matrix $\tilde{\mathbf{G}}(\hat{z})$ by similarity transformation as given by

$$\begin{aligned} \tilde{\mathbf{G}}(\hat{z}) &= \mathbf{T}_G^{-1}\mathbf{G}(\hat{z})\mathbf{T}_G \\ &= \text{diag}\{\tilde{G}_0(\hat{z}), \tilde{G}_1(\hat{z}), \dots, \tilde{G}_{N-1}(\hat{z})\} \end{aligned} \quad (44)$$

so that $\bar{\mathbf{Y}}(\hat{z}) = \mathbf{T}_G\tilde{\mathbf{G}}(\hat{z})\mathbf{T}_G^{-1}\mathbf{X}(\hat{z})$. The idea behind this transformation is that an element $Y_k(\hat{z})$ of the transformed output vector is dependent only on the corresponding element of the input vector $\mathbf{X}(\hat{z})$. Computationally, this process provides a more efficient way to obtain $\bar{\mathbf{Y}}(\hat{z})$ from $\mathbf{X}(\hat{z})$. However, because of involvement of the matrix \mathbf{T}_G and its inverse \mathbf{T}_G^{-1} , the input signal vector $\mathbf{X}(\hat{z})$ needs to be preprocessed by the transformation \mathbf{T}_G^{-1} followed by one diagonal transfer function $\tilde{\mathbf{G}}(\hat{z})$ and its outputs to be processed by \mathbf{T}_G . The matrix \mathbf{T}_G is found to be equal to $\mathbf{V}_G\mathbf{W}$, a product of two matrices, by linear algebraic analyses discussed in Appendix. The values of the elements

of $\tilde{\mathbf{G}}(\hat{z})$ is given by

$$\begin{aligned} \tilde{G}_k(\hat{z}) &= H_0(\hat{z}) + j \sum_{n=1}^{N-1} V_{G,N}^n W_N^{kn} H_{N-n}(\hat{z}), \\ k &= 0, 1, \dots, N-1 \end{aligned} \quad (45)$$

where $V_{G,N} = e^{-j\pi/2N}$ and $W_N = e^{j2\pi/N}$. The matrices \mathbf{V}_G is defined by

$$\mathbf{V}_G = \text{diag}\{1, V_{G,N}, \dots, V_{G,N}^{N-1}\} \quad (46)$$

and \mathbf{W} is obtained as (A.13) in Appendix. The matrix \mathbf{T}_G^{-1} is the inverse of \mathbf{T}_G and is equal to $\mathbf{W}^{-1}\mathbf{V}_G^{-1}$ where

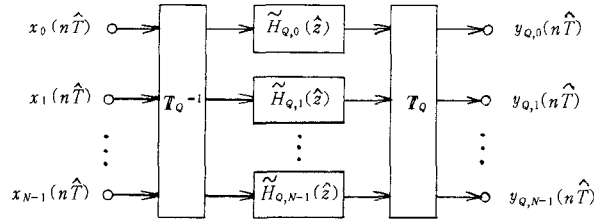
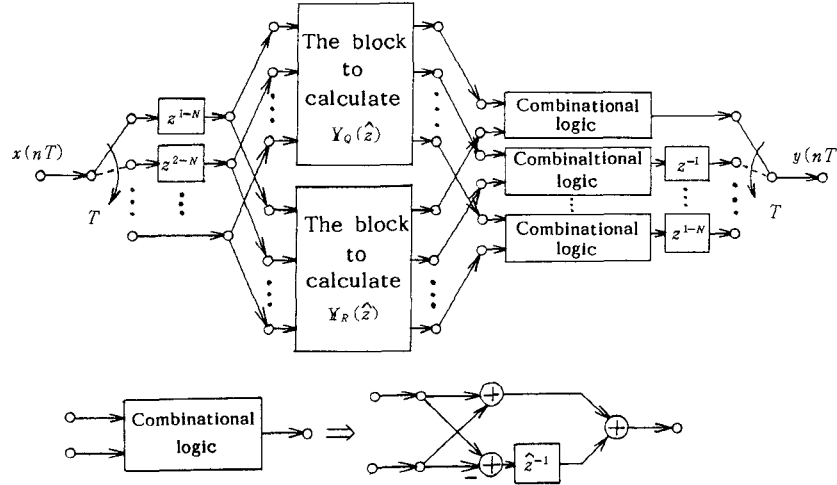
$$\mathbf{V}_G^{-1} = \text{diag}\{1, V_{G,N}^{-1}, V_{G,N}^{-2}, \dots, V_{G,N}^{-(N-1)}\}. \quad (47)$$

and \mathbf{W}^{-1} is also obtained as (A.14) in Appendix.

The multiplication of any N component vector, whose elements are parts of a signal sample sequence, with \mathbf{W}^{-1} implies N -point FFT computation of the concerned sequence (see Appendix). However, before FFT computation, the processing by \mathbf{V}_G which is just a diagonal matrix, is just like scaling the input signal samples. Similarly, the post-processing also consists of two parts: first by \mathbf{W} and then finally by \mathbf{V} . Multiplication by \mathbf{W} implies IFFT computations and that by \mathbf{V} , which is only a diagonal matrix, implies linearly scaling the sample values. The complete block diagram to implement $H(z)$ is shown in Fig. 10.

B. Complex Transfer Function

For the sake of the completeness of the mathematical treatment, and to take care of the special circumstances, we will consider the case when the transfer function to be implemented has some complex valued coefficients. Obviously, the desired output vector $\mathbf{Y}(\hat{z})$ is given by (38). The

Fig. 11. Block diagram to compute $\mathbf{Y}_Q(\hat{z})$.Fig. 12. High speed computation of $Y(z)$ for the case of complex coefficients.

output vectors $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$ will be calculated separately. Like in Section IV-A, the matrices $\mathbb{H}_Q(\hat{z})$ and $\mathbb{H}_R(\hat{z})$ will be converted into diagonal ones $\tilde{\mathbb{H}}_Q(\hat{z})$ and $\tilde{\mathbb{H}}_R(\hat{z})$, respectively, by similarity transformation. By doing that, number of multiplications in the z -domain given by (39), which are actually convolutions in time domain, are reduced. Essentially, these transformations result in pre-processing, consisting of sample scaling followed up by FFT computations, and post processing, consisting of IFFT computations followed up by sample scaling.

Let us first calculate $\mathbf{Y}_Q(\hat{z})$ by transforming $\mathbb{H}_Q(\hat{z})$ to $\tilde{\mathbb{H}}_Q(\hat{z})$ given by

$$\begin{aligned} \tilde{\mathbb{H}}_Q(\hat{z}) &= \mathbb{T}_Q^{-1} \mathbb{H}_Q(\hat{z}) \mathbb{T}_Q \\ &= \text{diag} \{ \tilde{H}_{Q,0}(\hat{z}), \tilde{H}_{Q,1}(\hat{z}), \dots, \tilde{H}_{Q,N-1}(\hat{z}) \} \quad (48) \end{aligned}$$

which in turn makes the vector $\mathbf{Y}_Q(\hat{z})$ equal to $\mathbb{T}_Q \tilde{\mathbb{H}}_Q(\hat{z}) \mathbb{T}_Q^{-1} \mathbf{X}(\hat{z})$. The matrix \mathbb{T}_Q is equal to the product of two matrices i.e., $\mathbb{V}_Q \mathbb{W}$. The matrix \mathbb{V}_Q is a diagonal one defined by

$$\mathbb{V}_Q = \text{diag} \{ 1, V_N, V_N^2, \dots, V_N^{N-1} \} \quad (49)$$

where $V_N = e^{-j\pi/N}$. The matrix \mathbb{W} is the same as described in Appendix. The inverse of the matrix \mathbb{T}_Q is equal to $\mathbb{W}^{-1} \mathbb{V}_Q^{-1}$ where

$$\mathbb{V}_Q^{-1} = \text{diag} \{ 1, V_N^{-1}, V_N^{-2}, \dots, V_N^{-(N-1)} \}. \quad (50)$$

The elements of $\tilde{\mathbb{H}}_Q(\hat{z})$ are given as

$$\begin{aligned} \tilde{H}_{Q,k}(\hat{z}) &= H_0(\hat{z}) + \sum_{n=1}^{N-1} V_N^n W_N^{kn} H_{N-n}(\hat{z}), \\ k &= 0, 1, 2, \dots, N-1. \quad (51) \end{aligned}$$

Obviously, the preprocessing consists of scaling by the values of elements of \mathbb{V}_Q^{-1} and followed up by N -point FFT computations. Subsequently, the post-processing consists of IFFT computations followed up by scaling. Fig. 11 shows the block diagram to compute $\mathbf{Y}_Q(\hat{z})$.

Next, $\mathbf{Y}_R(\hat{z})$ can be calculated by transforming $\mathbb{H}_R(\hat{z})$ to $\tilde{\mathbb{H}}_R(\hat{z})$. The corresponding preprocessing matrix \mathbb{T}_R^{-1} is equal to \mathbb{W}^{-1} indicating that preprocessing consists only of FFT computations. Essentially, the post-processing consists only of IFFT computations. The elements of $\tilde{\mathbb{H}}_R(\hat{z})$ are given by

$$\begin{aligned} \tilde{H}_{R,k}(\hat{z}) &= H_0(\hat{z}) + \sum_{n=1}^{N-1} W_N^{kn} H_{N-n}(\hat{z}), \\ k &= 0, 1, 2, \dots, N-1. \quad (52) \end{aligned}$$

After computing $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$ we proceed to compute the desired output vector $\mathbf{Y}(\hat{z})$ using (38). Fig. 12 shows the block diagram to compute $\mathbf{Y}(\hat{z})$. Two separate blocks are used to compute the elements of vectors $\mathbf{Y}_Q(\hat{z})$ and $\mathbf{Y}_R(\hat{z})$ which are combined at the output. The input signal samples are delayed by z^{1-N}, z^{2-N}, \dots units successively. This is because the preprocessing consists of FFT computations of the input signal samples and hence the successive groups of input signal samples are delayed by successively reduced delay units in order that the corresponding samples, in different groups, but belonging to same sequential order appear simultaneously on the time frame. Similarly the post-postprocessing consists of IFFT processing and hence the successive sequences of the output samples, provided by $\tilde{\mathbb{H}}_Q(\hat{z})$ and $\tilde{\mathbb{H}}_R(\hat{z})$, are subjected to successively increasing amounts of delays in order to

TABLE III
VALUES OF c , a_i , AND b_i OF IIR LOW-PASS FILTER IN EXAMPLE 1
OF SECTION IV

coefficients	real-part	imag.-part
c	1.68678E-6	0.00000
a_1, \dots, a_{10}	-1.00000	0.00000
b_1	0.740805	0.531756
b_2	0.740805	-0.531756
b_3	0.438515	0.413467
b_4	0.438515	-0.413467
b_5	0.571400	0.293639
b_6	0.571400	-0.293639
b_7	0.530860	0.175150
b_8	0.530860	-0.175150
b_9	0.511770	0.0581848
b_{10}	0.511770	-0.0581848

make them appear in a proper sequence in the time frame of a single output $y(nT)$.

C. Illustrative Examples

This section presents a couple of examples of digital filter design, performed along the procedure outlined in Sections IV-A and B, starting from a given set of specifications. Just like the approach of Section III-C, first a transfer function $H(z)$ is obtained which satisfies the given specifications by any of the suitable methods available in the literature. Subsequently starting from that $H(z)$, the component transfer functions $\tilde{G}_k(\hat{z})$ for $k=0,1,2,\dots,N-1$ for the case when $H(z)$ is real, or a pair of sets of them $\tilde{H}_{Q,k}(z)$ and $\tilde{H}_{R,k}(\hat{z})$ for $k=0,1,2,\dots,N-1$ for the case when $H(z)$ has complex coefficients are obtained. The magnitude responses of the filter are plotted to check the conformation to the given specifications. The value of N is selected from the consideration of the factor by which the speed up must take place.

(i) Example 1: Low-Pass Filter

To design a LP filter with $N=8$ having specifications of $\omega_c T = 0.2\pi$, $\alpha_{\max} = 3$ dB, $\omega_{\min} T = 0.35\pi$, and $\alpha_{\min} = 55$ dB. Using the method outlined in [6], the transfer function which satisfies these specifications is given by

$$H(z) = c \prod_{m=1}^{10} \frac{1 - a_m z^{-1}}{1 - b_m z^{-1}}. \quad (53)$$

The values of the coefficients a_m and b_m for $m=1,2,\dots,10$ are given in Table III. Using (2), (5), (43) and (44) we get

$$\tilde{G}_k(\hat{z}) = \frac{\sum_{m=0}^{10} g_{m,k} \hat{z}^{-m}}{\prod_{m=1}^{10} (1 - b_m^8 \hat{z}^{-1})}. \quad (54)$$

The values of $g_{m,k}$ for $m=0,1,2,\dots,10$ and $k=0,1,2,\dots,7$ are calculated but not attached for the sake of lack of space. Fig. 13 shows the magnitude plot for the designed filter.

(ii) Example 2: Bandpass Filter

Design a bandpass digital filter satisfying following specifications: The passband extends over the range governed by $0.15\pi < \omega T < 0.55\pi$. The range of the stop-band is $-\pi < \omega T < 0$ and $0.7\pi < \omega T$. The minimum attenuation in the stop band is 30 dB and the maximum attenuation in the passband is 3 dB.

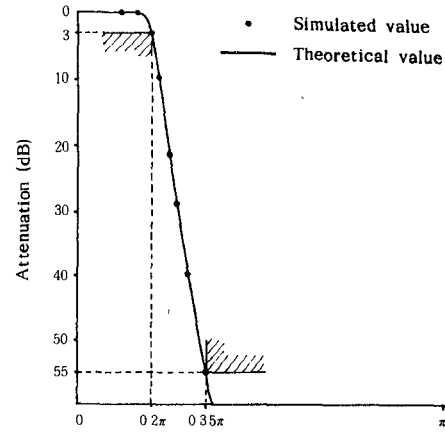


Fig. 13. Magnitude response of the low-pass filter in Example 1 of Section IV.

TABLE IV
VALUES OF c , \bar{a}_i , AND \bar{b}_i OF IIR BAND-PASS FILTER IN EXAMPLE 2
OF SECTION IV

coefficients	real-part	imag.-part
c	3.41175E-4	0.00000
$\bar{a}_1, \dots, \bar{a}_6$	-1.00000	0.00000
\bar{b}_1	0.702045	0.492925
\bar{b}_2	0.702045	-0.492925
\bar{b}_3	0.57134	0.293666
\bar{b}_4	0.57134	-0.293666
\bar{b}_5	0.51589	0.0970438
\bar{b}_6	0.51589	-0.0970438

TABLE V
VALUES OF c , a_i , AND b_i OF IIR BAND-PASS FILTER IN EXAMPLE 2
OF SECTION IV

coefficients	real-part	imag.-part
c	3.41175E-4	0.00000
a_1, \dots, a_6	-0.453991	-0.891007
b_1	-0.120478	0.849310
b_2	0.757921	0.401743
b_3	-2.27542E-3	0.642389
b_4	0.521041	0.375746
b_5	0.147743	0.503718
b_6	0.320676	0.415604

Assume that a desired value of N is 4. The approach followed in the present example is to convert the above given specifications into that which corresponds to a low-pass filter whose magnitude characteristics is the shifted version, along the frequency axis, of the desired bandpass filter. The specification of such a low-pass filter is given by $\omega_c T = 0.2\pi$, $\alpha_{\max} = 3$ dB, $\omega_{\min} T = 0.35\pi$ and $\alpha_{\min} = 30$ dB.

The transfer function which satisfies the specifications of the low-pass filter is given by

$$P(z') = c \prod_{m=1}^6 \frac{(1 - \bar{a}_m z'^{-1})}{(1 - \bar{b}_m z'^{-1})}. \quad (55)$$

The values \bar{a}_m and \bar{b}_m are given in Table IV. Let us perform the phase transformation on the variable z' , such that the transformed function $H(z)$ is a bandpass filter, given by $z = e^{-j\theta} z'$ and $\theta = 0.35\pi$. Thus the transfer function is given by

$$H(z) = c \prod_{m=1}^6 \frac{(1 - a_m z^{-1})}{(1 - b_m z^{-1})} \quad (56)$$

where the coefficients a_m and b_m are given in Table V.

TABLE VI
VALUES OF $q_{m,k}$ OF IIR BAND-PASS FILTER IN EXAMPLE 2 OF
SECTION IV

k	m	real-part	imag.-part
0	0	2.23134E-2	-3.10848E-2
0	1	-1.47697E-1	-3.62621E-2
0	2	-1.24750E-1	9.55890E-2
0	3	5.58359E-2	8.84698E-2
0	4	9.96392E-3	-1.23493E-2
0	5	-3.74568E-4	-8.81755E-5
0	6	5.63596E-8	1.89633E-7
1	0	4.09346E-2	4.47797E-2
1	1	1.86858E-1	-6.46190E-1
1	2	-9.21907E-1	1.84369E-1
1	3	2.05259E-1	2.74853E-1
1	4	1.57833E-2	-2.86720E-2
1	5	-5.43878E-4	-4.80919E-5
1	6	5.63596E-8	1.89633E-7
2	0	-4.57113E-2	1.35896E-2
2	1	-3.92578E-2	2.63592E-1
2	2	1.69079E-1	2.29602E-1
2	3	1.49930E-1	3.47813E-2
2	4	-3.96829E-3	2.04841E-2
2	5	-4.36422E-4	1.13138E-4
2	6	5.63596E-8	1.89633E-7
3	0	-1.61720E-2	-2.72844E-2
3	1	-1.12995E-1	7.08006E-2
3	2	-1.75964E-2	1.40824E-1
3	3	8.29077E-2	2.96671E-2
3	4	2.44519E-3	1.30492E-2
3	5	3.35817E-4	2.30999E-5
3	6	5.63596E-8	1.89633E-7

Obviously, $H(z)$ is a transfer function with complex coefficients. Using (2), (5), (35), (37), and (48) we get

$$\tilde{H}_{Q,k}(\hat{z}) = \frac{\sum_{m=0}^6 q_{m,k} \hat{z}^{-m}}{\prod_{m=1}^6 (1 - b_m^4 \hat{z}^{-1})}$$

$$\tilde{H}_{R,k}(\hat{z}) = \frac{\sum_{m=0}^6 r_{m,k} \hat{z}^{-m}}{\prod_{m=1}^6 (1 - b_m^4 \hat{z}^{-1})} \quad (57)$$

The values $q_{m,k}$ and $r_{m,k}$ for $m=0,1,2,\dots,6$ and $k=0,1,2,3$ are given in Table VI and Table VII, respectively. Fig. 14 shows the magnitude plot of the filter designed.

V. PRACTICAL IMPLEMENTATION USING DSP

A. System Description

A multi-DSP based hardware system has been designed and built to implement signal processing system developed along the lines discussed in Sections III and IV. Broadly speaking, the complete system can be viewed as consisting of two parts: I/O part and the signal processing part. The I/O part handles both analog and digital input signal samples and has the facility to produce both kinds of outputs. The signal processing part constitutes of four units of DSP's and it can perform the exchange of data with any compatible external I/O system, like the one used here, along a global bus consisting of data and control lines. The multiprocessor system has two distinct modes of operation: program dumping mode and program execution mode. The

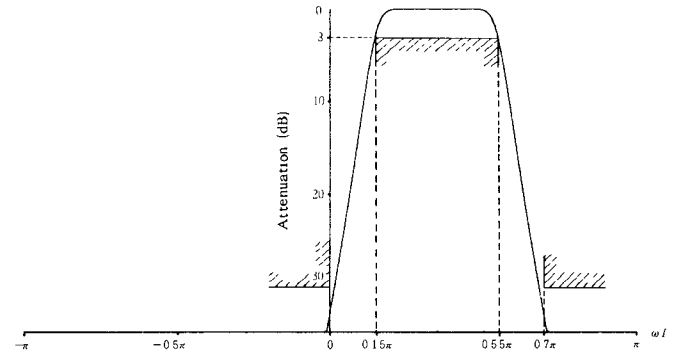


Fig. 14. Magnitude response of bandpass filter in Example 2 of Section IV.

TABLE VII
VALUES OF $r_{m,k}$ OF IIR BAND-PASS FILTER IN EXAMPLE 2 OF
SECTION IV

k	m	real-part	imag.-part
0	0	-4.96798E-2	8.17992E-3
0	1	3.19887E-1	1.22543E-1
0	2	-2.86570E-1	-2.99200E-1
0	3	1.74401E-2	1.86771E-1
0	4	1.66775E-2	-1.57905E-2
0	5	4.56188E-4	-1.12613E-4
0	6	5.63596E-8	1.89633E-7
1	0	1.87726E-2	-5.62807E-2
1	1	-5.88461E-1	-2.19895E-1
1	2	-2.55778E-1	8.32160E-1
1	3	3.16228E-1	5.88683E-2
1	4	1.18669E-3	-3.13384E-2
1	5	-5.31505E-4	6.88610E-5
1	6	5.63596E-8	1.89633E-7
2	0	3.28668E-2	1.59003E-2
2	1	2.49267E-2	-1.66163E-1
2	2	-1.61018E-1	1.32476E-1
2	3	1.03661E-1	3.30838E-2
2	4	-1.21657E-4	-1.53704E-2
2	5	-3.64178E-4	7.82453E-5
2	6	5.63596E-8	1.89633E-7
3	0	-5.94826E-4	3.22004E-2
3	1	1.30556E-1	-8.45444E-2
3	2	-1.91808E-1	-1.50518E-2
3	3	5.57041E-2	7.94855E-2
3	4	6.48152E-3	-1.20554E-2
3	5	-3.38815E-4	-3.45233E-5
3	6	5.63596E-8	1.89633E-7

former mode is used to download the object code, corresponding to the signal processing task on hand, from an external facility, and the later mode is provided to execute the signal processing programs. The external facility consists of console editor, assembler, a ROM burner, as well as interfaces to backup data storage and printer, all integrated in one hardware package. The concerned system monitor is ROM based. The hardware block diagram is shown in Fig. 15.

The I/O part consists of an A/D convertor followed up by a latch to store the digital value of the converted signal sample before it can be passed on to the signal processing system through the global bus. The signal line marked SOC is the start convert input command to the A/D convertor. A clock generator is fed to a programmable divider whose output is given to the SOC line of the A/D convertor. This ensures availability of input signal samples at a rate variable on choice. The board has a D/A convertor to provide an analogue output. There are two level of latches between

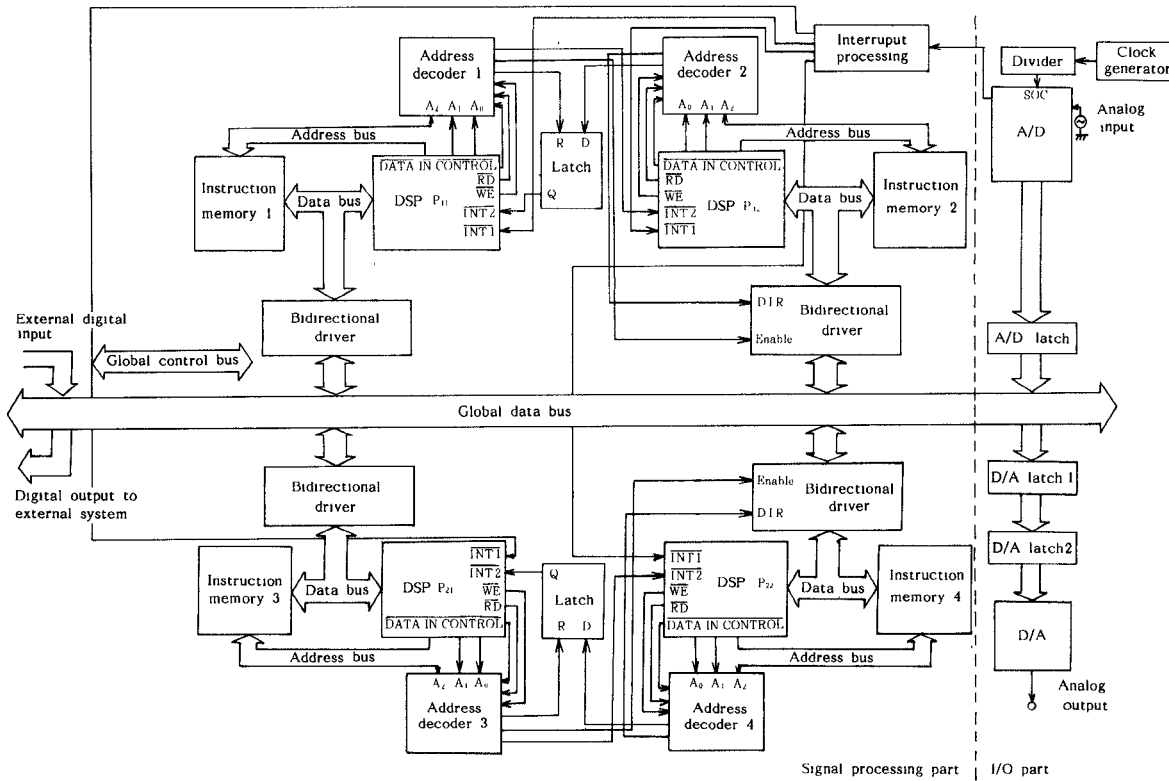


Fig. 15. Block diagram of the hardware system.

the global bus and the D/A convertor. This is necessary to ensure that the rate at which the output signal samples are available, to the user, matches the input signal sampling rate. The first latch closer to the global bus stores the data calculated by the DSP at the time instant governed by the data outputting instruction. The next start convert command, to sample the input analog signal, also strobes the data present in the first latch, into the second latch which feeds the D/A convertor. So no matter what time a DSP provides the calculated data out, the output of the D/A convertor changes at the instants which are only governed by the input signal sampling rate. However, on user choice, one level of latch can be made transparent in case of special circumstances.

The signal processing system has on board memory which is of two types: a common memory shared by all the four processors and four individual blocks of private memories. One such unit of private memory is associated to a DSP each. The data and code stored in private memories can be accessed directly by the concerned processor only. This kind of memory configuration makes the present system a tightly coupled multi-processor system. Each processor has its local data, address, and control busses to access the software program stored in the corresponding instruction memory. However, the processors communicate with each other, the common memory and the external I/O system through a tristated global bus. This global bus is isolated from the local busses of the processor as well as those of the I/O components like A/D and D/A convertor by buffers, latches or transceivers. The global bus consists of the data bus, I/O port selecting address lines,

A/D and D/A interface lines and timing control signal lines.

A delayed multipath digital filter discussed in Section III, and shown in Fig. 4, is presented here as an example of signal processing implemented on the present hardware. This example is also a demonstration of the software adaptability of the given system to implement some of the hardware features, of the task concerned, which are not directly available as hardware elements. The two pairs of input/output switches S_{i1} , S_{i2} , S_{o1} , and S_{o2} are effectively implemented, for exchanging data between tristate global bus and the appropriate DSP, by proper enable command to route the data in a desired direction. Moreover, the delay element of the path P_2 is not incorporated in hardware. This is accomplished by reorganization of the input sample sequence stream to subpaths P_{21} and P_{22} . The adder of the Fig. 4 also does not actually exist as a hardware element but is implemented by a suitable software instruction in DSP's P_{11} and P_{12} . Only the DSP's corresponding to subpaths P_{11} and P_{12} give out data to the D/A convertor. The processors P_{21} and P_{22} just pass the output data values, they calculate, on to P_{11} and P_{12} , respectively.

B. Program Flow

As far as the operation of the system is concerned, the processors P_{11} and P_{21} form a processing pair while the other two processors form yet another pair. Fig. 16 shows the flowchart corresponding to the software associated to one such pair. The program flowchart associated to the other pair is also the same. The program bodies inscribed

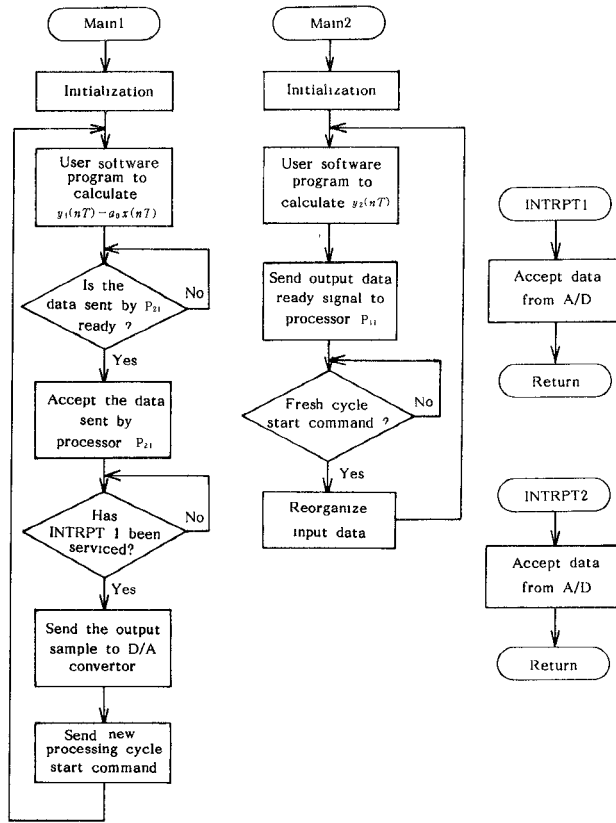


Fig. 16. Process flowchart.

as Main1 and Main2 correspond to the main software routines associated to processors P_{11} and P_{21} respectively. Likewise, there are two interrupt subroutines INTRPT1 and INTRPT2 corresponding to processors P_{11} and P_{21} . The two processors accept fresh input signal samples by jumping to the respective interrupt routines. The terms defined as $y_1(nT)$ and $y_2(nT)$ correspond to the output signal samples given by an expression similar to

$$y(nT) = \sum_{i=0}^p a_i x(nT - iT). \quad (58)$$

In general it is assumed that the four transfer functions corresponding to each of the four processing paths are independent and individually selectable so that the processing times, associated to each of the paths, have no constraints as far as their relative lengths are concerned.

VI. DISCUSSION

An N -path filter structure, to increase the signal processing throughput speed to N times that possible by a single filter block was proposed. However, this results in appearance of unwanted passbands in the frequency response of the composite transfer function. This is because of certain missing powers of z which can not be realized in the composite transfer function in z domain. A method to overcome this problem, by having several blocks of such N -path structures with the input signal samples fed to the successive blocks after successively increasing number of delay units, was proposed as one solution. Separate design

techniques of second order as well as n th-order FIR and IIR digital filters were presented. Another advantage, this method is seen to offer, is that the poles of the desired transfer function, if close to the unit circle on the z -plane, are pushed away from the circumference towards the origin by the transformation of the type given by (21). This implies that the constituent transfer functions of the present system are less sensitive, from the stability point of view, to variations in the values of the coefficients. Although this approach provided the solution to the problem of unwanted passbands, yet it still has a problem remaining as far as the implementation complexity is concerned. For an N path implementation, we need N^2 transfer functions, to form the parallel paths, which perform the signal processing parallelly in time. This implies that hardware complexity increases as square function with the factor by which the signal throughput rate is speeded up.

Subsequently, another improvement is proposed by which the N -path transfer function matrix is reduced to a diagonal one by similarity transformation. This enables, the N^2 constituent transfer function blocks to be implemented by only N constituent transfer function blocks. However, the input signal samples need to be preprocessed by FFT computations and the signal samples, which are the outputs of the constituent transfer function blocks, need to be postprocessed by IFFT computations. Moreover, in case the desired transfer function has complex coefficients, $2N$ constituent transfer function blocks are needed instead of N . Looking at the resulting structure from the point of view of the complete system, we find that between the input and output signal samples, there are three distinct processing blocks operating in tandem: an N -point FFT processor, N or $2N$ parallel transfer function blocks and an N -point IFFT processor in that order. However, the system throughput rate is governed by that part of the three part system which takes the largest time. If T_1 , T_2 , and T_3 were the processing times of the three parts mentioned above, respectively, the overall system throughput rate f is bounded by

$$f < \frac{1}{\text{largest}\{T_1, T_2, T_3\}}. \quad (59)$$

However, this system also has its own limitations. Even for an input signal which has only real valued samples and a transfer function, to be implemented, which has only real valued coefficients, the outputs of the FFT processors are complex in general. Moreover, the coefficients of the constituent transfer functions are also complex. This implies that a single complex multiplication of the type $a_i x(nT - iT)$ in the convolution equation (58) actually needs 4 multiplication operations followed by 2 independent additions because both the quantities a_i and $x(nT - iT)$, in general are complex. Hence unless the largest individual constituent transfer function has an order which is order of magnitude less than that of the original transfer function, proposed to be implemented, the factor by which the throughput rate speed up takes place will be substantially less than the projected number N . Hence no significant

advantage is gained by the later method for a value of N which is low, i.e., less than 10. Thus the methods of Sections III and IV are not rival approaches but complementary ones, respectively. The method outlined in Section III is suited for low values of N and that of Section IV is preferred for larger values of N . This is because the former is too complex and expensive at larger values of N while the latter may not give reasonable speed-up factor at relatively low values of N .

APPENDIX

FFT AND IFFT FROM SIMILARITY TRANSFORMATION

Let an $N \times N$ matrix be defined by

$$\mathbb{P} = \begin{bmatrix} P_0 & \alpha P_{N-1} & \alpha P_{N-2} & \cdots & \alpha P_1 \\ P_1 & P_0 & \alpha P_{N-1} & \cdots & \alpha P_2 \\ P_2 & P_1 & P_0 & \cdots & \alpha P_3 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ P_{N-1} & P_{N-2} & P_{N-3} & \cdots & P_0 \end{bmatrix} \quad (\text{A.1})$$

in which α is a complex number satisfying $\alpha\alpha^* = 1$ where α^* is the complex conjugate of α . There exists a matrix \mathbb{T} for a given \mathbb{P} defined in (A.1) such that a transformation of the type

$$\tilde{\mathbb{P}} = \mathbb{T}^{-1} \mathbb{P} \mathbb{T} = \text{diag} \{ \tilde{P}_0, \tilde{P}_1, \tilde{P}_2, \dots, \tilde{P}_{N-1} \} \quad (\text{A.2})$$

converts \mathbb{P} into a diagonal matrix $\tilde{\mathbb{P}}$. The columns of \mathbb{T} are the eigenvectors of \mathbb{P} . Let us first calculate the value of $|\mathbb{P}|$, then evaluate the eigenvalues of \mathbb{P} and finally find out the eigenvectors of \mathbb{P} . It shall be seen that, in general, for a matrix \mathbb{P} of (A.1), the matrix \mathbb{T} can be expressed in form of a product of two matrices: one of which is a diagonal matrix and the other is such that multiplication by that

$(k+1)$ th element of the first column becomes

$$\begin{aligned} & P_k + \tau P_{k-1} + \cdots + \tau^{k-1} P_1 + \tau^k P_0 \\ & + \alpha \tau^{k+1} P_{N-1} + \cdots + \alpha \tau^{N-1} P_{k+1} \\ & = \tau^k (P_0 + \alpha \tau P_{N-1} + \cdots + \alpha \tau^{N-k-1} P_{k+1} \\ & + \tau^{-k} P_k + \cdots + \tau^{-1} P_1). \end{aligned} \quad (\text{A.4})$$

Since α is located on the unit circle in the complex plane, we can use the identity $\tau^{-k} = \alpha \tau^{N-k}$ to obtain the right-hand side of (A.4) equal to

$$\tau^k (P_0 + \alpha \tau P_{N-1} + \alpha \tau^2 P_{N-2} + \cdots + \alpha \tau^{N-1} P_1). \quad (\text{A.5})$$

The expression for α , which in general is a complex number, is $e^{j\theta_\alpha}$. The term τ_k , which is the k -th root of equation $\tau^N = \alpha^*$ can be defined by $\tau_k = V_N W_N^k$ where $V_N = e^{-j\theta_\alpha/N}$ and $W_N = e^{j2\pi/N}$.

The value of the determinant \mathbb{P} is given by

$$\det[\mathbb{P}] = \prod_{k=0}^{N-1} \left(P_0 + \alpha \sum_{n=1}^{N-1} V_N^n W_N^{kn} P_{N-n} \right). \quad (\text{A.6})$$

Corresponding to the eigenvalues λ of \mathbb{P} , the equation

$$(\mathbb{P} - \lambda \mathbb{I}) = \prod_{k=0}^{N-1} \left(P_0 - \lambda + \alpha \sum_{n=1}^{N-1} V_N^n W_N^{kn} P_{N-n} \right) = 0, \quad (\text{A.7})$$

must be satisfied. The eigenvalues are given by

$$\lambda_k = P_0 + \alpha \sum_{n=1}^{N-1} V_N^n W_N^{kn} P_{N-n}, \quad k = 0, 1, 2, \dots, N-1. \quad (\text{A.8})$$

The corresponding eigenvector \mathbb{U}_k is governed by the equation

$$(\mathbb{P} - \lambda_k \mathbb{I}) \mathbb{U}_k = \begin{bmatrix} -S & \alpha P_{N-1} & \alpha P_{N-2} & \cdots & \alpha P_1 \\ P_1 & -S & \alpha P_{N-1} & & \alpha P_2 \\ P_2 & P_1 & -S & & \alpha P_3 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ P_{N-1} & P_{N-2} & P_{N-3} & \cdots & -S \end{bmatrix} \begin{bmatrix} U_{k,0} \\ U_{k,1} \\ U_{k,2} \\ \vdots \\ U_{k,N-1} \end{bmatrix} = \mathbf{0} \quad (\text{A.9})$$

implies IFFT computations. The inverse of this matrix represented as \mathbb{T}^{-1} is a product of two matrices: one of them is such a matrix that a multiplication by it implies FFT computations and the other is a diagonal matrix.

Performing a linear combination of the elements of the first column with τ^{r-1} times the corresponding element of that of r th column for $r = 2, 3, \dots, N$, we obtain

$$\mathbb{P} = \begin{bmatrix} P_0 & + & \alpha \tau P_{N-1} & + & \alpha \tau^2 P_{N-2} & + & \cdots & + & \alpha \tau^{N-1} P_1 & \alpha P_{N-1} & \alpha P_{N-2} & \cdots & \alpha P_1 \\ P_1 & + & \tau P_0 & + & \alpha \tau^2 P_{N-1} & + & \cdots & + & \alpha \tau^{N-1} P_2 & P_0 & \alpha P_{N-1} & \cdots & \alpha P_2 \\ P_2 & + & \tau P_1 & + & \tau^2 P_0 & + & \cdots & + & \alpha \tau^{N-1} P_3 & P_1 & P_0 & \cdots & \alpha P_3 \\ & & & & \vdots & & & & & \vdots & \vdots & & \vdots \\ P_{N-1} & + & \tau P_{N-2} & + & \tau^2 P_{N-3} & + & \cdots & + & \tau^{N-1} P_0 & P_{N-2} & P_{N-3} & \cdots & P_0 \end{bmatrix} \quad (\text{A.3})$$

where τ is one of the N roots of the equation $\tau^N = \alpha^*$. After the above mentioned linear combinations, the

where

$$S = \alpha \sum_{n=1}^{N-1} V_N^n W_N^{kn} P_{N-n}.$$

Evaluating $(l+1)$ th row of (A.9) we get the solution of

an element of the k th eigenvector \mathbf{U}_k as

$$\begin{aligned} & P_l U_{k,0} + P_{l-1} U_{k,1} + \cdots + P_2 U_{k,l-2} + P_1 U_{k,l-1} - S U_{k,l} \\ & + \alpha P_{N-1} U_{k,l+1} + \cdots + \alpha P_{l+1} U_{k,N-1} \\ & = U_{k,l} \left(-S + \alpha P_{N-1} \frac{U_{k,l+1}}{U_{k,l}} + \cdots + \alpha P_{l+1} \frac{U_{k,N-1}}{U_{k,l}} \right. \\ & \quad \left. + P_l \frac{U_{k,0}}{U_{k,l}} + \cdots + P_1 \frac{U_{k,l-1}}{U_{k,l}} \right). \end{aligned} \quad (\text{A.10})$$

One of the solutions for $U_{k,n}$, which satisfies (A.10) by using (A.9) is $V_N^n W_N^{kn}$. Consequently, the complete eigenvector \mathbf{U}_k is given by

$$\mathbf{U}_k = [1, V_N W_N^k, V_N^2 W_N^{2k}, \dots, V_N^{N-1} W_N^{k(N-1)}]^T. \quad (\text{A.11})$$

The matrix \mathbf{T} is calculated to be

$$\mathbf{T} = \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ V_N & V_N W_N & V_N W_N^2 & \cdots & V_N W_N^{N-1} \\ V_N^2 & V_N^2 W_N^2 & V_N^2 W_N^4 & \cdots & V_N^2 W_N^{2(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ V_N^{N-1} & V_N^{N-1} W_N^{N-1} & V_N^{N-1} W_N^{2(N-1)} & \cdots & V_N^{N-1} W_N^{(N-1)^2} \end{bmatrix} = \mathbf{V} \mathbf{W} \quad (\text{A.12})$$

where

$$\begin{aligned} \mathbf{V} &= \text{diag} \{1, V_N, V_N^2, \dots, V_N^{N-1}\} \\ \mathbf{W} &= \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & W_N & W_N^2 & \cdots & W_N^{N-1} \\ 1 & W_N^2 & W_N^4 & \cdots & W_N^{2(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & W_N^{N-1} & W_N^{2(N-1)} & \cdots & W_N^{(N-1)^2} \end{bmatrix}. \end{aligned} \quad (\text{A.13})$$

The matrix \mathbf{T}^{-1} , which is the inverse of transformation \mathbf{T} , is given by $\mathbf{T}^{-1} = \mathbf{W}^{-1} \mathbf{V}^{-1}$ where

$$\begin{aligned} \mathbf{V}^{-1} &= \text{diag} \{1, V_N^{-1}, V_N^{-2}, \dots, V_N^{-(N-1)}\} \\ \mathbf{W}^{-1} &= \frac{1}{N} \begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & W_N^{-1} & W_N^{-2} & \cdots & W_N^{-(N-1)} \\ 1 & W_N^{-2} & W_N^{-4} & \cdots & W_N^{-2(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & W_N^{-(N-1)} & W_N^{-2(N-1)} & \cdots & W_N^{-(N-1)^2} \end{bmatrix}. \end{aligned} \quad (\text{A.14})$$

From (A.14) it is obvious that premultiplying a vector, whose component elements consist of samples of a discrete time sequence, by \mathbf{W}^{-1} amounts to evaluation of DFT (discrete Fourier transform) of that sequence. This can be achieved in practice efficiently by FFT computations. Likewise, premultiplication by \mathbf{W} amounts to IFFT computations.

ACKNOWLEDGMENT

The authors would like to express their thanks to H. Nakajo and K. Sako of Kobe University, Kobe City, Japan, for their help rendered during experiment.

REFERENCES

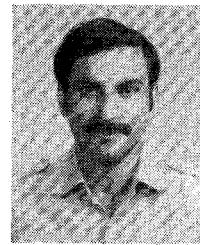
- [1] T. Nishitani, R. Murata, Y. Kawakami, and H. Goto, "A single chip digital signal processor for telecommunication applications," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 372-376, Aug. 1981.
- [2] Y. Hagiwara, Y. Kita, T. Miyamoto, Y. Toba, H. Hara, and T. Akazawa, "A single chip digital signal processor and its application to real time speech analysis," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-31, pp. 339-346, Feb. 1983.
- [3] Shimada, Tsuda, et al., "Digital signal processor LSI-MB8763," *Japanese Inst. Communication Eng. J.*, CAS82-11 (1982-12) (Japanese).
- [4] S. K. Mitra and K. Hirano, "All digital N -path filter," in *Proc. 1983 European Conf. on Circuits Theory and Design*, pp. 358-361, Sept. 1983.
- [5] K. Sugahara, K. Hayashi, K. Hirano, and S. K. Mitra, " N -path digital filters," in *Proc. IEEE Int. Conf. on Acoust., Speech, and Signal Processing*, March 1984.
- [6] K. Hirano, H. Sakaguchi, and S. K. Mitra, "Explicit design formulae for digital tan filters with lowpass, highpass, bandpass and bandstop characteristics," *J. Franklin Inst.*, vol. 307, pp. 263-290, May 1979.



Katsuhiko Hayashi was born in Akashi, Japan in 1959. He received the B.E. and M.E. degrees from Kobe University in 1983, 1985, respectively.

In 1985, he joined Matsushita Electric Industrial Company, Ltd. His research interests are in digital signal processing.

✱

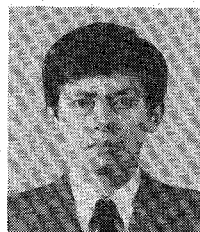


Kaushal K. Dhar received the B.E. degree in electrical communication engineering, from Indian Institute of Science, Bangalore, India, in 1973. In 1976 he received the M.Tech degree in electrical engineering from Indian Institute of Technology Kanpur, India.

He worked in the research and development wing of Hindustan Instruments Ltd., New Delhi, India, till 1981. He worked in the area of microprocessor based test and measuring instruments. He has been at Kobe University, Kobe, Japan,

since 1982 on a Research Scholarship from Japanese Ministry of Education. He is engaged in development of algorithm as well as design of hardware systems for digital signal processing. His current research interests are design and implementation of digital signal processing algorithms.

✱

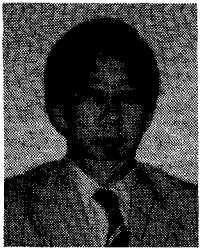


Kazunori Sugahara (M'83) was born in Kobe, Japan, on May 29, 1956. He received the B.E. degree from Yamanashi University, Kofu, in 1979, and M.E. degree from Tokyo Institute of Technology, Tokyo, in 1981.

Since 1981 he has been with the Department of Electrical Engineering, Kobe Technical College as a lecturer. His research interest is in the field of digital signal processing.

Mr. Sugahara is a member of the Institute of Electronics and Communication Engineers

of Japan.



Kotaro Hirano (S'60-M'65-SM'76) received the B.Eng., M.Eng., and Dr. Eng. degrees in communication engineering from Osaka University, Osaka, Japan, in 1960, 1962, and 1965, respectively.

He joined Kobe University, Kobe, Japan, in 1965, as an Associate Professor of Electrical Engineering and currently he is a full Professor as well as Chairman of Electronic Engineering. His current research interests include the design of one- and multi-dimensional digital filters and

applications of digital signal processors. He has been a member of Publicity or Technical Program Committee of IEEE International Symposium on Circuits and Systems for the past few years. He was chairman of a series of Kobe International Symposia, and a member of Organizing Committee of 1985 IEEE International Workshop on Digital Signal Processing at Kyoto, Japan.

Dr. Hirano is a member of Eta Kappa Nu and the Institute of Electronics and Communication Engineers of Japan.
