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FILU-200/LX4180

⇨ 300 MIPS RISC + DSP Core

Features

- Verilog core combines the Lexra LX4180 RISC functionality with the Massana FILU-200 DSP in a single core
- High-performance 32-bit MIPS® I Instruction Set Architecture
- High-performance dual MAC 16-bit DSP architecture with 20-bit internal data path and 44-bit accumulation
- MIPS 16™ code compression and ETJAG debug support
- Synthesizable Verilog – single clock design
- Extensive MIPS third-party tools availability
- Enables DSP development in C

Microcoded DSP Functions

Set of DSP functions include:

- ADSL and ADSL.Lite DSP functions
- Real and Complex FFT/IFFT
- FIR filters
- Adaptive filters
- 1^{st}, 2^{nd} & N^{th} order IIR filters
- Real and Complex Matrix/ Vector operations

A library of advanced DSP functions is available.

Applications

- Data communications
  - Cellular/Wireless
  - Wireline (xDSL)
- High end consumer products

Introduction

The FILU-200/LX4180 is an integrated 32-bit RISC core from LEXRA and a 16-bit fixed-point DSP coprocessor core from Massana. The LX4180 is a 32-bit R3000®-class processor that executes all MIPS® I instructions except for unaligned loads and stores. The LX4180 provides performance, power consumption, and die size optimized for embedded SOC applications. The FILU-200 DSP coprocessor core has a set of pre-programmed DSP functions are accessed through a C function call from the Lexra LX4180. This core provides 100 MIPS for the RISC and 200 MIPS for DSP in parallel.

The FILU-200/LX4180 is available in synthesizable Verilog and facilitates the development of custom systems in silicon that require DSP capability with high performance. Thus retaining the advantages of industry standard development tools such as compilers, linkers and assemblers. The FILU-200/LX4180 provides optimal price/performance value and broad software support ideal for SOC applications in data communications and high end consumer products.

The FILU DSP coprocessor core is capable of implementing various DSP functions which are microcoded and are invoked by the RISC core via a shared RAM. The LX4180 has Master control of the shared RAM via control/status bits. The microcoded kernel includes FIR and IIR filters, FFT, correlation, matrix operations and Taylor series.

The basic set of DSP functions are hardwired but RAM based functions can extend the DSP functionality after production. A library of advanced DSP functions is available.

It is expected that the user will develop their application entirely in C using an API to invoke DSP functions. To aid in the development process C and Verilog models are provided to allow system simulation. An evaluation board is available to allow the user to develop their own system applications.

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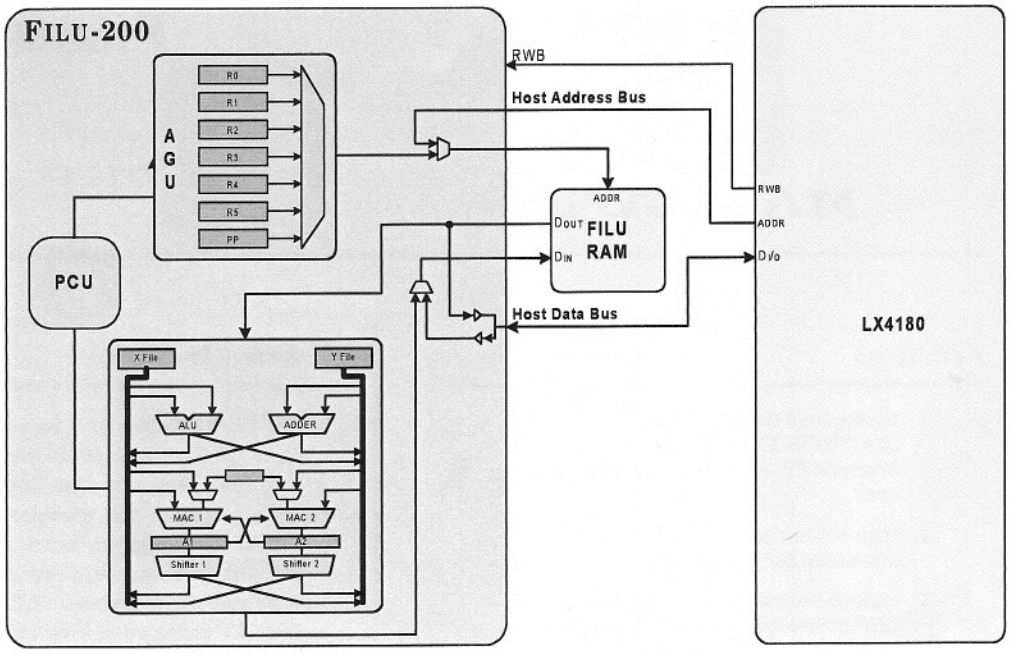

Figure 1 FILU-200/LX4180 *block diagram.*

DSP Benchmarks

The following benchmarks assume a 100 MHz clock.

Function	Data Points	Num of Coeff	Num of Cycles	Exec Time µs
Real FIR	N =100	p = 20	N(p/2+1)+p+18	**11 µs**
Real FFT	N = 1024	-	$N(\log_4 N+1)+49$	**62 µs**
Complex FFT	N = 1024	-	$2N(\log_4 N+½)+30$	**103 µs**
Complex Mult[1]	N = 256	N = 256	3N+9	**8 µs**
2nd Order IIR	N = 256	M = 8	2N+17	**5 µs**
G.Lite receiver[2]	N = 256	-	5370	**54 µs**

[1]Complex vector multiply of 256 complex data points.

[2]Assumes 20 coefficients for the TEQ, 256 points for FFT, 128 tones and a DMT symbol period of 250 µs.

Technical Specification

- ❑ Fully synthesizable – library independent
- ❑ Synchronous RAM
- ❑ 32-bit interface between LX4180 and FILU-200
- ❑ 3.5 mm^2 in 0.25 µm TLM
- ❑ Power consumption 425 mW

Hardware & Software Interface

There is a very simple hardware and software interface between the LX4180 and FILU-200. The FILU RAM is memory mapped into the LX4180 address space. An API allows the LX4180 to use C function calls to access the DSP functions. These automatically generate the appropriate initialization vector for the FILU.

- ❑ Coefficients & data written as vectors in FILU RAM, accessed with pointers
- ❑ A busy bit indicates start/end of FILU processing. This can be configured to interrupt the LX4180
- ❑ LX4180 has Master control of FILU RAM via control/status bits

For More Information

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