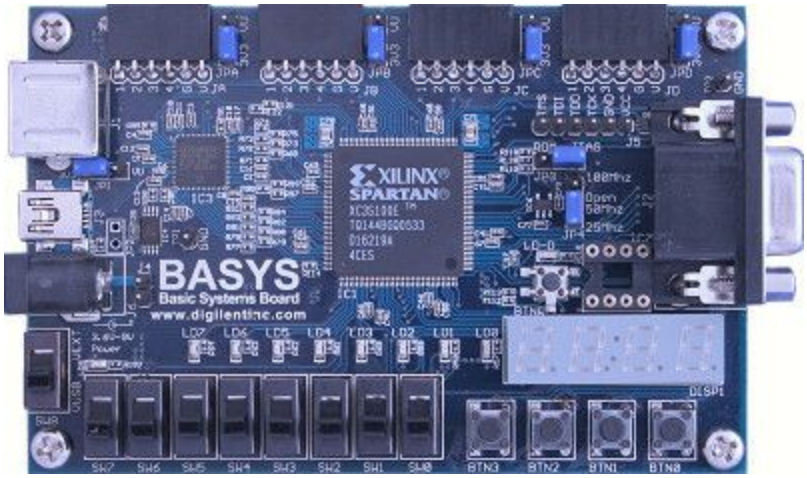
INTRODUCTION

In this project our aim is to design very basic ATM(Automated Teller Machine) using Verilog HDL and to implement our ATM design on the BASYS FPGA board.

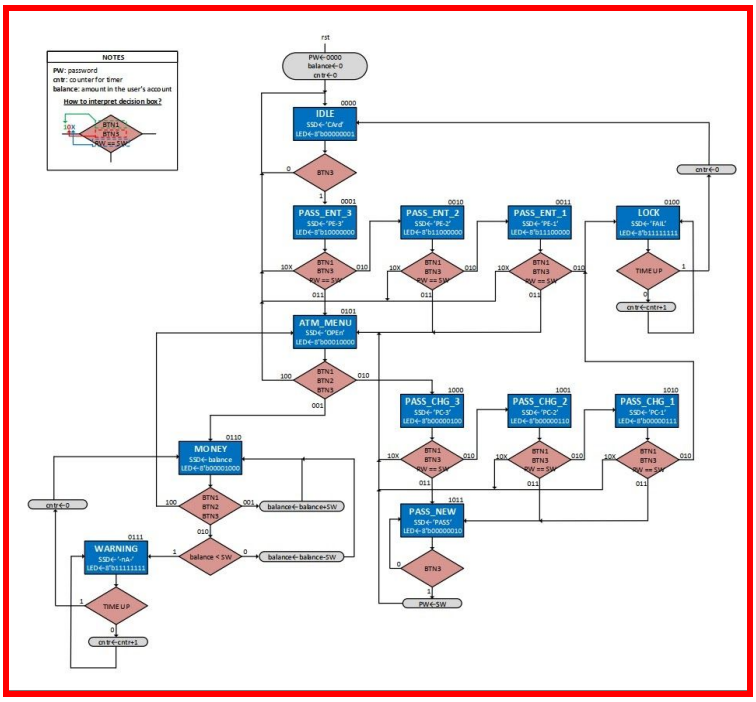
MATERIALS

- ISE design suite 14.7 (for programming verilog)
- BASYS FPGA BOARD



PROCEDURE

1. ASM chart of the assignment is created to understand
    - Inputs: rst, clk, BTN1, BTN2, BTN3, SW
    - States: ATM_MENU, IDLE, LOCK, MONEY, PASS_CHG_1, PASS_CHG_2, PASS_CHG_3, PASS_ENT_1, PASS_ENT_2, PASS_ENT_3, PASS_NEW, WARNING
    - Outputs LED's, SSD



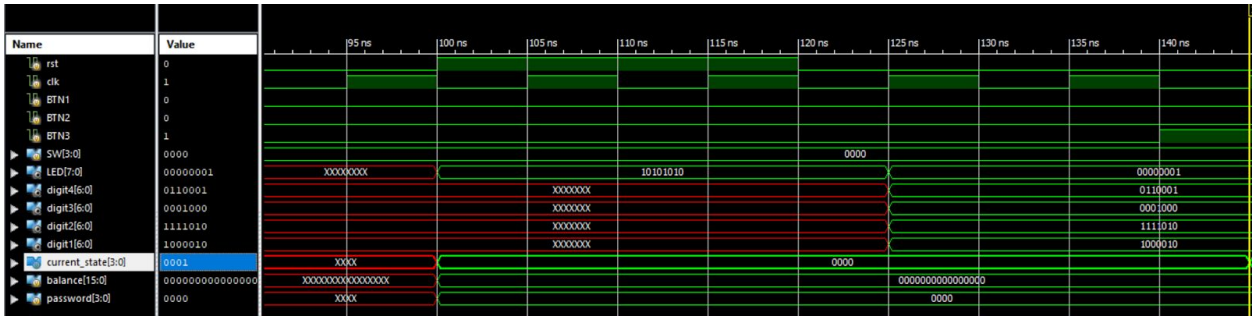
2. Project's "state transition" (atm_code.v) parts are implemented on verilog HDL with 3 always statement:
    - 1 sequential always statement for state transitions and
    - 1 combinatorial always statement for next state definitions.
    - 1 sequential always statement for locking our ATM for desired second according to related state.

3. Project's outputs are assigned another combinatorial always statement.(top_module.v and related givcn modules and pins.ucf file for implementing design on FPGA board)
    - 1 combinatorial always statement for FPGA outputs (LED's and SW)

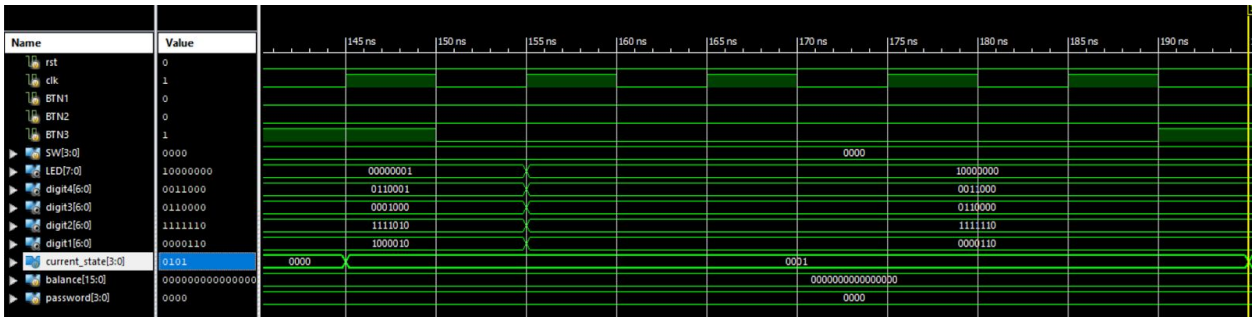
SIMULATION RESULTS

Simulation screenshots based on simulation scenario.

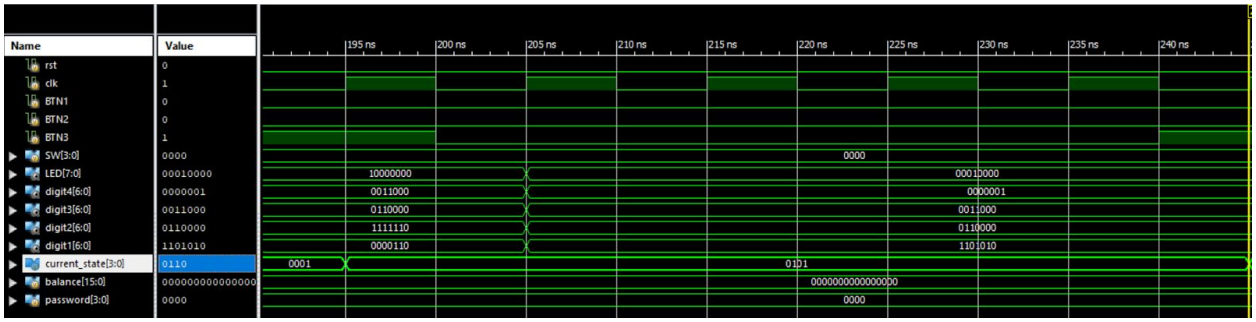
a.Reset Circuit



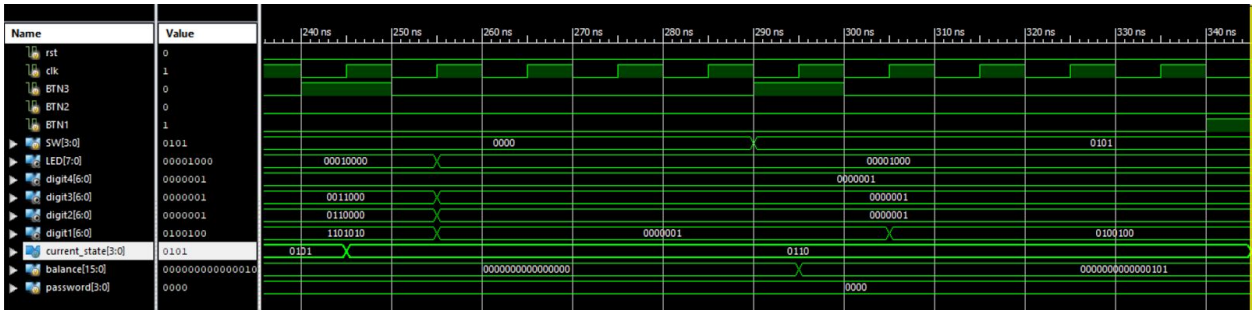
b.Inset the debit card by pressing BTN3



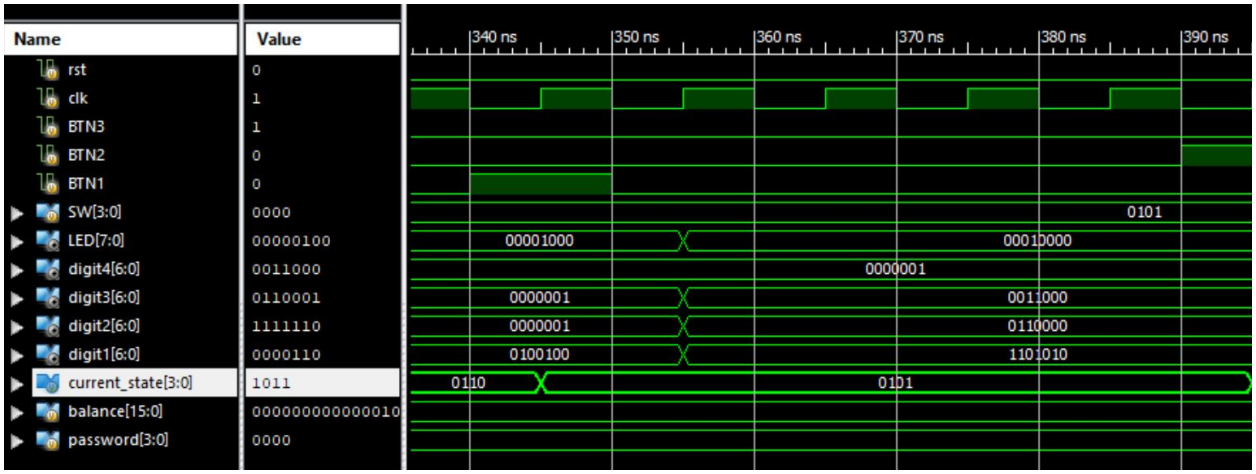
c.Enter the password correctly and go to the ATM menu state.



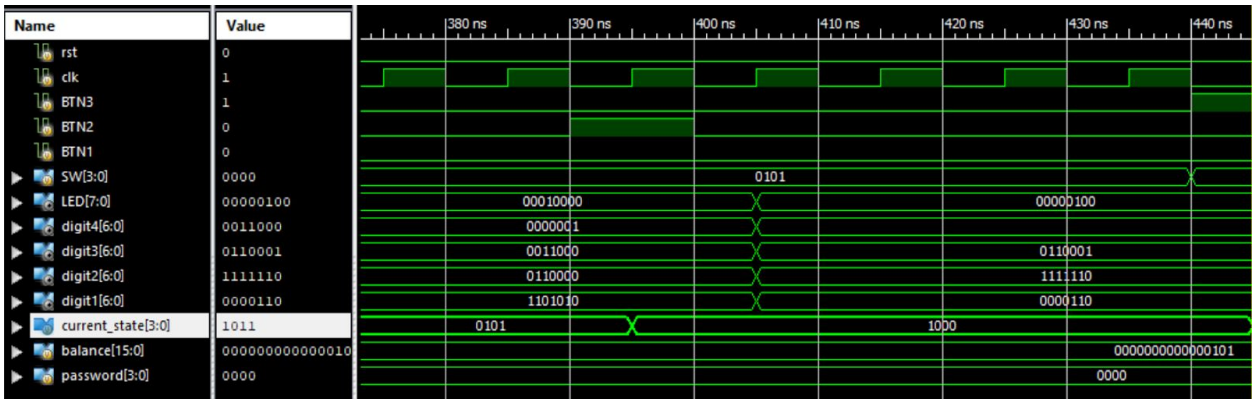
d.Go to the money operation state by pressing BTN3 AND e. Deposit 5 into your account



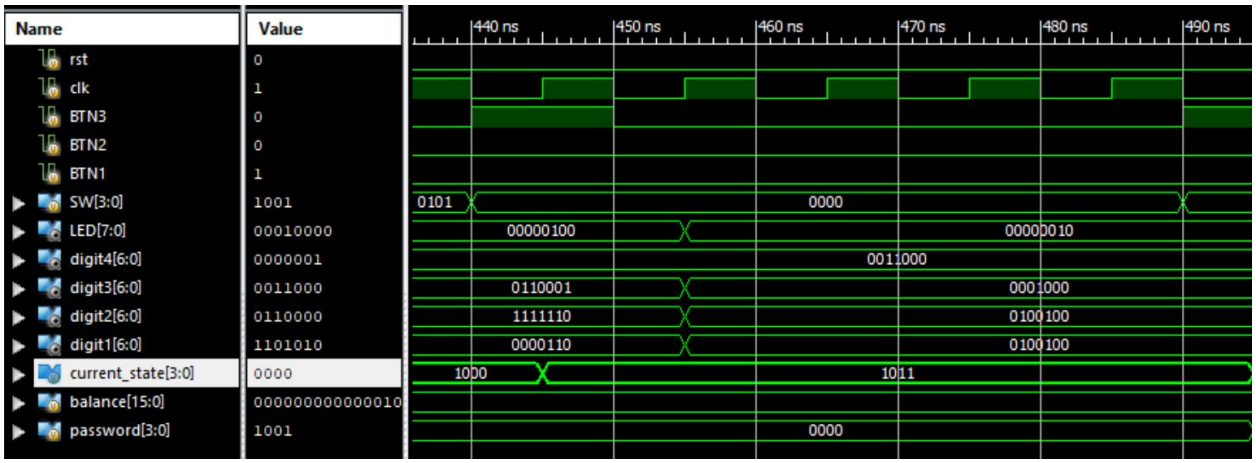
f.Go back to the ATM menu state by pressing BTN1



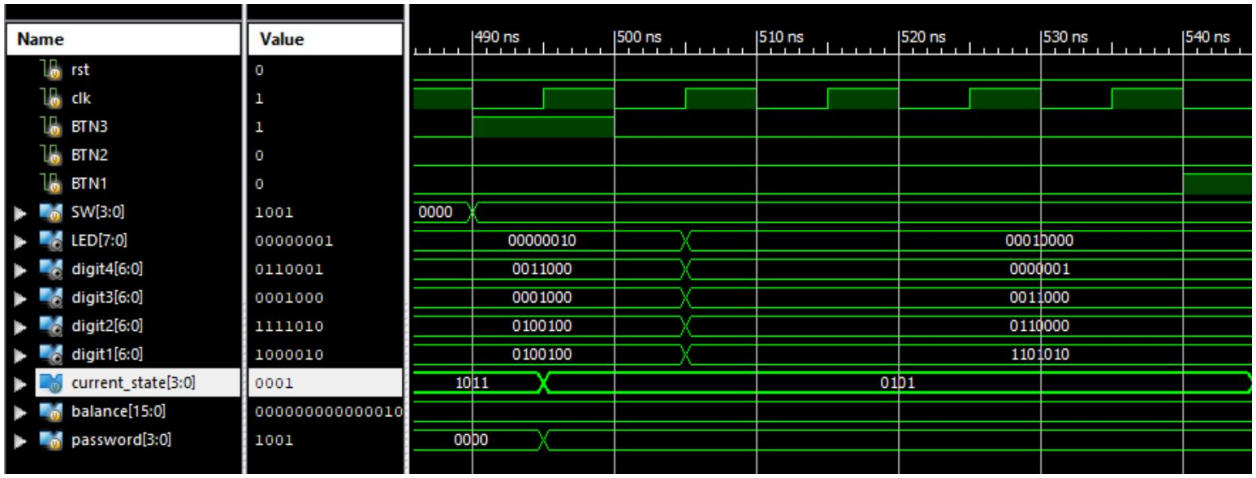
g. Go to password change state by pressing BTN2



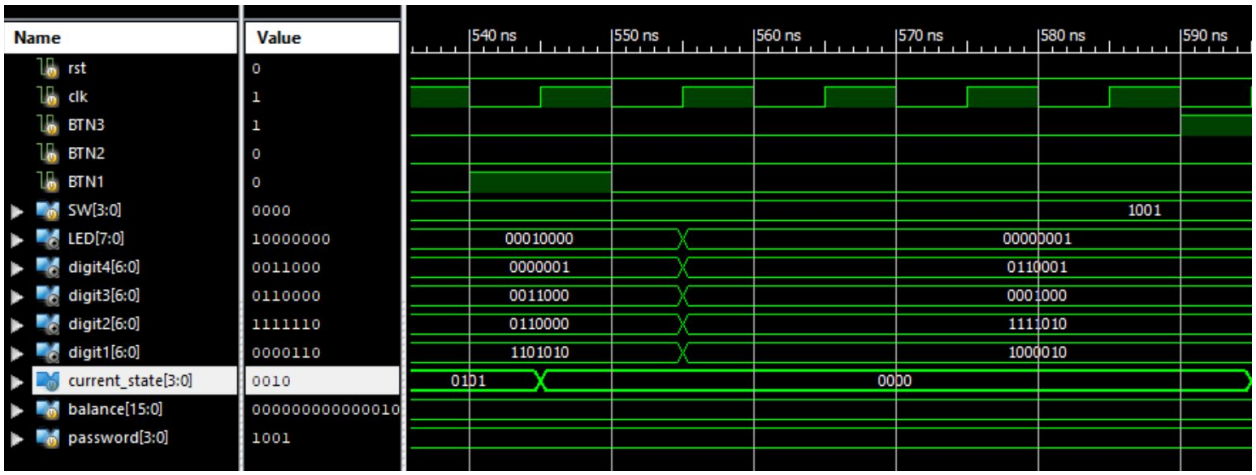
h.Enter your current password correctly



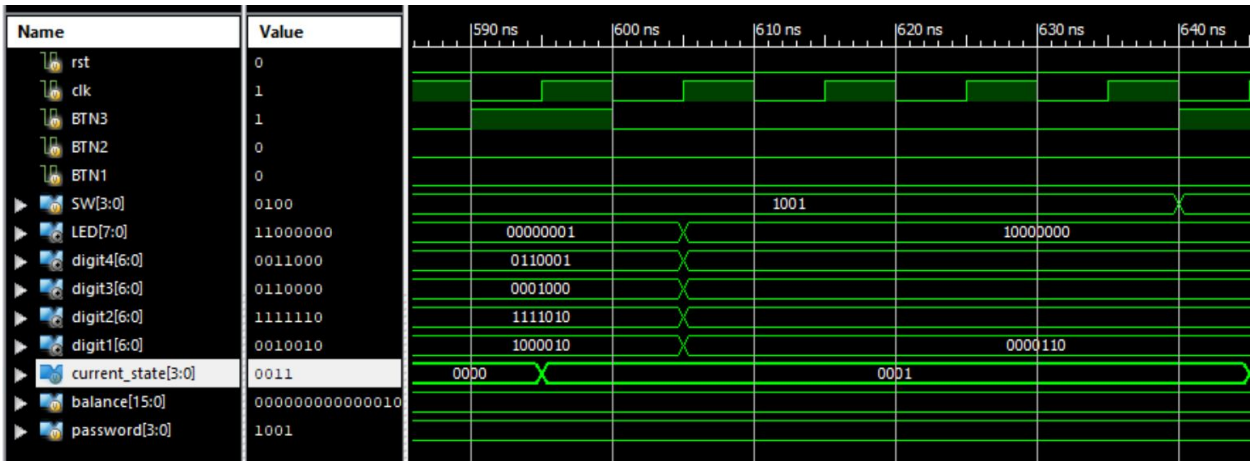
i.Enter the new password



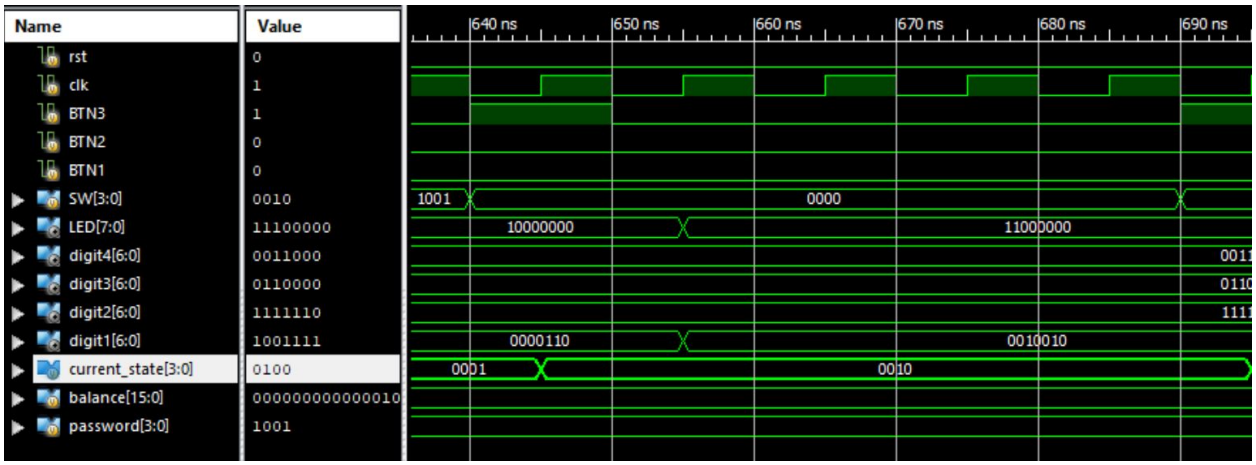
J. Log out from the ATM by pressing BTN1

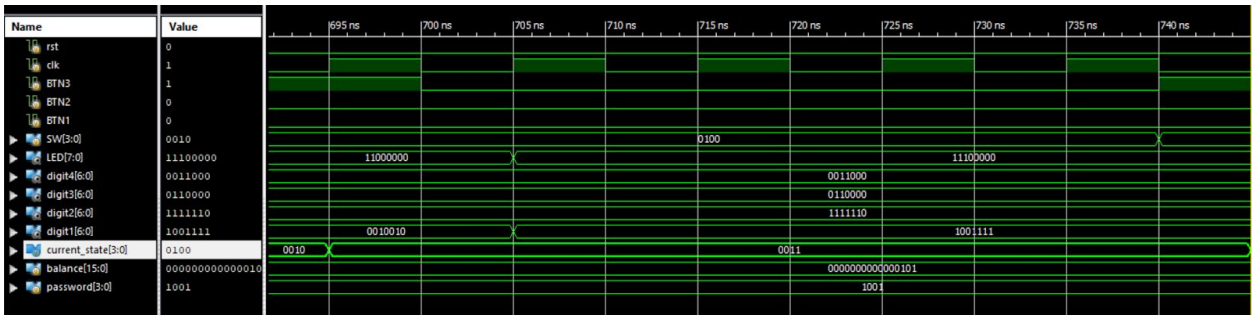


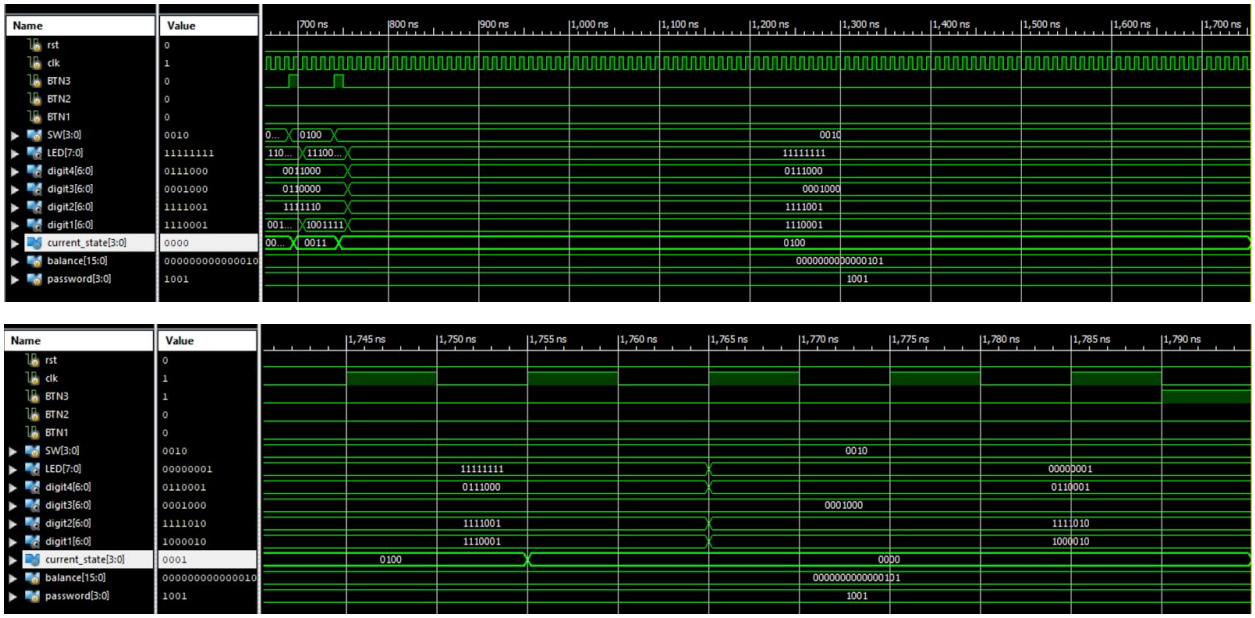
K. Inset the debit card by pressing BTN3



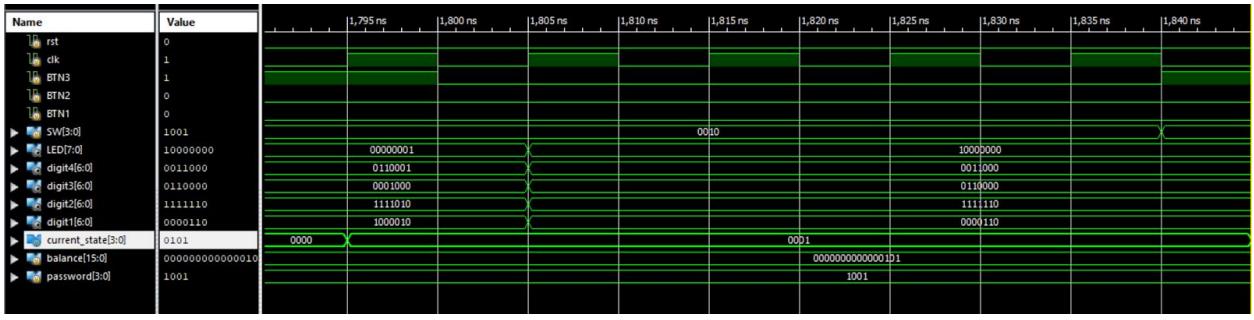
L. Enter the password wrong for 3 times



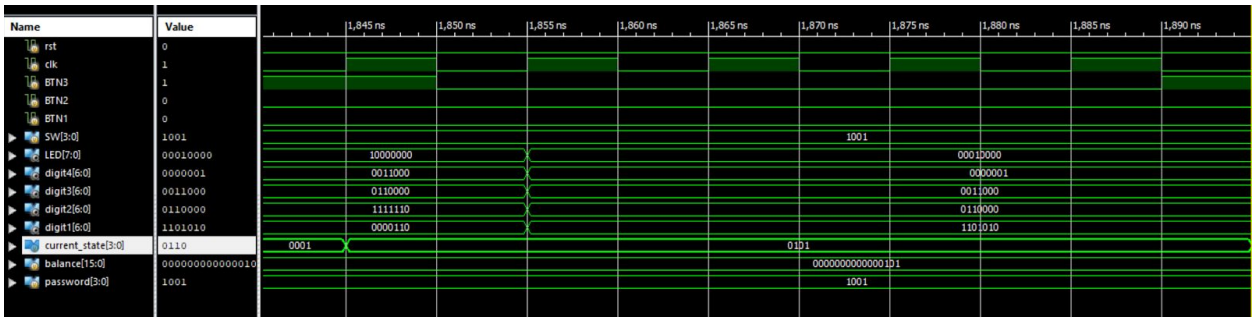




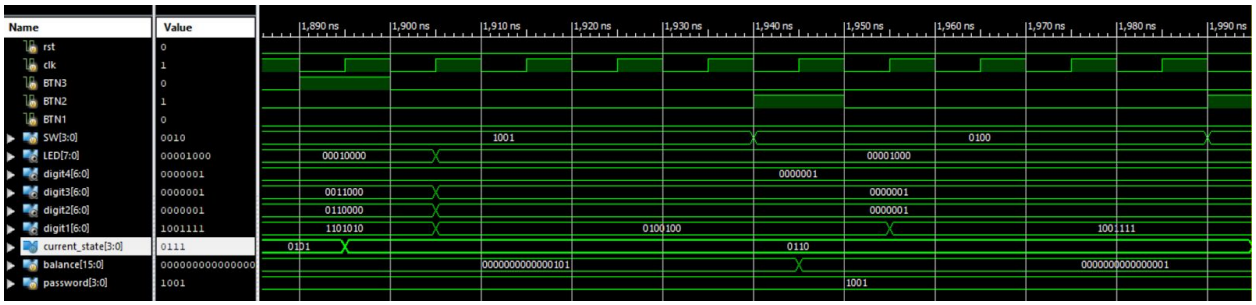
M. Inset the debit card by pressing BTN3



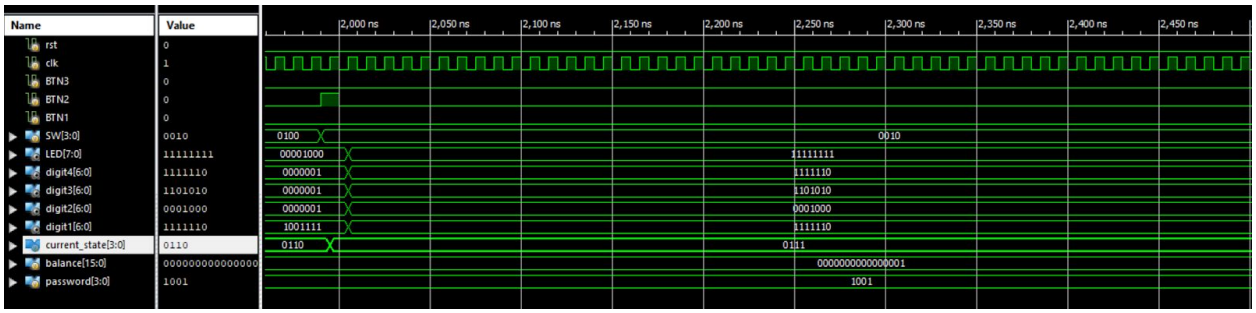
N.Enter the password correctly and go to the ATM menu state

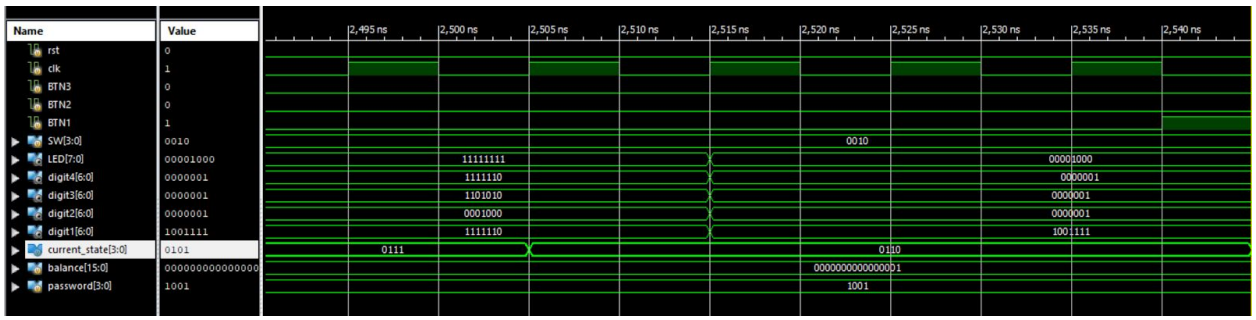


O. Go to the money operation state by pressing BTN3 AND P. Withdraw 4 from your account

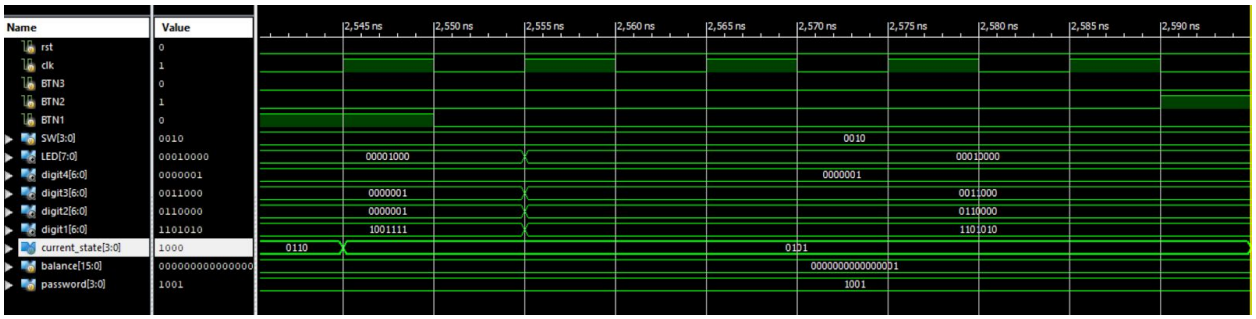


Q. Withdraw 2 from your account

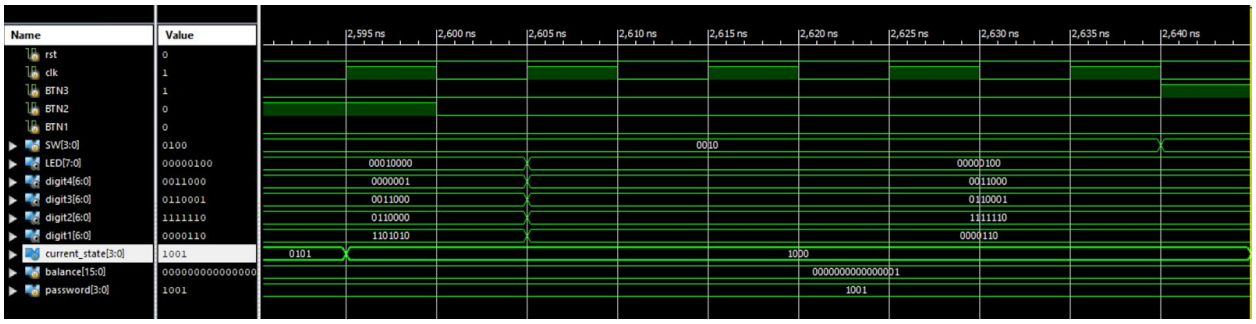




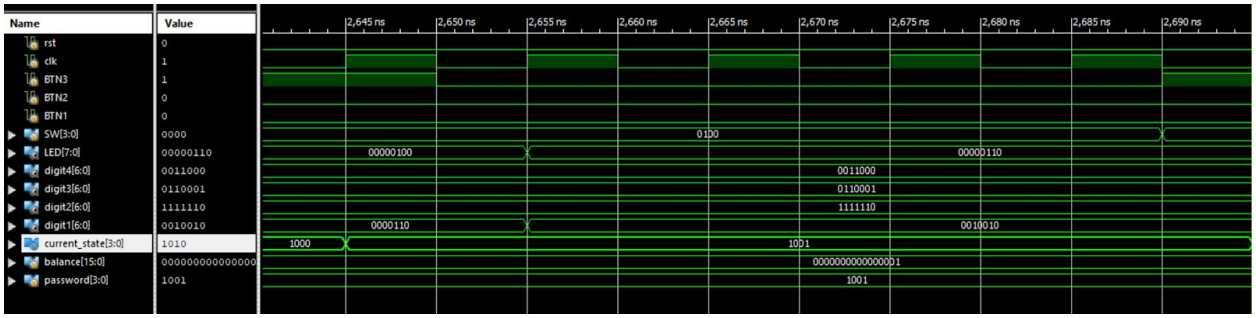
R.Go back to the ATM menu state by pressing BTN1

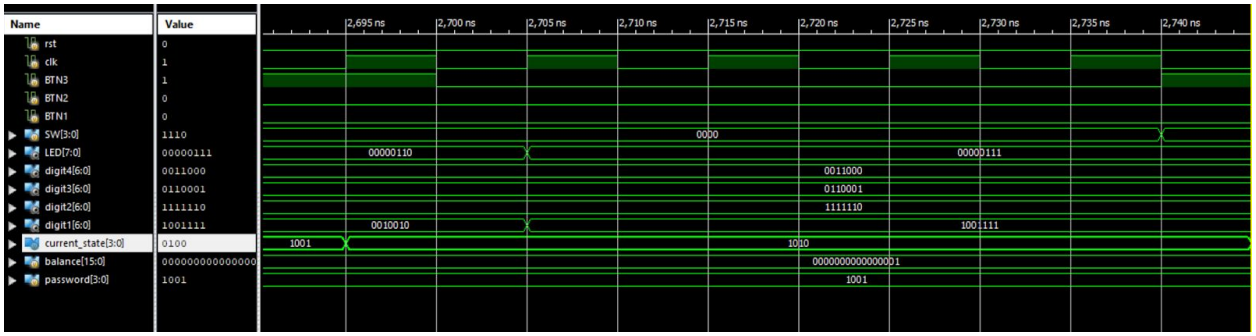


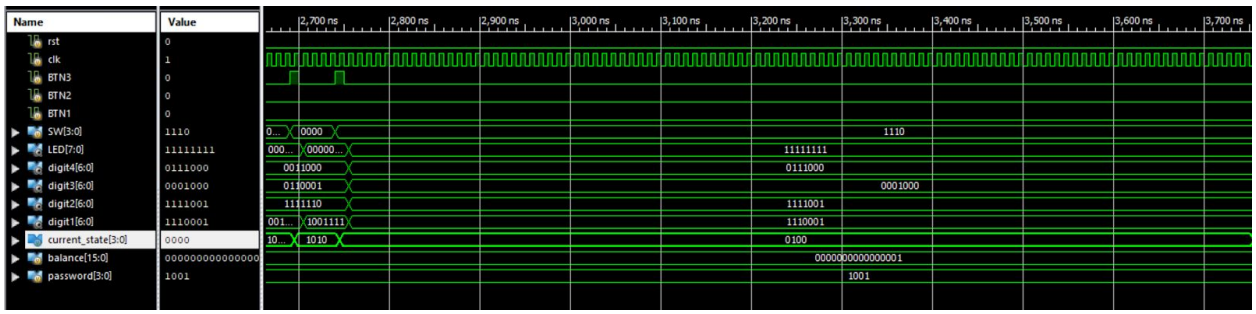
S. Go to the password change state by pressing BTN2

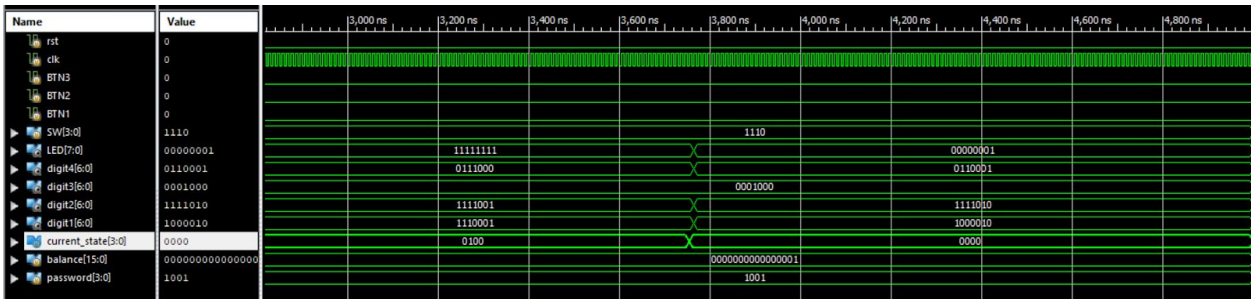


T. Enter a current password wrong for 3 times








Name
Value
rst
0
clk
0
BTN3
0
BTN2
0
BTN1
0
SW[3:0]
1110
LED[7:0]
00000001
digit4[6:0]
0110001
digit3[6:0]
0001000
digit2[6:0]
1111010
digit1[6:0]
1000010
current_state[3:0]
0000
balance[15:0]
0000000000000000
password[3:0]
1001
3,000 ns
3,200 ns
3,400 ns
3,600 ns
3,800 ns
4,000 ns
4,200 ns
4,400 ns
4,600 ns
4,800 ns
1110
11111111
00000001
0111000
0110001
0001000
1111001
1111010
1110001
1000010
0100
0000
0000000000000001
1001

IMPLEMENTATION DETAILS

FOR Synthesis

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	172	960	17%
Number of Slice Flip Flops	167	1920	8%
Number of 4 input LUTs	323	1920	16%
Number of bonded IOBs	28	108	25%
Number of GCLKs	2	24	8%

- Percentage of the utilized 4 input LUTs are 16% for synthesis

Clock information for synthesis

- Delay of the circuit is 17.608 ns which is assumed by the synthesis

FOR Implementation

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	167	1,920	8%	
Number of 4 input LUTs	250	1,920	13%	
Number of occupied Slices	182	960	18%	
Number of Slices containing only related logic	182	182	100%	
Number of Slices containing unrelated logic	0	182	0%	
Total Number of 4 input LUTs	321	1,920	16%	
Number used as logic	250			
Number used as a route-thru	71			
Number of bonded IOBs	28	108	25%	
Number of BUFGMUXs	2	24	8%	
Average Fanout of Non-Clock Nets	3.28			

- Percentage of the utilized 4 input LUTs are 16% for implementation

Clock information for implementation

- Delay of the circuit is 18.809 ns which is assumed by the implementation