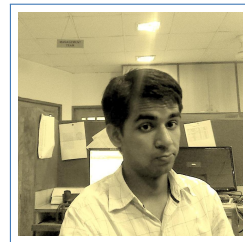


Dilawar Singh

Curriculum Vitae

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Info

Born June 5th, 1985 at Nichalpur (India)
Home Nichalpur, Bugwara, Bijnor, U.P. - 246745
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Academic Background

- 2014- **Ph. D.**, NCBS Bangalore.
Modelling memory across scale, PI: Prof. Upinder Bhalla
- 2010-2013 **Ph. D.**, IIT Bombay, withdrawn.
VLSI CAD, Thesis advisor: Prof. Sachin Patkar
- 2007-2009 **M. Tech.**, IIT Bombay, Microelectronics and VLSI.
My thesis project was on **fabrication of micro-electrode arrays for retinal prosthesis**. Thesis advisor: Prof. Dinesh K. Sharma.
- 2003-2007 **B. Tech.**, Dr. MGR ERI, Chennai.
Instrumentation and Control Engineering

Publications

- 2018 Dilawar Singh e Upinder Singh Bhalla. "Subunit exchange enhances information retention by CaMKII in dendritic spines". In: *eLife* 7. DOI: 10.7554/eLife.41412. URL: <https://doi.org/10.7554/eLife.41412>.
- 2013 P. Saxena et al. "Hardware-software scalable architectures for Gaussian elimination over GF(2) and higher galois fields". In: *PECCS 2013 - Proceedings of the 3rd International Conference on Pervasive Embedded Computing and Communication Systems*, pp. 195–201.
- 2012 D. Singh. "Self-reliance of Indian intellectuals". In: *Economic and Political Weekly* 47.39, pp. 4–5.

Work Experience

- 2013-2014 **Research Fellow**, NCBS Bangalore.
MOOSE Simulator, PI: Prof. Upinder Bhalla
- 2009-2010 **Design Engineer**, Kritical Solutions Noida.
Embedded systems/Firmware development Development of firmware for movie-cameras on DINI board with RTOS Multi. Image stabilization using Kalman filtering. Maintenance of version control system and servers hosted on Solaris OS.

Skills

Languages C/C++, Python, Haskell, VHDL/Verilog/Bluespec, SQL, PHP, Lua, L^AT_EX
CAD Tools KiCAD, Cadence, Xilinx and Altera tools, Ngspice