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HW2 Report

For this homework, I followed the website for the setup of the simulator.
https://www.gem5.org/documentation/learning_gem5/part1/building/

I used this website for matrix multiplication:

https://learn.drukinfotech.com/matrix-multiplication-using-text-file-in-c/

I used this website for random matrix generation:

https://mxncalc.com/matrix-generator

From original website, I downloaded all the required dependencies with:

```
sudo apt install build-essential git m4 scons zlib1g zlib1g-dev libprotobuf-dev
protobuf-compiler libprotoc-dev libgoogle-perftools-dev python-dev python
```

Then, I cloned the gem5 repository:

```
git clone https://gem5.googlesource.com/public/gem5
```

After that, in order to build first gem5, I compiled this line which took over 2 hours to be done:

```
cd gem5
```

```
scons build/X86/gem5.opt -j2
```

Here, -j2 represents the number of CPUs of the virtual machine ubuntu.

Questions:

- Which files in the simulator you mainly changed?

I added the c files and text files of matrices to the simulator. However, even though the matrix_mul.c was working correctly to get output from gem5, I added x86 files to the simulator as well.

```
gcc -static -o matrix_mul.x86 matrix_mul.c
```

I added this static file (matrix_mul.x86) to the gem5.

- What is the main code you added into the simulator (not all the lines, just your main change is enough)

I added matrix_mul.x86 to the file: tests/test-progs/hello/bin/x86.

Also, I changed a line from a file which has path of /home/ubu/gem5/configs/learning_gem5/part1.

The line (63) from two_level.py was:

"tests/test-progs/hello/bin/x86/linux/hello " instead of hello I wrote matrix_mul. Otherwise, the simulator had error saying wrong path.

I changed the L1 cache size in l1d & l1i. Then I changed the cache block size as cacheline_size from the below command:

```
build/X86/gem5.opt configs/example/se.py --cmd=tests/test-progs/hello/bin/x86/linux/matrix_mul.x86 --cpu-type=TimingSimpleCPU --caches --l1d_size=64kB --l1i_size=64kB --cacheline_size=8
```

- Table showing the L1 hit rate for different block sizes for the L1 data cache.

Hit rate = overall hit / (overall hit / overall miss)

L1 Cache Size	Hit Rate (Instruction Cache)	Hit Rate (Data Cache)
1B	Error	Error
2B	Error	Error
4B	Error	Error
8B	0.99718071	0.9946280881
16B	0.998494633	0.9969771311
32B	0.9991309894	0.9983112843
64B	0.9994723605	0.9990199333
128B	0.9996696006	0.9994303374
256B	0.9997869148	0.9994299513
512B	0.9998318512	0.9997822529

If the L1 cache size is 1B or 2B, I got the warning saying the block size must be at least 4 and a power of 2.

> *warn: The `get_runtime_isa` function is deprecated. Please migrate away from using this function.*
>
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>
> *Global frequency set at 1000000000000 ticks per second*
>
> *warn: No dot file generated. Please install pydot to generate the dot file and pdf.*
>
> *build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)*
>
> *build/X86/sim/system.cc:196: warn: Cache line size is neither 16, 32, 64 nor 128 bytes.*
>
> *build/X86/mem/cache/tags/base_set_assoc.cc:65: fatal: Block size must be at least 4 and a power of 2*

If the L1 cache size 4B, I got the warning saying that cache line size is neither 16,32,64 nor 128 bytes.

> *warn: The `get_runtime_isa` function is deprecated. Please migrate away from using this function.*
>
> *warn: The `get_runtime_isa` function is deprecated. Please migrate away from using this function.*

Global frequency set at 1000000000000 ticks per second

warn: No dot file generated. Please install pydot to generate the dot file and pdf.

build/X86/mem/dram_interface.cc:690: warn: DRAM device capacity (8192 Mbytes) does not match the address range assigned (512 Mbytes)

build/X86/sim/system.cc:196: warn: Cache line size is neither 16, 32, 64 nor 128 bytes.

Details:

8b

instruction => hit 1375890, miss = 3840

data => hit 443998, miss = 2398

16b

instruction => hit 1377653, miss 2077

data => hit 444586, miss 1348

32b

instruction => hit 1378531, miss 1199

data => hit 445148, miss 753

64b

instruction => hit 1379002, miss 728

data => hit 445451, miss 437

128 b

instruction=> hit 1379274, miss 456

data => hit 445624, miss 254

256 b

instruction=> hit 1379436, miss 294

data => hit 445322, miss 151

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512b

instruction => hit 1379498, miss 232

data => hit 445374, miss 97

- Graph showing the changes in the hit rate according to the block size for L1 data cache.