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Evaluating SpTRSV Design Performance for FPGAs

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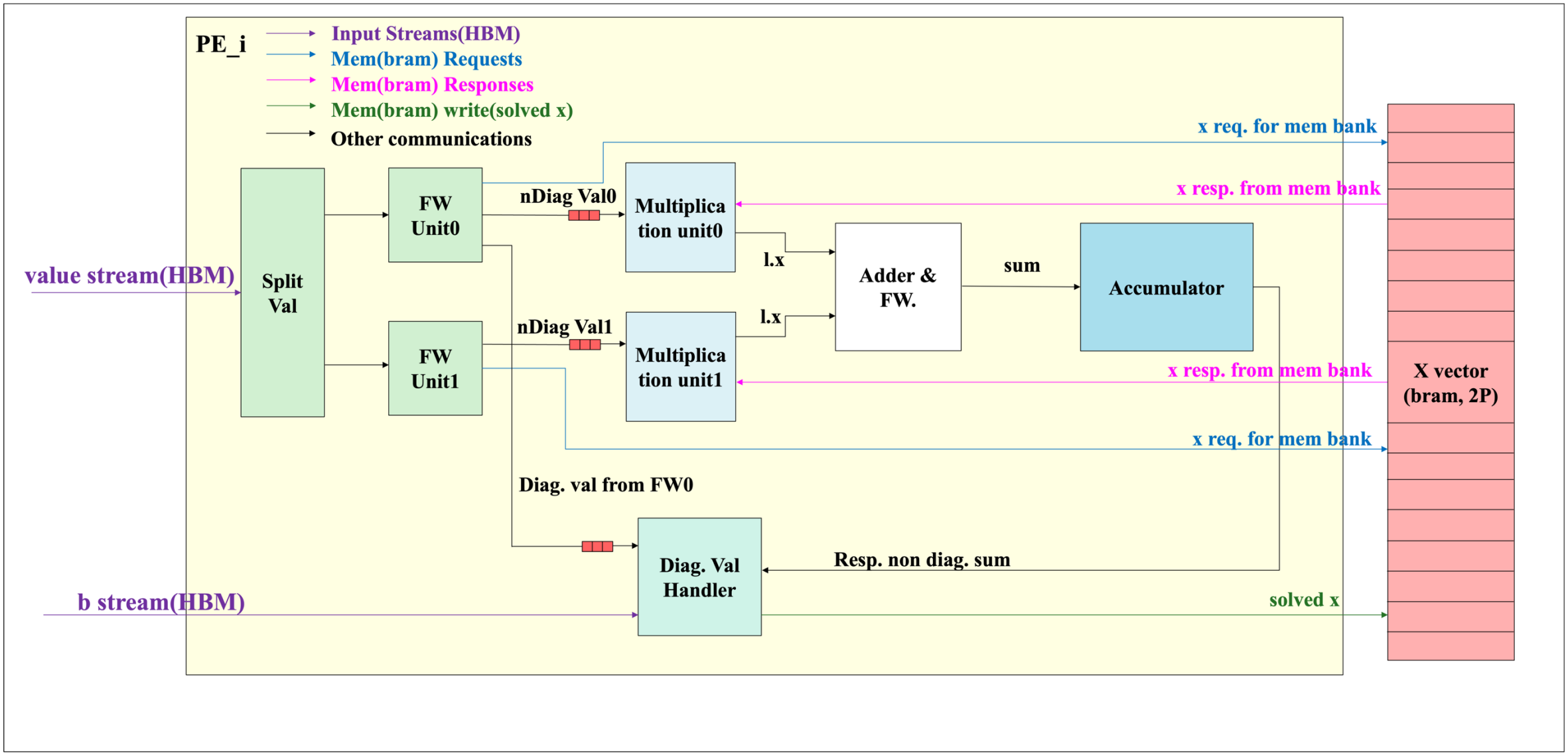
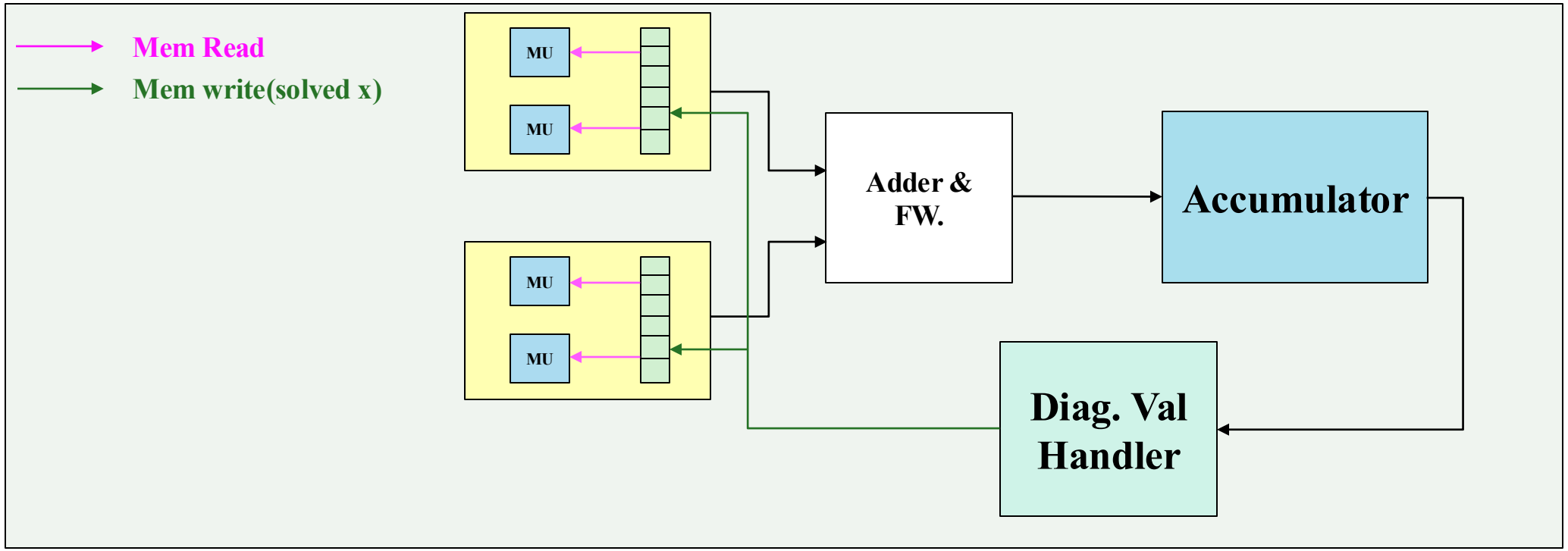
PE architecture (example for 2 multiplication units design)



A PE group (PEG)

- A PE Group
  - Has a multiple multiplication units.
  - Has an X vector bank for each 2 multiplication units (duplicates)
  - Share the adder & FW unit, accumulator and Diag. Val Handler

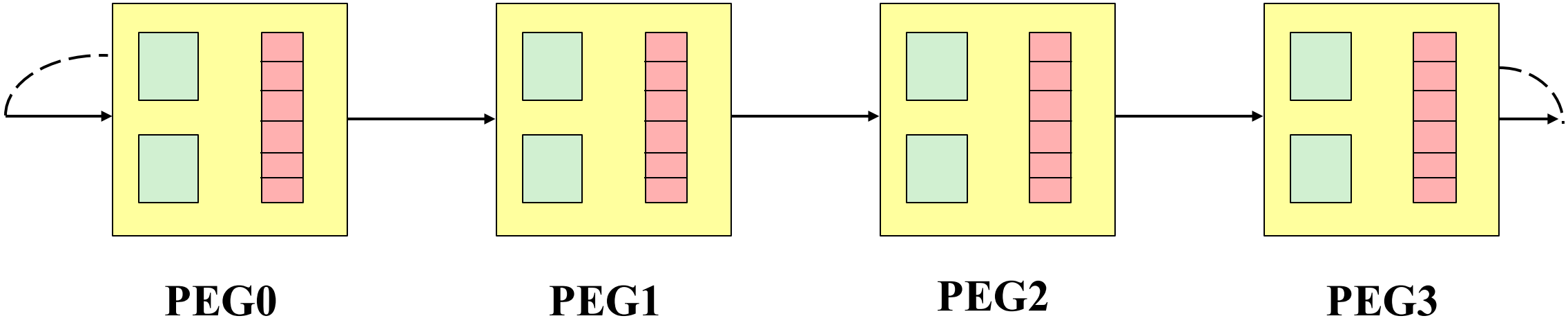


Chain broadcasting solved X among PEGs

SFU

- A value solved by one PE group might required by another PE to solve another row. Therefore, solved x value sharing is needed.

- A chain broadcasting mechanism is used to share data among different PE groups.

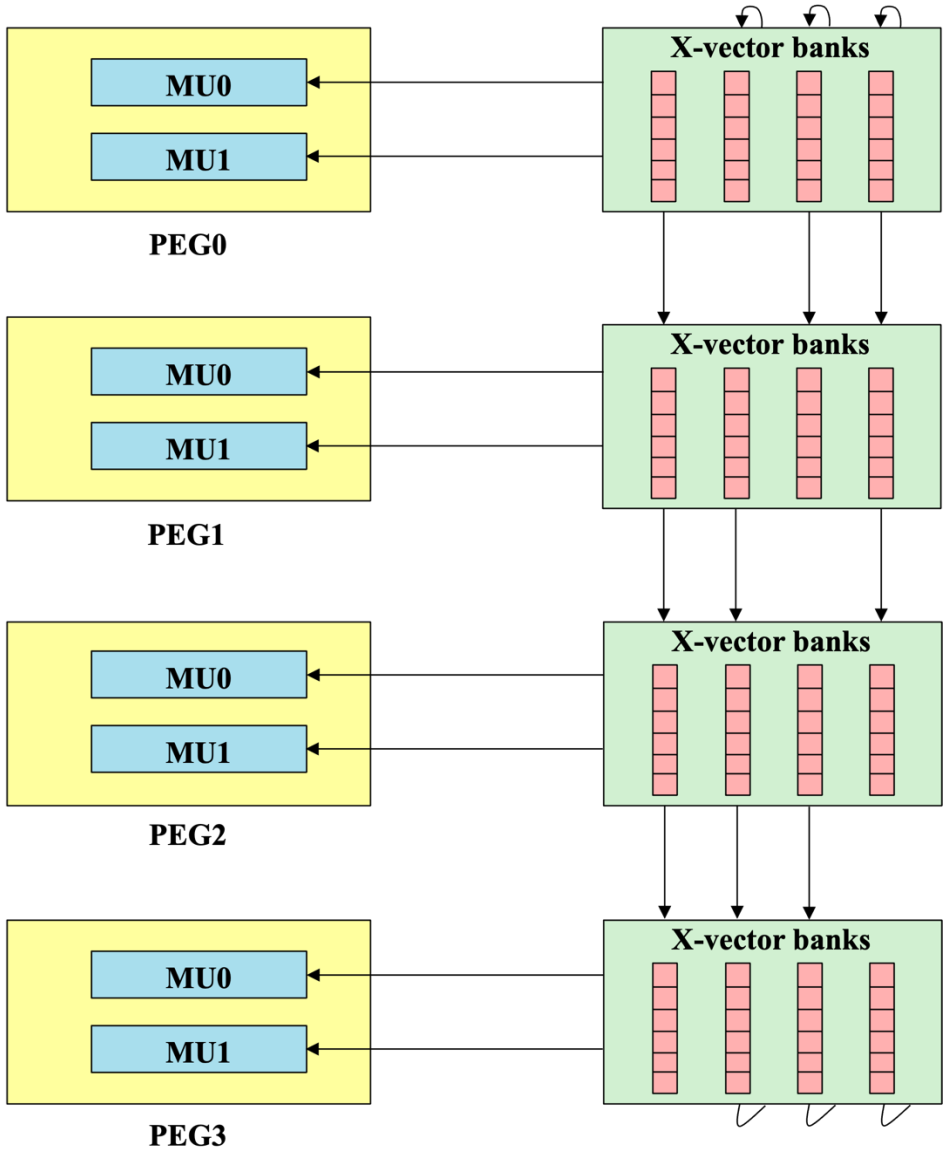


Chain broadcasting with X vector partitioning – 4 PEG example

SFU

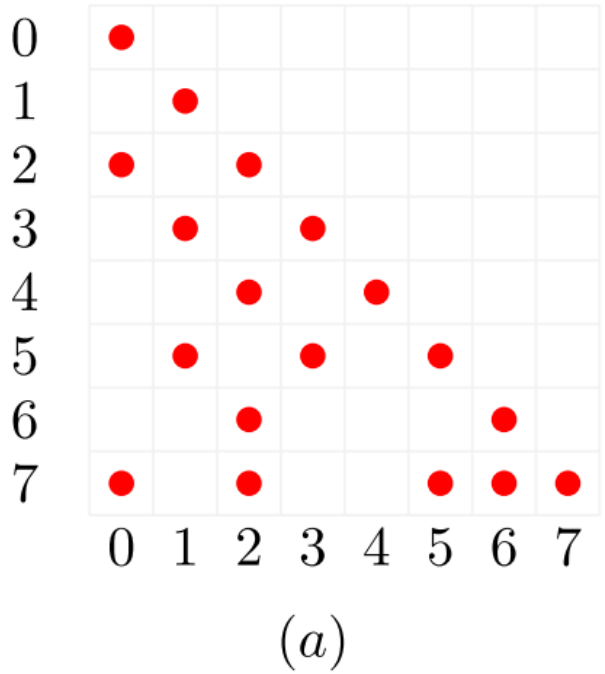
- We asses the impact of partitioning.
- Number of x partitions = # PE Groups
  - i.e., Each PE Group has its own bank to write. Therefore, no write waiting bubbles.
- Multiplication units have access to cyclic access to memory banks.
  - i.e.,

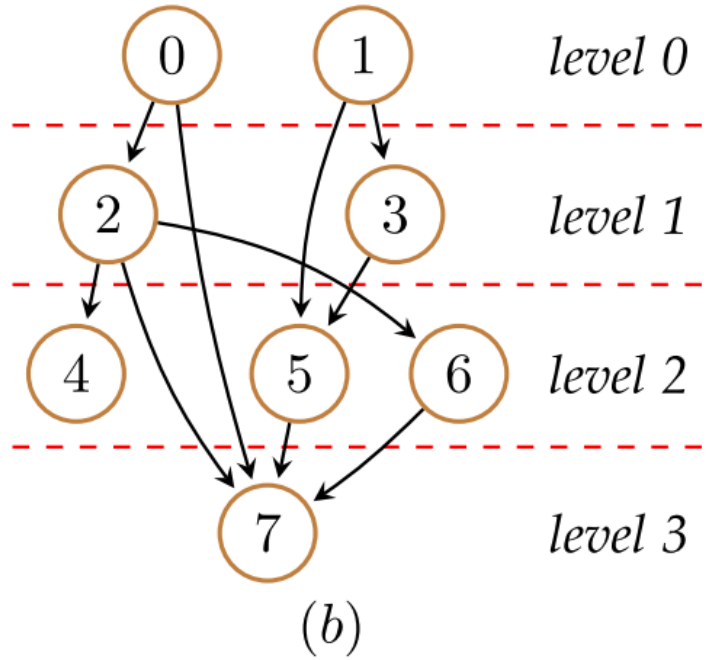
  MU 0 has access to partitions 0, 2
  MU 1 has access to partitions 1, 3
  - This leads to imbalance in data streams.



Level set row scheduling

- We send data according to the level set of the input matrix.
- Rows within a level can be calculated parallelly.
  - All their dependencies are solved and available in memory banks.
- There is a synchronization barrier among levels.



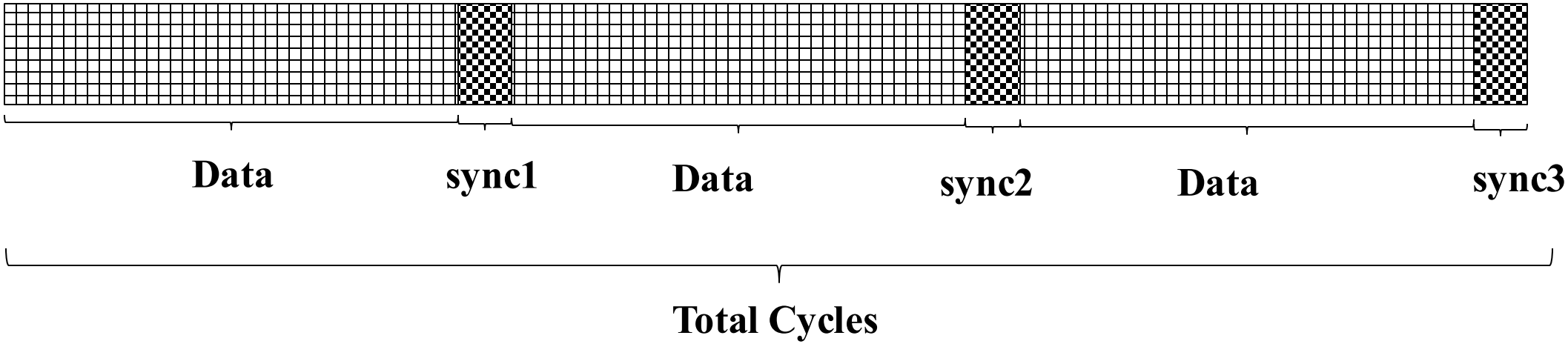


Synchronization time = Time for the last row to be solved (Pipeline depth) + Time to update memory banks in all the PE Groups (#PE groups -1)

- We built an analytical model to calculate the time estimations.

Definitions – synchronization cost

- Synchronization cost



$$\text{Sync cost} = \text{sync1} + \text{sync2} + \text{sync3}$$

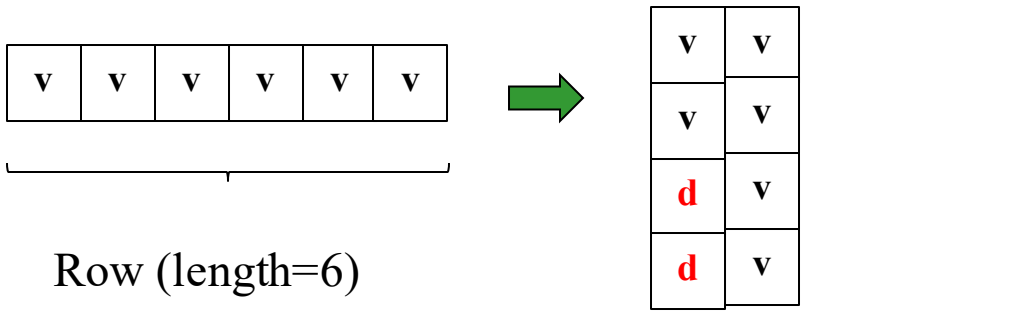
$$\text{Sync cost percentage} = \frac{sync\ cost}{Total\ Length}$$

Definitions – dummy data

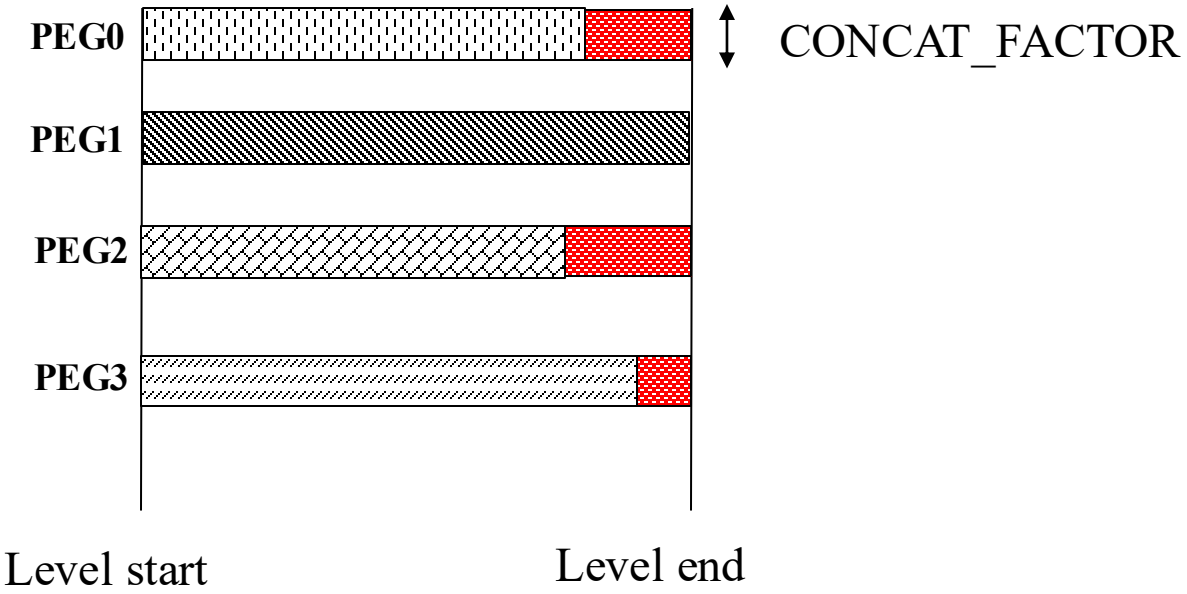
- Dummy data
  - Imbalanced row
  - Imbalanced PEs

- CONCAT_FACTOR = Number of MUs in a PE Group

- Imbalanced row

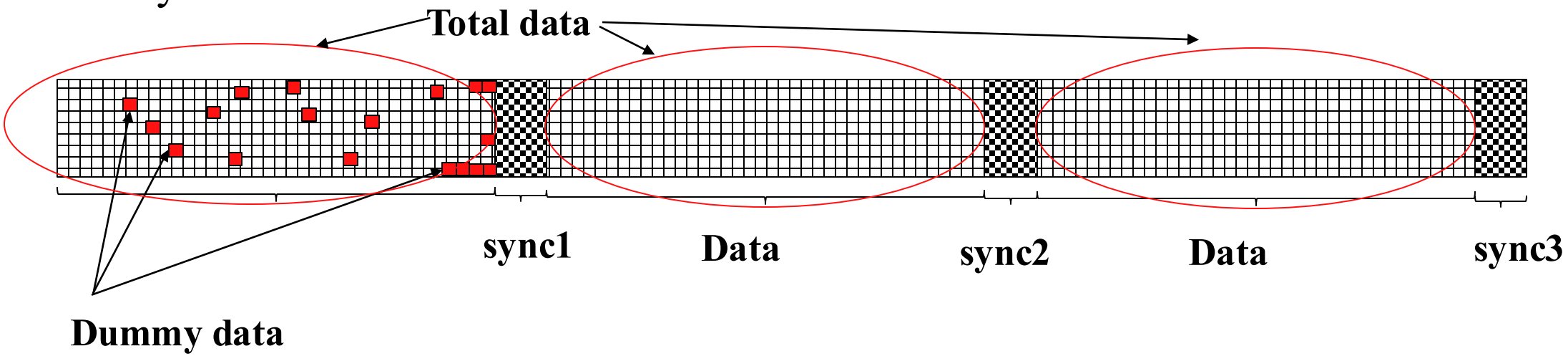


- Imbalanced PEs



Definitions – dummy data

- Dummy data

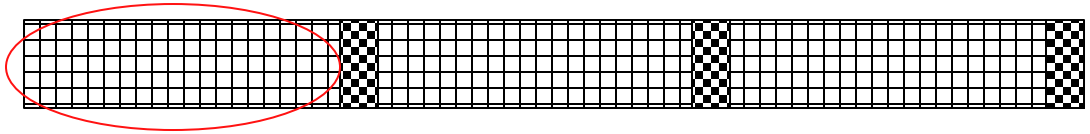


$$\text{Total dummy data} = (\text{Imbalanced row}) + (\text{Imbalanced PE})$$

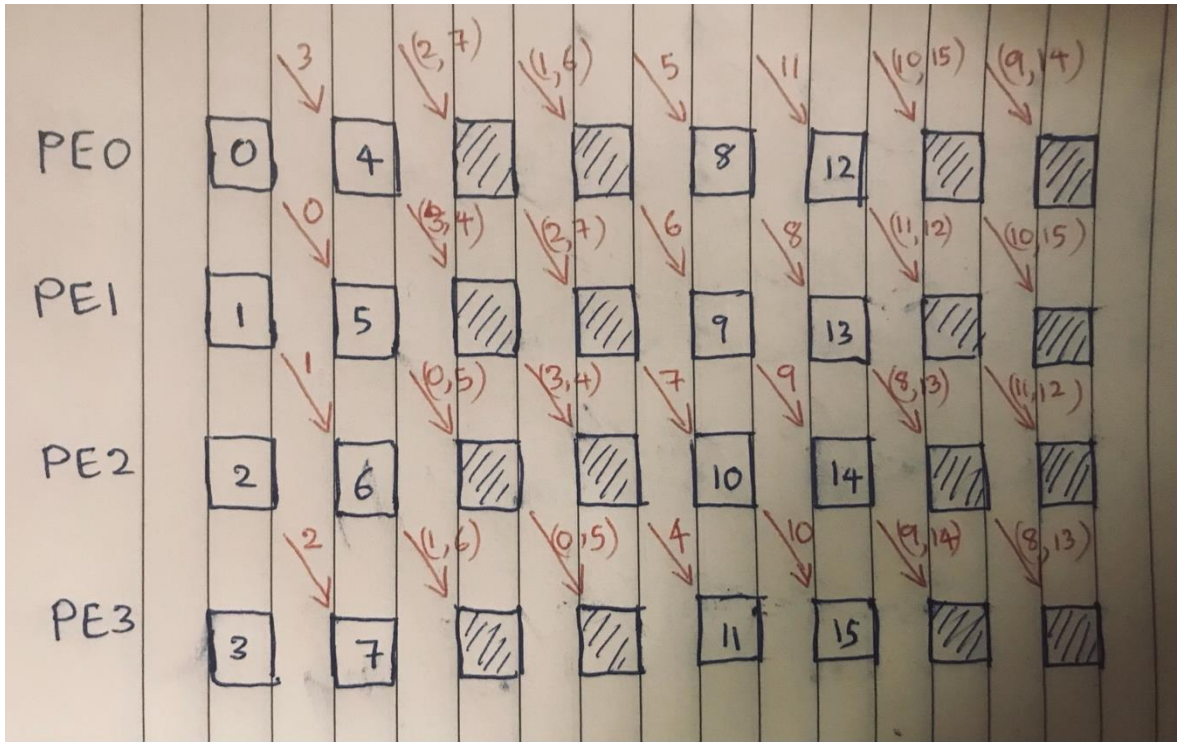
$$\text{Dummy data percentage} = \frac{Total\ dummy\ data}{Total\ data}$$

Definitions – pipeline bubbles

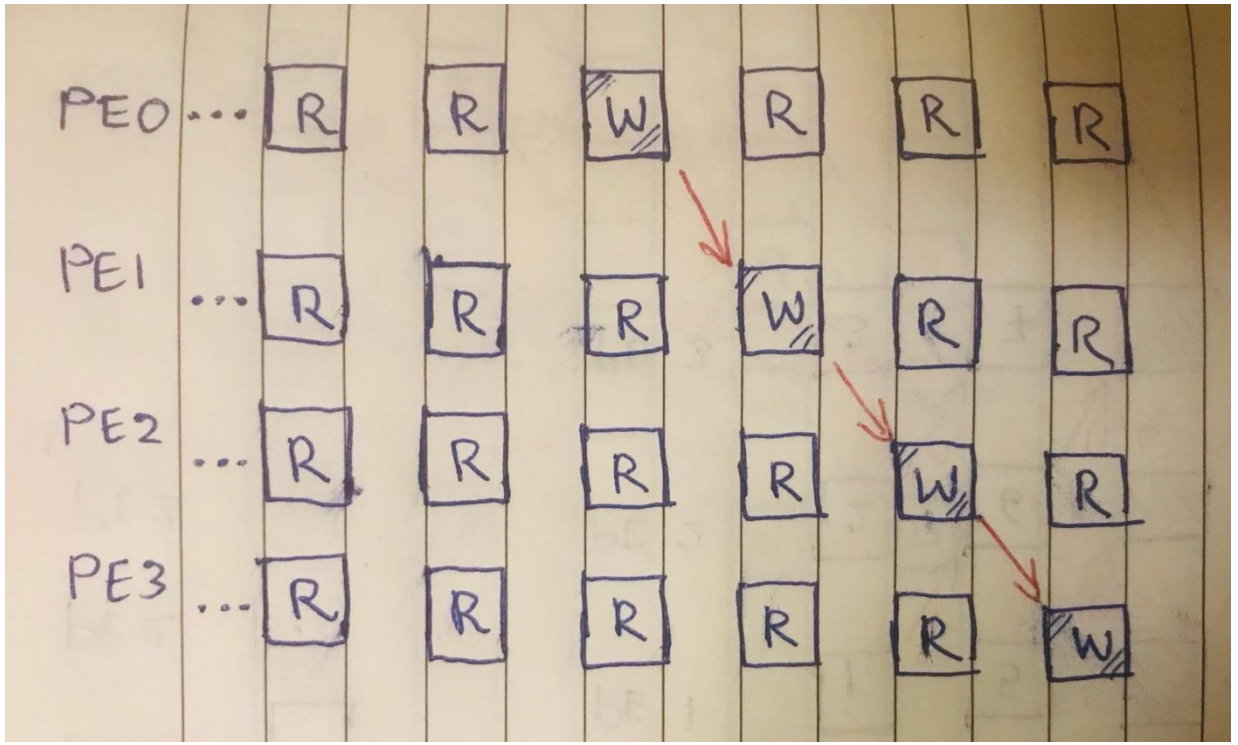
- Bubbles within a level



- Write-write conflicts

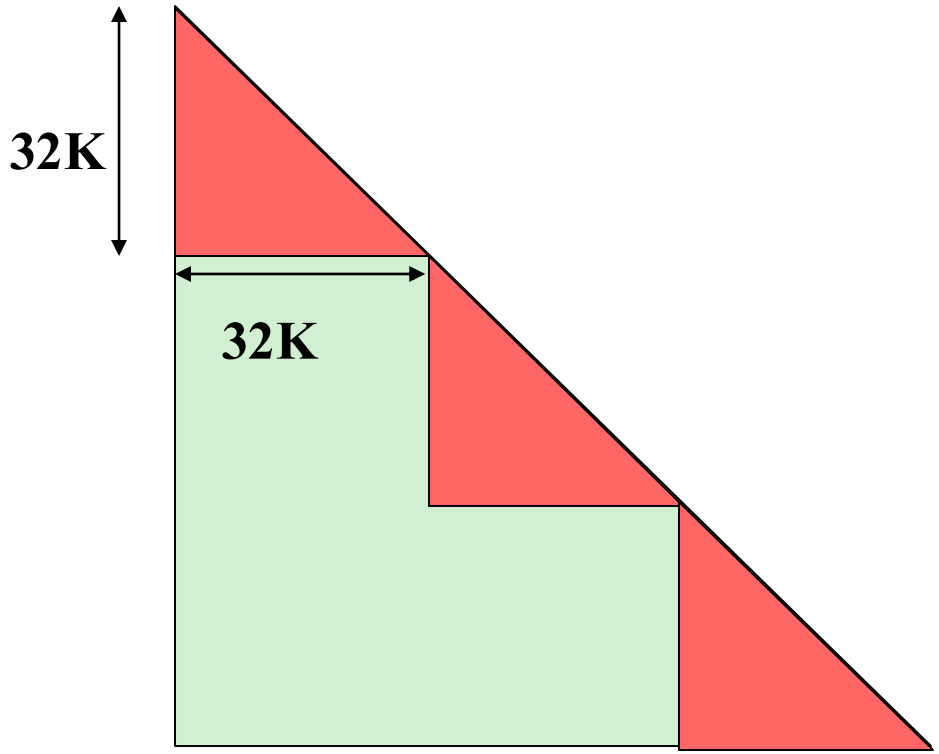


- Write-read conflicts

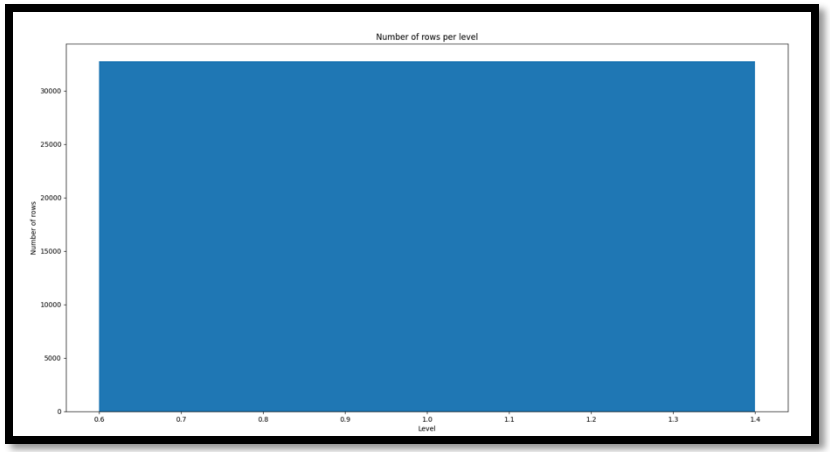


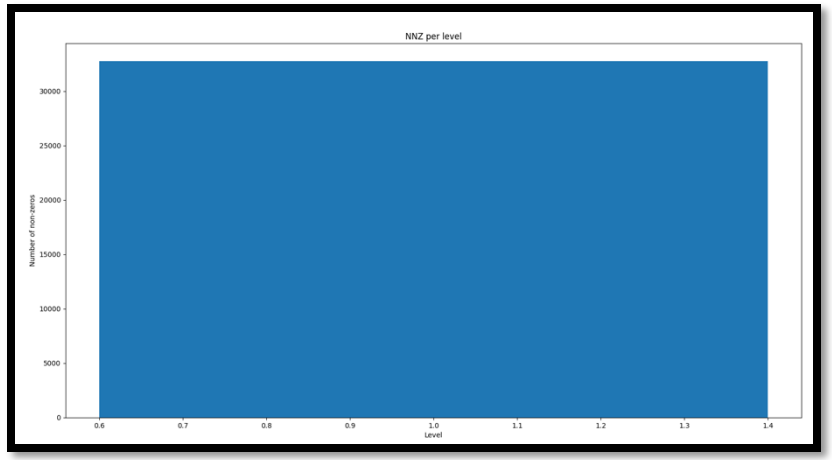
HW configuration

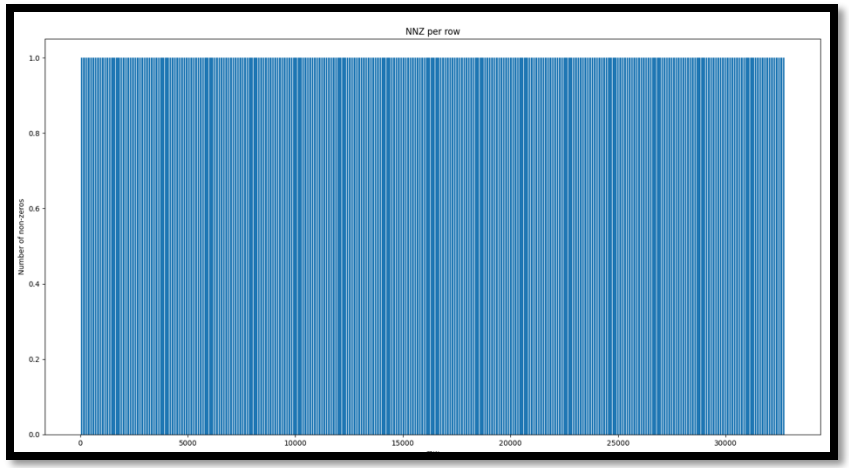
- CONCAT_FACTOR = # MUs in a PE Group = 4
- Number of PE Groups = 48
- Required HBM ports = 24
- Calculate time only for the 1st tile (size of 32K x 32K) using SpTRSV performance analysis model



parabolic_fem



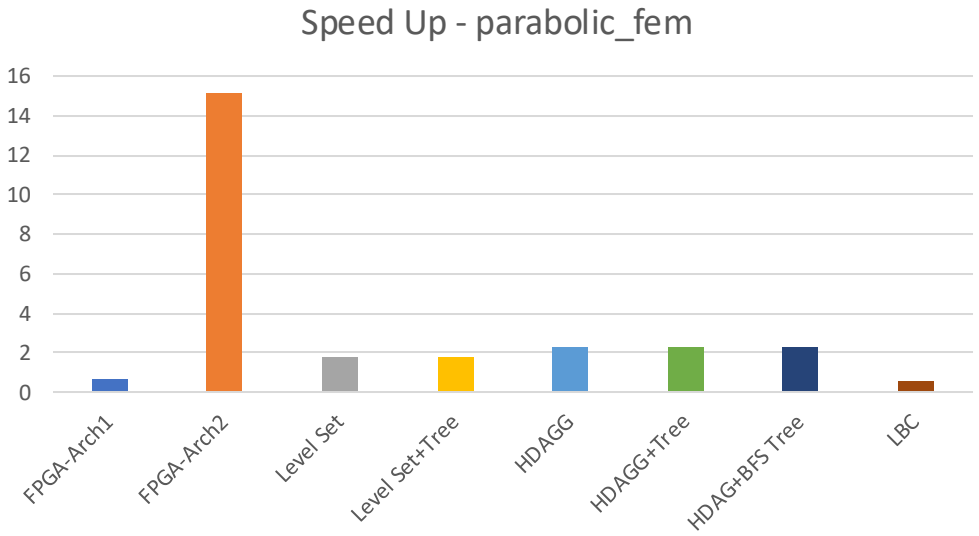




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=32768

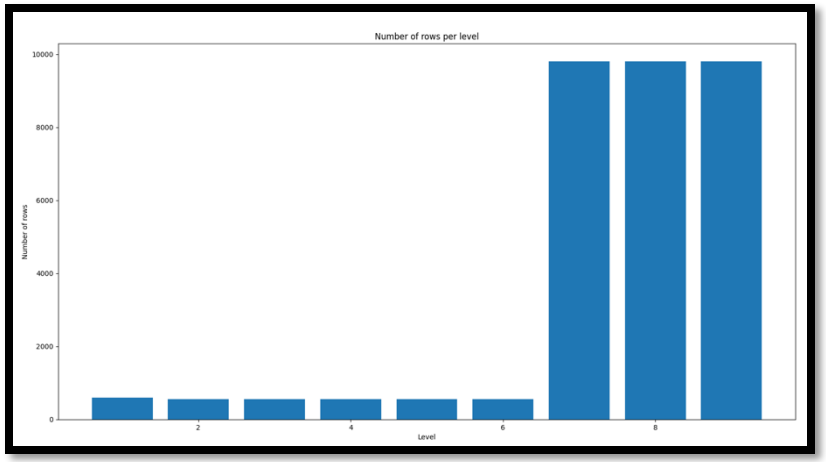
- **Number of levels=1**
  - The largest level=1, **The largest level size=32768**
  - The smallest level=1, **The smallest level size=32768**

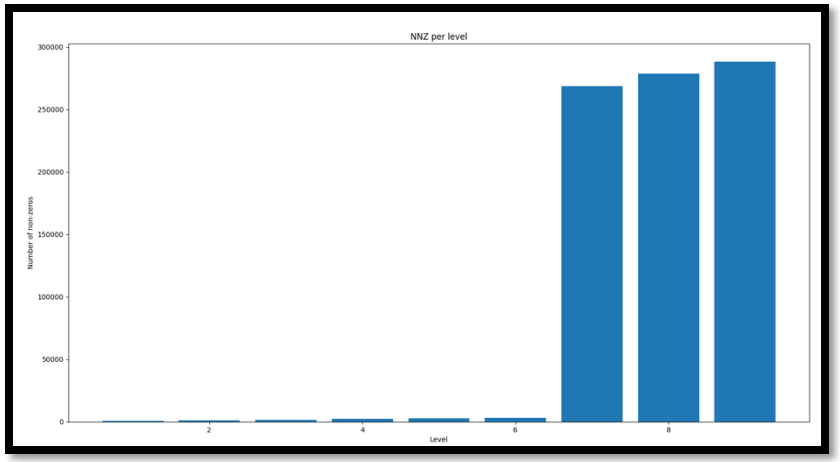
Feature	**Arch 1**	**Arch 2**
Dummy data percentage	75.01% (Row-74.96%, PE-0.05%)	75.01% (Row-74.96%, PE-0.05%)
Bubbles	15686(95.42%)	-
Sync. Cycles	70(0.43%)	70(9.30 %)
Total cycles	16349	753
Total time(with 225MHz)	0.000073 s	0.000003 s

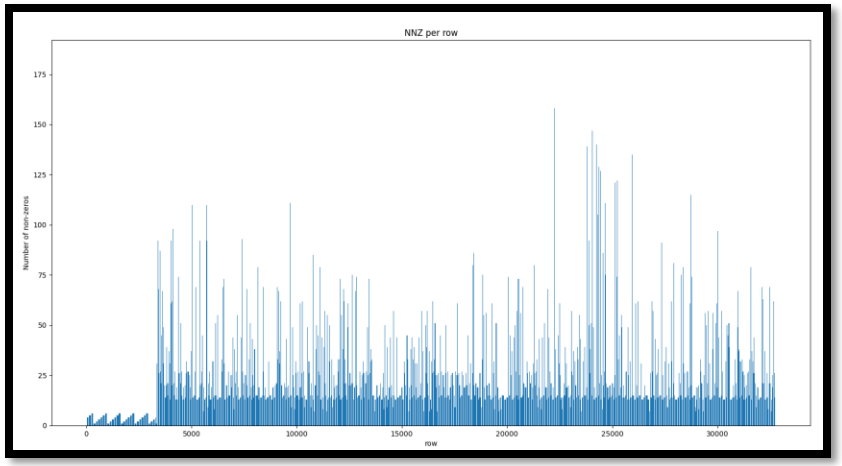


- Max number of PEs utilized = 48
  - MUs are not utilized at all

bundle_adj



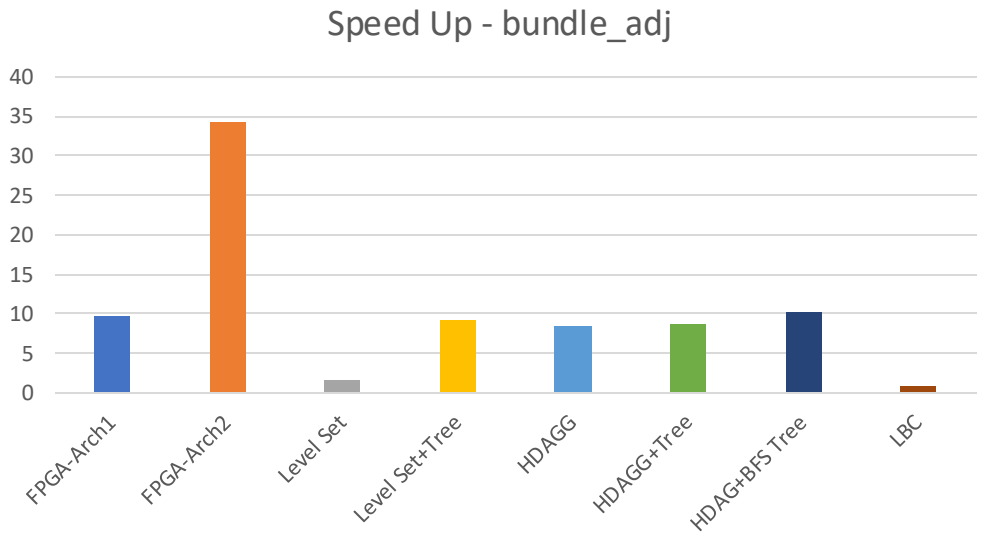




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=847146

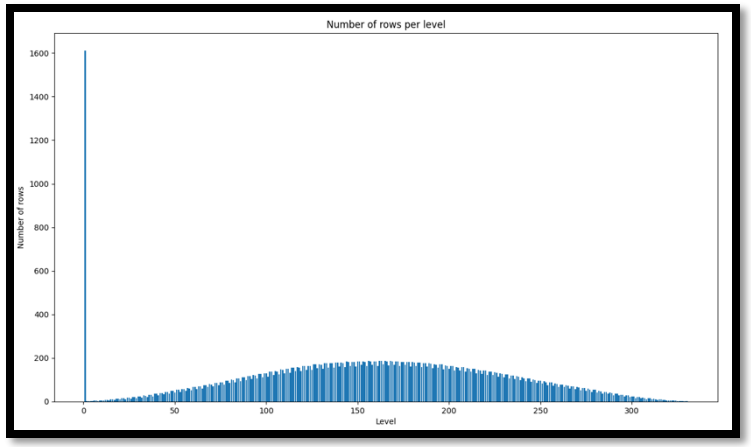
- **Number of levels=9**
  - The largest level=8, **The largest level size=9804**
  - The smallest level=6, **The smallest level size=552**

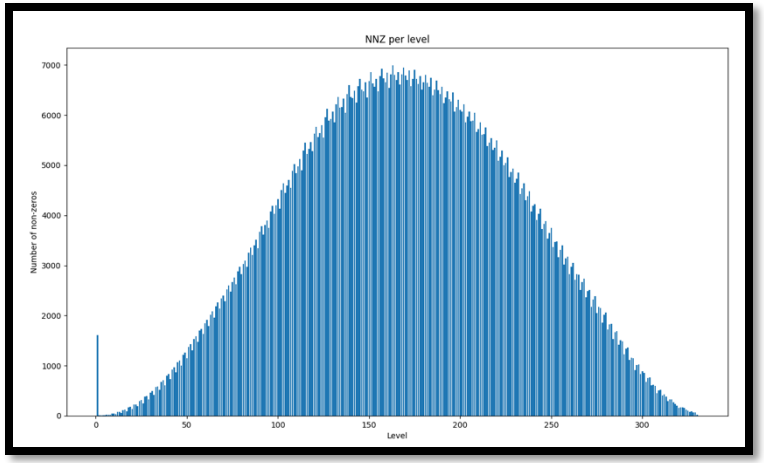
Feature	Arch 1	Arch 2
Dummy data percentage	6.48% (Row-6.32%, PE-0.16%)	32.45% (Row-22.58%, PE-9.88%)
Bubbles	21010(78.54%)	-
Sync. Cycles	1022(3.82%)	1022(13.53%)
Total cycles	26750	7554
Total time(with 225MHz)	0.000119 s	0.000034 s

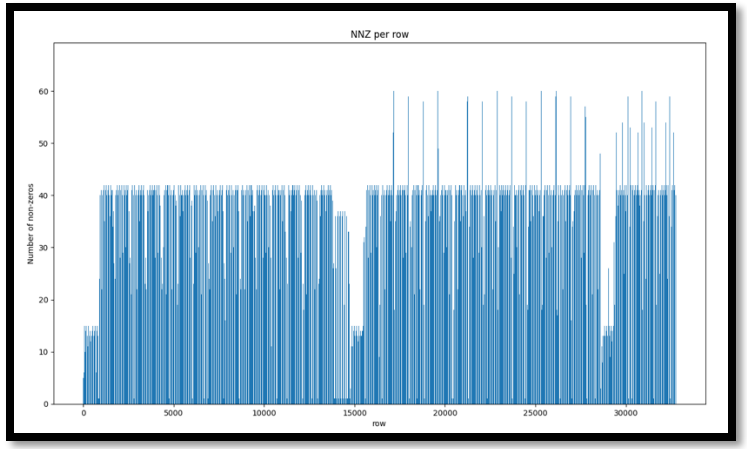


- Max number of PEs utilized = 48

consph



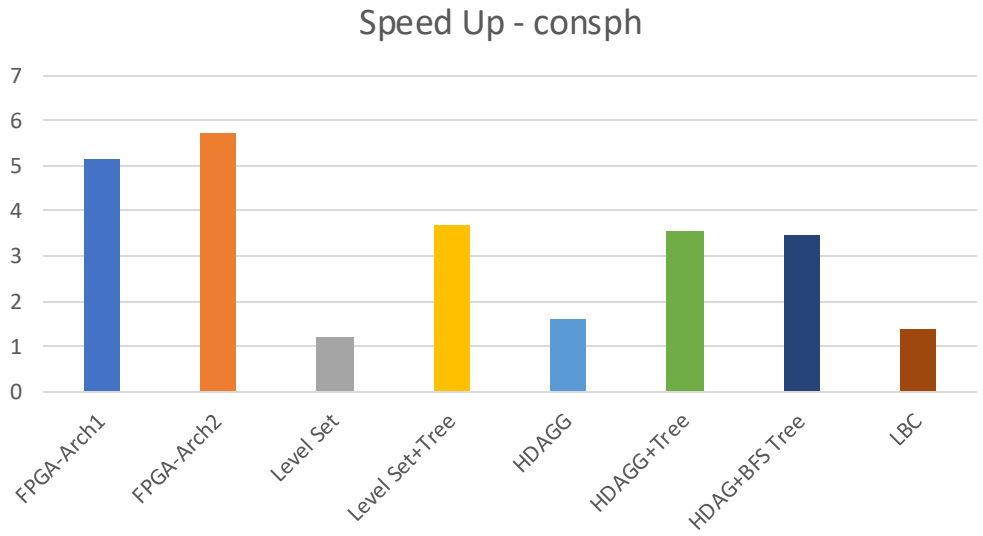




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=1140030

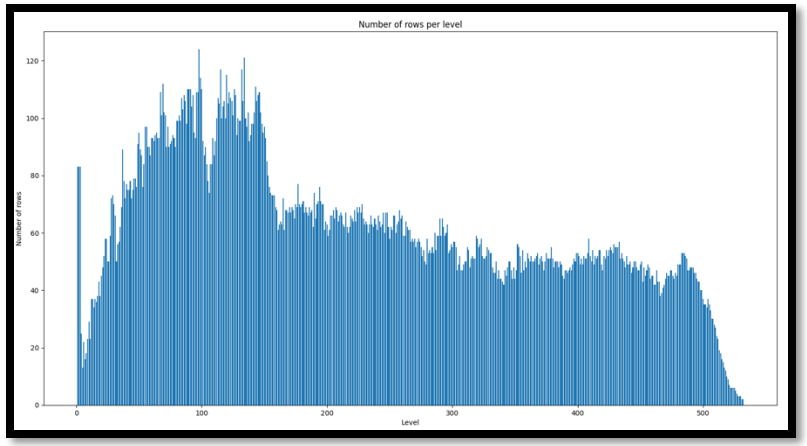
- **Number of levels=330**
  - The largest level=1, **The largest level size=1612**
  - The smallest level=330, **The smallest level size=1**

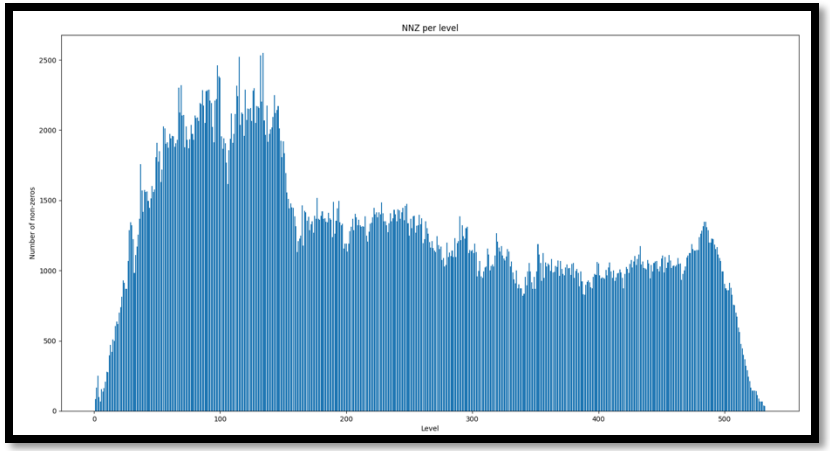
Feature	Arch 1	Arch 2
Dummy data percentage	23.62% (Row-3.70%, PE-19.92%)	49.22% (Row-15.71%, PE-33.51%)
Bubbles	9819(17.45%)	-
Sync. Cycles	39221(69.70%)	39221(77.03%)
Total cycles	56268	50914
Total time(with 225MHz)	0.000250 s	0.000226 s

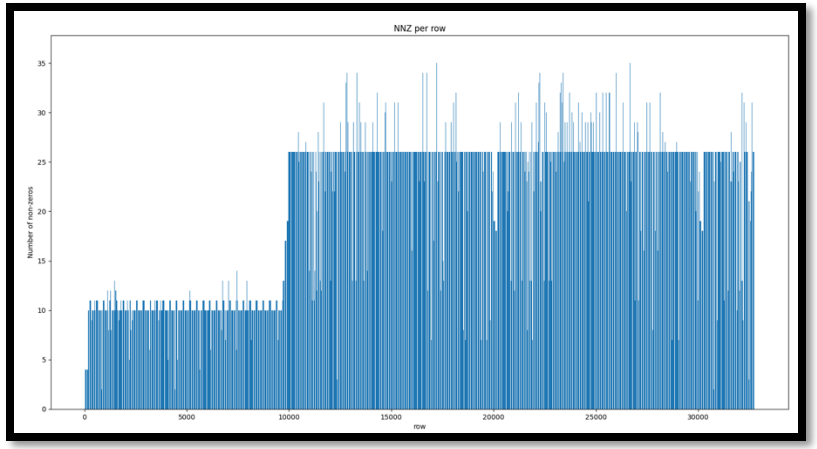


- Max number of PEs utilized = 48

bone010



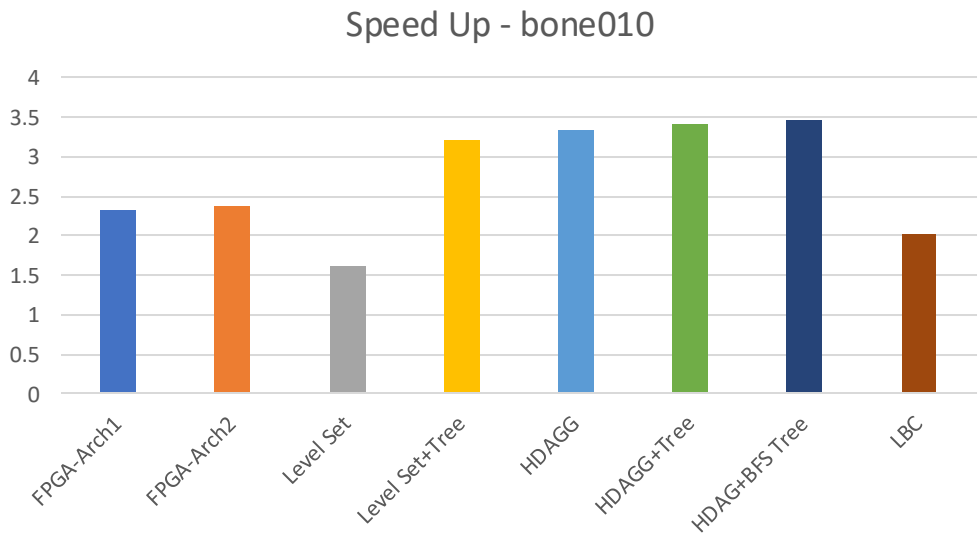




- Triangle Matrix Parameters :: rows=32768, columns=32768, nnz=671231

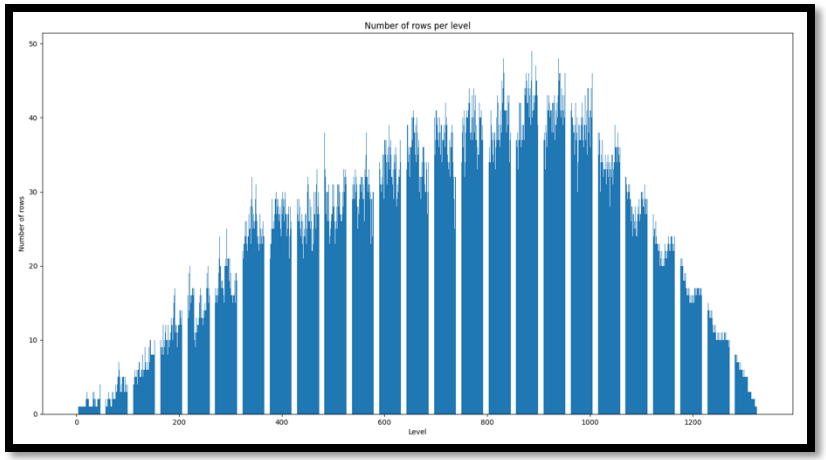
- **Number of levels=532**
  - The largest level=98, **The largest level size=124**
  - The smallest level=532, **The smallest level size=2**

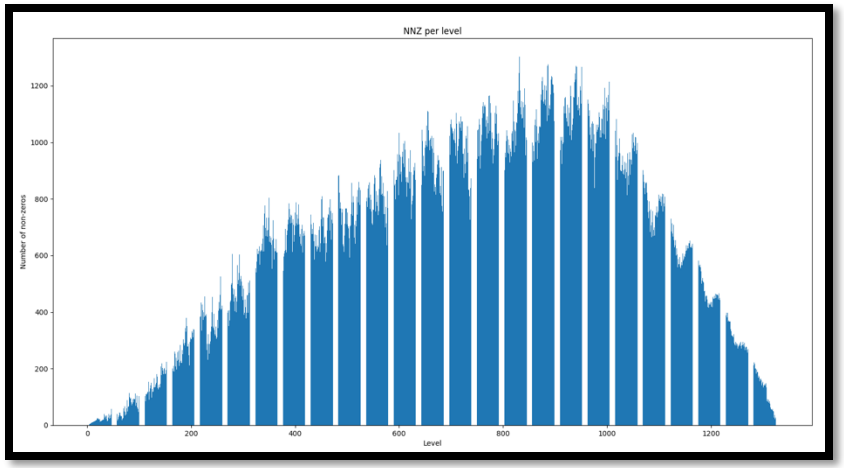
Feature	Arch 1	Arch 2
Dummy data percentage	31.55% (Row-6.01%, PE-25.53%)	54.31% (Row-13.47%, PE-40.85%)
Bubbles	4088(5.68%)	-
Sync. Cycles	63259(87.83%)	63259(89.21%)
Total cycles	72028	70911
Total time(with 225MHz)	0.000320 s	0.000315 s

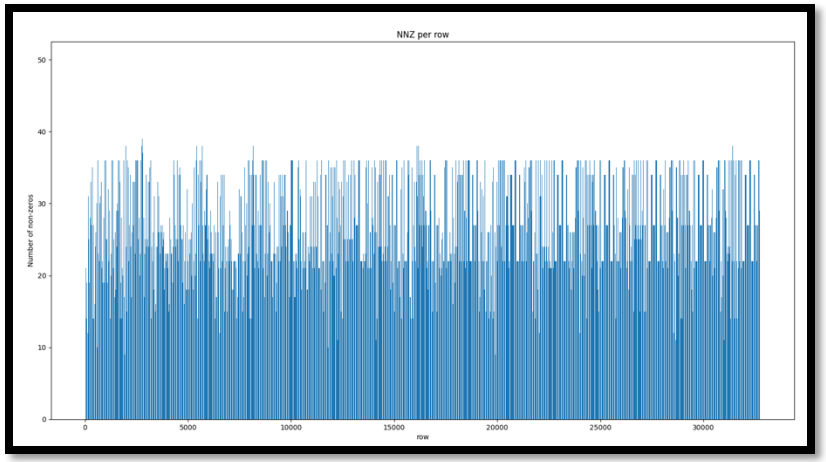


- Max number of PEs utilized = 48

PFlow_742



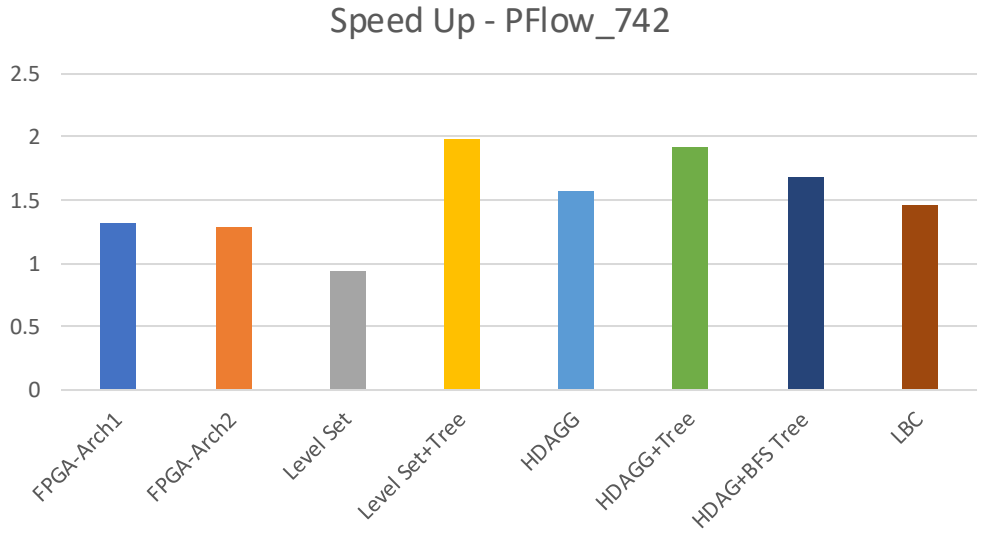




- Triangle Matrix Parameters :: rows=32768, columns=32768, nnz=872367

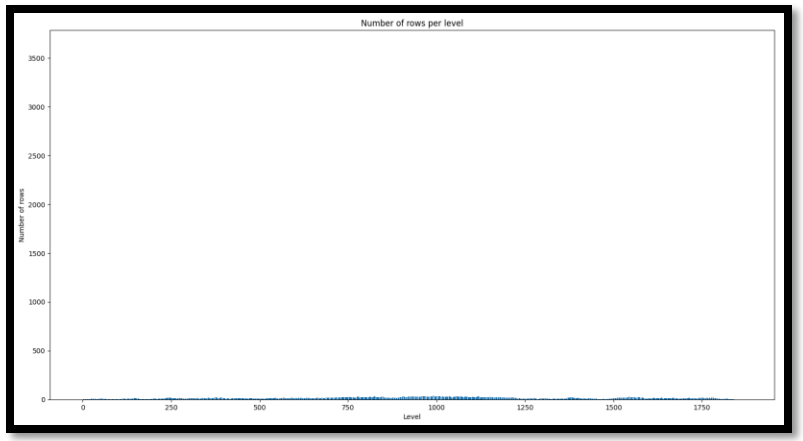
- **Number of levels=1328**
  - The largest level=887, **The largest level size=49**
  - The smallest level=1328, **The smallest level size=1**

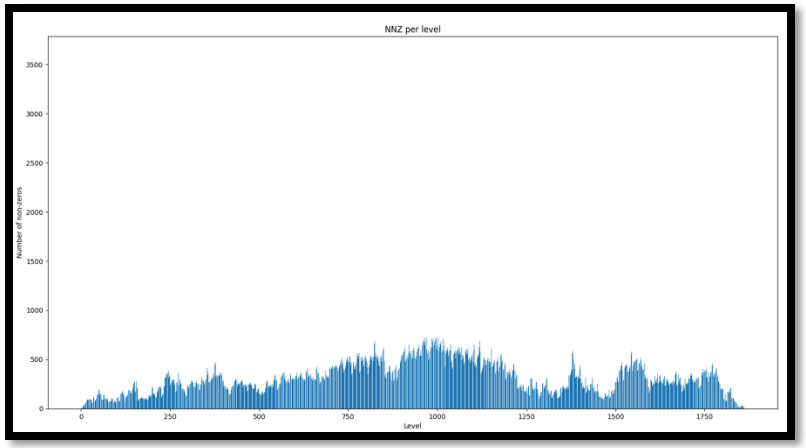
Feature	**Arch 1**	**Arch 2**
Dummy data percentage	61.12% (Row-2.07%, PE-59.05%)	73.40% (Row-9.18%, PE-64.22%)
Bubbles	1(0.00%)	-
Sync. Cycles	157983(93.11%)	157983(90.24%)
Total cycles	169670	175063
Total time(with 225MHz)	0.000754 s	0.000778 s

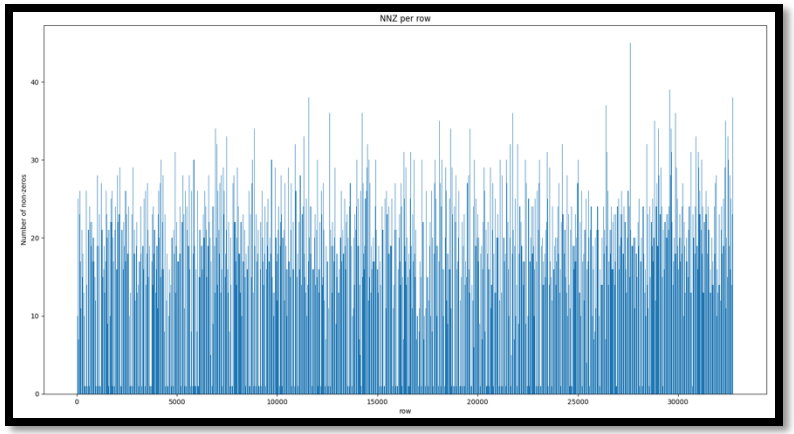


- Max number of PEs utilized = 48

Hook_1498



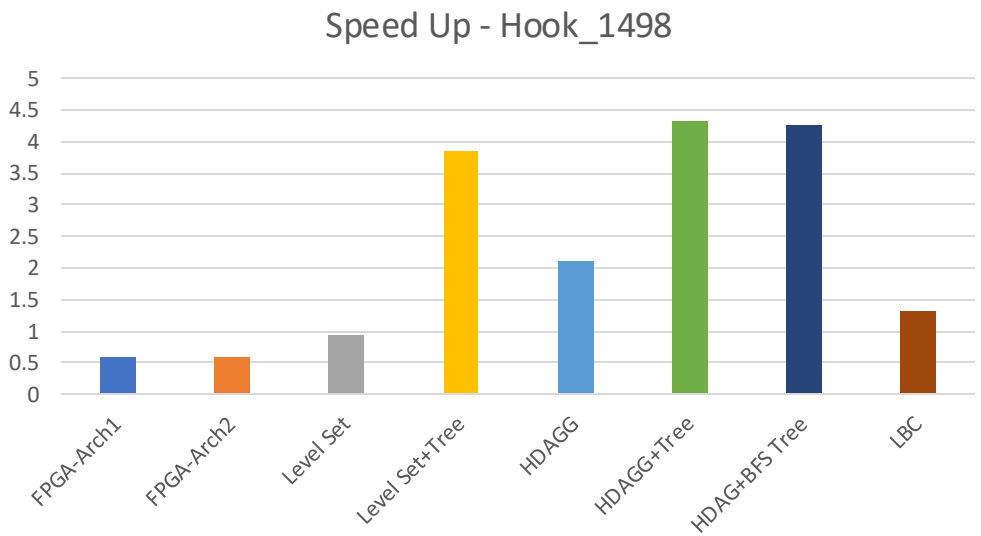




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=584223

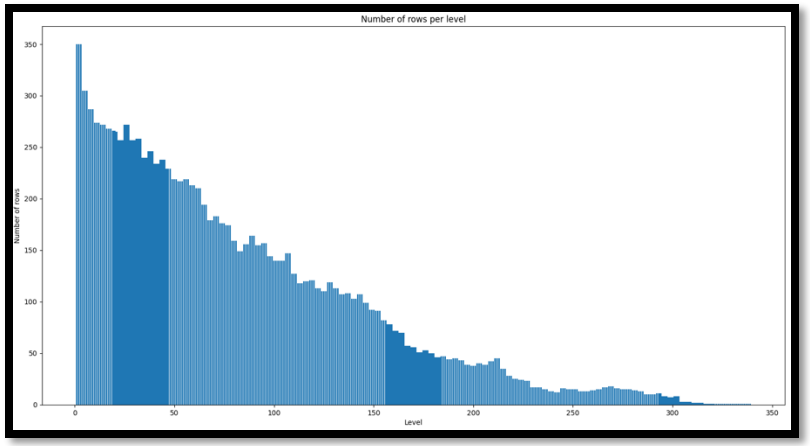
- **Number of levels=1861**
  - The largest level=1, **The largest level size=3606**
  - The smallest level=1861, **The smallest level size=1**

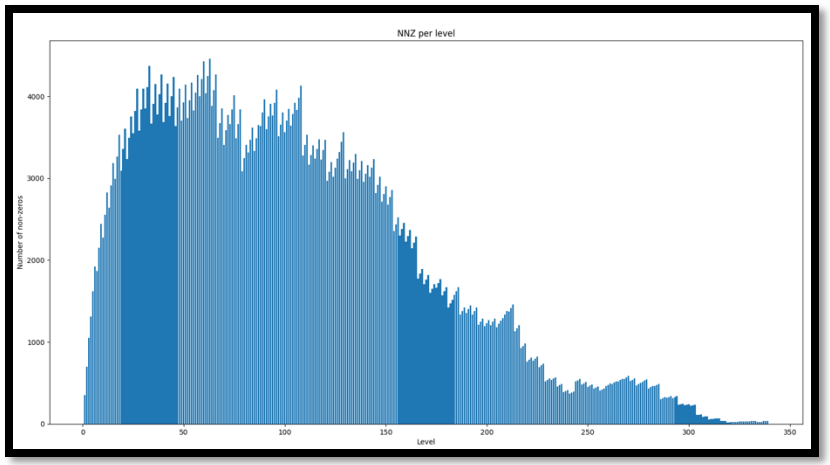
Feature	Arch 1	Arch 2
Dummy data percentage	79.31% (Row-1.94%, PE-77.37%)	85.61% (Row-6.84%, PE-78.77%)
Bubbles	1702(0.72%)	-
Sync. Cycles	221410(93.10%)	221410(91.28%)
Total cycles	237819	242551
Total time(with 225MHz)	0.001057 s	0.001078 s

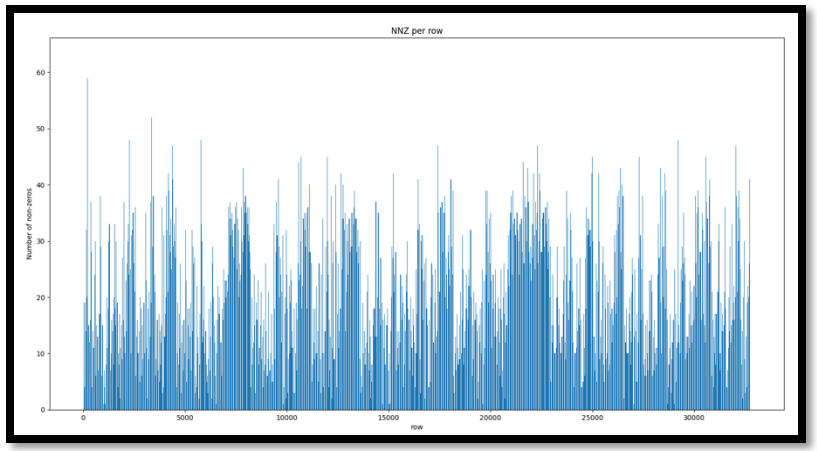


- Max number of PEs utilized = 48
  - MUs of 38 to 48 is not utilized at all

ldoor



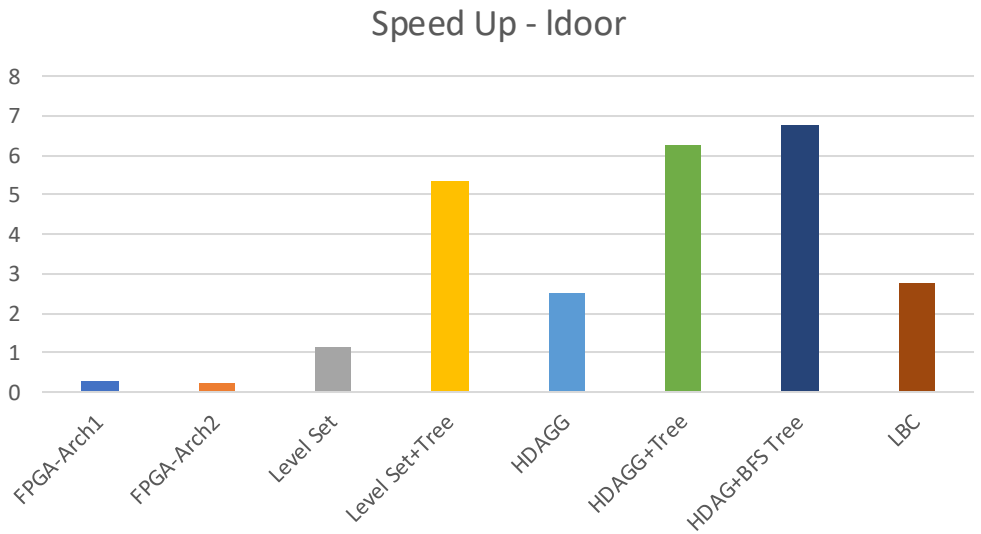




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=669542

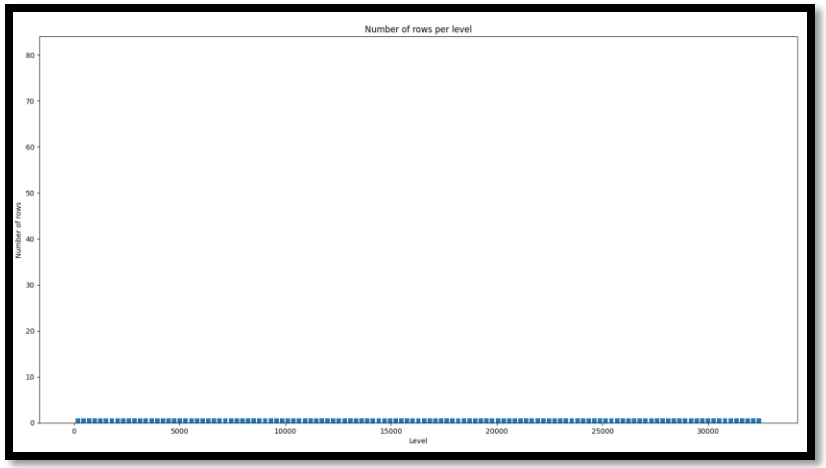
- **Number of levels=4675**
  - The largest level=1, **The largest level size=1247**
  - The smallest level=4668, **The smallest level size=1**

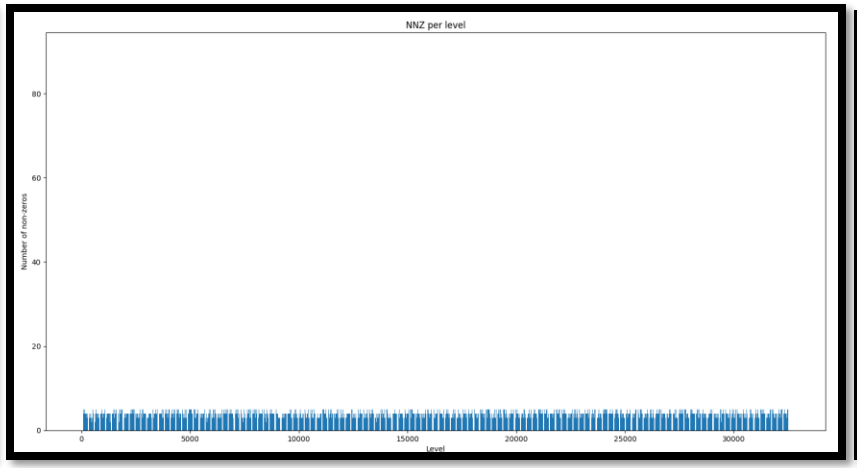
Feature	**Arch 1**	**Arch 2**
Dummy data percentage	91.28% (Row-0.67%, PE-90.61%)	94.37% (Row-3.13%, PE-91.23%)
Bubbles	2356(0.39%)	-
Sync. Cycles	556276(92.93%)	556276(89.99%)
Total cycles	598608	618179
Total time(with 225MHz)	0.002660 s	0.002747 s

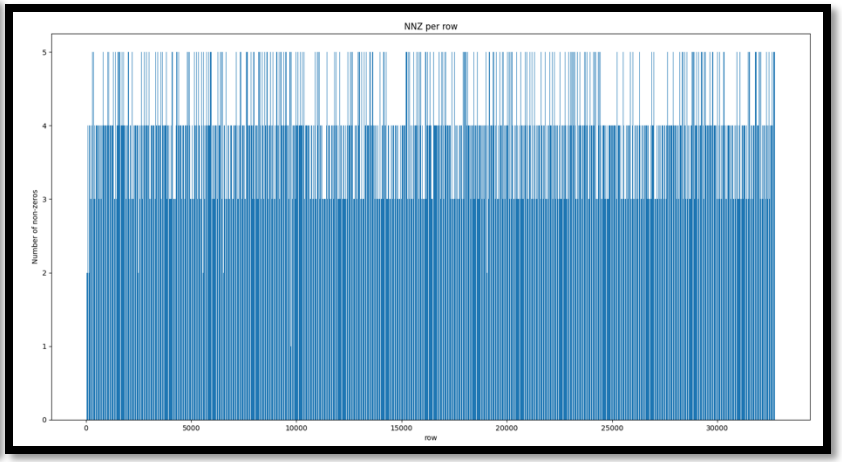


- Max number of PEs utilized = 48

tmt_sym



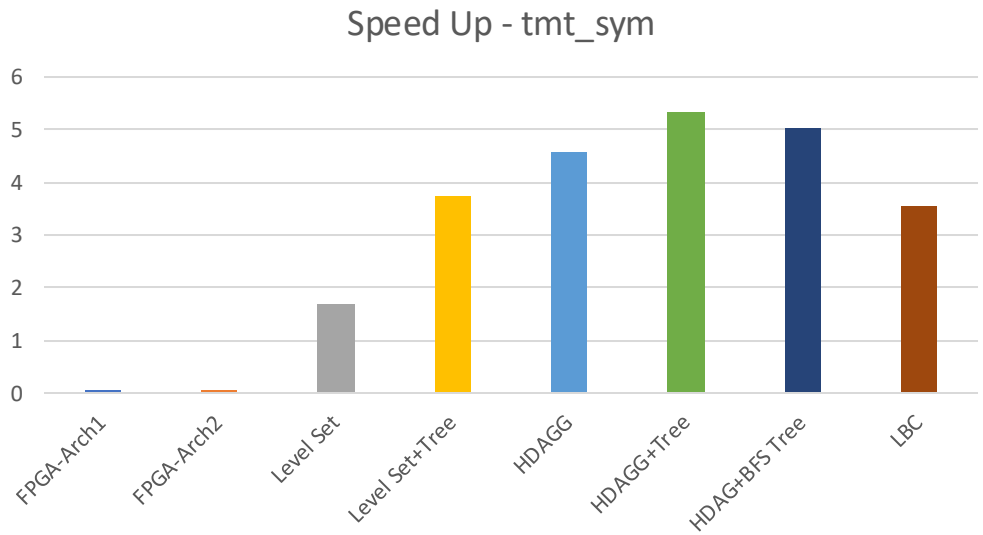




- Triangle Matrix Paramters :: rows=32768, columns=32768, nnz=129930

- **Number of levels=32587**
  - The largest level=1, **The largest level size=80**
  - The smallest level=32587, **The smallest level size=1**

Feature	Arch 1	Arch 2
Dummy data percentage	98.33% (Row-0.42%, PE-97.91%)	98.64% (Row-0.73%, PE-97.91%)
Bubbles	0(0.00%)	-
Sync. Cycles	3877804(98.96%)	3877804(98.73%)
Total cycles	3918373	3927536
Total time(with 225MHz)	0.017415 s	0.017456 s



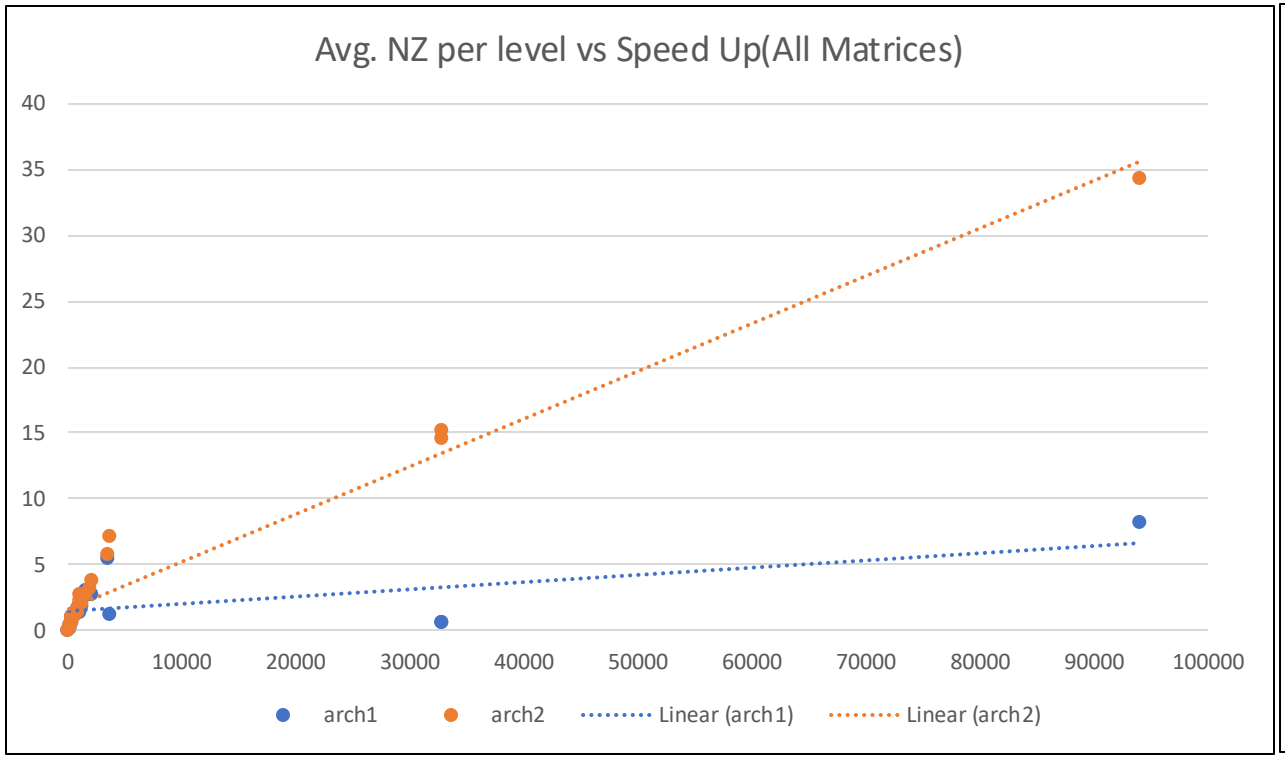
- Max number of PEs utilized = 1

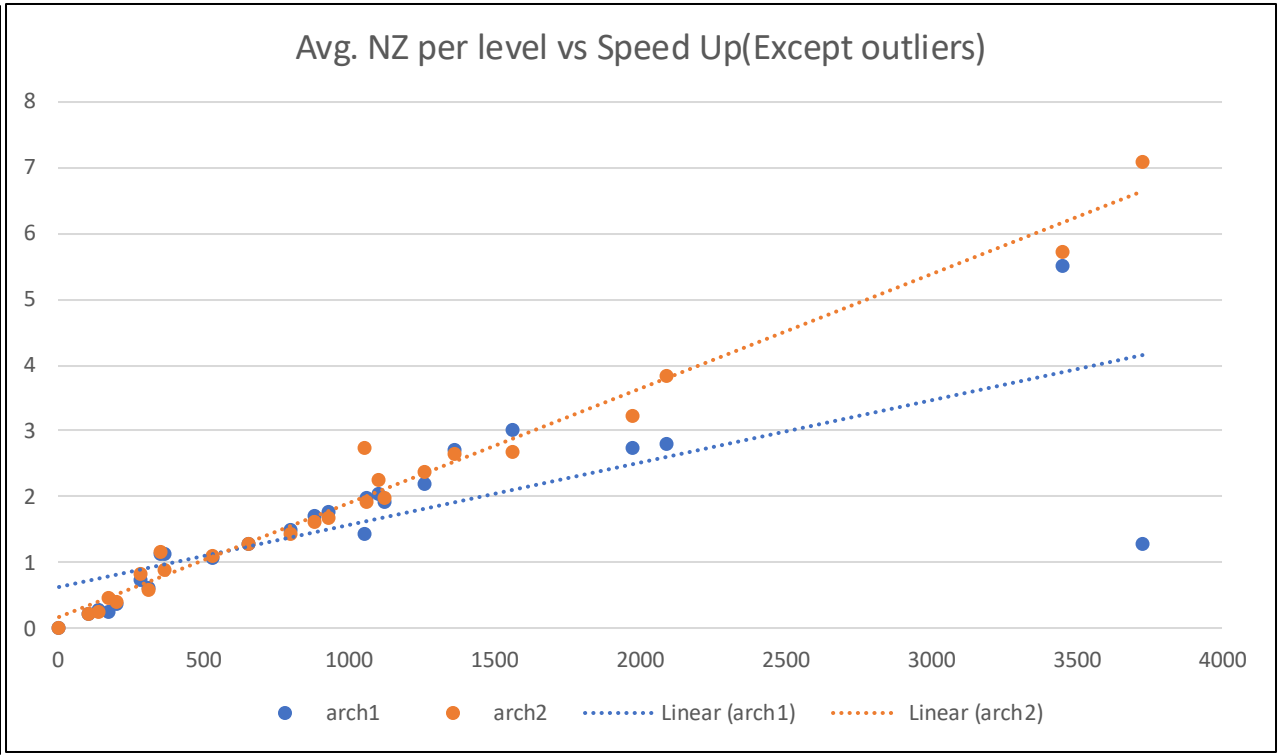
SpTRSV Trend for the 1st tile

SFU

Matrix	Rows	NNZ	Number of levels	Avg. NZ per level	Speed Up - arch1	Speed Up - arch2
tmt_sym	32768	129930	32587	3.987172799	0.016613953	0.015327645
pdb1HYS	32768	1935836	18003	107.528523	0.227560351	0.217025768
ldoor	32768	669542	4675	143.2175401	0.276998496	0.256748771
lung2	32768	81917	471	173.9214437	0.243606806	0.4591875
af_shell10	32768	559336	2728	205.0351906	0.362658344	0.387255333
StocF-146	32768	242834	848	286.3608491	0.742778072	0.827290426
Hook_149	32768	584223	1861	313.9296077	0.599532994	0.577586851
para-4	32768	170074	482	352.8506224	1.137099743	1.15426959
atmosmo	32768	108650	295	368.3050847	1.126966435	0.876721094
ship_003	32768	561740	1055	532.4549763	1.067329693	1.087307878
PFlow_74	32768	872367	1328	656.9028614	1.292644728	1.283779563
Emilia_92	32768	635379	795	799.2188679	1.481342451	1.427562235
crankseg_	32768	3012121	3411	883.0609792	1.720634962	1.599454345
Geo_1438	32768	636906	684	931.1491228	1.760148496	1.680605699
vas_stoke	32768	254852	242	1053.107438	1.444024733	2.729426573
Fault_639	32768	703747	664	1059.85994	1.986387863	1.926345403
shipsec8	32768	477631	434	1100.532258	2.043838047	2.244310837
inline_1	32768	455940	405	1125.777778	1.911089022	1.974573293
bone010	32768	671231	532	1261.712406	2.187738889	2.376679762
Flan_1565	32768	1179664	865	1363.77341	2.695256348	2.637915883
bmwcra_1	32768	1138727	729	1562.039781	3.024231207	2.683534664
audikw_1	32768	670323	339	1977.353982	2.749618845	3.227319886
boneS10	32768	655205	313	2093.306709	2.809867095	3.823909722
consph	32768	1140030	330	3454.636364	5.512659574	5.717168142
kkt_powe	32768	48498	13	3730.615385	1.269364706	7.0861875
parabolic_	32768	32768	1	32768	0.627107877	15.16604167
Freescale1	32768	32768	1	32768	0.615421233	14.62266667
bundle_ad	32768	847146	9	94127.33333	8.22899359	34.38988971

SpTRSV Trend for the 1st tile





Summary

- Level set architecture is efficient if
  - The triangle has a lesser levels and bigger levels
  - i.e., Higher NNZ per level

- Speed up depends on the Average NNZ per level.
  - Higher workload within a level benefits the parallelization on FPGA.

- Higher the number of levels, synchronization cost becomes very high. Sync. Cost depends on
  - Total pipeline depth of the architecture(around 72 cycles)
  - PE group synchronization for solved x(#PE groups-1 cycles)

Thank You!