Athanasios Grigorios Tsarnadelis

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Experience

Digital Design Engineering Intern — Arpil.2025 – Oct.2025

Infineon Technologies

Dresden, Germany

- During my internship, I contributed to the design and sign-off of an Automotive Motor Control SoC based on the Arm Cortex-M
- I gained hands-on experience in RTL coding (Verilog, System Verilog, VHDL).
- I worked on digital design and sign-off flows, including RTL linting, low-power intent verification, generation of UPF and timing constraint (SDC) files, and synthesis flows using industry standard tools from Synopsys and Cadence.
- I was responsible for identifying bottlenecks in platform-based IC development workflows and implementing automation solutions using Unix and Python scripting alongside AI integration.
- During this process, I collaborated with senior Digital, Analog, Concept, and Verification engineers in an international team, gaining exposure to automotive microcontroller development.
- This strengthened my problem-solving skills and deepened knowledge of digital IC design methodologies and semiconductor development practices.
- Relevant Skills: RTL, Verilog, System Verilog, VHDL, RTL sign-off, UPF, timing constraints (SDC), synthesis, AI, automotive microcontroller development, cross-functional collaboration

Education

Master of Science, Electrical and Computer Engineering — Oct.2020 – Dec.2025

School of Electrical and Computer Engineering, Aristotle University

Thessaloniki, Greece

- Grade 8.75 / 10
- During the studies, I got involved in multiple team projects, which helped me develop my team spirit and soft skills
- My involvement in academic projects provided me with the knowledge of Integrated circuit design process, from turning specifications to RTL code, using System Verilog assertions for verification and utilizing Cadence tools for physical implementation. Also, my engagement with analog electronics equipped me with better understanding of CMOS devices and their physical characteristics
- Relevant classes: Analog Electronics, Digital Hardware Design, VSLI design, Digital VLSI-ASIC design, RF Telecommunication electronics
- Relevant projects: RISC-V CPU design in Verilog, Floating Point Multiplier Design and Verification in SystemVerilog, CPU Synthesis and Layout using Cadence Genus and Innovus, OpAmp design

Undergraduate Student — Oct.2018 – Sept.2020

School of Electrical And Computer Engineering, University of Patra

Patra

Due to being accepted in Aristotle University, I terminated my studies in Patra, while continuing studying Electrical and Computer Engineering, this time in Thessaloniki.

High School Diploma — June 2018

Chrysoupoli High School, Kavala, Greece

Grade 19.8/20

Skills

- Critical thinking
- Excellent communication in international teams
- Time management
- Flexibility
- Honesty and integrity
- Problem modeling and solving

Software

- Synopsys Spyglass
- Cadence Conformal Low Power
- Cadence Genus
- Cadence Innovus
- Cadence Virtuoso
- Git / Perforce / Clearcase
- Tcl
- Python
- C / C++
- Unix
- Atlassian Confluence

Languages

- Greek (Mother tongue)
- English (Fluent Spoken and Written)
- German (Intermediate Spoken and Written)

Interests

- Music (Drummer for 8+ years)
- Cooking
- Arduino prototyping (Smart irrigation for precision farming)
- Videogames