

RTX 2000/2001 Instruction Set

Subroutine Call

0aaa aaaa aaaa aaaa

call aaaaaaaaaa0

Subroutine Return

return from subroutine

return from subroutine

ALU

		{NOT}	shift
DROP	DUP	{NOT}	shift
OVER	SWAP	ai	shift
SWAP	DROP	{NOT}	shift
DROP		{NOT}	shift
		ai	shift
SWAP	DROP	{NOT}	shift
SWAP		{NOT}	shift
SWAP	OVER	ai	shift
DUP		{NOT}	shift
OVER	OVER	{NOT}	shift
		ai	shift

Step Math Functions

See Programmer's Ref. Manual I

Branch

1000	0bba	aaaa	aaaa	?DUP	OBANCH
1000	1bba	aaaa	aaaa		OBANCH
1001	0bba	aaaa	aaaa		BRANCH
1001	1bba	aaaa	aaaa		NEXT

Register and I/O Access

1011	000i	00; g	G0	DROP	{NOT}
1011	111i	00; g	G0		{NOT}
1011	cccc	00; g	G0	OVER	alu
1011	000i	10; g	DUP	G!	{NOT}
1011	111i	10; g	G!		{NOT}
1011	cccc	10; g	G0	SWAP	alu

Short Literal

1011 000i x1; d	dddd	d DROP	{NOT}
1011 111i 01; d	dddd	d	{NOT}
1011 cccc 01; d	dddd	d OVER	au
1011 111i 11; d	dddd	d SWAP	{NOT}
1011 cccc 11; d	dddd	d SWAP	au

User Space	1st cycle	2nd cycle

1100	000i	00; u	uuuu	u	∅	SWAP	{NOT}
1100	111i	00; u	uuuu	u	∅	SWAP	{NOT}
1100	cccc	00; u	uuuu	u	∅	SWAP	{NOT}
1100	000i	10; u	uuuu	DUP	u !		
1100	111i	10; u	uuuu	DUP	u !		
1100	cccc	10; u	uuuu	u	∅	SWAP	alu

IBC

IB5	IB4	IB3	IB2	IB1	IB0	TC1	TC0	CYC	RND	DPS
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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[illegible]

1101 000i	x0; x	xxxx	D SWAP	{NOT}
1101 111i	00; x	xxxx	SWAP	SWAP {NOT}
1101 cccc	00; x	xxxx	D SWAP	SWAP OVER alu
1101 111i	10; x	xxxx	D SWAP	DROP {NOT}
1101 cccc	10; x	xxxx	D SWAP	alu

Memory Access	1st cycle	2nd cycle
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111s 000i 00;x xxxx	0 SWAP	{NOT}
111s 111i 00;x xxxx	0 SWAP	SWAP {NOT}
111s cccc 00;x xxxx	0 SWAP	SWAP OVER a lu
111s 000p 01;x xxxx	{SWAP DROP} DUP 0 SWAP	NOP
111s 111p 01;d dddd	{SWAP DROP} 0 d	NOP
111s aaap 01;d dddd	{SWAP DROP} DUP 0 SWAP d SWAP a lu	NOP
111s 000i 10;x xxxx	OVER SWAP !	{NOT}
111s 111i 10;x xxxx	OVER SWAP !	DROP {NOT}
111s cccc 10;x xxxx	0 SWAP	a lu
111s 000p 11;x xxxx	{OVER SWAP} SWAP OVER !	NOP
111s 111p 11;d dddd	{OVER SWAP} ! d	NOP
111s aaap 11;d dddd	{OVER SWAP} SWAP OVER ! d SWAP a lu	NOP

$s = 0$ for word access($@/!$), 1 for byte access ($C@/C!$)

{SWAP DROP} and {OVER SWAP} are performed if $p = 0$

cccc	aaa	function
0010	001	AND
0011		NOR
0100	010	SWAP -
0101		SWAP -C
0110	011	OR
0111		NAND
1000	100	+
1001		+C
1010	101	XOR
1011		XNOR
1100	110	-
1101		-C

ssss	function	ssss	function
0000	no shift	1000	N2*
0001	0<	1001	N2*C
0010	2*	1010	D2*
0011	2*C	1011	D2*C
0100	cU2/	1100	cUD2/
0101	c2/	1101	cD2/
0110	U2/	1110	UD2/
0111	2/	1111	D2/

C

[illegible]

M

SWI	EI5	EI4	EI3	T2	T1	T0	EI2	RSV	PSV	RSU	PSU	EI1
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IBC

IB5	IB4	IB3	IB2	IB1	IB0	TC1	TC0	CYC	RND	DPS
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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ggggg	register
00000	I read/wrt
00001	I push/pop
00010	I stream
00011	CR
00100	MD
00101	SQ
00110	SR
00111	PC
01000	IMR
01001	SPR
01010	reserved
01011	IVR/SLR
01100	IPR
01101	DPR
01110	UPR
01111	CPR
10000	IBC
10001	UBR
10010	reserved
10011	Timer 0
10100	Timer 1
10101	Timer 2
10110	MLR
10111	MHR

int		vector
0	NMI	vvvvvv0111100000
1	E11	vvvvvv0111000000
2	PSU	vvvvvv0110100000
3	RSU	vvvvvv0110000000
4	PSV	vvvvvv0101100000
5	RSV	vvvvvv0101000000
6	E12	vvvvvv0100100000
7	TC0	vvvvvv0100000000
8	TC1	vvvvvv0011100000
9	TC2	vvvvvv0011000000
10	E13	vvvvvv0010100000
11	E14	vvvvvv0010000000
12	E15	vvvvvv0001100000
13	SWI	vvvvvv0001000000
-1	none	vvvvvv1000000000